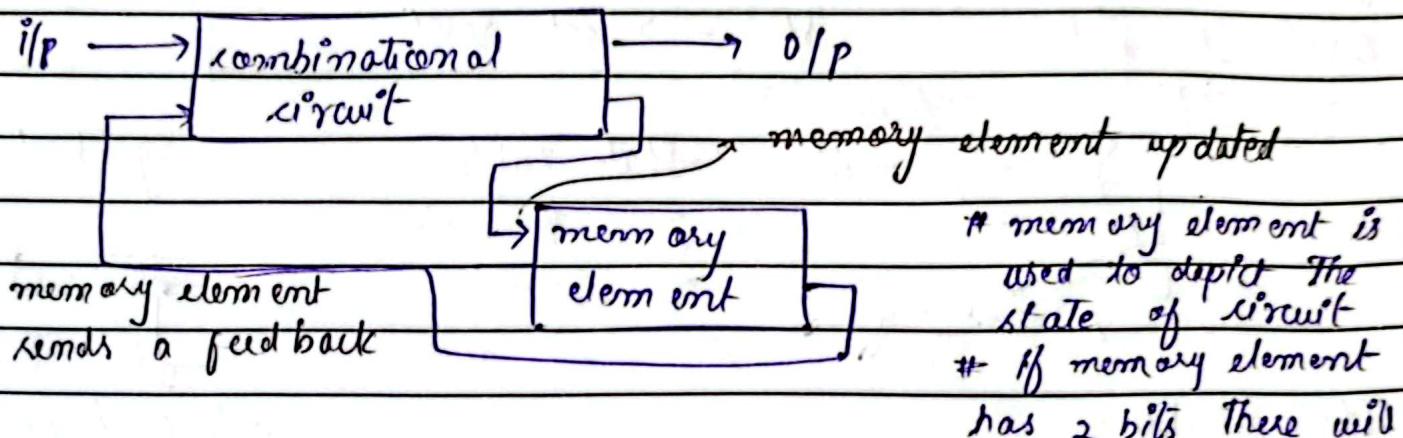


New Chapter :-

Date: _____

- # a completely filled kmap corresponds to $T_F = 1$
- # a completely unfilled kmap corresponds to $T_F = 0$

SEQUENTIAL CIRCUITS :-



* In combinational circuits if i/p is given we can predict the o/p but in sequential circuit if i/p's are given we can't predict the o/p.

- . In combinational circuit The o/p at any given time entirely depend on current i/p's.
- . In sequential circuit o/p depends both on current i/p's and current state of network/circuit.
- . The behaviour of sequential circuit is described by a mathematical model known as a sequential machine (finite state machine) and can be represented by a state list or a state diagram.

Page #



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- # invalid i/p done bc had miltb $S=1$ and $R=1$ dedia uske bad aqr no change i/p dede miltb $S=0$ and $R=0$ kyu miltb hata ha.
- # after invalid i/p if we provide no change i/p there would be a race condition.

Date: 13 - Sep - 24.

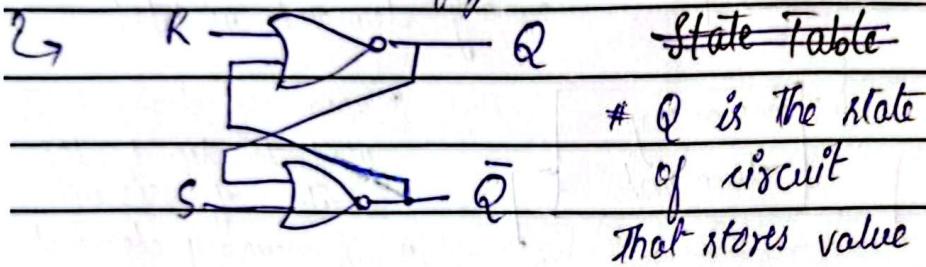
Memory elements

latches and flip flops:- Bistable devices that store 1 bit of info.

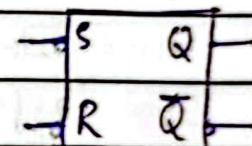
Latch :-

Basic SR Latch :- $SR \rightarrow$ set reset

Cross couple nor configuration



Symbol :-



State Table :-

active high i/p

Q_t	S	R	Q_{t+1}	SR Latch
0	0	0	0	
0	0	1	0	# 1 latch & flip flops
0	1	0	1	store 1 bit.
0	1	1	0 (invalid)	# 64 bit register
1	0	0	1	→ 64 bit flip flops
1	0	1	0	# set → put a one
1	1	0	1	# reset → put a zero
1	1	1	0 (invalid)	# state table has i/p as well as the present state (Q_t)

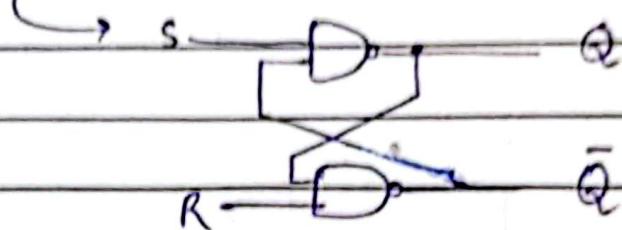
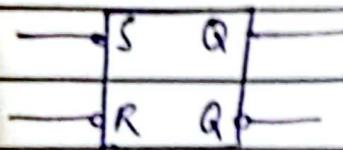
Characteristic table

S	R	Q_{t+1}	
0	0	Q_t (no change)	of the set
0	1	0	# invalid i/p also called
1	0	1	Indeterminate

Date: _____

active low i/p SR Latch

cross couple nand configuration



indeterminate

Q_t	S	R	Q_{t+1}
0	0	0	1 (invalid)
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1 (invalid)
1	0	1	1
1	1	0	0
(1)	1	1	1

↳ when both i/p's are inactive the present state will remain the same.

S	R	Q_{t+1}
0	0	1 (invalid)
0	1	1
1	0	0
1	1	Q_t (No change command)

in active low i/p SR Latch
0 shows the activeness of i/p and 1 shows that the i/p is not active.

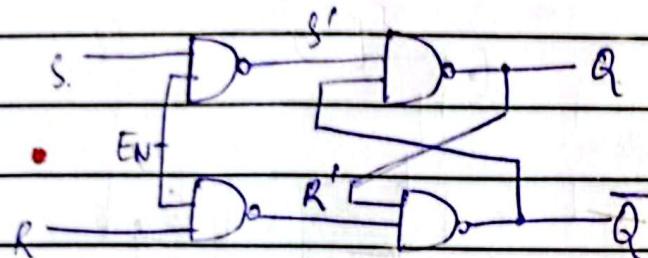
in active high i/p SR Latch
1 shows activeness of i/p and 0 shows the inactiveness of i/p.



$$A \Rightarrow D \quad A \Rightarrow \bar{D} \quad \bar{A} \Rightarrow D \quad \bar{A} \Rightarrow \bar{D}$$

Date: 19 - Sep - 2024

Gated SR Latch :- It behaves like active high SR Latch
 Nand implementation :- Symbol :-



S	Q
EN	
R	\bar{Q}

Characteristic Table :-

Characteristic Equation.

EN	Q_t	S	R	Q_{t+1}
1	0	0	0	0 (NC)
1	0	0	1	0
1	0	1	0	1
1	0	1	1	invalid
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	invalid
(0)	Q_t	x	x	Q_t

↳ if nand gate is enabled

then the present state Q_t

will become Q_{t+1} . i.e. $Q_{t+1} = Q_t$.

Q_t	S	R	00	01	11	10
0	0	1	0	1	X	1
1	1	0	D	X	0	1

1 shows that nand gate is enabled and zero shows that nand gate is disabled.

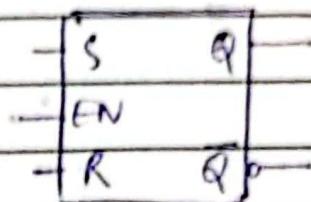
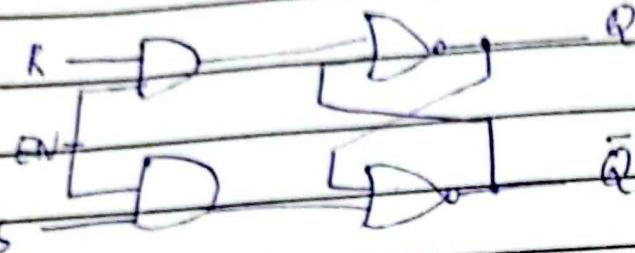
$$Q_{t+1} = Q_t \bar{R} + S$$

It too behaves as active high flip flop

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CMOS Implementation :-

Symbols:-



EN	Q_t	S	R	Q_{t+1}
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	inv
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	inv
0	Q_t	X	X	Q_t

Q_t	SR	00	01	11	10
0	0	0	1	X	1
1	1	D	1	X	D

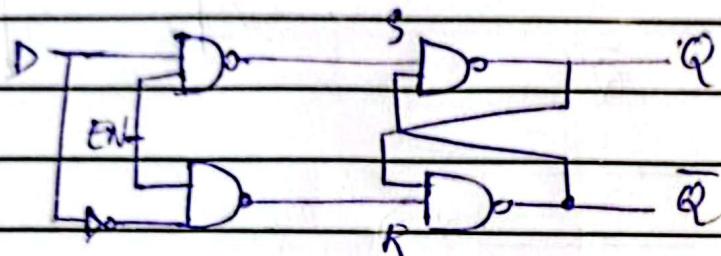
Characteristic eq :-

$$Q_{t+1} = S + Q_t \bar{R}$$



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D Latch :- It behaves as low flip
- transparent, data, delay



Characteristic Table :-

EN	Q _t	D	Q _{t+1}
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1
0	Q _t	X	Q _t

Characteristic eq :-

$$Q_{t+1} = D$$

→ Q_{t+1} will be equal to
the value of D.

→ Latches are level triggered.

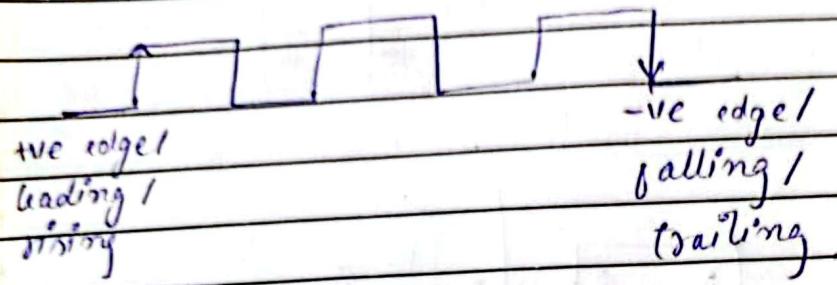
↳ we don't use level triggered
devices we use edge triggered
devices.

→ in level triggering devices time
management is difficult.

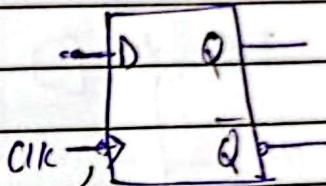
→ -ve edge trigger symbol → +ve edge triggered
register = 64 flip flops

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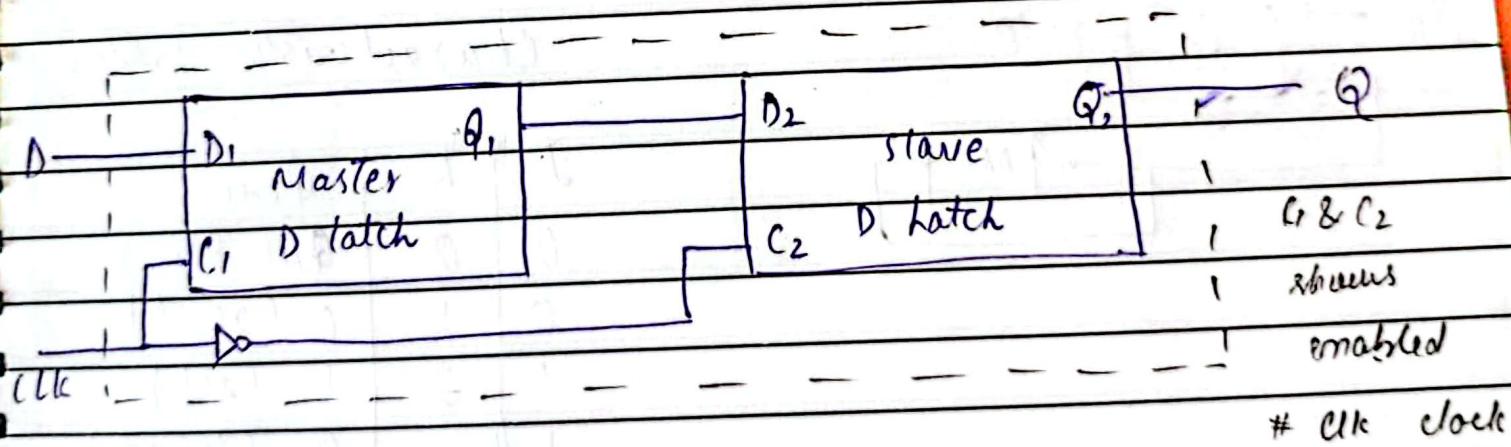
FLIP FLOPS :- (edge triggered devices)
- Latches are level triggered.



Master Slave D flip flop :-



-ve edge triggered symbol



initially both latches are reset

Clk	D ₁	C ₁	Q ₁	D ₂	C ₂	Q ₂	Q̄ ₂	initial state
0	X	0	0	0	1	0	1	means no i/p D ₁ .
0	1	0	0	0	1	0	1	
1	1	1	1	1	0	0	0	
0	X	0	1	1	1	1	1	

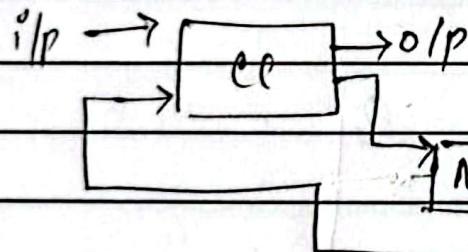
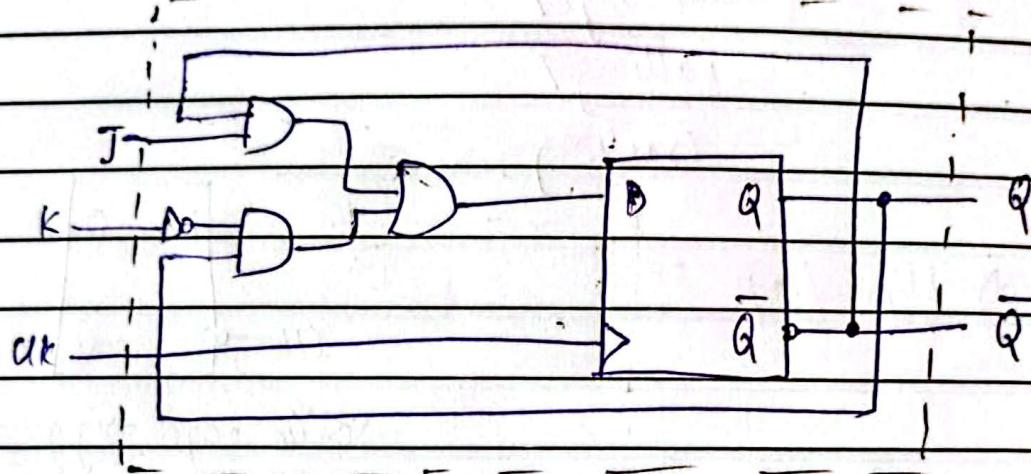
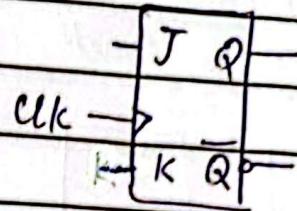


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JK flip flops :-

$J \rightarrow$ set

$K \rightarrow$ reset



Characteristic table :-

J	K	Q_{t+1}
0	0	Q_t (Nc)
0	1	0 (reset)
1	0	1 (set)
1	1	\overline{Q}_t (toggle)

Clk	Q_t	J	K	Q_{t+1}
↑	0	0	0	0
↑	0	0	1	0
↑	0	1	0	1
↑	0	1	1	1
↑	1	0	0	1
↑	1	0	1	0
↑	Page #	1	0	1
↑	1	1	1	0

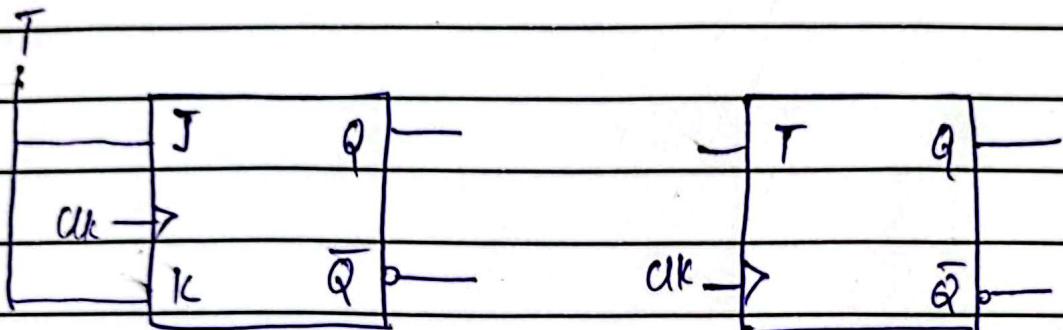
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$\downarrow /, /0 \quad Q_F \times \times / \quad Q_F$

T flip flop:- (toggle flip flop)

agr toggle kommanad dedi Jiu ip ka invert milga.



Q_t	T	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	-1	0