**IF/ID REG (48 BITS):**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| INPUT | BITS | **47-32** | **31-16** | **15-0** |
| Signal | PC+1 | INSTRUCTION | IMM/IN |

**ID/IE REG (88 BITS):**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | BITS | 87-73 | 72-57 | 56-54 | 53-51 | 50-48 | 47-32 | 31-16 | 15-0 |
|  | SIGNAL | Controller Signals | PC + 1 | RSRC1 ADD | RSRC2 ADD | RDST ADD | RSRC1 Value | RSRC2 Value | IMM OR IN |

**Controller Signals:**

SET\_CLEAR       <= Decode\_Buffer\_OUT(87 downto 86);

Write\_back      <= Decode\_Buffer\_OUT(85);

MEM\_SRC         <= Decode\_Buffer\_OUT(84);

SP\_INC          <= Decode\_Buffer\_OUT(83);

SP\_DEC          <= Decode\_Buffer\_OUT(82);

MEM\_WRITE       <= Decode\_Buffer\_OUT(81);

Out\_Signal      <= Decode\_Buffer\_OUT(80);

ALU\_SRC         <= Decode\_Buffer\_OUT(79);

ALU\_Operation   <= Decode\_Buffer\_OUT(78 downto 76);

CIN\_Signal      <= Decode\_Buffer\_OUT(75);

CALL\_Signal     <= Decode\_Buffer\_OUT(74);

MEM\_TO\_REG      <= Decode\_Buffer\_OUT(73);

**IE/MEM1 REG (65 BITS):**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | BITS | 64-49 | 48-41 | 40-25 | 24-9 | 8-6 | 5-3 | 2-0 |
|  | SIGNAL | PC+1 | Controller Signals | ALU\_RESULT | RSRC2\_VALUE | Rsrc1\_add | Rsrc2\_add | Rdst\_add |

**Controller Signals:**

Write\_back      <= EX\_MEM1\_Buffer(48);

MEM\_SRC         <= EX\_MEM1\_Buffer (47);

SP\_INC          <= EX\_MEM1\_Buffer (46);

SP\_DEC          <= EX\_MEM1\_Buffer (45);

MEM\_WRITE       <= EX\_MEM1\_Buffer (44);

Out\_Signal      <= EX\_MEM1\_Buffer (43);

CALL\_Signal     <= EX\_MEM1\_Buffer (42);

MEM\_TO\_REG      <= EX\_MEM1\_Buffer (41);

**Mem1/MEM2 REG (64 BITS):**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | BITS | 63-48 | 47-41 | 40-25 | 24-9 | 8-6 | 5-3 | 2-0 |
|  | SIGNAL | PC+1 | Controller Signals | READ\_ADD | WRITE\_DATA | Rsrc1\_add | Rsrc2\_add | Rdst\_add |

WB\_OUT <= BUFF\_OUT(47);

MEM\_TO\_REG\_OUT <= BUFF\_OUT(46);

SP\_INC\_OUT <= BUFF\_OUT(45);

SP\_DEC\_OUT <= BUFF\_OUT(44);

MEMW\_OUT <= BUFF\_OUT(43);

OUT\_SIG\_OUT <= BUFF\_OUT(42);

CALL\_SIG\_OUT <= BUFF\_OUT(41);

**MemStage2 (64 BITS):**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | BITS | 63-48 | 47-41 | 40-25 | 24-9 | 8-6 | 5-3 | 2-0 |
|  | SIGNAL | PC | Controllsignals | Mem\_Read | Write\_Data | Rsrc1 | Rsrc2 | Rdst |

WB\_OUT <= BUFF\_OUT(47);

MEM\_TO\_REG\_OUT <= BUFF\_OUT(46);

SP\_INC\_OUT <= BUFF\_OUT(45);

SP\_DEC\_OUT <= BUFF\_OUT(44);

MEMW\_OUT <= BUFF\_OUT(43);

OUT\_SIG\_OUT <= BUFF\_OUT(42);

CALL\_SIG\_OUT <= BUFF\_OUT(41);

**MemSt2/Wb REG (44 BITS):**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | BITS | 43 | 42 | 41 | 40-25 | 24-9 | 8-6 | 5-3 | 2—0 |
|  | SIGNAL | Wb | M2r | outEn | Memst2 | Memst1 | RSRC1 Value | RSRC2 Value | Rdst |