**IF/ID REG (48 BITS):**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| INPUT | BITS | **47-32** | **31-16** | **15-0** |
| Signal | PC+1 | INSTRUCTION | IMM/IN |

**ID/IE REG (88 BITS):**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | BITS | 87-73 | 72-57 | 56-54 | 53-51 | 50-48 | 47-32 | 31-16 | 15-0 |
|  | SIGNAL | Controller Signals | PC + 1 | RSRC1 ADD | RSRC2 ADD | RDST ADD | RSRC1 Value | RSRC2 Value | IMM OR IN |

SET\_CLEAR       <= Decode\_Buffer\_OUT(87 downto 86);

Write\_back      <= Decode\_Buffer\_OUT(85);

MEM\_SRC         <= Decode\_Buffer\_OUT(84);

SP\_INC          <= Decode\_Buffer\_OUT(83);

SP\_DEC          <= Decode\_Buffer\_OUT(82);

MEM\_WRITE       <= Decode\_Buffer\_OUT(81);

Out\_Signal      <= Decode\_Buffer\_OUT(80);

ALU\_SRC         <= Decode\_Buffer\_OUT(79);

ALU\_Operation   <= Decode\_Buffer\_OUT(78 downto 76);

CIN\_Signal      <= Decode\_Buffer\_OUT(75);

CALL\_Signal     <= Decode\_Buffer\_OUT(74);

MEM\_TO\_REG      <= Decode\_Buffer\_OUT(73);

**MemSt2/Wb REG (44 BITS):**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | BITS | 43 | 42 | 41 | 40-25 | 24-9 | 8-6 | 5-3 | 2—0 |
|  | SIGNAL | Wb | M2r | outEn | Memst2 | Memst1 | RSRC1 Value | RSRC2 Value | Rdst |