Final Exam - CSC 137

College of Engineering & Computer Science

(Include the Test question along with solution)

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1. Figure 8.7 illustrates a single-cycle data path for the example Acc-Instruction set Architecture processor. It consists of fetch, decode, execute, and write-back units. During each clock cycle, an instruction is fetched, decoded, and executed, and the result (if any) is written back to register ACC, X, or 1-bit status register (SR).what is function of MUX 3 in the execution unit. Circle the best Answer. (20 Pts)
   A. MUX 3 is needed to choose the operand when the operand is an immediate data or when the operand is an address and indicates memory content.
   B. MUX 3 is needed so control signals for Add/Cmp can be selected for op code execution.
   [✓ C. A and B]
   D. None of the above.

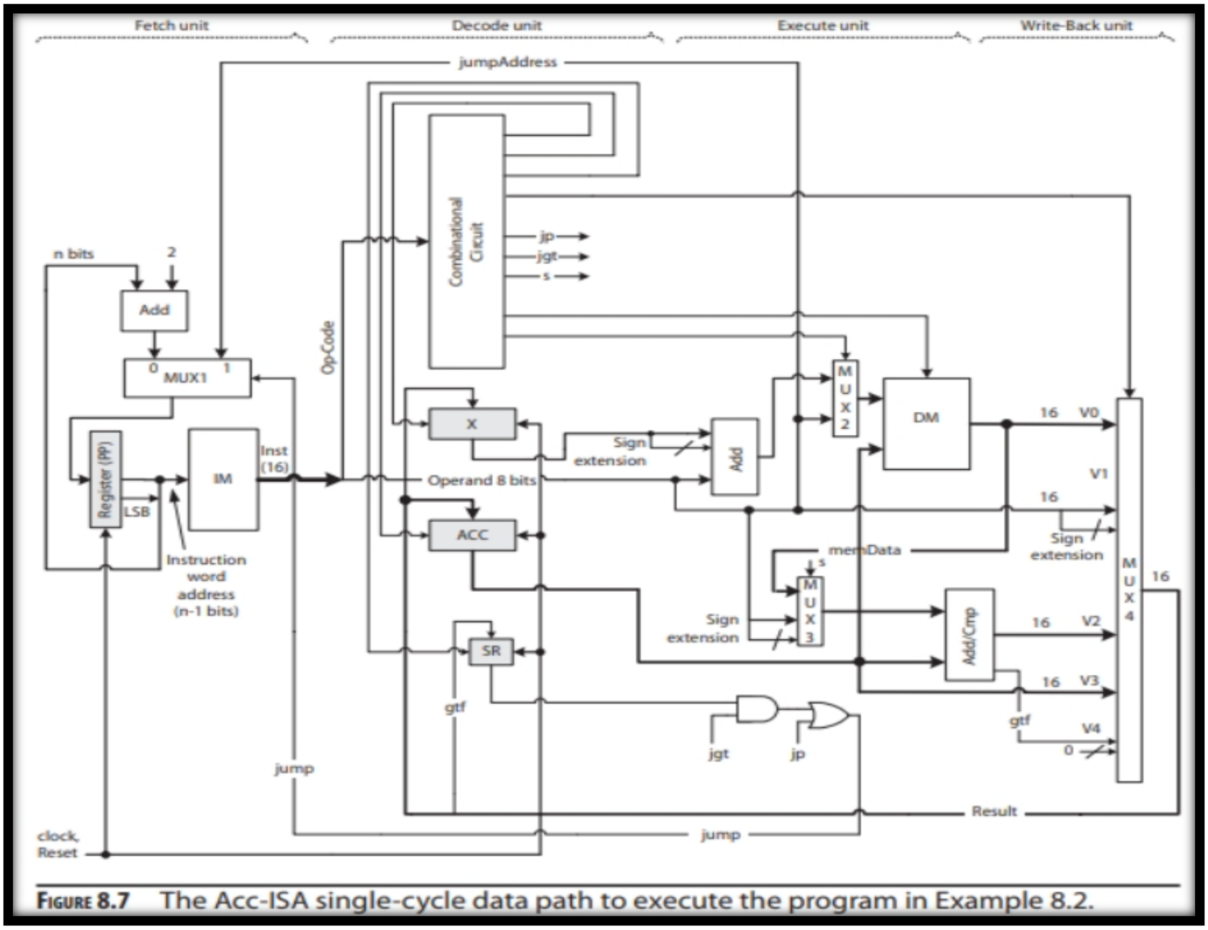


FIGURE 8.7 The Acc-ISA single-cycle data path to execute the program in Example 8.2.

2. A memory write cycle is similar to a read cycle, except that data must be placed on the data bus at the same time that _ce is asserted or within a maximum delay after _we is asserted to minimize the time the data bus is used. Figure 7.17 illustrates an SRAM memory write cycle. (20pts)

   A. A memory cycle is initiated by which component in the computer motherboard?

      Answer: DMA Controller

   B. Generally, how many CPU clock cycles does it take to complete a memory cycle?

      Answer: 2 clock cycles

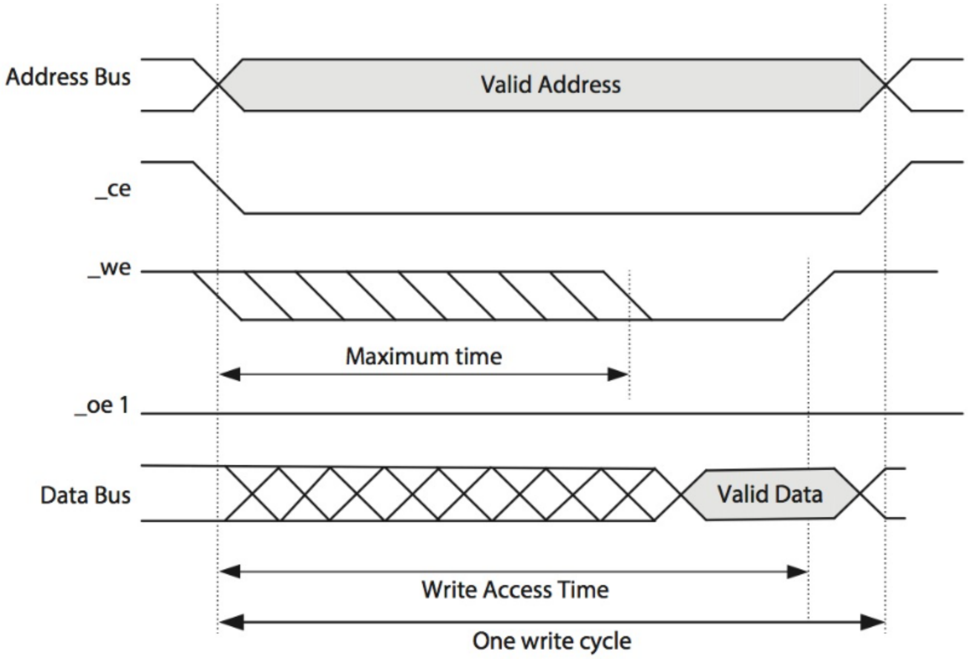


FIGURE 7.17 An SRAM write cycle from a memory point of view.

3. Consider the sequential circuit in Figure 5.32. Assuming that the Flip-Flips register set-up time, clock-to-q, and clock-skew are each 0.1 ns, determine the upper bound for its clock frequency. Propagation delay for AND gate is 0.2 ns and EOR is 0.3 ns. (10 pts)

Ans: 1.67ghz

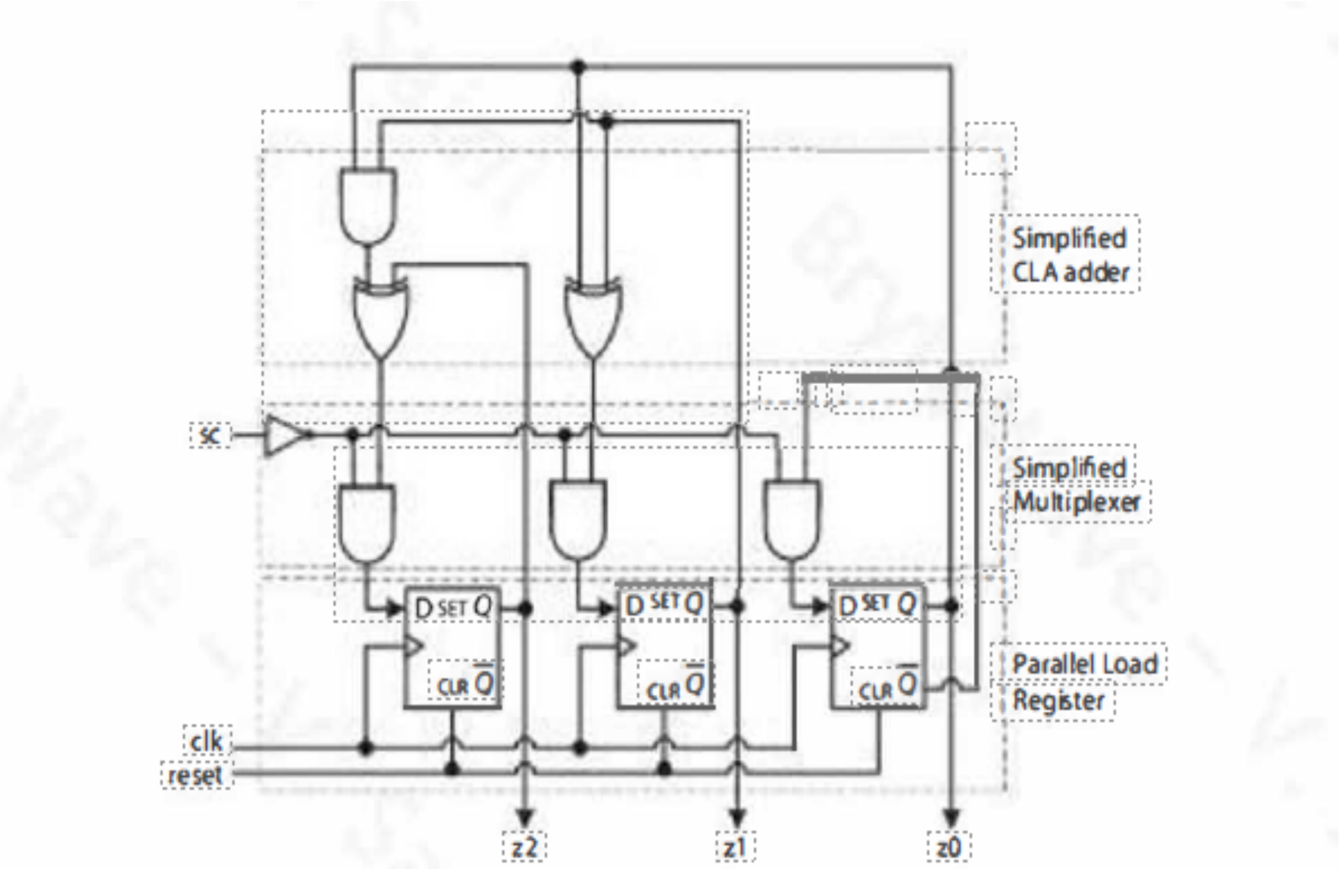


FIGURE 5.32 A synchronously cleared bit-parallel mod-8 up-counter using a simplified CLA adder and a simplified MUX.

$t\_critical = t\_clk\_to\_q + t\_CLA + t\_MUX$

$t\_critical = 0.1\,ns + 0.2ns + 0.3ns = 0.6ns$

$f\_max = \frac{1}{t\_critical} = \frac{1}{0.6ns} = 1.67\,Ghz$

4. What is the 16-bit FP number representation of -10.3 in hexadecimal with 1-bit sign, 4-bit biased exponent, and 11-bit fraction, where bias offset = 7? Please identify the key components of FP number representation (20 pts)

-10.3

10/2 = 5 remainder = 0

5/2 = 2 remainder = 1

2/2 = 1 remainder = 0

1/2 = 0 remainder = 1

10 in binary = 1010

.3x2 = .6 0

.6x2 = 1.2 1

.2x2 = .4 0

.4x2 = .8 0

.8x2 = 1.6 1

.6x2 = 1.2 1

.2x2 = .4 0

.4x2 = .8 0

.3 in binary = .01001100

-10.3 = 1010.01001100

11 01 = D

0010 = 2

0 100 = 4

11 00 = C

$\boxed{D 2 4 C}$

-10.3 in 16 bit format is 1 1010 01001001100

sign bit is 1

exponent bits are (7+3=10) = 1010

10/2 = 5 0

5/2 = 2 1

2/2 = 1 0

1/2 = 0 1

10 = 1010

significant bits are 01001001100

5. Stated below is the equation that estimates the minimum clock period (τ_m) required to run the Multicycle data path. How many cycles (clock cycles) will be required to complete portion of the computation A + B ? The whole Computation is A + B + C + D or A + B + C – D. (10 pts)

I attached a 2nd pdf with the remainder of my work !!!

Ans: .79413

$$\tau_m >= \Delta_{mux1} + \Delta_{add/sub} + \Delta_{mux2} + T_{st} + T_{cq} + T_{cs}$$

$\tau_m = \tau$-multicycle

A multi cycle algorithm to implement R <---- A + B + C + D or A + B + C – D; (5 possible simple operations)

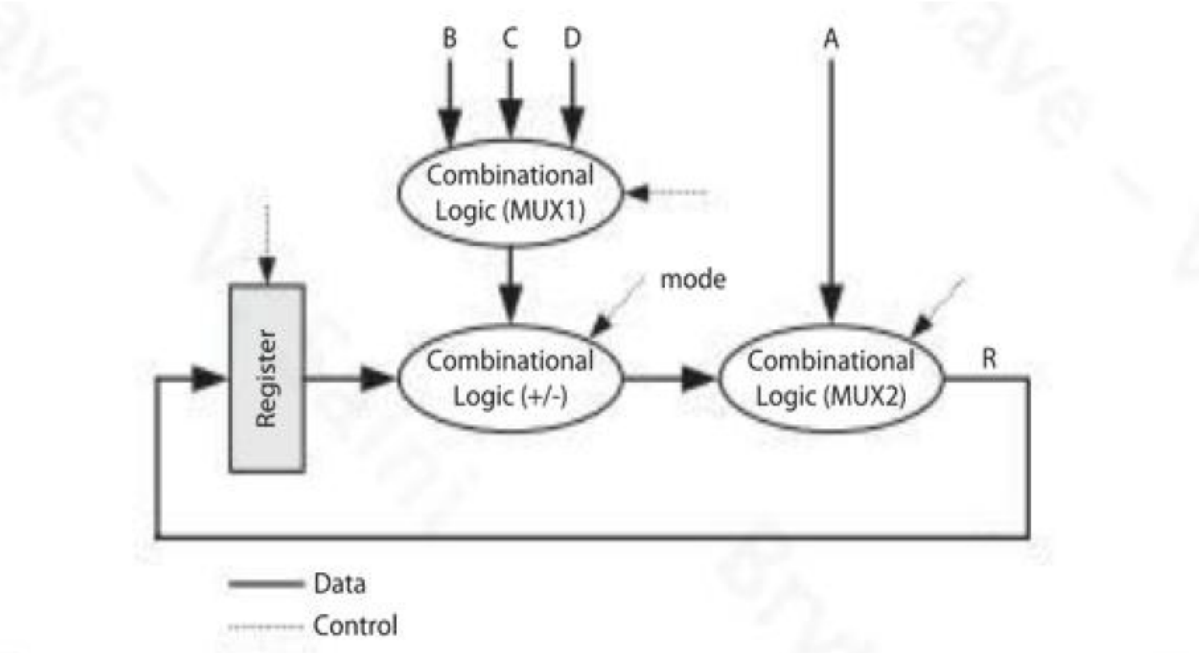

B
C
D
A
Combinational Logic (MUX1)
mode
Register
Combinational Logic (+/-)
Combinational Logic (MUX2)
R
Data
Control

FIGURE 6.3 A multicycle data path requiring four clock cycles to compute $A+B+C+D$ or $A+B+C-D$.

Tm = T_multicycl

$C_0 = \cancel{0}0/2 =$

$C_1 = \frac{J\cdot 20}{2\pi 1}$,

$C_2 = \frac{J\cdot 20}{2\pi\cdot 2}$ –

$C_3 = \frac{J\cdot 20}{2\pi\times 3}$, J

$c_{yk} = H(jk\omega_0)\, c_{kx}$

c_{yk} = at k = 0

$c_{y0} = 2\times 10 = 20$

J $c_{y1} = 1.96\angle -11.30 \times \frac{10}{\pi}\angle 90° = 6.23\angle 73.7°$

$c_{y2} = 1.856\angle 21.80 \times \frac{5}{\pi}\angle 90° = 2.95\angle 68.2°$

J $c_{y3} = 1.71496\angle 30.96 \times \frac{10}{3\pi}\angle 90° =$

$1.81\angle 59.04°$

6. Consider a 16-bit data bus SDRAM. Given that the clock frequency of the bus is 100MHz, what is the peak memory bandwidth in megabyte per second (MBs)? (10 pts)

$$\frac{100 \cdot 10^6 \ \frac{\text{cycle}}{\text{sec}} \times 16 \text{ bit}}{8 \text{ bytes per bit}} = 200 \times 10^6 \text{ B/s} = \boxed{200 \text{ MB/s}}$$

7. Computation is performed by a RISC ISA. A = B * (C + D). What is the value in R4 after the execution of code line # 5: (M[B] = 6; M[C] = 11; M[D] = 15) ie: Code line # 5 has been completed. (10 pts)

What is the value of R4 after execution of Line # 5 - MUL R5, R3, R4 R4 = 6

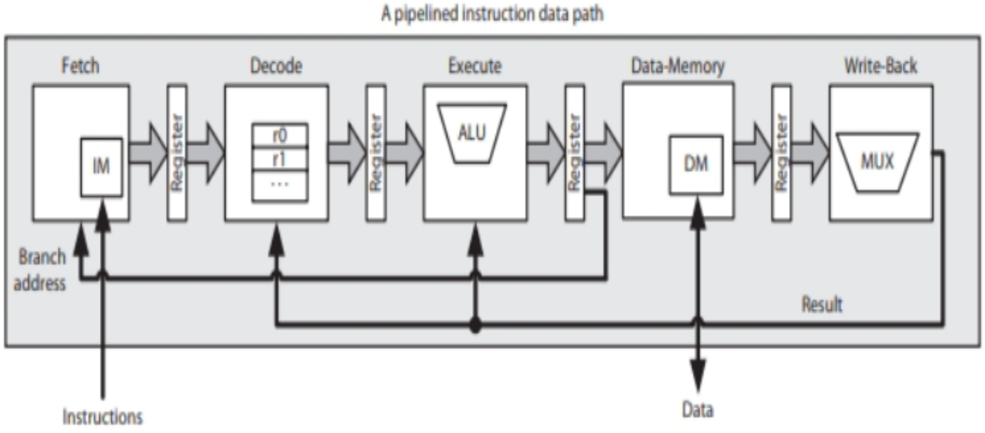


FIGURE 8.17 A five-stage RISC-ISA pipelined data path.

LD R1 (c)

RISC-ISA: Example of assembly program

```
1. LD     R1,    (C)
2. LD     R2,    (D)
3. ADD    R3,    R1, R2
4. LD     R4,    (B)
5. MUL    R5,    R3, R4
6. ST     (A),   R5
```

①

Fetch: LD R1, (C)

Decode: LD R1, (C)

Execute: (memory operation)

Data Memory: Load M[C] into R1 (M[C] = 11

write back: No write backs for code.

② LD R2 (D)

Fetch: LD R2, (D)

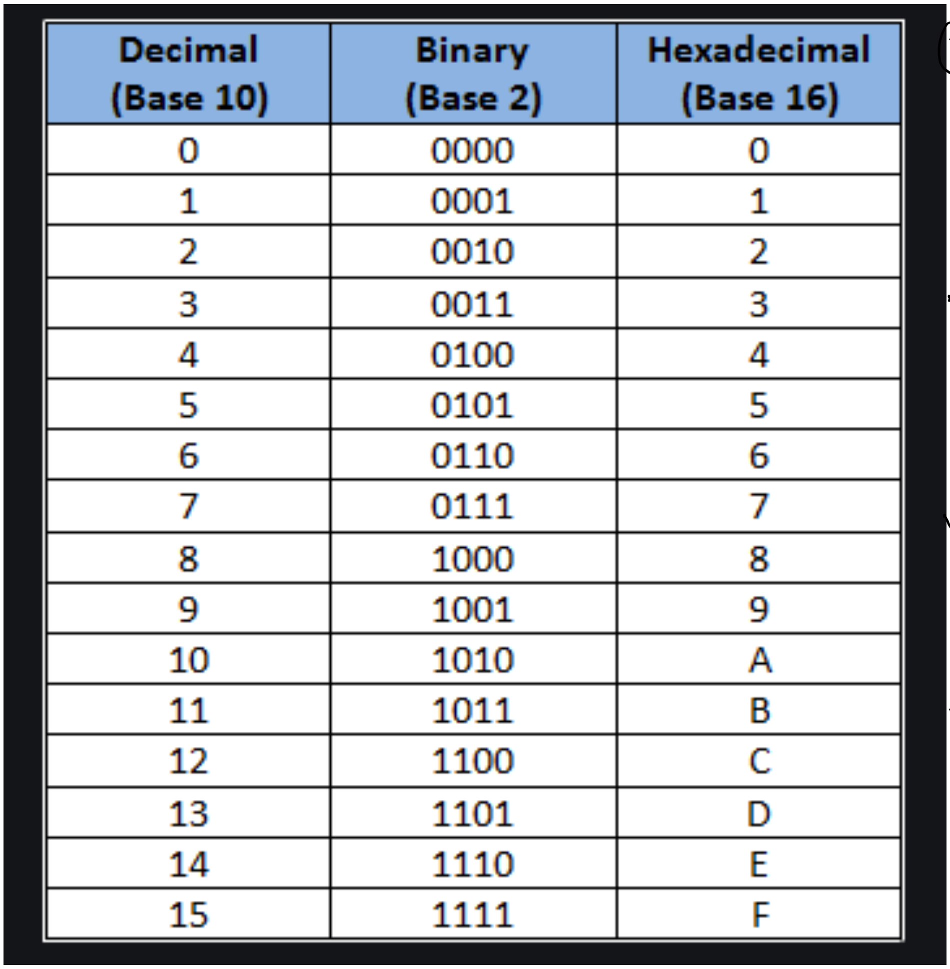
Decode: LD R2, (D)

Execute L (memory operation)

Data Memory: (Load M[D] into R2 (M[D] = 15)

write-back: (no write-back for loads)

Decimal to Binary to hexadecimal Number Conversion Table



Decimal (Base 10)	Binary (Base 2)	Hexadecimal (Base 16)
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

④ ADD R3 R1 R2

Fetch: ADD R3, R1, R2

Decode: ADD R3, R1, R2

execute: Add values in R1 & R2 store result in R3

Data mem: no data mem

write-back: write the result to r3.

③ Add R3, R1, R2:

Fetch: ADD R3, R1, R2

Decode: ADD R3, R1, R2

execute: ADD values in R1 & R2, store result in R3

Data memory: no Data mem

write back: write the result to r3

MUL R5, R3, R4:

- Fetch: MUL R5, R3, R4
- Decode: MUL R5, R3, R4
- Execute: Multiply the values in R3 & R4 store result in R5
- R5 = 156