

1. Using analytical methods calculate the following for the given set of tasks:

- Calculate the system hyperperiod: which value = Least Common Multiplier of all tasks periodicities:

Button_1_PERIOD	50
Button_2_PERIOD	50
Transmitte_PERIOD	100
Receive_PERIOD	20
LOAD_1_PERIOD	10
LOAD_2_PERIOD	100

Hyperperiod=100

- Calculate the CPU load:

- "button1_monitor" & "button2_monitor" tasks execution time: 14 uSec (2 Hyperperiod)
- "periodic transmitter" task execution time: 18.8uSec (1 Hyperperiod)
- "uart receiver" task execution time: 22.3 uSec (5 Hyperperiod)
- "load1_simulator" and "load2_simulator" tasks execution time: 5 mSec (10 Hyperperiod) and 12 mSec (1 Hyperperiod)

$CPU_L = ((14 \mu s * 2) * 2 + 18.8 \mu s + 22.3 \mu s * 5) + 5 ms * 10 + 12 ms / 100 ms) * 100\%$

$= 136 \mu s + 50 ms + 12 ms / 100 ms * 100\% = 62.136\%$

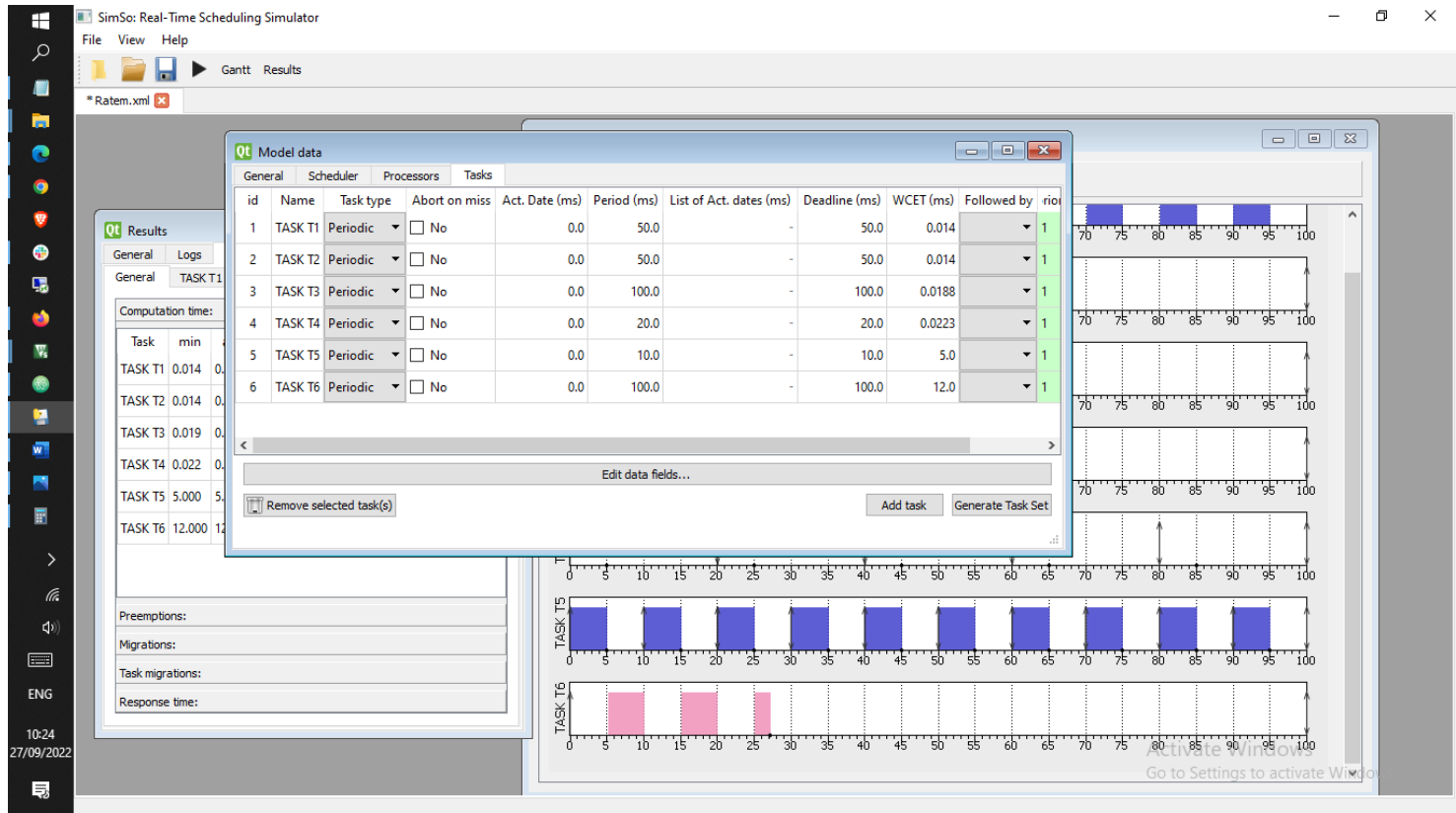
- Check system schedulability using URM and time demand analysis techniques (Assuming the given set of tasks are scheduled using a fixed priority rate-monotonic scheduler):

$U \leq n[2^{1/n} - 1]$, $n=6 \rightarrow U_{rm} = 6(2^{1/6} - 1) = 0.734$

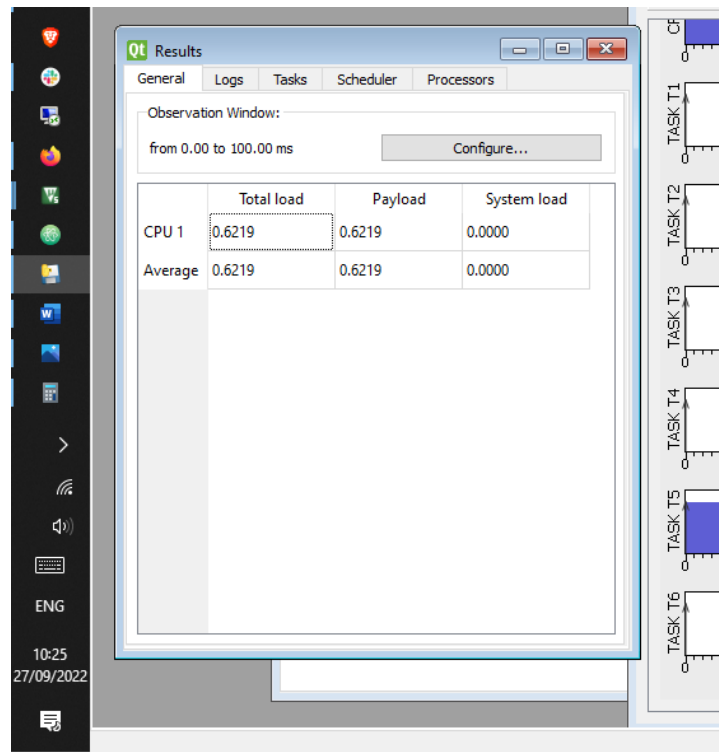
$U = \sum C_i/P_i = 14 \mu s / 50 ms + 14 \mu s / 50 ms + 18.8 \mu s / 100 ms + 22.3 \mu s / 20 ms + 5 ms / 10 ms + 12 ms / 100 ms = 0.620748$

, Then $U < U_{rm} \rightarrow$ it's **Schedulable** Systems.

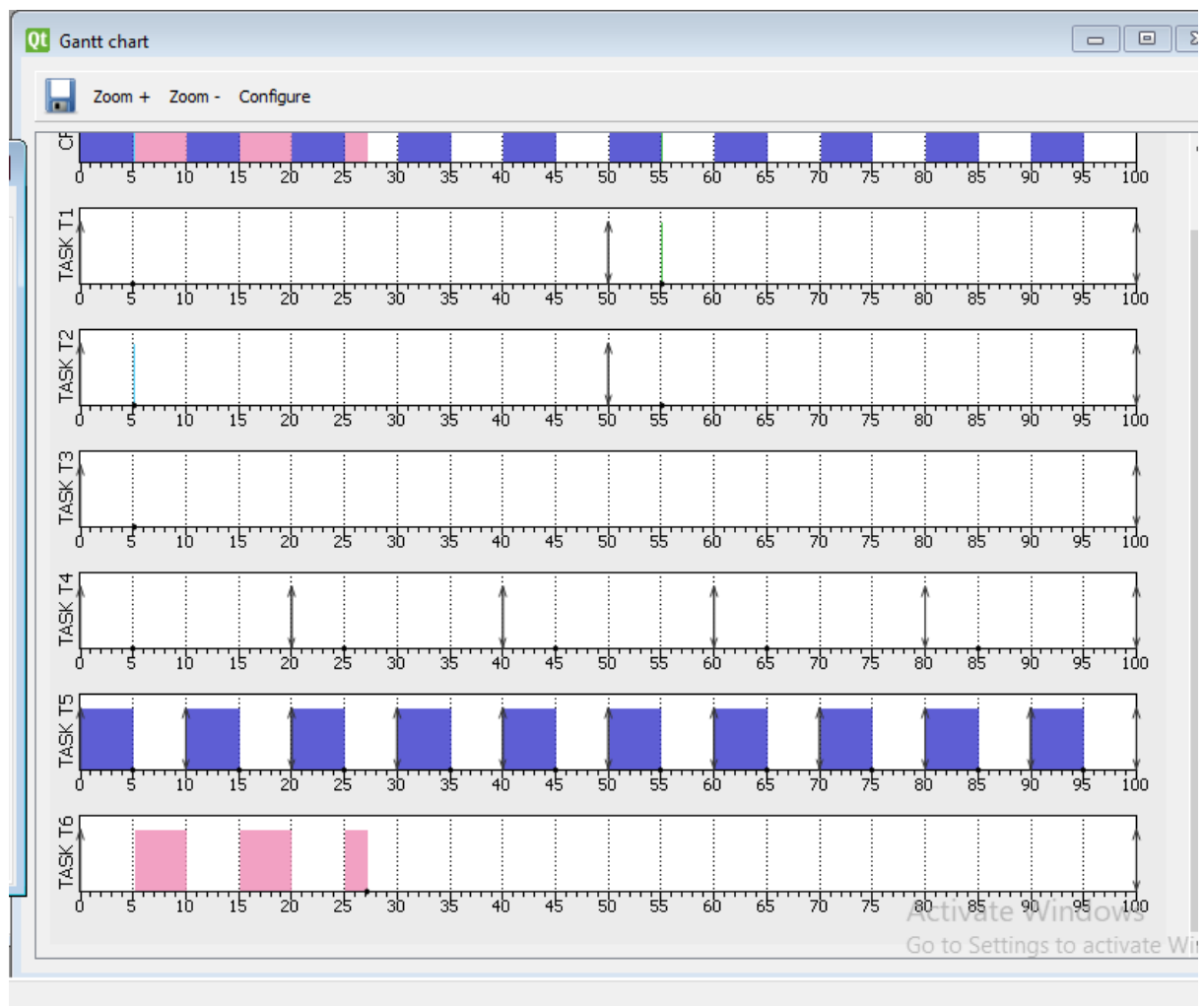
2. Using Simso offline simulator, simulate the given set of tasks assuming:



- CPU Load:



- Gantt chart



- CPU Load and Logic Analyzer

The CPU load is 62% as showed, so the system is not too much loaded and worked successful.

Watch 1	
Name	Value
cpu_Load	62
system_Time	10277333
button_1_TaskTotalTime	3863
button_2_TaskTotalTime	3943
periodic_TaskTotalTime	2997
uart_TaskTotalTime	10085
load_1_TaskTotalTime	5188870
load_2_TaskTotalTime	1244440

The screenshot shows the uVision IDE interface. The main window displays the source code for `main.c` with the following code snippet:

```

479 for( i=0 ; i <= x1Tick; i++) { /*12 ms delay*/
480
481     vTaskDelayUntil( &xLastWakeTime , LOAD_2_PERIOD);
482
483     /*pin inection of idel task*/
484     GPIO_write(PORT_0, PIN0, PIN_IS_LOW);
485 }
486
487

```

The Logic Analyzer window shows a timing diagram with multiple channels. The channels are labeled as follows:

- Channel 1: ...000>> 17
- Channel 2: ...000>> 16
- Channel 3: ...000>> 18
- Channel 4: ...000>> 19
- Channel 5: ...000>> 20
- Channel 6: ...000>> 21
- Channel 7: ...000>> 22
- Channel 8: ...000>> 23
- Channel 9: ...000>> 24
- Channel 10: ...000>> 25

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The General Purpose Input/Output 0 (GPIO 0) window shows the following configuration:

IO0DIR	IO0SET	IO0CLR	IO0PIN
0xEFFF0000	0x00010000	0x00000000	0x0001FCFF

The Logic Analyzer window also shows a timing diagram with a time scale of 135.6299 s to 135.6304 s. The diagram shows multiple channels of digital signals, with some channels showing a transition from 0 to 1.