

I Made up top level is 8x3Mux.

Deficiencies

It works on Alu part except mult. For Mult, control.v works in part 1, I loaded the test, I can navigate through the states, I wrote dede shift and adder functions in datapath, but I could not do the binding part, so mult also does not work.

32bitadder

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help

ColumnLayout Default

sim - Default

Instance Design unit Design unit type Visibility Total coverage

32bit_adder_test 32bit_adder Module +ACC=<...

adder32bit 32bit_adder Module +ACC=<...

4bit_adder 4bit_adder Module +ACC=<...

FA0 full_adder Module +ACC=<...

first_half_adder Module +ACC=<...

seco...half_adder Module +ACC=<...

final...full_adder Process +ACC=<...

FA1 full_adder Module +ACC=<...

FA2 full_adder Module +ACC=<...

FA3 full_adder Module +ACC=<...

4bit_adder 4bit_adder Module +ACC=<...

4bit_adder 4bit_adder Module +ACC=<...

Objects

Name Value Kind Mode

a SIO Net In

b SIO Net In

sum SIO Net Out

carry_out SIO Net Out

Processes (Active)

Name Type (filtered) State Order Parent Path

Wave - Default

Now 0.00 ns

Cursor 1 0 ns 0.00 ns 0.5 ns

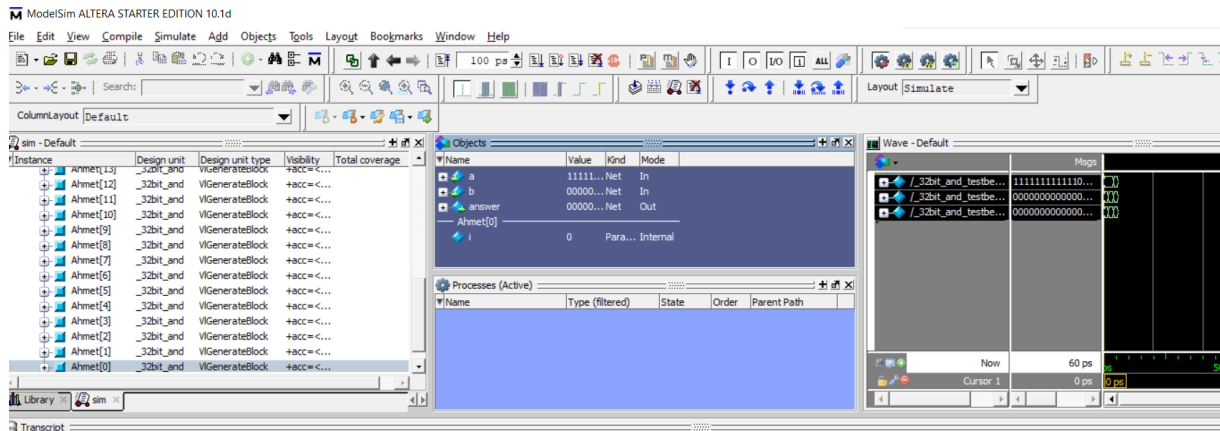
Transcript

```
# -- Compiling module _32bit_adder
#
# Top level modules:
# _32bit_adder
vlog -reportprogress 300 -work work C:/altera/13.1/workspaces/hwl/_32bit_adder_test.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov 2 2012
# -- Compiling module _32bit_adder_test
#
# Top level modules:
# _32bit_adder_test
ModelSim> vsim work._32bit_adder_test
# vsim work._32bit_adder_test
# Loading work._32bit_adder_test
# Loading work._32bit_adder
# Loading work.full_adder
# Loading work.half_adder
VSM6> step -current
# time = 0, a = 11111111, b= 99999999, answer= aaaaaaa,carry_out=0 ,carry_in=0
```

In 32 bit adder file I call 4 bit adder 8 times and I create a 32 bit adder.

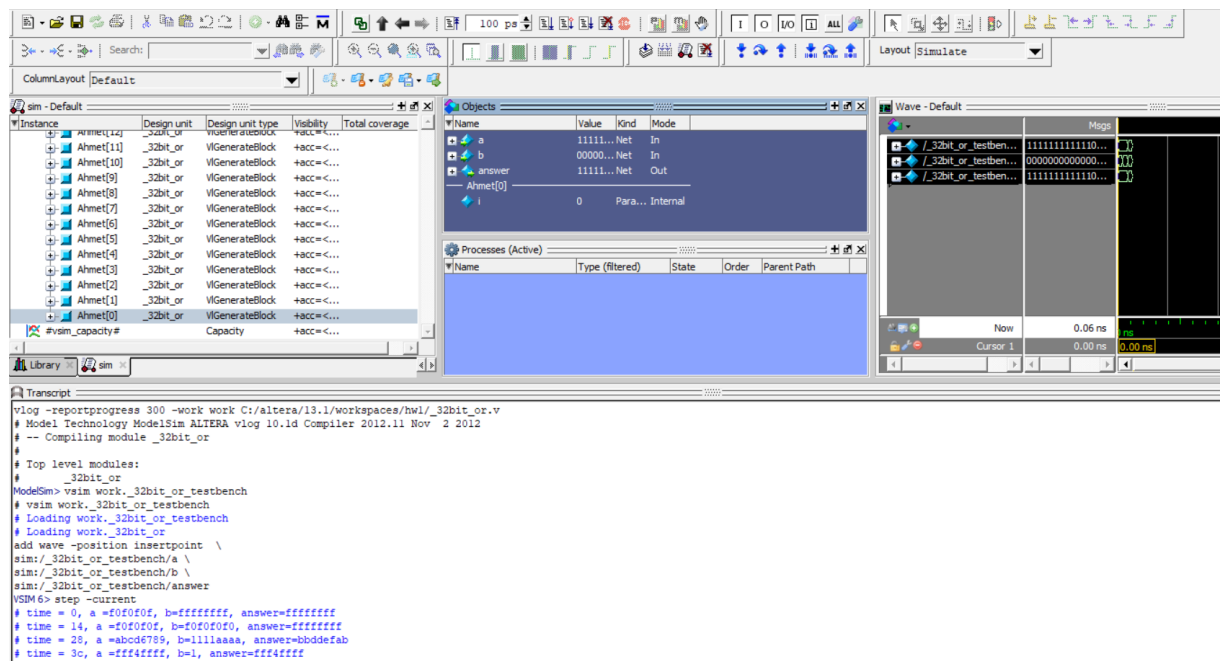
I send zero to carry_in .

32bitand



I call and operator 32 times.

32bitor



I call lor operator 32 times.

32bitslt

The screenshot displays the ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov 2 2012 interface. The Project Navigator on the left shows the design hierarchy for the 32-bit subtractor. The Objects window in the center lists the variables: 'a' (SIO Net In), 'b' (SIO Net In), 'sum' (SIO Net Out), and 'carry_out' (SIO Net Out). The Processes (Active) window is empty. The Wave window on the right shows the simulation timeline with a cursor at 0.00 ns. The Transcript window at the bottom shows the simulation log, including the compilation of the module _32bit_slt_test and the loading of the work directory.

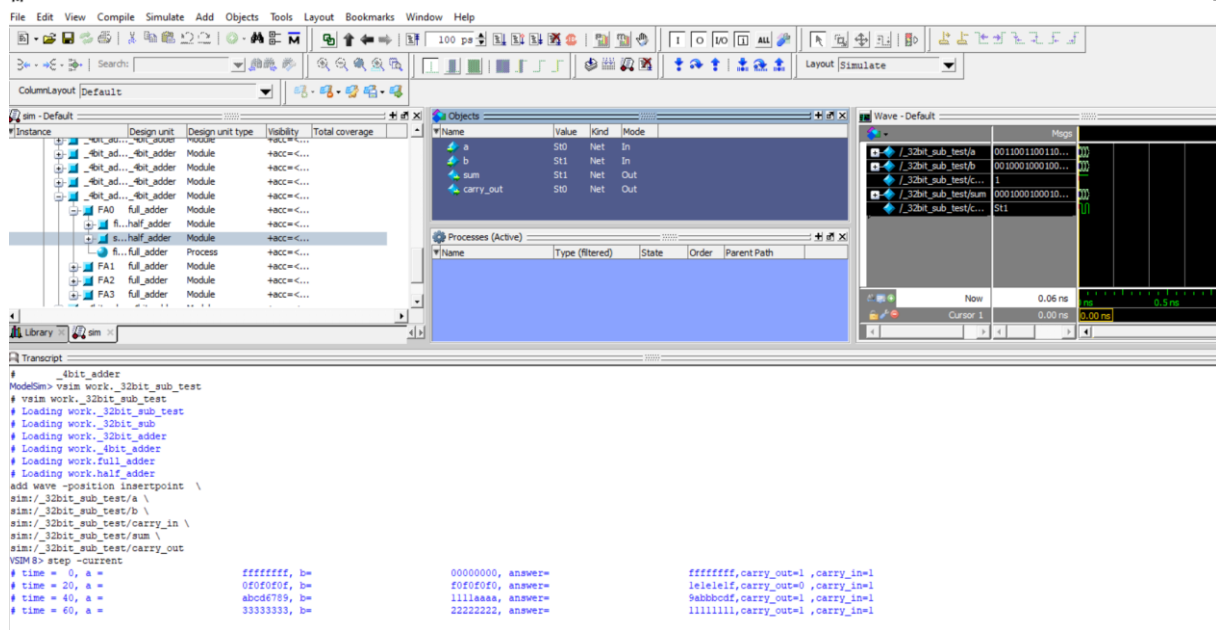
```

# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov 2 2012
# -- Compiling module _32bit_slt_test
#
# Top level modules:
#
# _32bit_slt_test
ModelSim> vsim work._32bit_slt_test
# vsim work._32bit_slt_test
# Loading work._32bit_slt_test
# Loading work._32bit_slt
# Loading work._32bit_sub
# Loading work._32bit_adder
# Loading work._4bit_adder
# Loading work.full_adder
# Loading work.half_adder
vSIM9> step -current
# time = 0, a = ffffffff, b= 00000000, carry_out=1 ,carry_in=0,result=1
# time = 20, a = 0f0f0f0f, b= f0f0f0f0, carry_out=0 ,carry_in=0,result=0
# time = 40, a = 11111111, b= 33333333, carry_out=0 ,carry_in=0,result=1
# time = 60, a = 33333333, b= 22222222, carry_out=1 ,carry_in=0,result=0

```

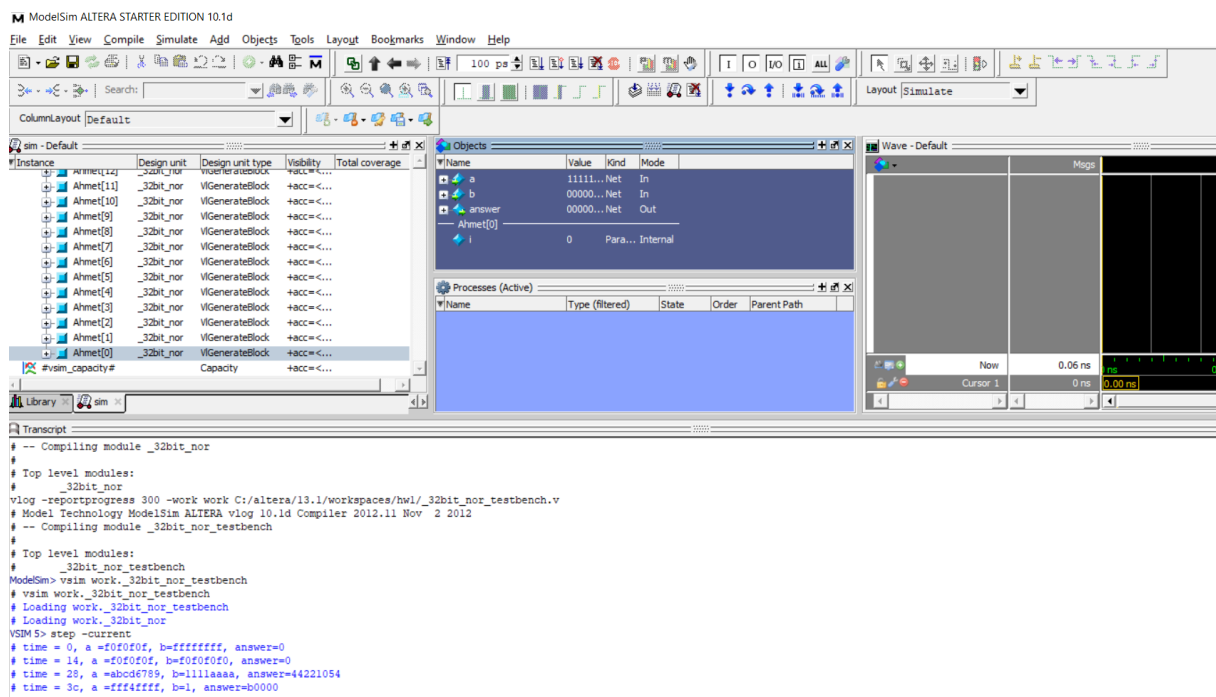
I call sub operator and I take most significant bit to result then I turned it.

32bitsub



I call adder operation before called adder operation i xor the B with select bit 32 times then i take B' so B is turned to B' so i can add A + (-B) then i return result.

32bit nor



I called 32 times nor operatör.

32bitxor

The screenshot shows the Altera ModelSim simulation environment. The main window displays the simulation results for a 32-bit XOR testbench. The Instance pane on the left lists 32 instances of the _32bit_xor module, each with a design unit of _32bit_xor and a design unit type of VGenerateBlock. The Objects pane in the center shows the signals a, b, answer, and i. The Wave pane on the right displays the timing of these signals, with a cursor at 0.00 ns. The Transcript pane at the bottom shows the simulation log, including the compilation of the _32bit_xor module and the simulation results for the 32-bit XOR operation.

```

log -reportprogress 300 -work work C:/altera/13.1/workspaces/hwl/_32bit_xor_testbench.v
Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
-- Compiling module _32bit_xor_testbench

Top level modules:
  _32bit_xor_testbench
ModelSim> vsim work._32bit_xor_testbench
vsim work._32bit_xor_testbench
Loading work._32bit_xor_testbench
Loading work._32bit_xor
add wave -position insertpoint \
sim:/_32bit_xor_testbench/a \
sim:/_32bit_xor_testbench/b \
sim:/_32bit_xor_testbench/answer
SIM 6> step -current
time = 0, a =f0f0f0f, b=ffffff, answer=f0f0f0f0
time = 14, a =f0f0f0f, b=f0f0f0f0, answer=ffffff
time = 28, a =ab0d6789, b=11111111, answer=badcod23
time = 3c, a =fff4ffff, b=1, answer=fff4ffff
  
```

I called xor operator 32 times.

Control Unit states

The screenshot displays the ModelSim ALTERA STARTER EDITION 10.1d interface. The main workspace is divided into several panels:

- Project Browser (Left):** Shows the design hierarchy with components like `Control_32bit_testbench`, `ctrl`, `#ALWAYS#19`, `#INITIAL#32`, and `#vsim_capacity#`.
- Objects Panel (Top Center):** A table listing simulation objects.

Name	Value	Kind	Mode
clk	0	Regis...Internal	
rst	1	Regis...Internal	
lsb	1	Regis...Internal	
lt	1	Regis...Internal	
multplicand	xxxxx	Pack	Internal
- Processes (Active) Panel (Bottom Center):** A table listing active processes.

Name	Type (filtered)	State	Order	Parent Path
#INITIAL#32	Initial	Active	1	/Control_32bit_te...
#ALWAYS#19	Always	Ready	2	/Control_32bit_te...
- Source Code (Right):** Shows the VHDL code for `Control_32bit_testbench`, with line numbers 46 through 57 visible. The code includes an `initial` block and an `endmodule` statement.
- Transcript (Bottom):** Displays the simulation log, including the loading of the testbench and the current state of the simulation at 50 ps.

In control units I reach the states one by one according to lsb and lt inputs .

According to the boolean expression that created using fsm and truth table I find next states .

Then present state will change clk cycles. Write and Shift signal are created then I send datapath these but mult result dont working.

8x3 ALU

ModelSim Altera Starter Edition 10.1

File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help

ColumnLayout: Default

sim - Default

Instance	Design unit	Design unit type	Visibility	Total coverage
_8x3muxTest	_8x3muxTest	Module	+acc=<...	
testmux	_8x3mux	Module	+acc=<...	
Ahmet2[31]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[30]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[29]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[28]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[27]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[26]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[25]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[24]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[23]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[22]	_8x3mux	ViGenerateBlock	+acc=<...	
Ahmet2[21]	_8x3mux	ViGenerateBlock	+acc=<...	

Objects

Name	Value	Kind	Mode
sum	01100...	Net	Out
a	01000...	Net	In
b	00100...	Net	In
select	111	Net	In
F1	01100...	Net	Internal
F2	01100...	Net	Internal

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
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Wave - Default

Msgs
/_8x3muxTest/a
/_8x3muxTest/b
/_8x3muxTest/select
/_8x3muxTest/sum

Now 0.08 ns
Cursor 1 0.00 ns

```

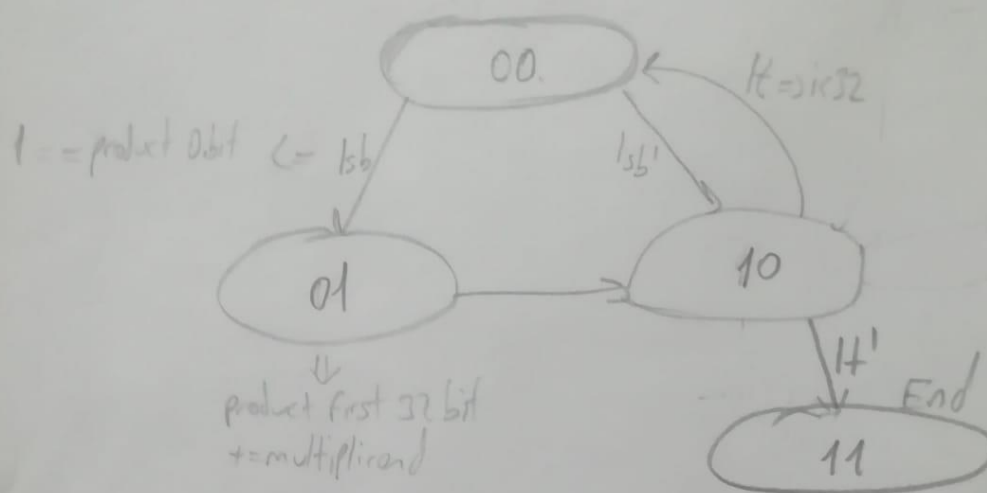
Transcript
sim:/_8x3muxTest/select \
sim:/_8x3muxTest/sum
VSIW 14> step -current
# Add -> time = 5, a = 33333333, b= 22222222,select=000 ,sum= 55555555
# Xor -> time = 10, a = 33333333, b= 22222222,select=001,sum= 11111111
# Sub -> time = 15, a = 33333333, b= 22222222,select=010,sum= 11111111
# Mult -> time = 20, a = 33333333, b= 22222222,select=011,sum= 00000000
# Slt -> time = 25, a = 33333333, b= 22222222,select=100,sum= 00000000
# Nor -> time = 30, a = 33333333, b= 22222222,select=101,sum= 00000000
# And -> time = 35, a = 33333333, b= 22222222,select=110,sum= 22222222
# Or -> time = 40, a = 44444444, b= 22222222,select=111,sum= 66666666
#
# Add -> time = 45, a = 44444444, b= 22222222,select=000 ,sum= 66666666
# Xor -> time = 50, a = 44444444, b= 22222222,select=001,sum= 66666666
# Sub -> time = 55, a = 44444444, b= 22222222,select=010,sum= 22222222
# Mult -> time = 60, a = 44444444, b= 22222222,select=011,sum= 00000000
# Slt -> time = 65, a = 44444444, b= 22222222,select=100,sum= 00000000
# Nor -> time = 70, a = 44444444, b= 22222222,select=101,sum= 99999999
# And -> time = 75, a = 44444444, b= 22222222,select=110,sum= 00000000
# Or -> time = 80, a = 44444444, b= 22222222,select=111,sum= 66666666

```

VSIW 15>

I called all modules in alu then i send the result to the A,B...H then using these equation i find the working module then i send it to or gate then i find the working module according to the select bit .(sum=A1S0'S1'S2'+B1S0'S1'S2'+C1S0'S1S2'+D1S0'S1S2'+E1S0S1'S2'+I1S0S1'S2'+G1S0S1S2'+H1S0S1S2)

STATE DIAGRAM



Truth Table

Inputs				Outputs				
s_1	s_0	lsb	lt	n_1	n_0	write	shift	less32
0	0	0	x	1	0	x	x	x
0	0	1	x	0	1	x	x	x
0	1	x	x	1	0	1	x	x
1	0	x	0	1	1	x	1	1
1	0	x	1	0	0	x	1	1
1	1	x	0	1	1	x	1	1
1	1	x	1	0	0	x	1	1

Derive Boolean Expression From the Truth Table

$$n_1 = s_1' s_0' / s_b' + s_1' s_0 + s_1 s_0' / t' s_0' / t'$$

$$n_0 = s_1' s_0' / s_b' + s_1 s_0' / t'$$

$$\text{write} = s_1' s_0$$

$$\text{shift} = s_1 s_0'$$

$$\text{less32} = s_1 s_0'$$

Instead of Mult, I put die or so that the system does not break, sir. I drew fsm for Mult and created tables, then I got boolean expressions and designed control unit. I did add and shift in datapath, but I couldn't combine them all and test, so mult doesn't work.

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HW3 REPORT

