Experiment 5
Operational Amplifiers-I

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Contents

1 Introduction

In this experiment, as students, we are expected to experiment with different kinds of Op-Amp circuits by completing the steps described in the fifth experiment laboratory manual. Throughout these steps, the basic characteristics of Op-Amps and the behavior of the Op-Amp circuits are expected to be learned. The output versus input characteristics is observed by connecting the signal generator to the oscilloscope and the circuit. The nonideal behavior of the componets are compared with the ideal simulation plots. The results of the steps were recorded and plotted for further comments.

2 Experimental Results

In this section, the results of Experiment 5 are discussed. Before the experiment begins neccessary adjustments are done on DC power supply. LM 741 operational amplifier integrated circuit is used in this experiment.

2.1 Step 1

In this step, circuits given in the laboratory manual are constructed and observations are made on them. The results of the experimental work are compared with simulation results done for preliminary work. $V_{in(t)}$ is taken as $3sin(1000\pi)$ Volts for this step.

2.1.1 a.

The basic comparator circuit given in Figure 1 is constructed on a breadboard.

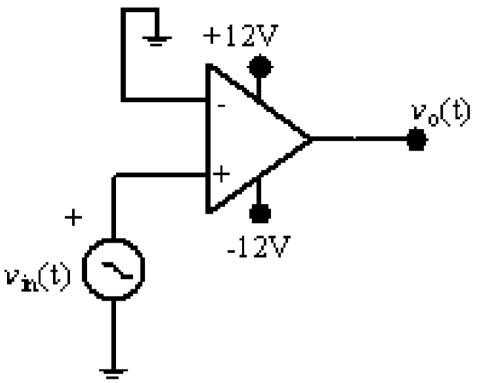

Figure 1: Circuit schematic for the Step 1 part a

Then the V_o vs V_{in} ,given in Figure 2, plotted.

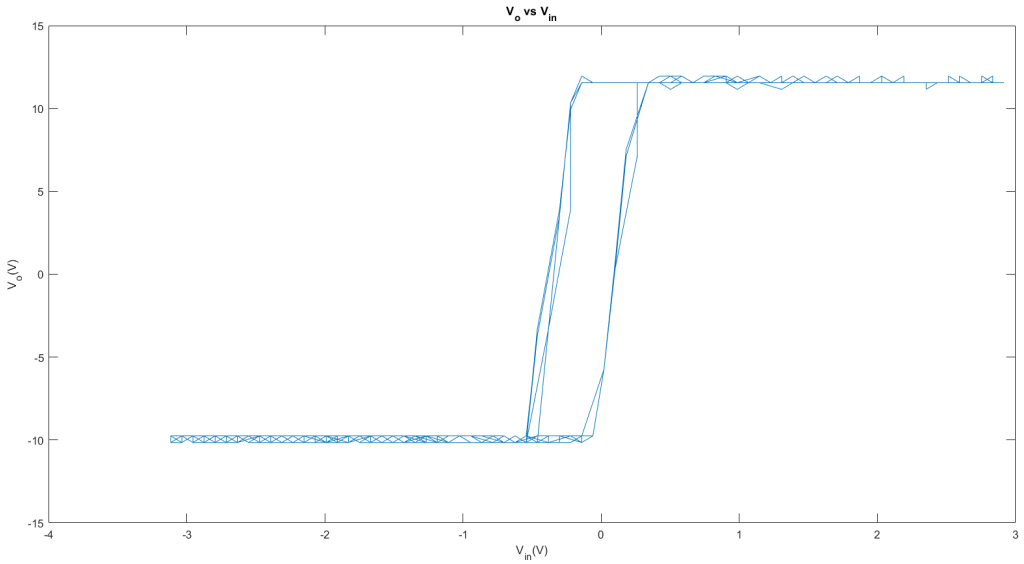

Figure 2: V_o vs V_{in}

It can be said that this Op-Amp configuration compares (with ground) and amplifies the signal propageted to non-inverting terminal. From plot, there is an unexpected gap at the linear region which is stemmed by the non-ideal behavior of the Op-Amp.

Basic comparator circuit is constructed in LTSpice environment as a part of preliminary work. The schematic is given in the Figure 3.

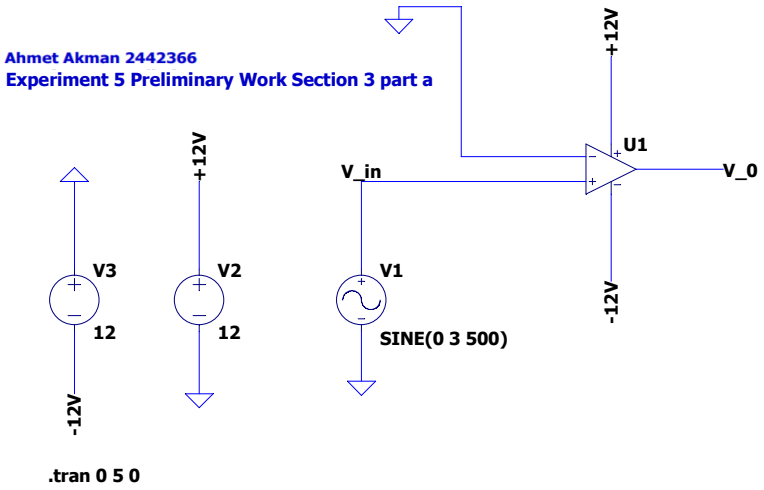

Figure 3: Circuit schematic for the basic comparator.

Then plot given in Figure 4 is obtained.

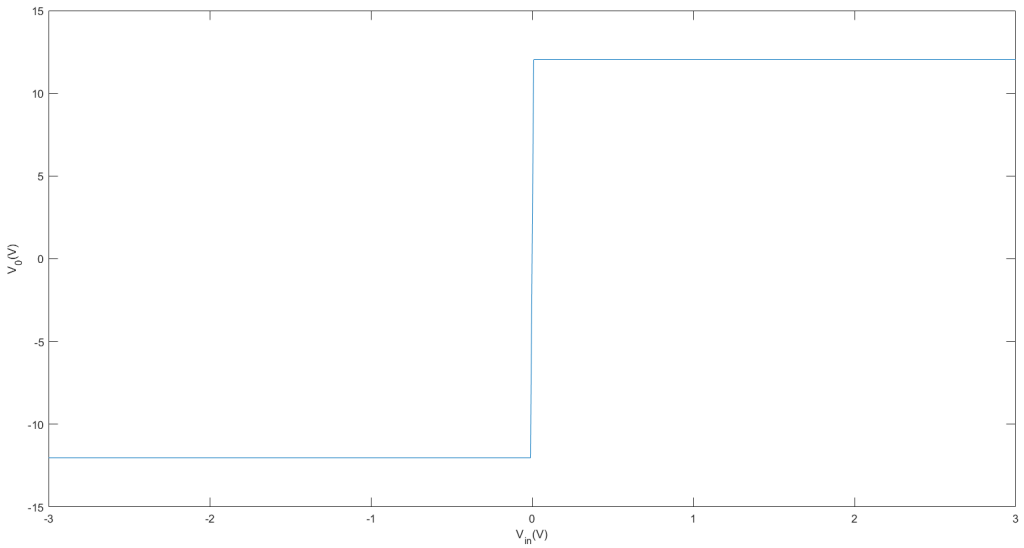

Figure 4: V_o vs Vin

This result show us the opamp model in the LTSpice simulation environment operates

almost like an ideal Op-Amp. The difference between an ideal and a non-ideal Op-Amp can also be observed from Figures 2 and 4.

2.1.2 b.

The buffer circuit is set on a breadboard. The schematic given in Figure 5 is taken as the reference.

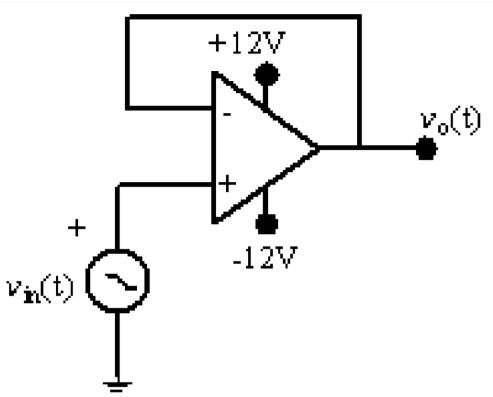

Figure 5: Circuit schematic for the Step 1 part b

The V_o vs V_{in} plot is obtained.

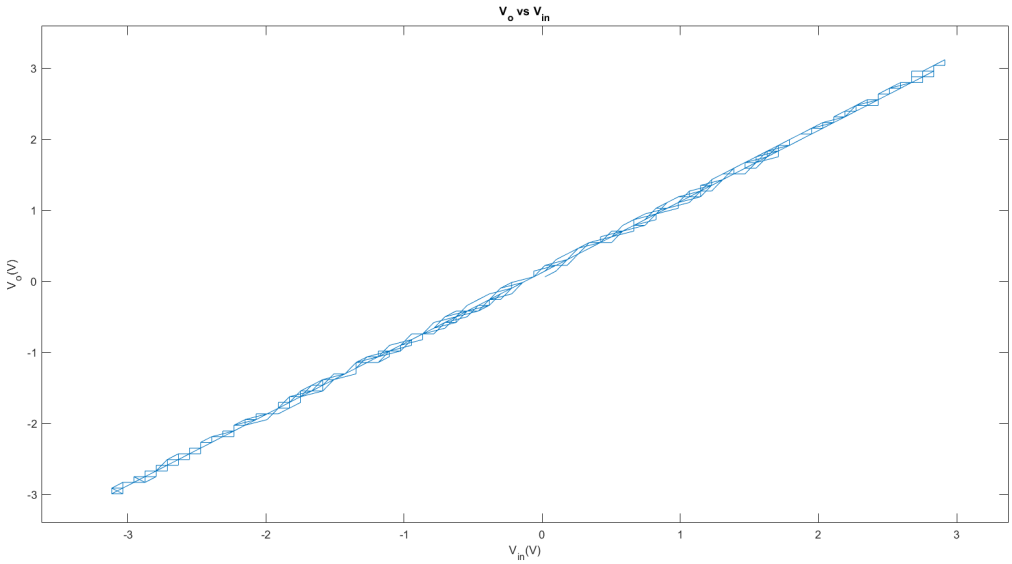

Figure 6: V_o vs V_{in}

As it can be seen from the plot, buffer circuit directly transfer the input voltage to its output terminal. This application can be used to isolate two circuit in order to prevent voltage drop at the source circuit since there is no flowing current . This example is explained in the Step 3.

Buffer circuit is constructed in LTSpice environment. The schematic is given in the Figure 7.

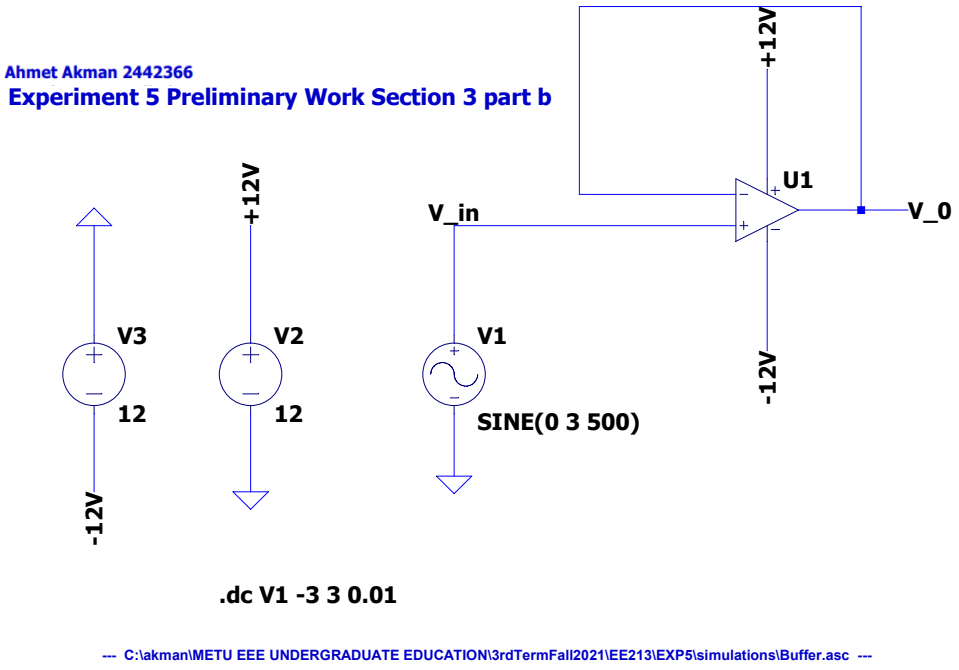

Figure 7: Circuit schematic for the buffer.

Then plot given in Figure 8 is obtained.

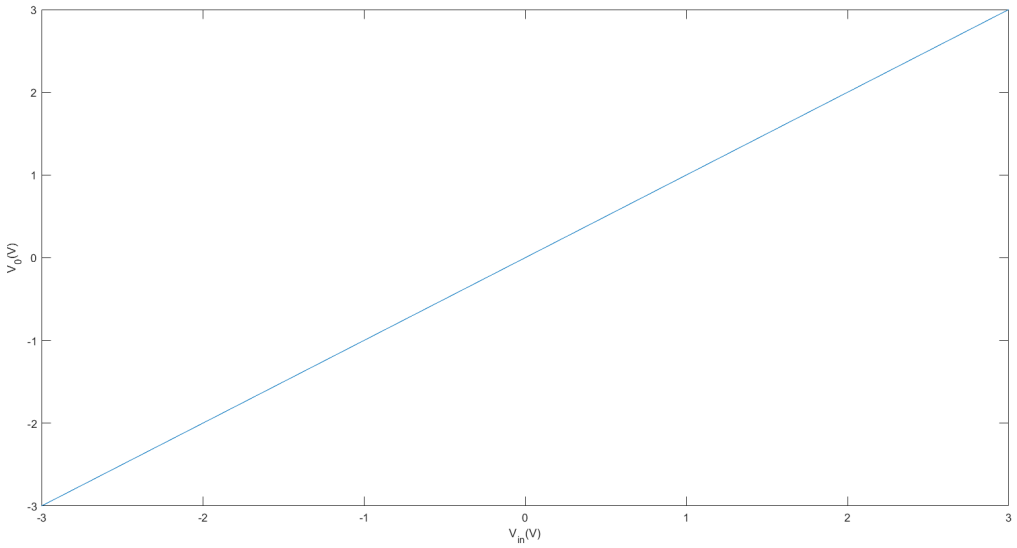

Figure 8: V_0 vs Vin

It can be said that the simulation plot is consistent with the real world experiment plot for the buffer configuration.

2.1.3 c.

The non-inverting amplifier circuit is set on a breadboard at the laboratory. The schematic given in Figure 9 is taken as the reference.

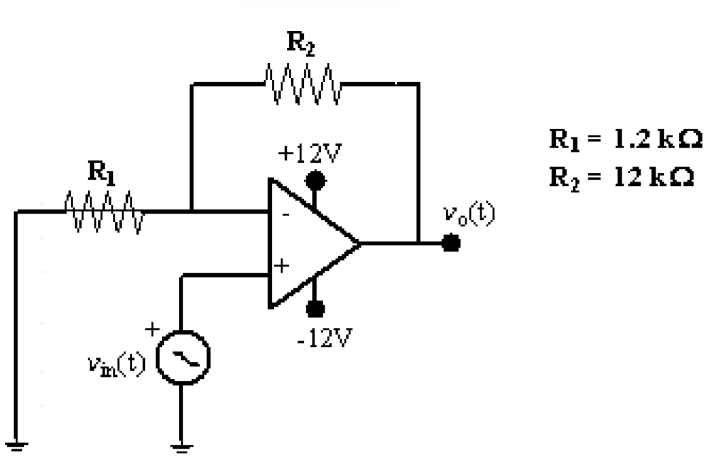

Figure 9: Circuit schematic for the Step 1 part c

Then using both channel oscilloscope probes, measurements taken at the nodes V_o and V_{in}. The plot is given in Figure 10.

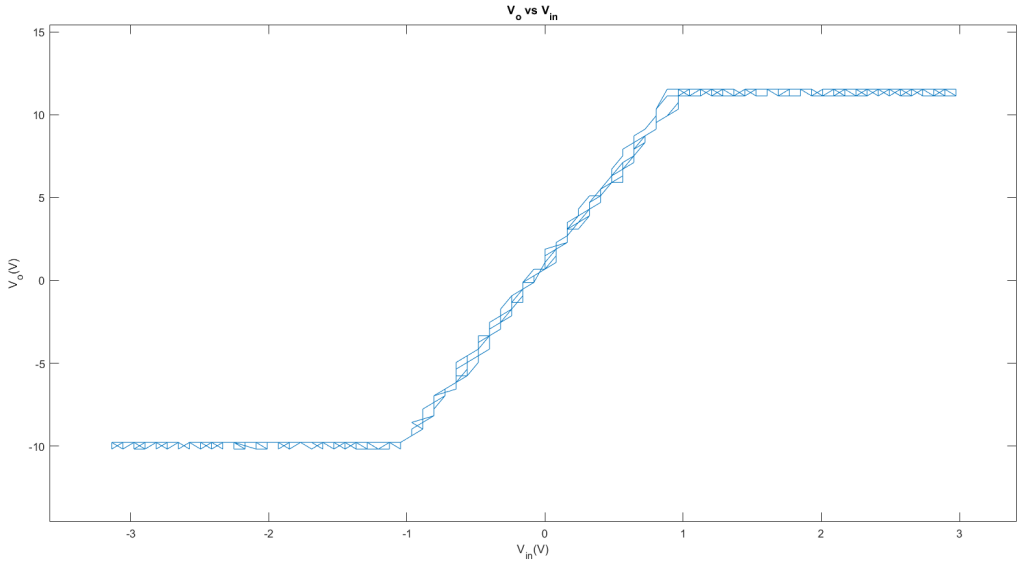

Figure 10: V_o vs V_{in}

The amplification rate can be measured by looking at the slope of the linear region. The slope is read as 11. It can be concluded that non-inverting configuration directly amplifies the signal at the non-inverting terminal according to the relation

$$\frac{Vout}{Vin} = \frac{R_2}{R_1}$$

in linear region as expected. Non-inverting amplifier circuit is constructed in LTSpice environment. The schematic is given in the Figure 11.

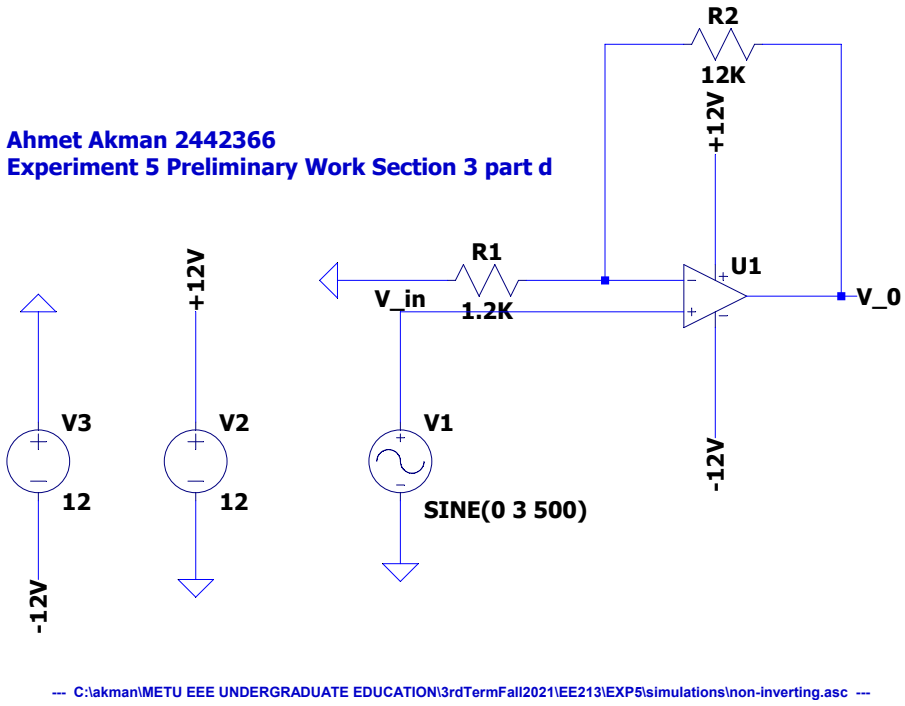

Figure 11: Circuit schematic for the non-inverting amplifier.

Then plot given in Figures 12 is obtained from simulation environment.

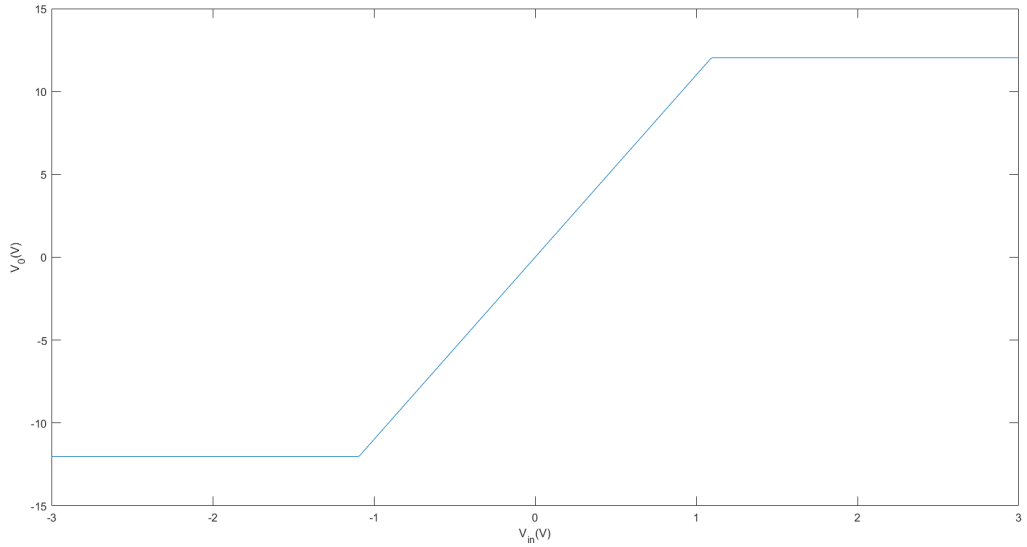

Figure 12: V_0 vs Vin

The amplification rate can be measured by looking at the slope of the linear region. The slope is read sa 11. By looking at the shape of Figure 10 and Figure 11, it can be said that the behavior is consistent. But, the negative saturation region of the real circuit is slightly greater. This is predicted to be stemmed from the non-ideality of the either LM741 component or the negative power line of the power supply.

2.2 Step 2

The inverting amplifier circuit is constructed at the laboratory according to the schematic given in Figure 13.

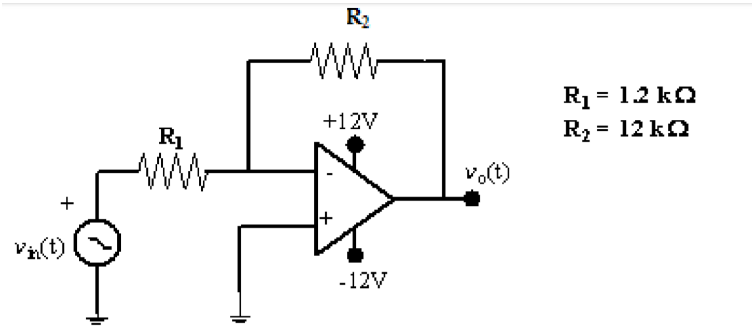

Figure 13: Circuit schematic for the Step 2

The measurement are made using first and second channels of oscilloscope instrument. Therefore, the plot in Figure 14 describes V_o vs V_{in} relation is obtained.

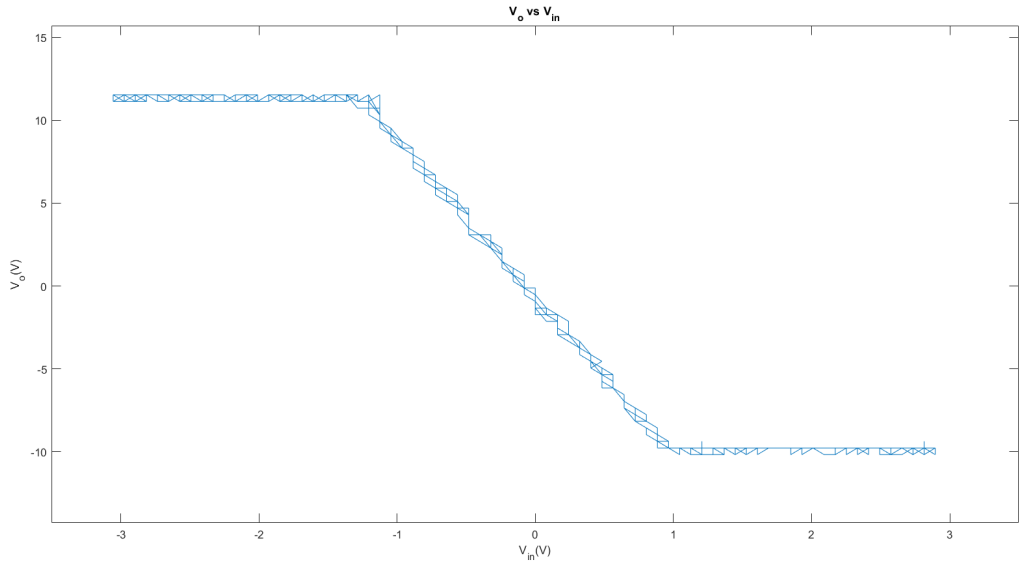

Figure 14: V_o vs V_{in}

It can be inferred that the amplifier amplifies the signal at the inverting channel by inverting. To obtain the expression relating the output voltage $V_0(t)$ to the input voltage $V_{in}(t)$ of a inverting amplifier setup, the circuit in Figure 13 is taken as the reference. Then current throught input terminals and the voltage of those terminals are taken as 0 since it is ideal amplifier. So the circuit simplifies to 2 terminals and 2 resistors. Then the following simplifications are followed.

$$\frac{Vin - 0}{R_1} = i$$

$$\frac{0 - Vo}{R_2} = i$$

So, the relation becomes as,

$$\frac{Vout}{Vin} = -\frac{R_2}{R_1}$$

Therefore it seems linear region of the plot given in Figure 14 approximately corresponds measurements. Which the signal is amplified by multiplying -11. Inverting amplifier circuit is constructed in LTSpice environment. The schematic is given in the Figure 15.

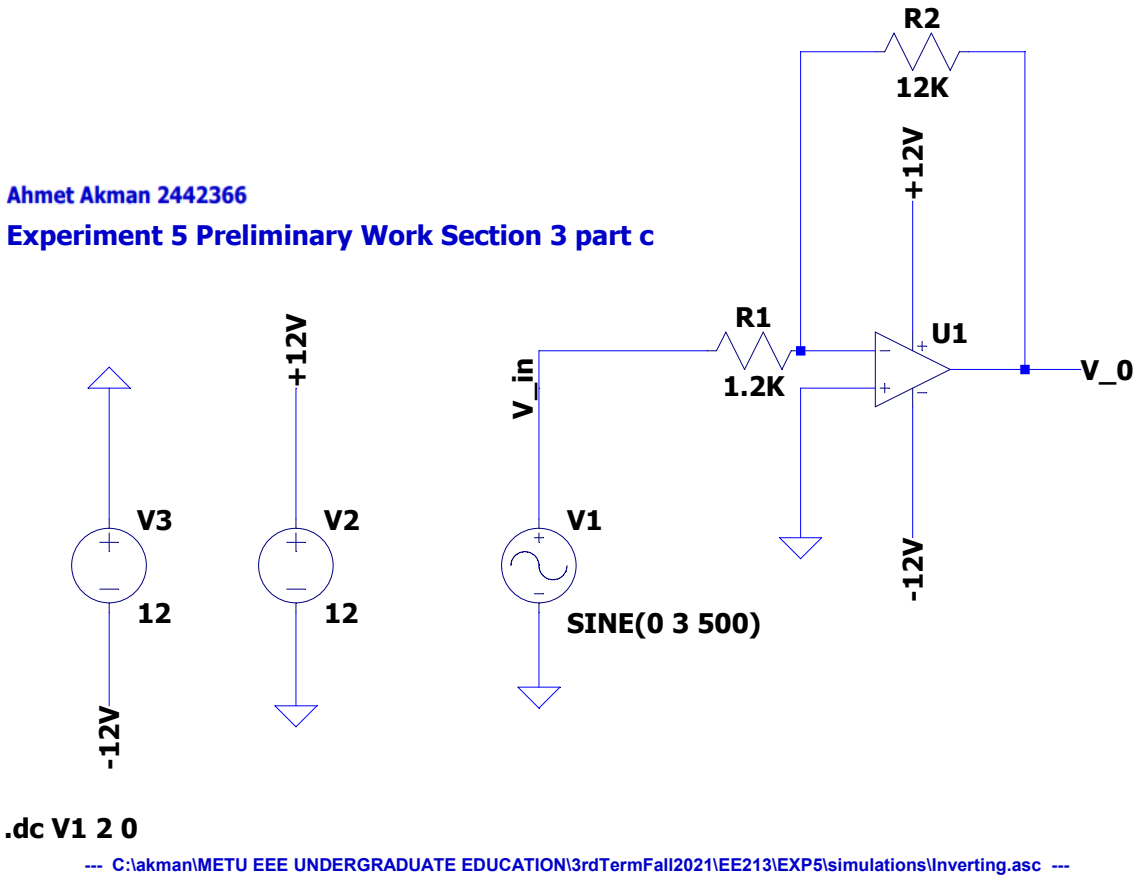

Figure 15: Circuit schematic for the inverting amplifier.

Then plot given in Figure 16 is obtained.

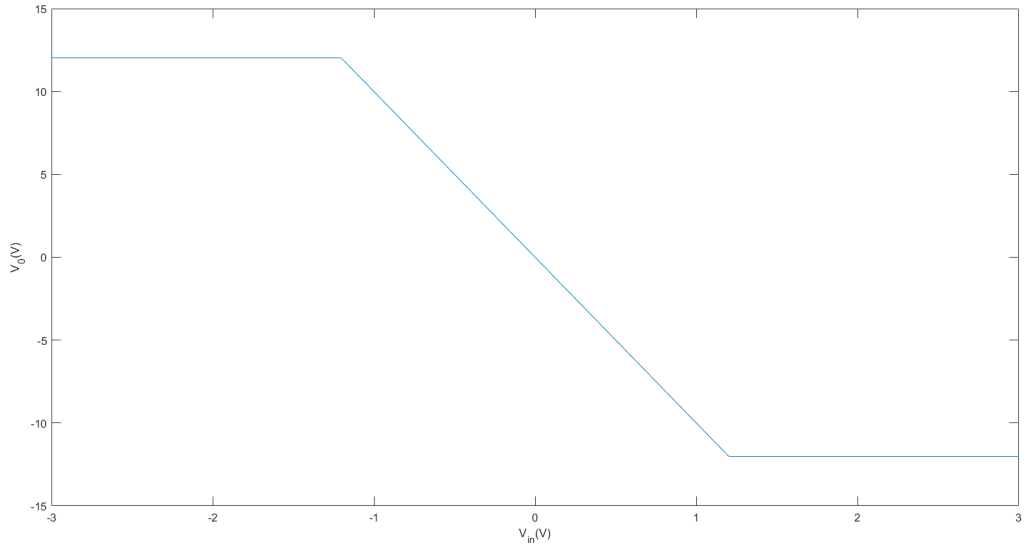

Figure 16: V_0 vs Vin

By evaluating the results of Figure 10 and Figure 11, it can be said that the behavior is consistent.

2.3 Step 3

In step 3 the circuit given in the Figure 17 is constructed. But since there was only one signal generator two signals with different amplitutes needed to be obtained using a circuitry.

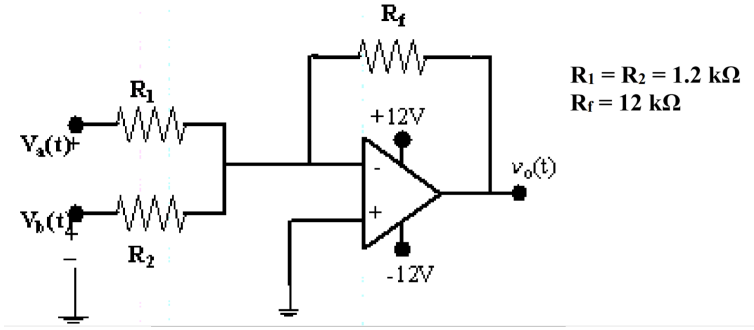

Figure 17: Circuit schematic for the Step 3

2.3.1 Voltage Divider and Buffer Circuit

Since there is need of getting the half of the signal voltage divider circuit is set. The general illustration of a voltage divider is given in Figure 18.

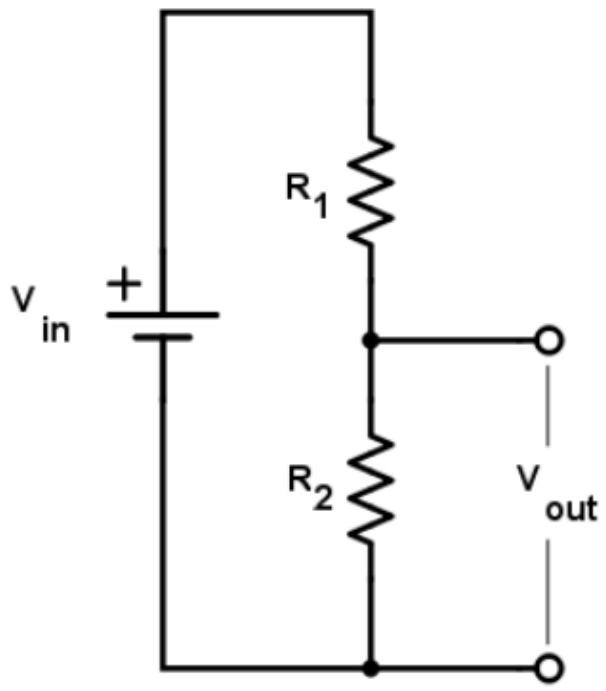

Figure 18: General voltage divider diagram

The relation between Vin and $Vout$ can be derived from the basic electric circuit relation. Whic is $Vout = Vin \times \frac{R_2}{R_1+R_2}$. So the have half of the voltage two of the 1kΩ resistor is used. As a result voltage is divided but to hold this relation the current coming from the branch of R_1 should be equal to the current going through the branch of R_2. If we directly connect this output terminal to the summing configuration current would go through the R_2 and R_f resistors of the summing circuit. Therefore it is needed to isolate those circuits. The buffer circuit explained in the step 2 part b is set.

2.3.2 a.

Using the voltage divider and buffer circuitry, the signal is propagated to the summing circuit. The plot of V_a, V_b, V_o against $Time$ is obtained using the signal value of $V_a(t) = 2V_b(t) = 4sin(1000\pi t)V$. The plot is obtained as given in Figure 19.

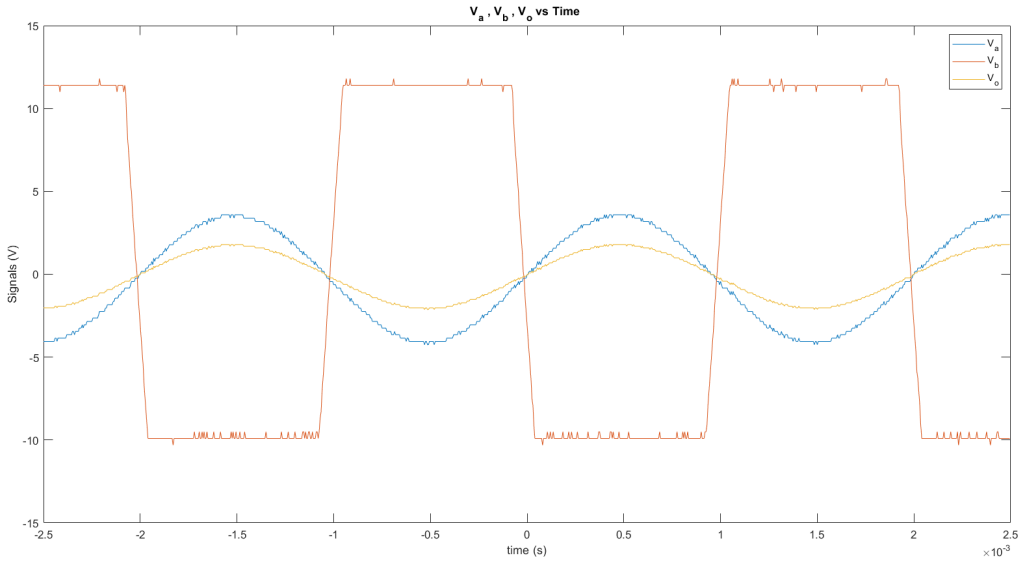

Figure 19: V_a, V_b, V_o vs $Time$

As a result it can be said that the signals are summed and amplified. But, after excessing linear region output signal is saturated.

2.3.3 b.

Using the voltage divider and buffer circuitry, the signal is supplied to the summing circuit. The plot of V_a, V_b, V_o against $Time$ is obtained using the signal value of $V_a(t) = 2V_b(t) = 2sin(1000\pi t)V$. The plot is obtained as given in Figure 20.

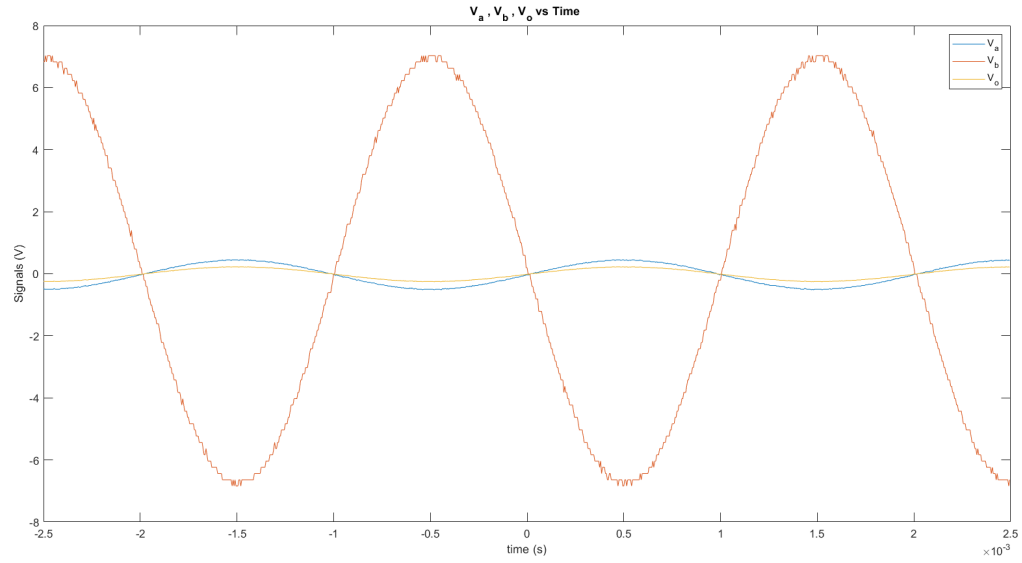

Figure 20: V_a, V_b, V_o vs $Time$

As a result it can be said that the signals are summed and amplified. But, in this setup the output signal is not saturated.

Summing amplifier circuit is constructed in LTSpice environment with the values of $V_a(t) = 2V_b(t) = 4sin(1000\pi t)V$. The schematic is given in the Figure 21.

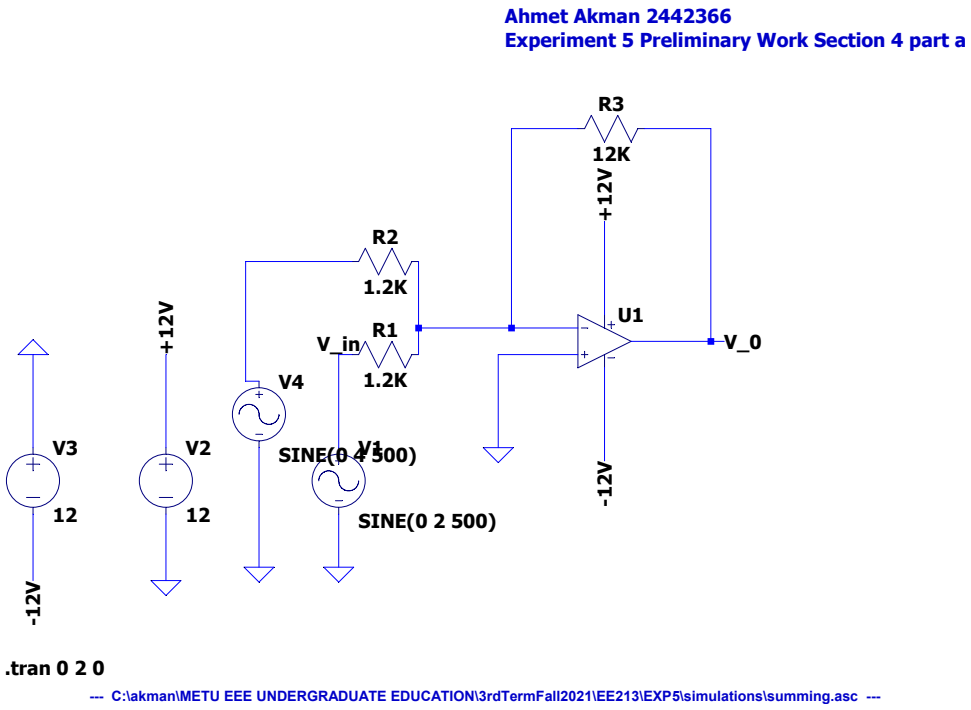

Figure 21: Circuit schematic for the summing amplifier.

Then plot given in Figure 22 is obtained.

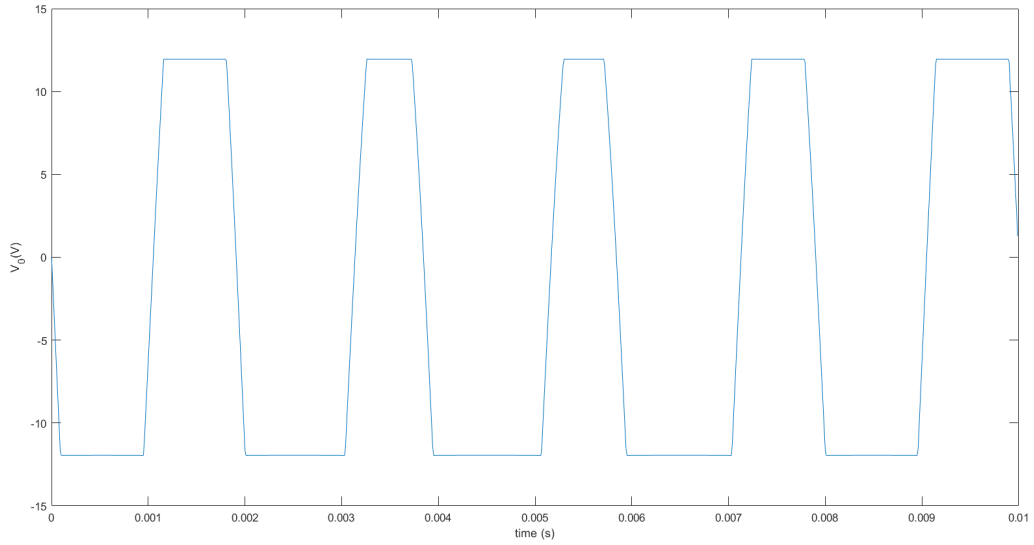

Figure 22: V_0 vs t

As a result we obtained the behavior of V_0 quite close to the Figure 19. Yet, the negative saturation region of the real circuit is slightly greater. This is expected to be stemmed from the non-ideality of the either LM741 component or the negative power line of the power supply.

3 Conclusion

In conclusion, in experiment 5, "Operational Amplifiers," as students, we have learned how basic circuit setups of Op-Amps can be constructed. Preliminary laboratory work is done via simulations of the basic Op-Amp circuits in LTSpice environment. As students, we have observed different characteristics of Op-Amp comparator , buffer , non-inverting , inverting and summing configurations and we have learned how voltage divider should be used when there is a load to the output terminal. To sum up,in this experiment, as students, we have experimented with how operates different kinds of operational amplifier circuits and how to work with voltage dividers.

Appendix I

Total time spent on/during:

- Pre-lab preparation: 6 hours (including the preliminary work and simulations)
- Experimental work: 2 hours (hours spent in lab)
- Report writing: 6 hours