Experiment 5 Preliminary Work
Bipolar Junction Transistor Characteristics

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1 Step 1

The document entitled "Notes on Transistors" is read.

2 Step 2

One can check whether the a known transistor is defective or not by connecting the probes of the multimeter to the p—¿n directions of the transistor . So that if the pn junction is operating one can say transistor is not defective. On the other hand given an unknown transistors is not defective one can determine whether it is npn or pnp by the same featre of the multimeter.

3 Step 3

Table 1: Resistance reading by color code convention.

	C547-B	C557-B
Collector Emitter Voltage (V)	45	-45
Collector Base Voltage (V)	50	-50
Emitter Base Voltage (V)	60	-5
Collector Current(A)	100mA	-100mA
β	110-800	120-800
Temperature Range (Celcius)	-55 to 150 C	-55 to 150 C

4 Step 4

The expected plot can be illustrated as given in Figure 1.

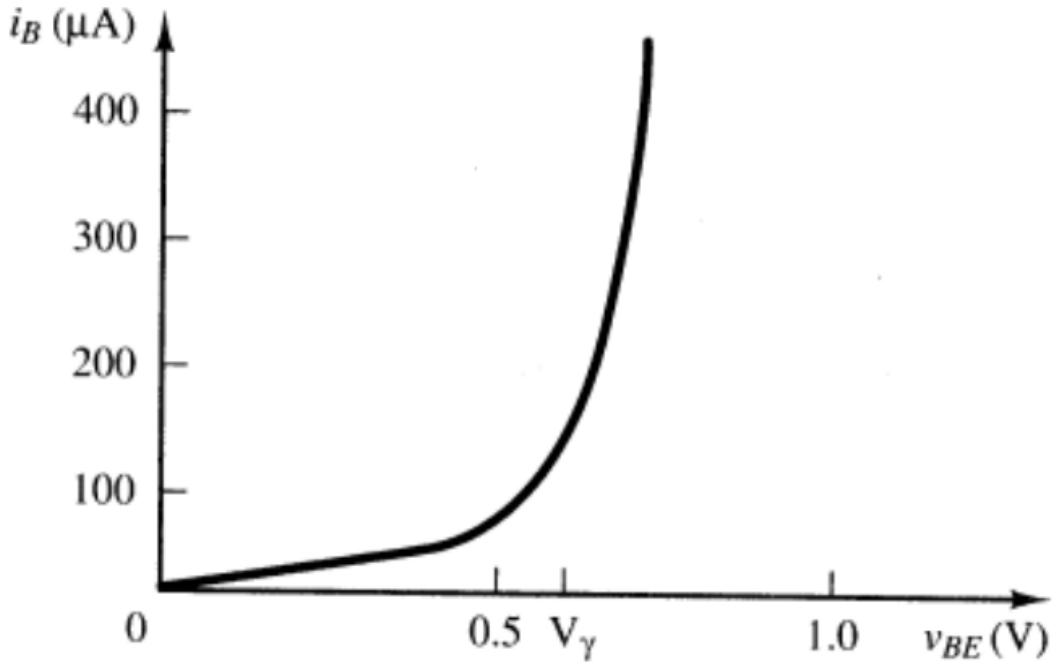

Figure 1: Expected plot (borrowed from the notes on transistors)

5 Step 5

6 Step 6

7 Step 7

7.1 a.

For this part the simulation is done with the reference circuit given in Figure 2.

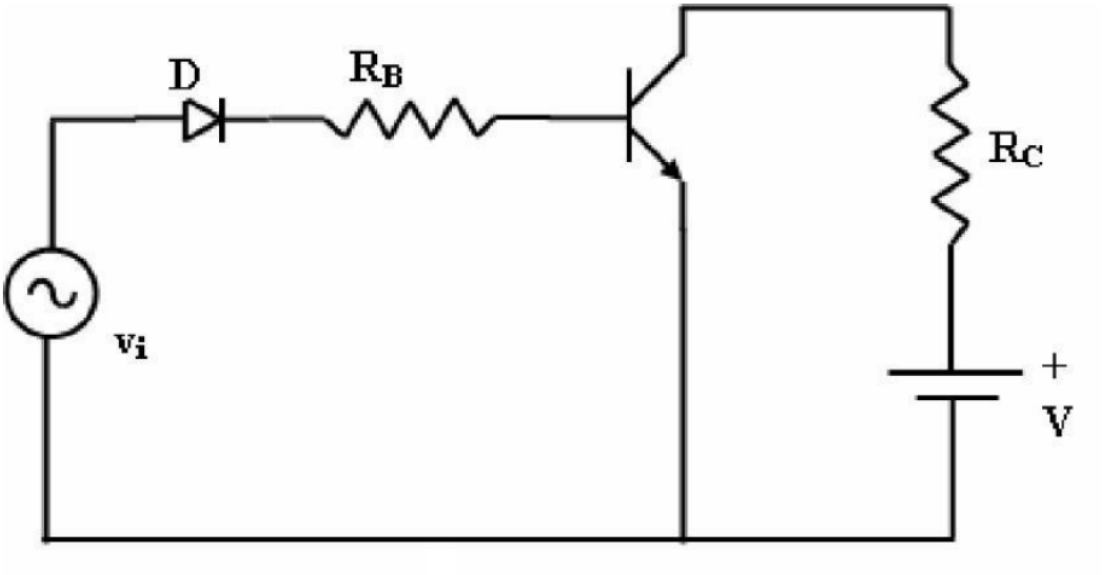

Figure 2: Circuit schematic for the step 7 a

The circuit given in Figure 3 is constructed in LTSpice simulation environment.

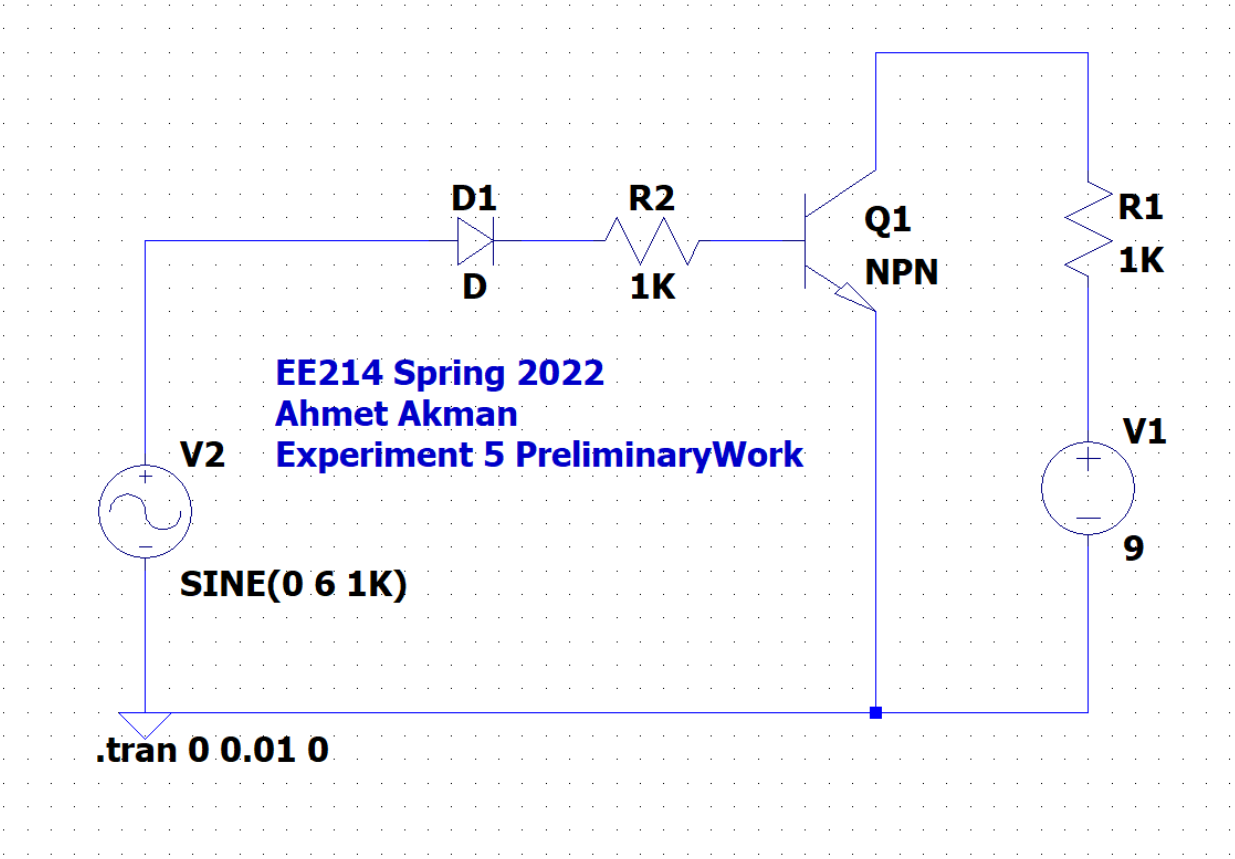

Figure 3: Circuit simulation schematic for the step 7 a

As a result plot given in Figure 4 is obtained.

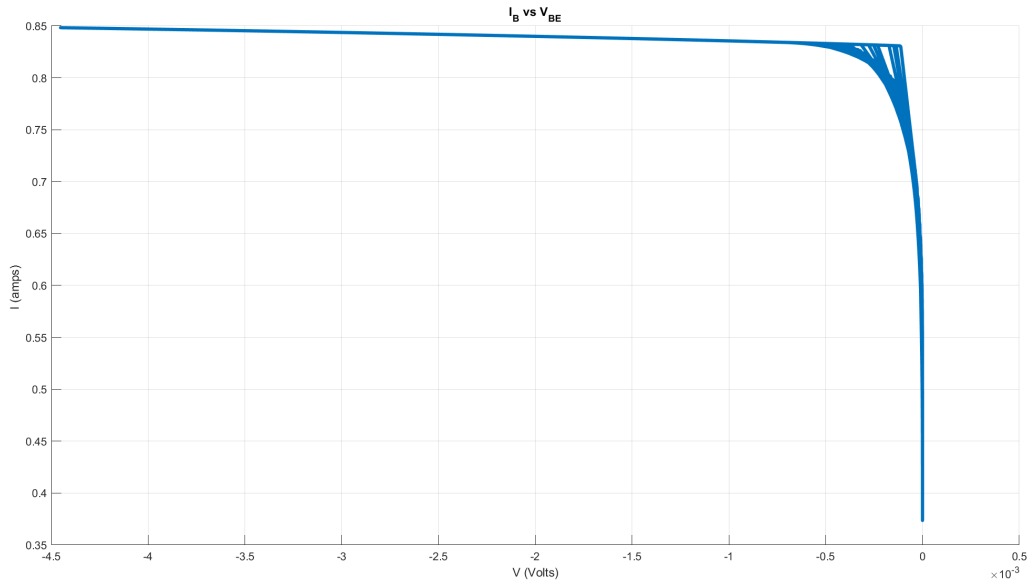

Figure 4: Plot for step 7 a

7.2 b.

For this part the simulation is done with the reference circuit given in Figure 5.

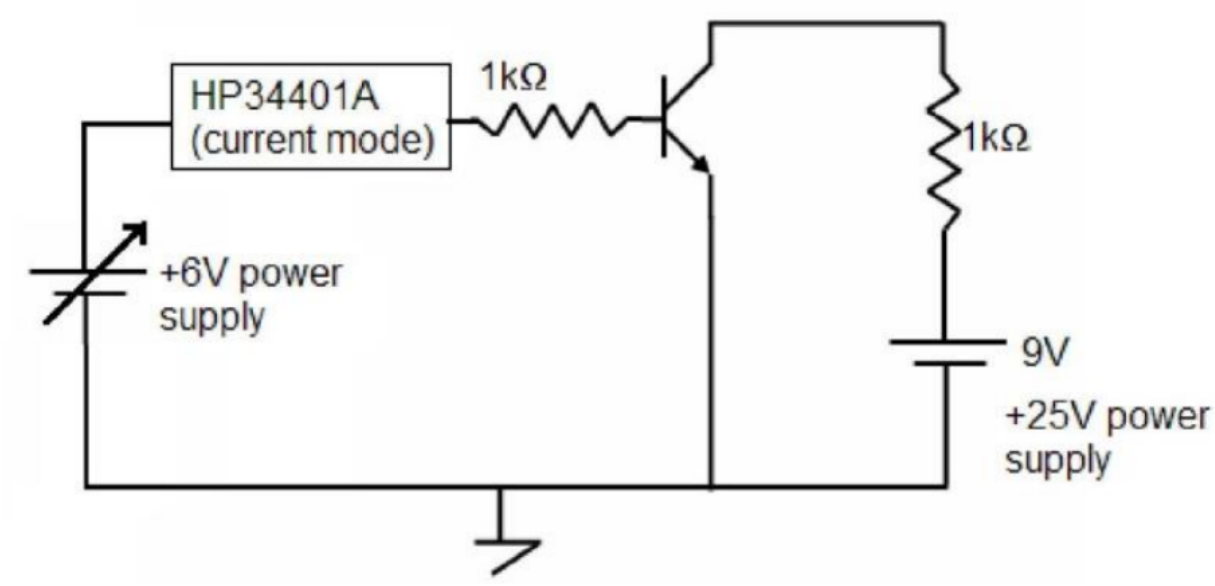

Figure 5: Circuit schematic for the step 7 b

The circuit given in Figure 6 is constructed in LTSpice simulation environment.

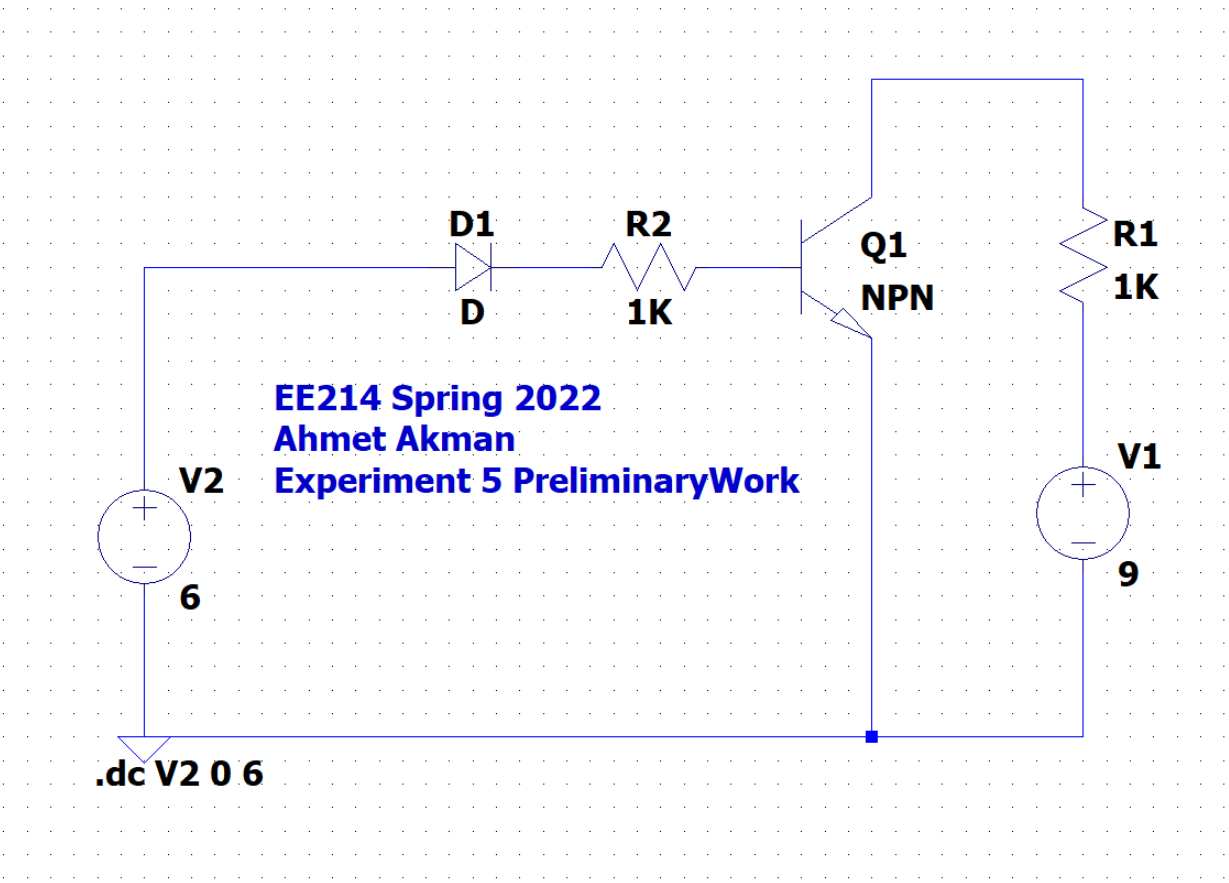

Figure 6: Circuit simulation schematic for the step 7 b

As a result plot given in Figure 7 is obtained.

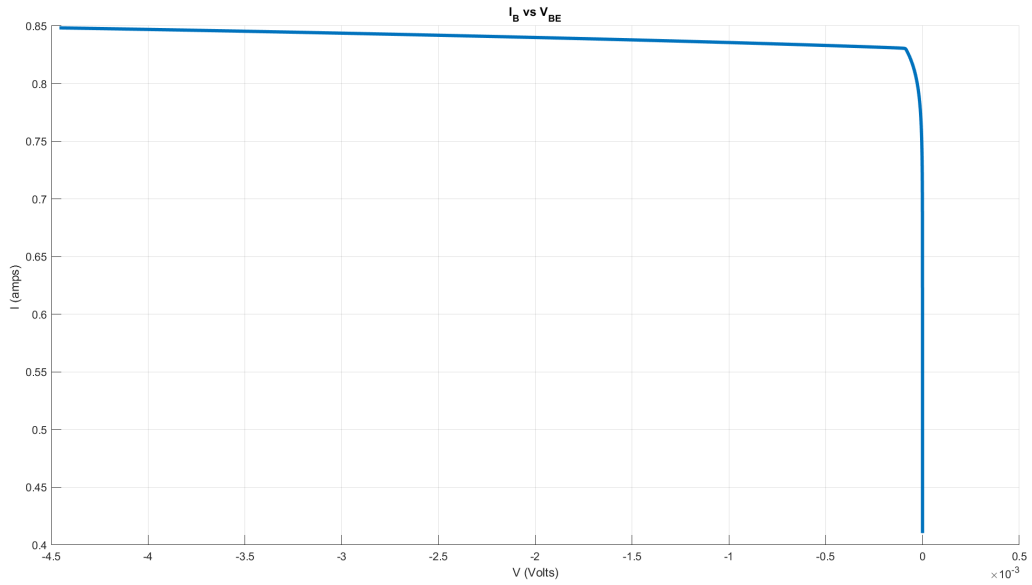

Figure 7: Plot for step 7 a

7.3 c.

For this part the simulation is done with the reference circuit given in Figure 8.

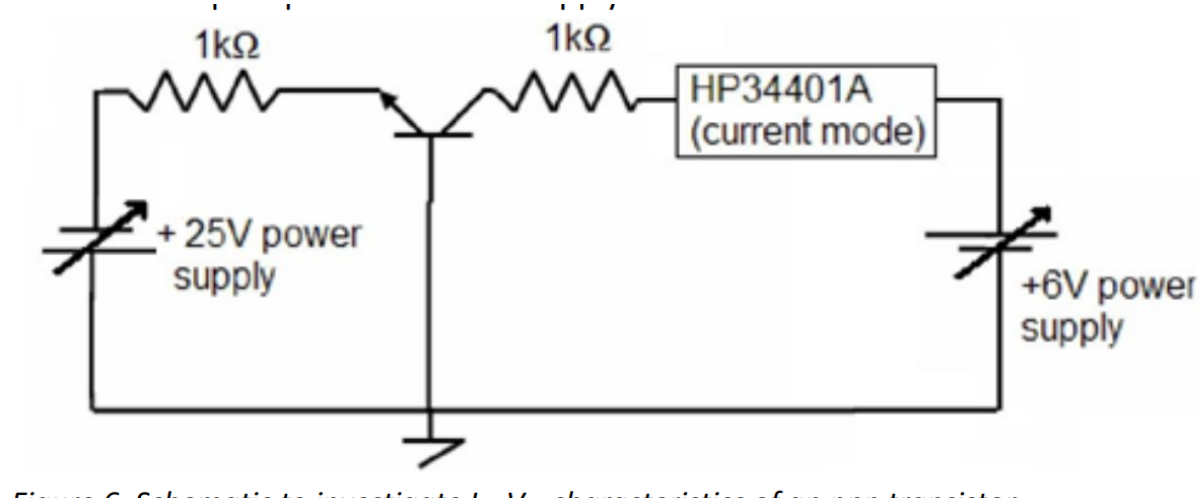

Figure 8: Circuit schematic for the step 7 c

The circuit given in Figure 9 is constructed in LTSpice simulation environment.

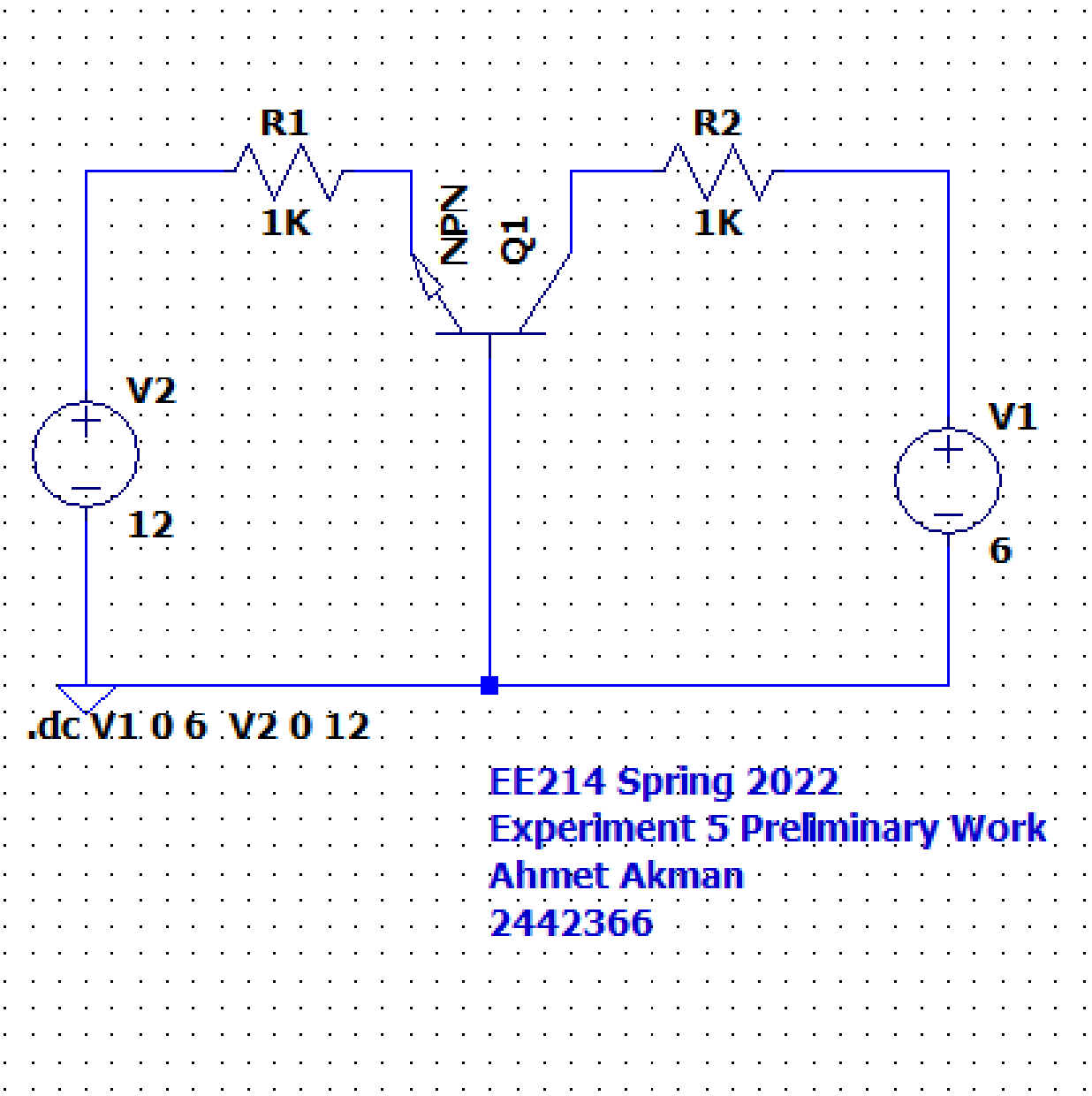

Figure 9: Circuit simulation schematic for the step 7 c

As a result plot given in Figure 10 is obtained.

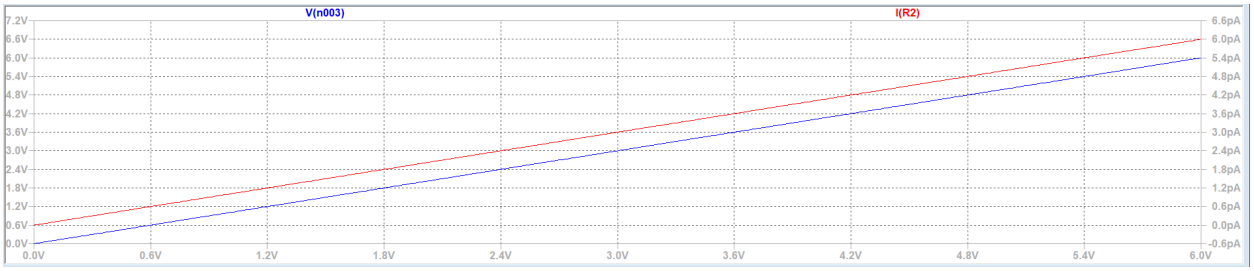

Figure 10: Plot for step 7 c

7.4 d.

For this part the simulation is done with the reference circuit given in Figure 11.

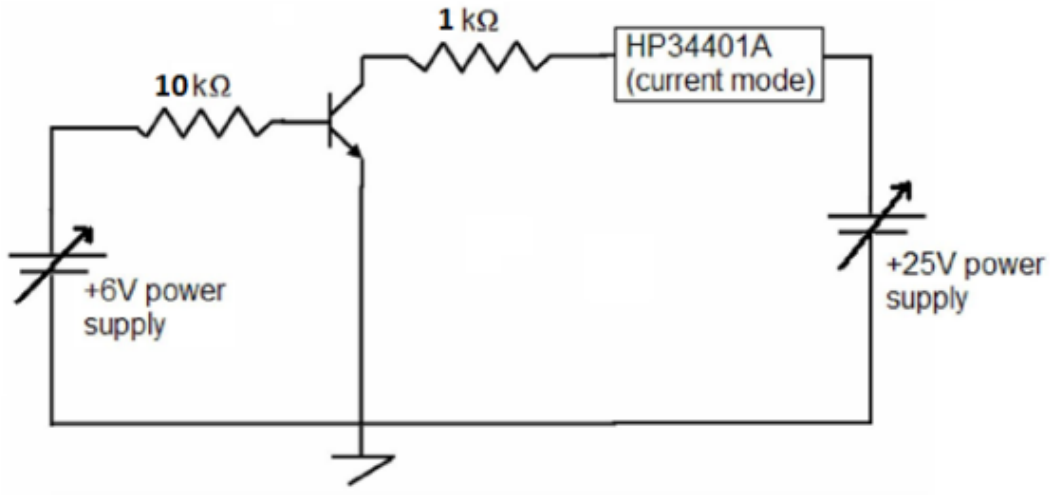

Figure 11: Circuit schematic for the step 7 d

The circuit given in Figure 12 is constructed in LTSpice simulation environment.

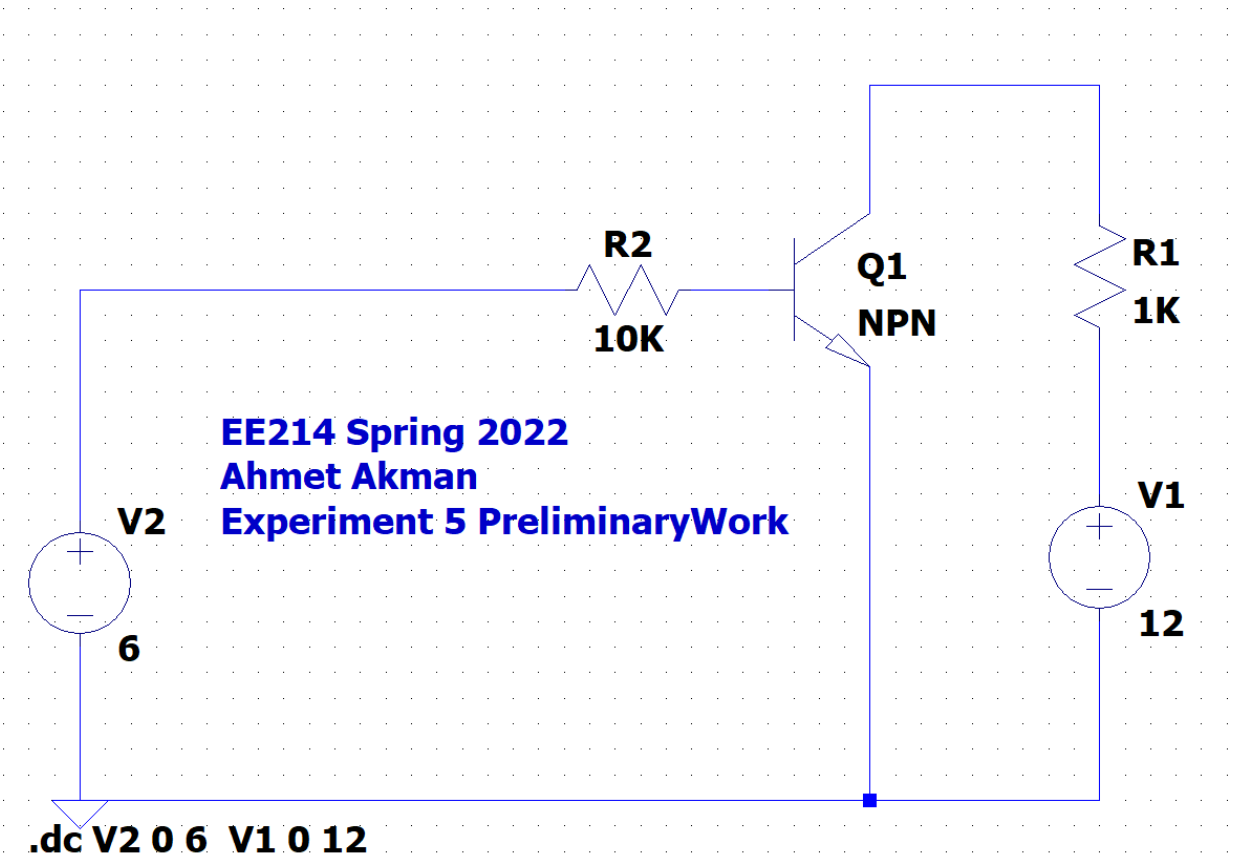

Figure 12: Circuit simulation schematic for the step 7 d

As a result plot given in Figure 13 is obtained.

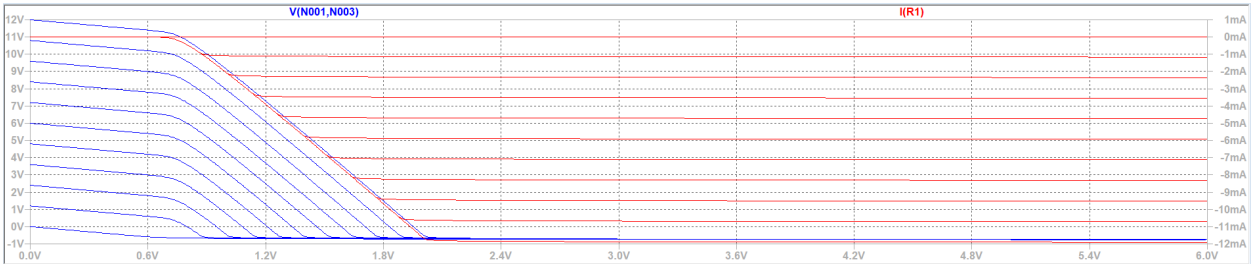

Figure 13: Plot for step 7 d

8 Conclusion

In this preliminary work document, some of the parameters of the different BJT's are examined. Then neccesssary simuloations concerning npn transistor characteristics are done and plotted.

Appendix A

The results of the some of the simulations are fetched from LTSpice and plotted in MATLAB in order to make the plots more readable and convenient.