Spring 2022 EE214 Experiment 1
Diodes and Rectifiers

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Contents

1 Introduction

In this document the actions corresponding requirements defined in the Experiment Manual are represented.

2 Experimental Results and Discussion

2.1 Step 1

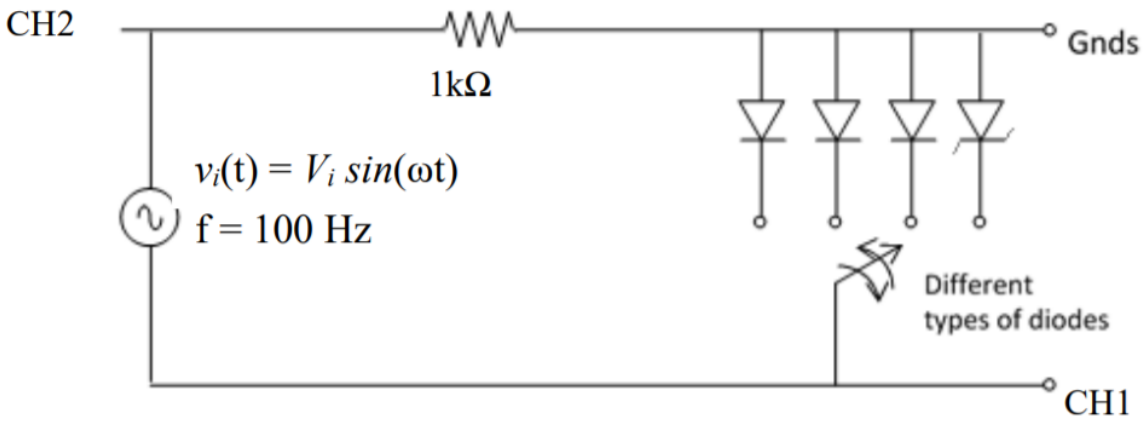

Figure 1: Circuit schematic for the step 1

2.1.1 a)

2.1.2 b)

We can call separation of lines in i-v graph as hysteresis effect. When we increase frequency to 10kHz, we observed hysteresis effect on the i-v characteristics of diode on the DSO screen. Since our diode can not change its state as fast as our high frequency voltage source supply, we observe this effect. To solve this problem and to be able to use diodes at high frequencies, there are "high speed" or "switching" diodes. These diodes can be used in high frequencies without observing hysteresis effect.

2.2 Step 2

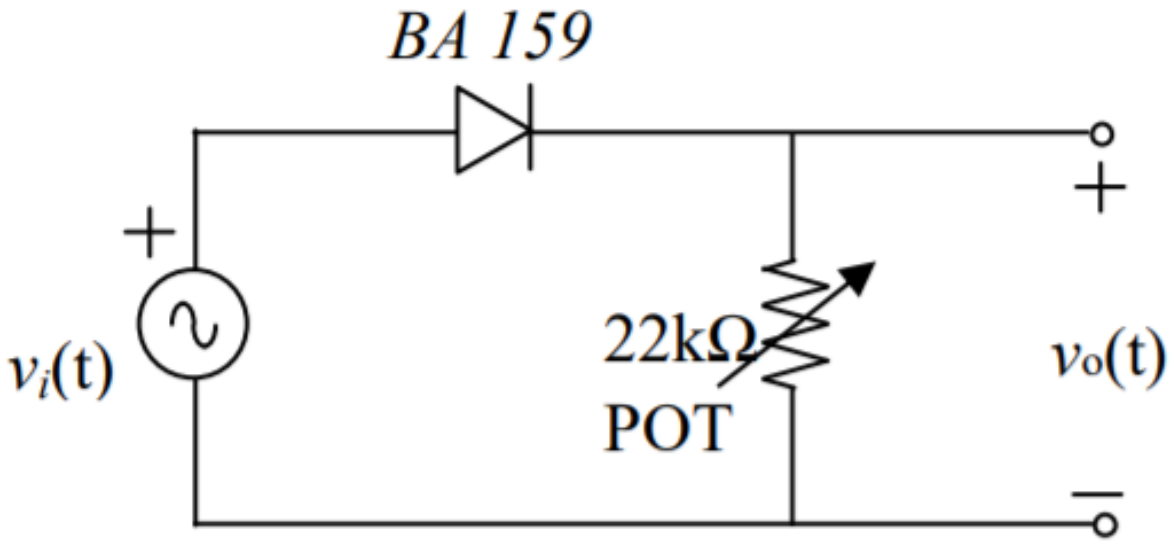

Figure 2: Circuit schematic for the step 2

For this part, we set the half-wave rectifier circuit given in Figure X and adjusted $v_i(t) = 2sin(2000\pi t)V$

2.2.1 a)

After setting POT to $1k\Omega$, we obtain output and input voltage waveforms on the graph indicaded in Figure X.

If we look at the graph carefully, we can realized that output voltage is slightly lower than input voltage since diode consumes energy. Then we measured the DC_{rms} of output value as 730mV using cursors of DSO. Output voltage waveform on the DSO screen is like same with the input waveform in positive cycles but zero when input is in the negative cycle.

2.2.2 b)

2.3 Step 3

In this third step, we set up the diode clamper circuit given in Figure X using the diode 1N4001 and set the voltage $v_i(t) = 10sin(200\pi t)V$. Then plotted the input and output voltage waveforms on the graph given in Figure X.

From above graph we can derive that output waveform is just shifted form of input waveform to below zero. Since diode prevent capacitor from discharged, in order peak value of output to be clamped above zero diode should go into negative bias.

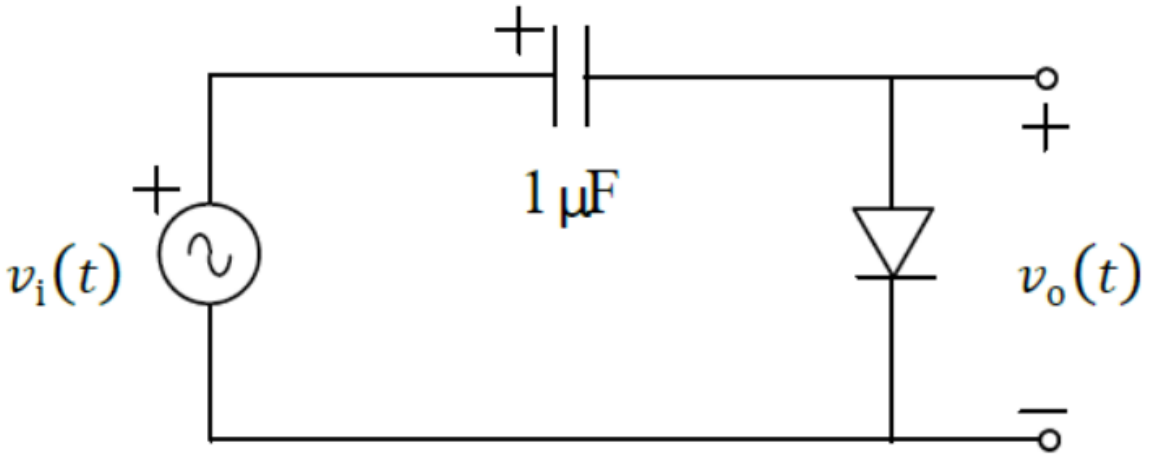

Figure 3: Circuit schematic for the step 3

2.4 Step 4

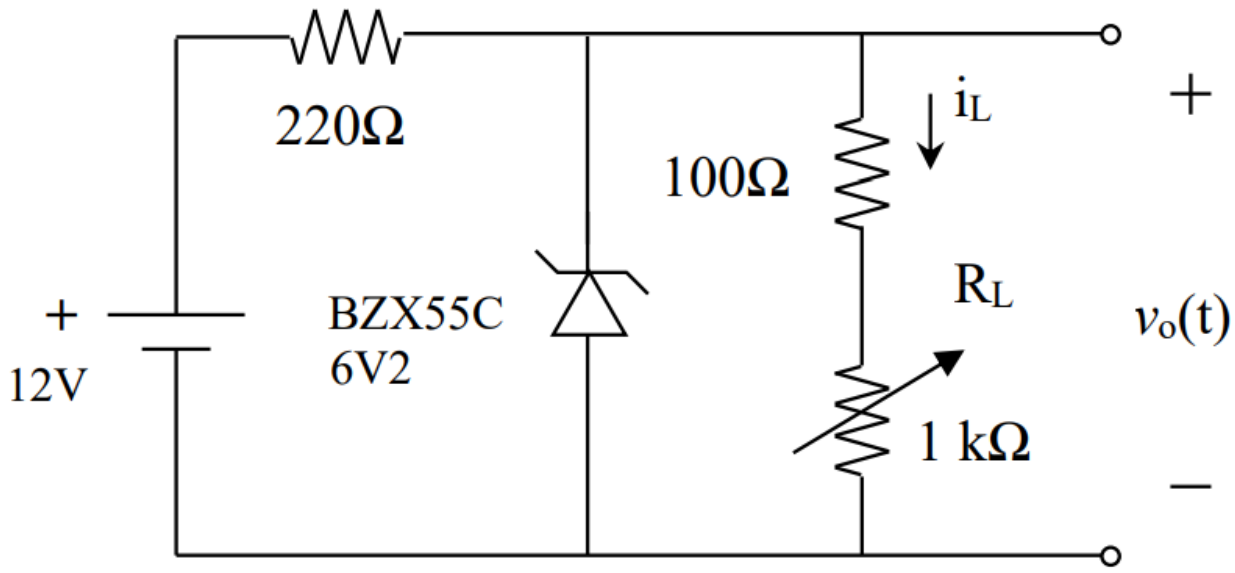

Figure 4: Circuit schematic for the step 4

3 Conclusion

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Appendix A

- PreLab Preprataion 6 hours
- Experimental Work 2 hours
- Report Wrining 6 hours