Experiment 1 Preliminary Work
Diodes and Rectifiers

Ahmet Akman 2442366

March 28, 2022

Contents

In this document the actions corresponding requirements defined in the Experiment Manual are represented.

1 Step 1

Notes on signal generators, oscilloscopes and multimeters are studied and reviewed the fundamentals.

2 Step 2

Notes on dioedes document is studied. The datasheets of the diodes to be used in this experiment are reviewed, which are 1N40007 , BA159 ,AA119 ,and BZX55C-6V2.

3 Step 3

In this step characteristics of linear modeled junction diodes are analyzed according to the I vs V equation as follows,

$$I = I_s[e^{\frac{qV}{nkT}} - 1]$$

Ideality constant n is taken 1 for both cases. From explanation in the manual $\frac{kT}{q}$ is taken as 25 mV at temperature (20∘C) . The common pievewise linear model for a junction diode is given in Figure 1.

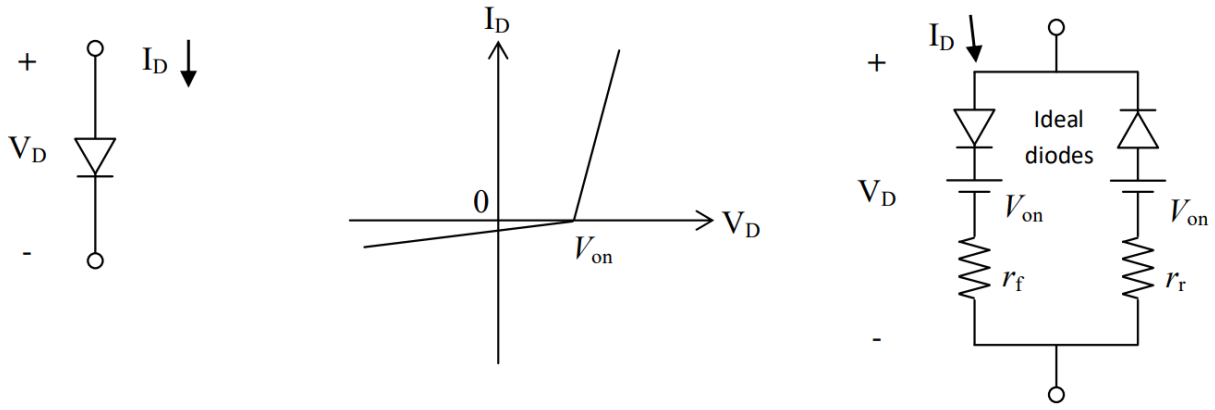

Figure 1: Common piecewise linear model for a junction diode.

3.1 a)

In table 1 the i-v values for the given voltages are obtained by taking the reverse saturation value 2.5xE-7 . The results are calculated using MATLAB.

Table 1: I vs V

V(Volts)	I (Amps)
-0.40	-2.499999718662063e-07
-0.20	-2.499161343430244e-07
0	0
0.10	1.339953750828606e-05
0.20	7.449894967604320e-04
0.30	0.040688447854751
0.40	2.221527380126968

Then the i versus v plot is obtained ,and given in Figure 2.

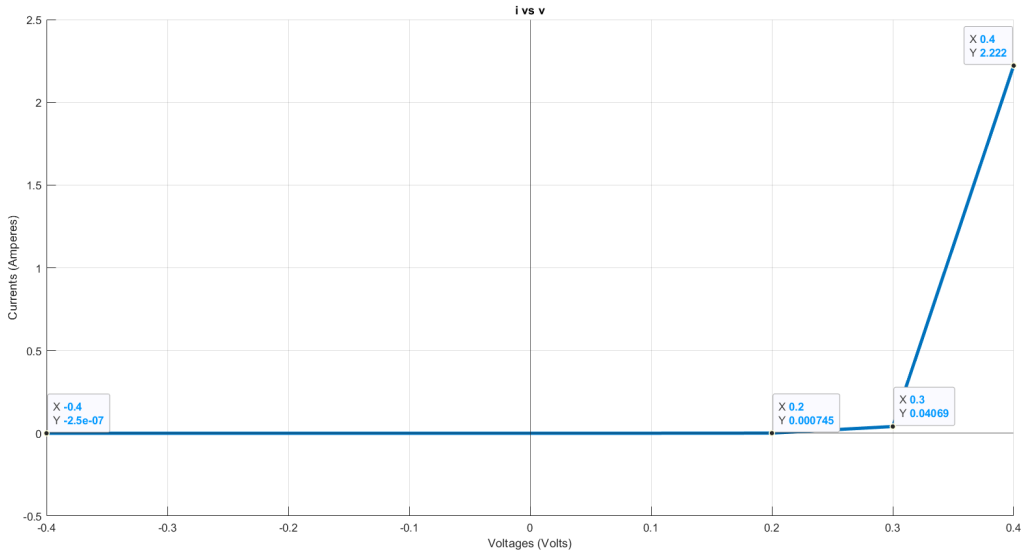

Figure 2: i versus v plot

Table 2: Parameters obtained from the plot

V_{on}	r_f	r_r
0.3V	0.046Ω	2.5Ω

So the piecewise linear model parameters are determined ,and provided in Table 2.

3.2 b)

In table 3 the i-v values for the given voltages are obtained by taking the reverse saturation value 1E-15 . The results are calculated using MATLAB.

Table 3: I vs V

V(Volts)	I (Amps)
-0.40	-9.999998874648254e-16
-0.20	-9.996645373720976e-16
0	0
0.20	2.979957987041728e-12
0.40	8.886109520507873e-09
0.50	4.851651944097903e-07
0.60	2.648912212884338e-05
0.70	0.001446257064290
0.80	0.078962960182680

Then the i versus v plot is obtained ,and given in Figure 2.

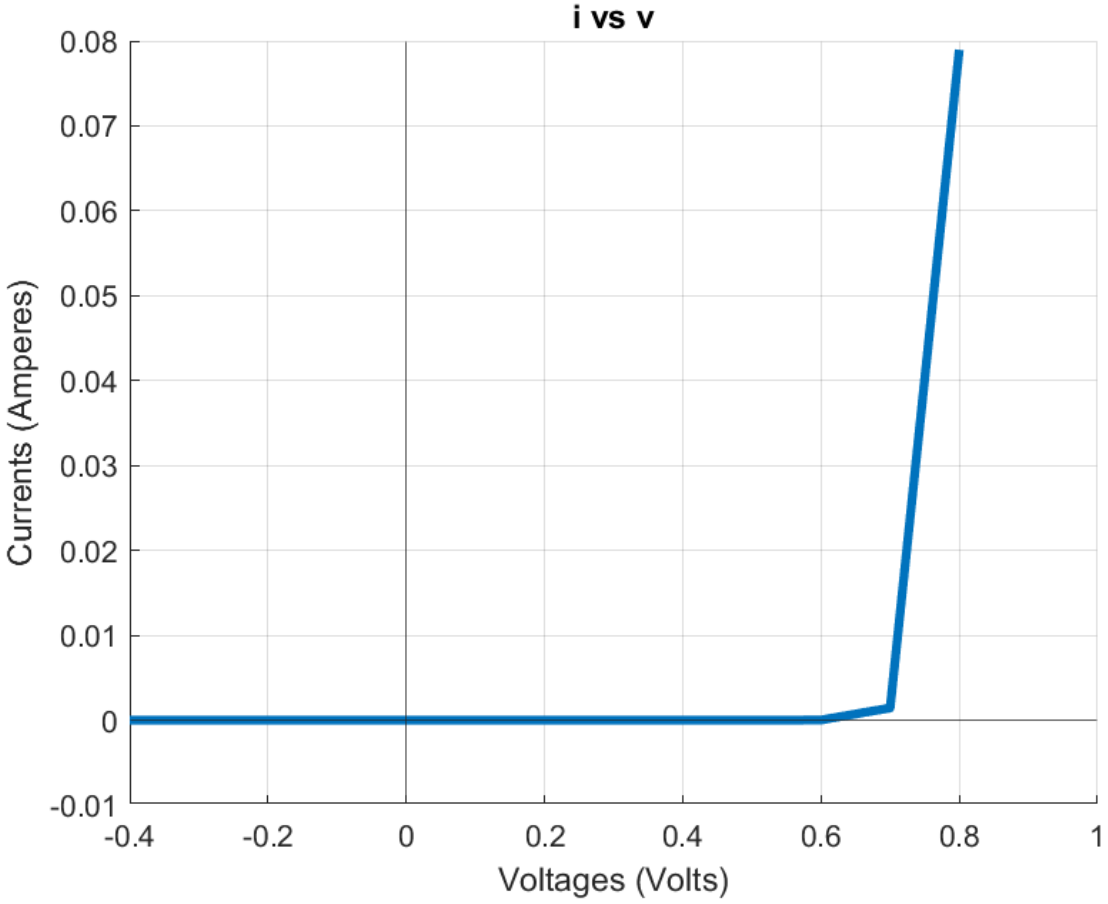

Figure 3: i versus v plot

Table 4: Parameters obtained from the plot

V_{on}	r_f	r_r
0.7V	1.2893Ω	68.97Ω

So the piecewise linear model parameters are determined ,and provided in Table 2.

4 Step 4

A practical half-wave rectifier circuit schematic taken as reference ,and given in Figure 4.

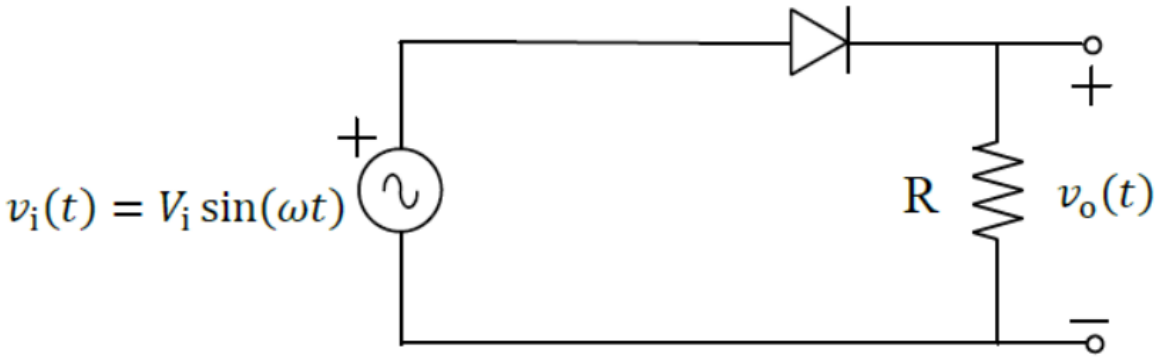

Figure 4: Half-wave circuit schematic for the Step 4

Then the following analysis ,given in Figure 5, is made on paper with the required sketch.

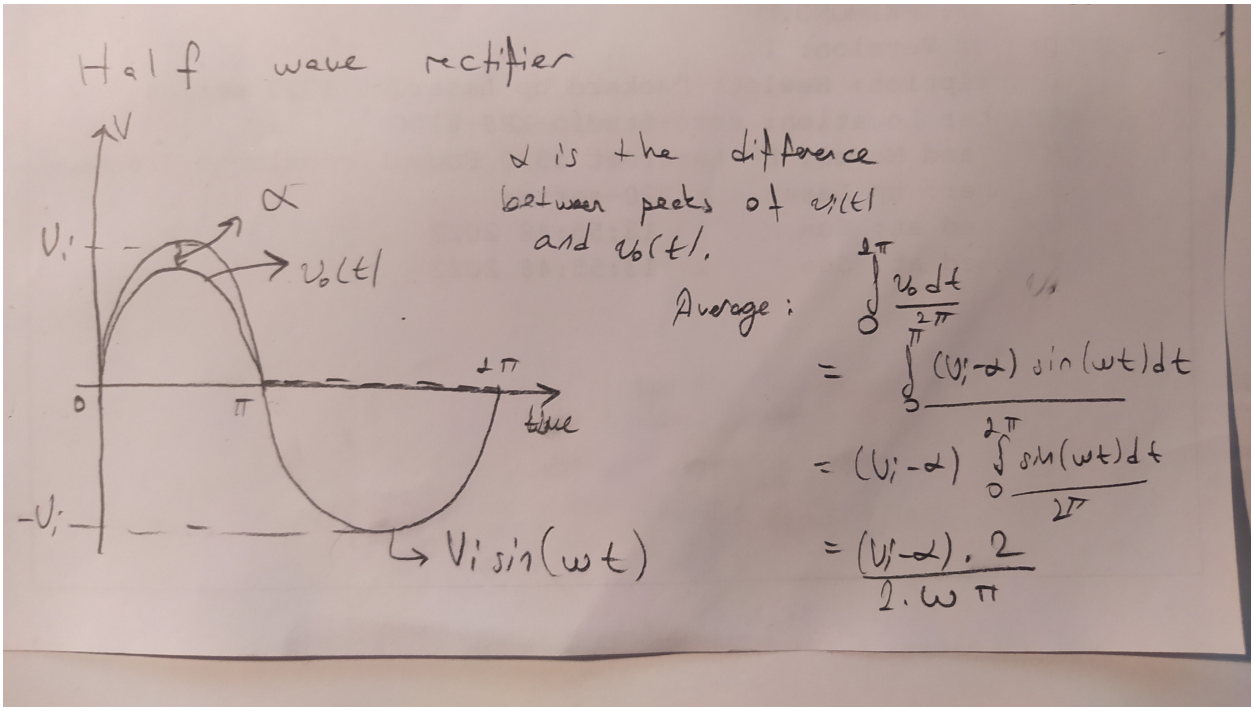

Figure 5: Half-wave circuit analysis for the Step 4

Here , α denotes the difference between the peaks of the v_o and v_i which is resulted from the forward resistance of the diode. So ;

$$\alpha = V_i * \frac{r_f}{r_f + R}$$

The derived expression for the average voltage is given in the Figure 5. The assumption is made that backward resistance is negligible.

5 Step 5

In step 5 the diode clamper circuit is analyzed. The circuit schematic given in Figure 6 is taken as the reference.

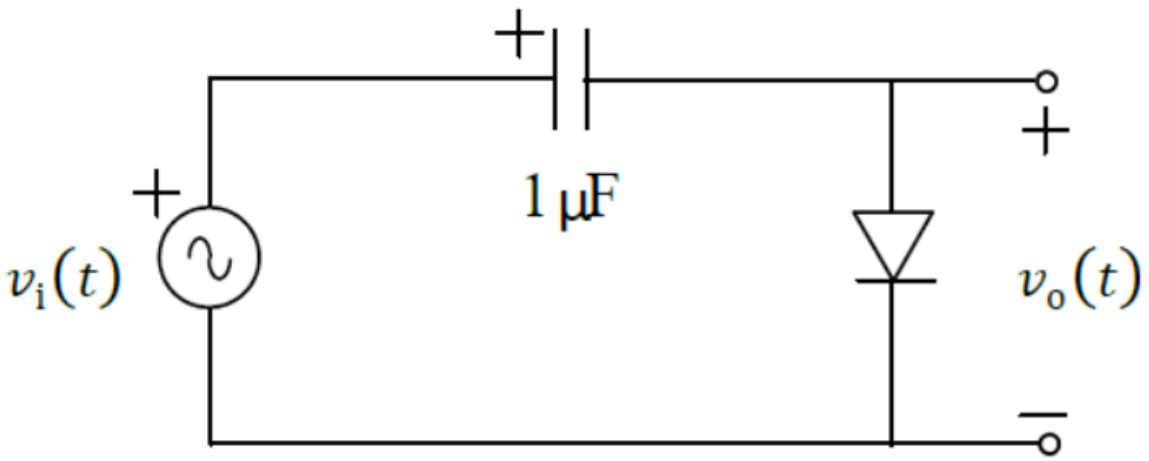

Figure 6: Diode clamper circuit schematic for the Step 5

Then the circuit presented in Figure 7 is constructed in LTSpice environment.

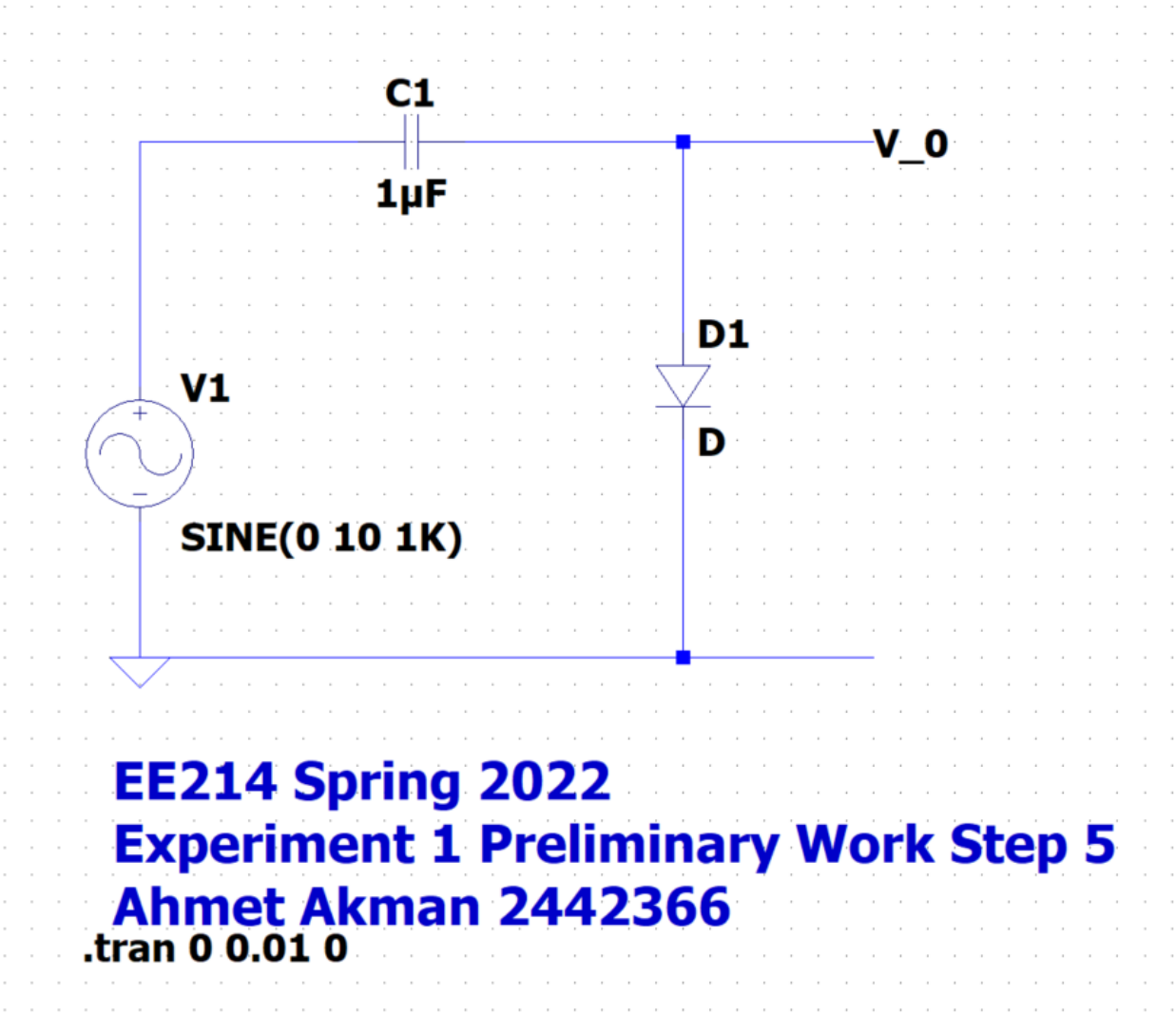

Figure 7: Diode clamper circuit simulation schematic for the Step 5

5.1 a)

First, the input is adjusted as a sine wave with amplitude 10 Volts. Then the plot given in Figure 8 is obtained.

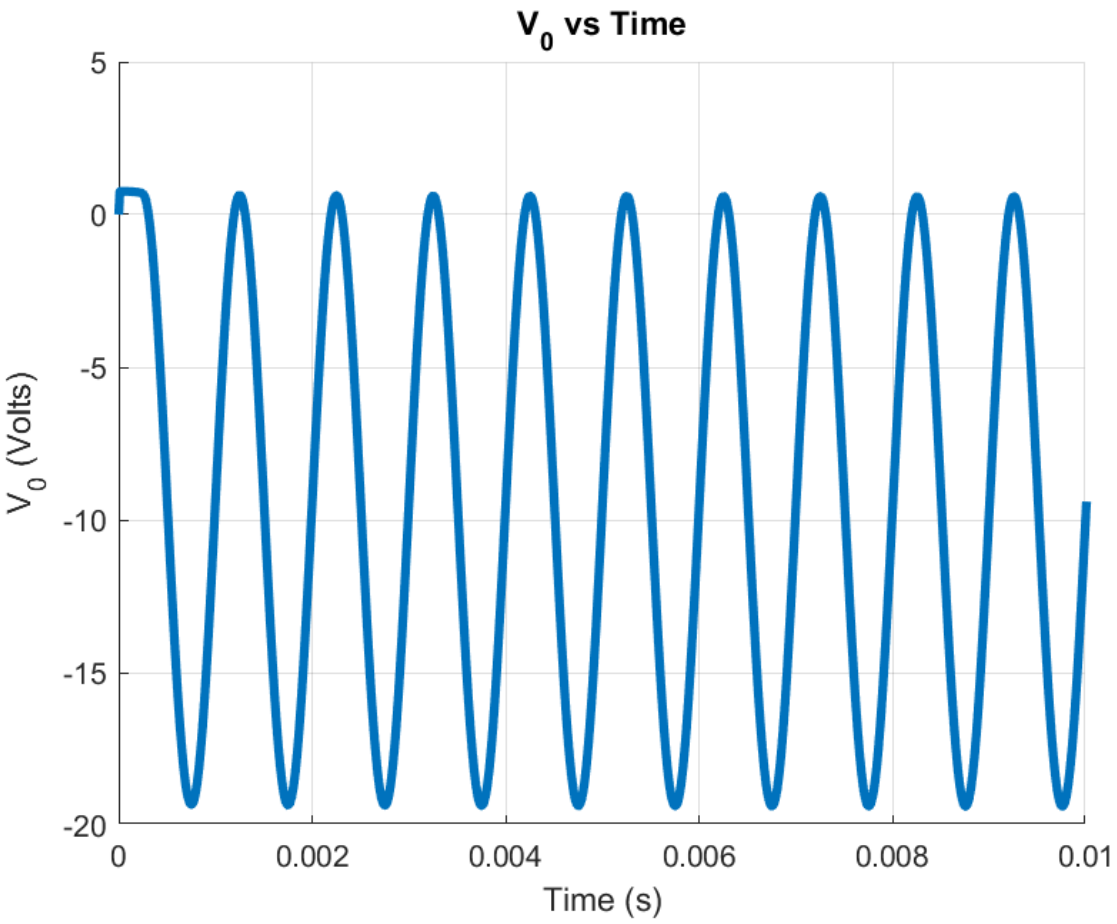

Figure 8: Diode clamper circuit simulation plot

As it can be observed the average value of the voltage across diode is appriximately -10 Volts.

5.2 b)

Secondly, the input is adjusted as a square wave with 10 Volts. Then the plot given in Figure 9 is obtained.

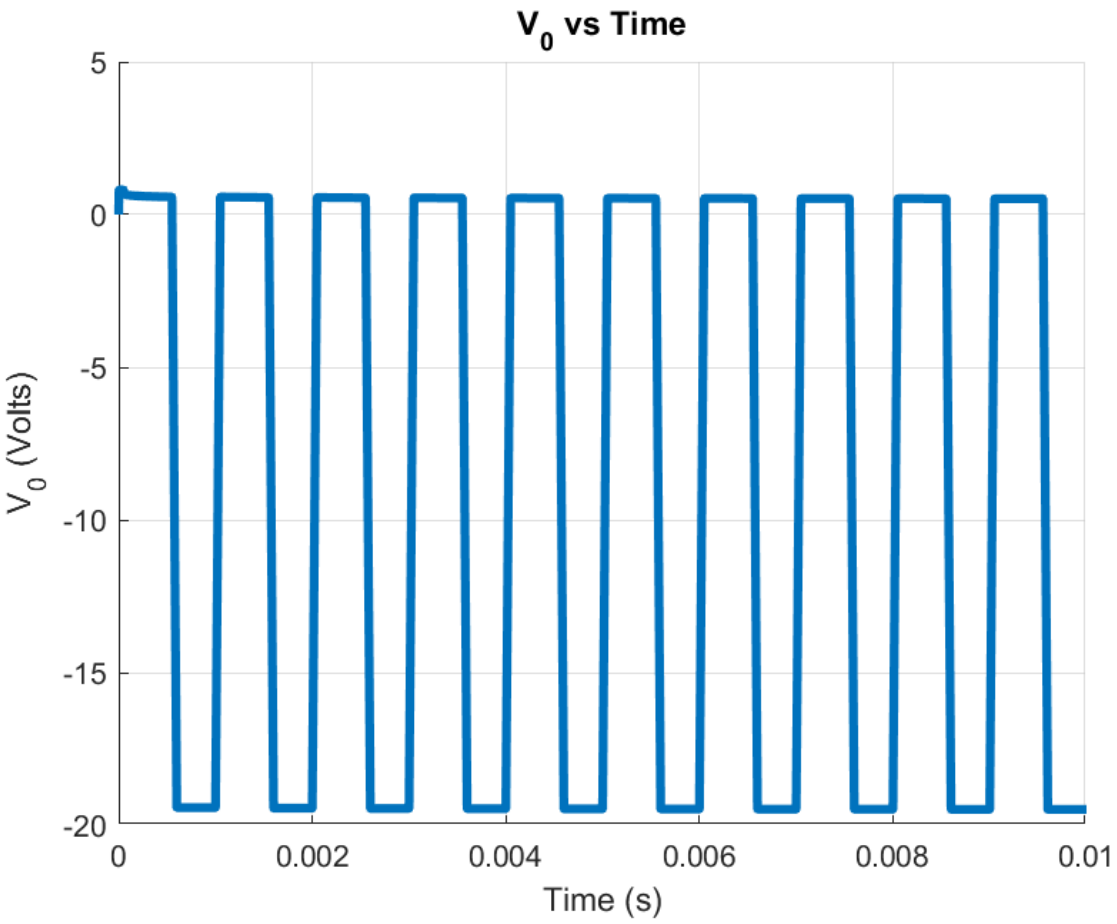

Figure 9: Diode clamper circuit simulation plot (Square wave input)

As it can be observed the average value of the voltage across diode is appriximately -10 Volts.

6 Step 6

For step 6 , the half wave rectifier circuit with a capacitive load is used the reference circuit is given in Figure 10. Also note that the plots wanted in the summary are given in Appendix B.

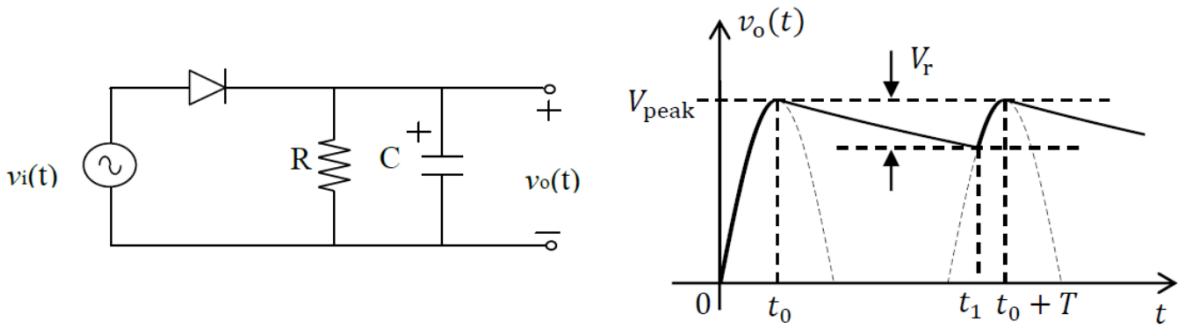

Figure 10: Half-wave rectifier circuit schematic for the Step 6

The simulate the circuit the structure in Figure 11 is constructed in LTSpice environment.

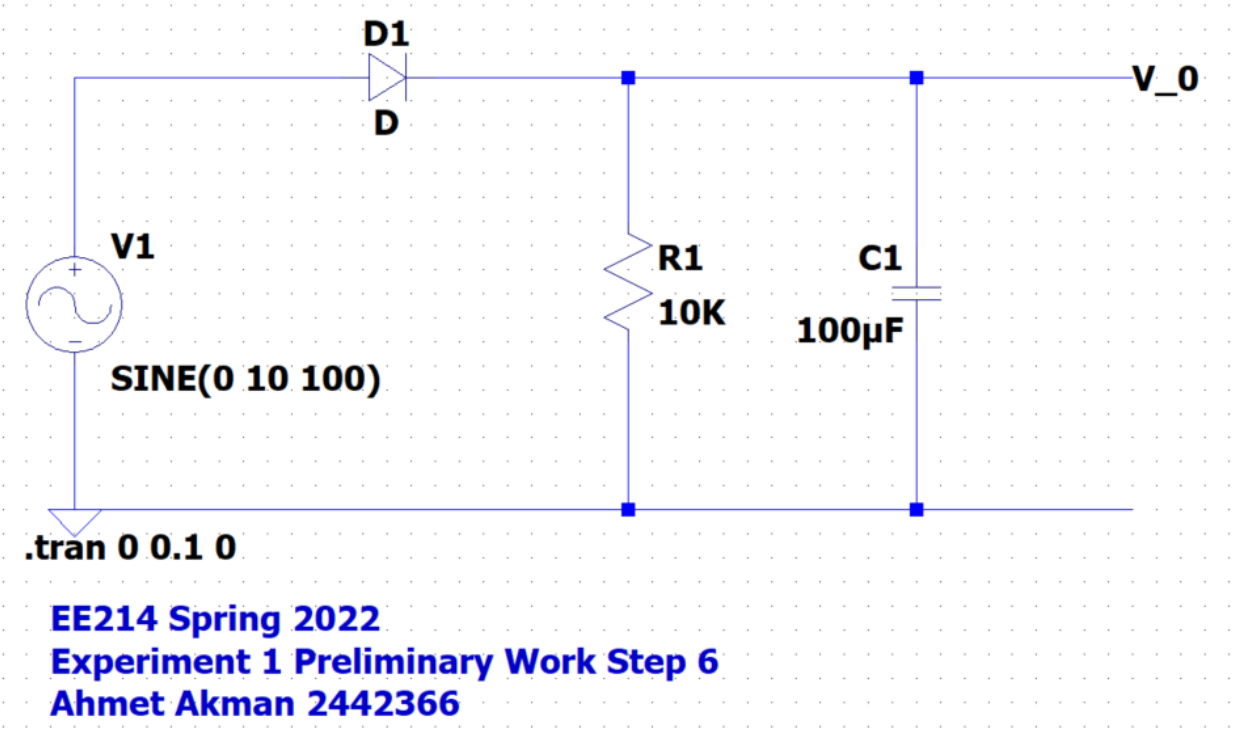

Figure 11: Half-wave rectifier circuit simulation schematic for the Step 6

6.1 a)

Here it is expected to find the value of Resistor which makes V_r value less than the 1 percent of the output voltage. Since output voltage can be approximated as equal to the input voltage, the deviation is needed to be in 0.1 Volts range. So, if the R value is selected as 1kΩ the requirement is barely become satisfied.

6.2 b)

As a result of the simulation work, the plot in Figure 12 is obtained.

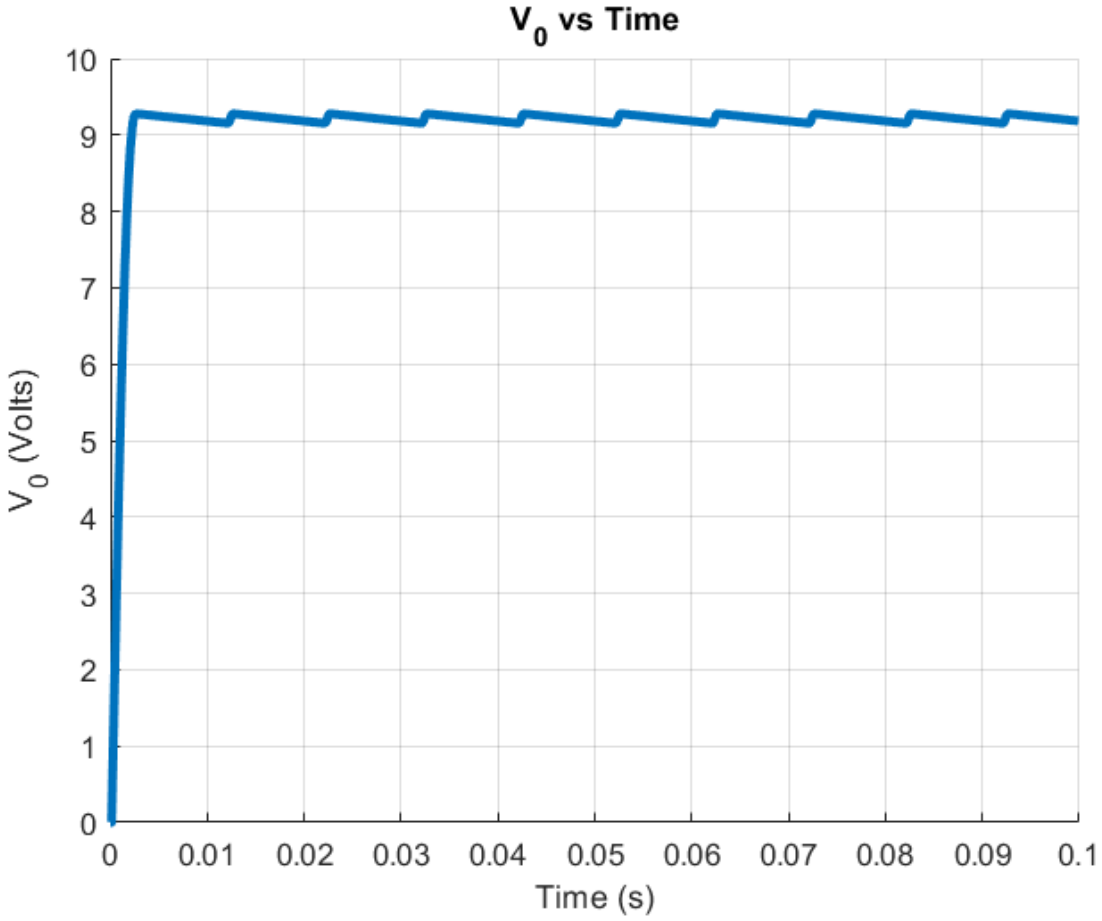

Figure 12: Half wave rectifier circuit simulation plot V_o

6.3 c)

As done in the Step 4, it can be said that V_r become equal to the V_{peak} . Also by the calculations mentioned in the Step 4 (assuming diode is ideal) V_{DC} becomes

$$V_{DC} = \frac{1}{20\pi^2}$$

7 Step 7

In step 7 the full-wave rectifier circuit is simulated according to the circuit schematic given in Figure 13.

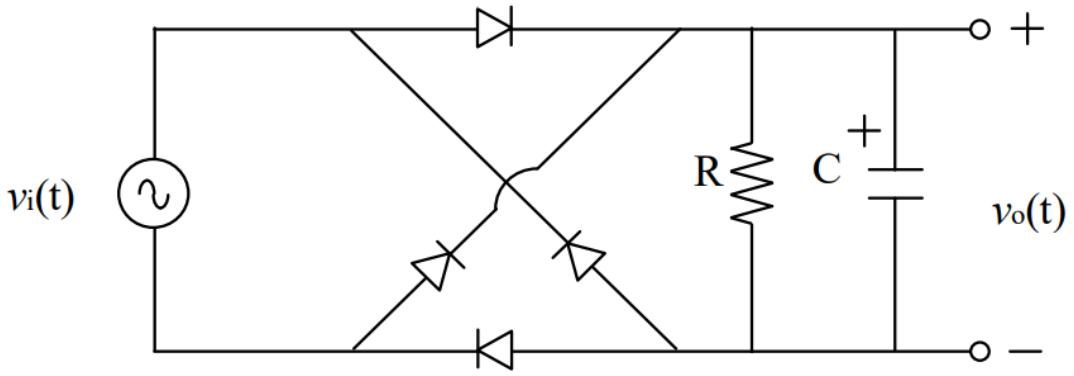

Figure 13: Full-wave rectifier circuit schematic for the Step 7

Then the circuit in Figure 14 is set in LTSpice environment.

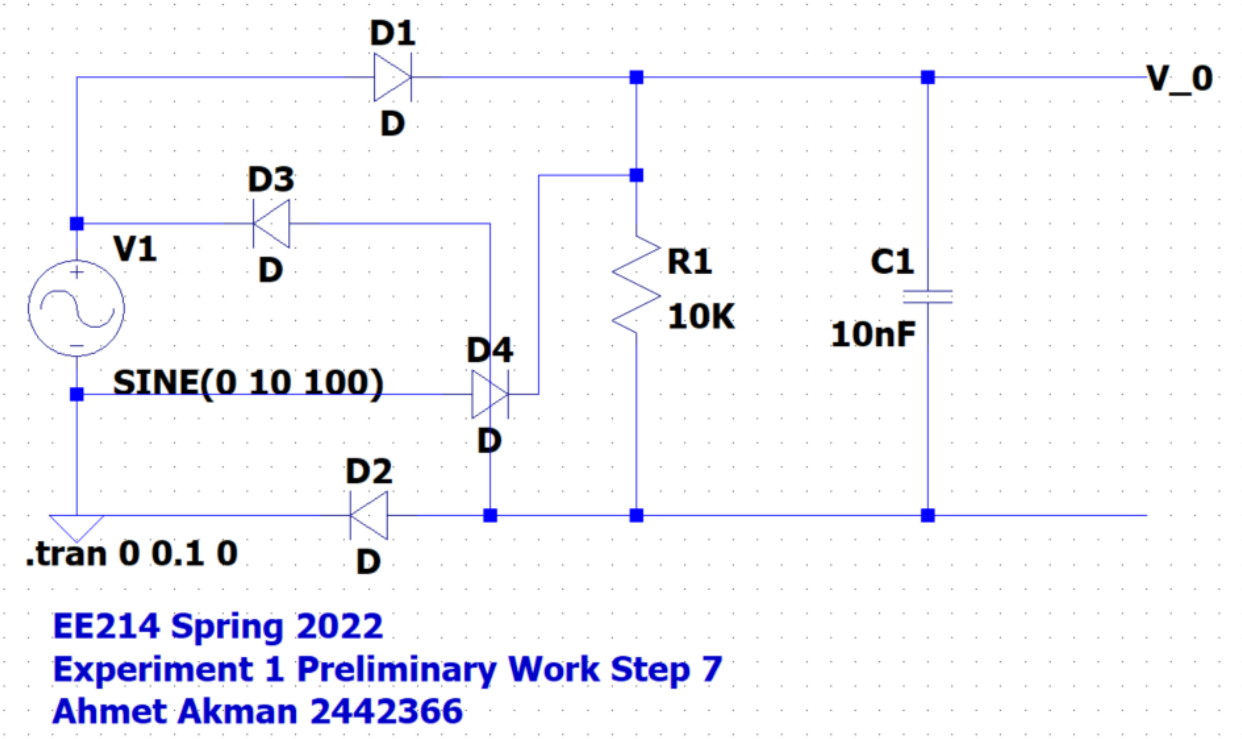

Figure 14: Full-wave rectifier circuit simulation schematic for the Step 7

The capacitive load is set to different loads. For the case of no capacitive load the plot in Figure 15 is observed.

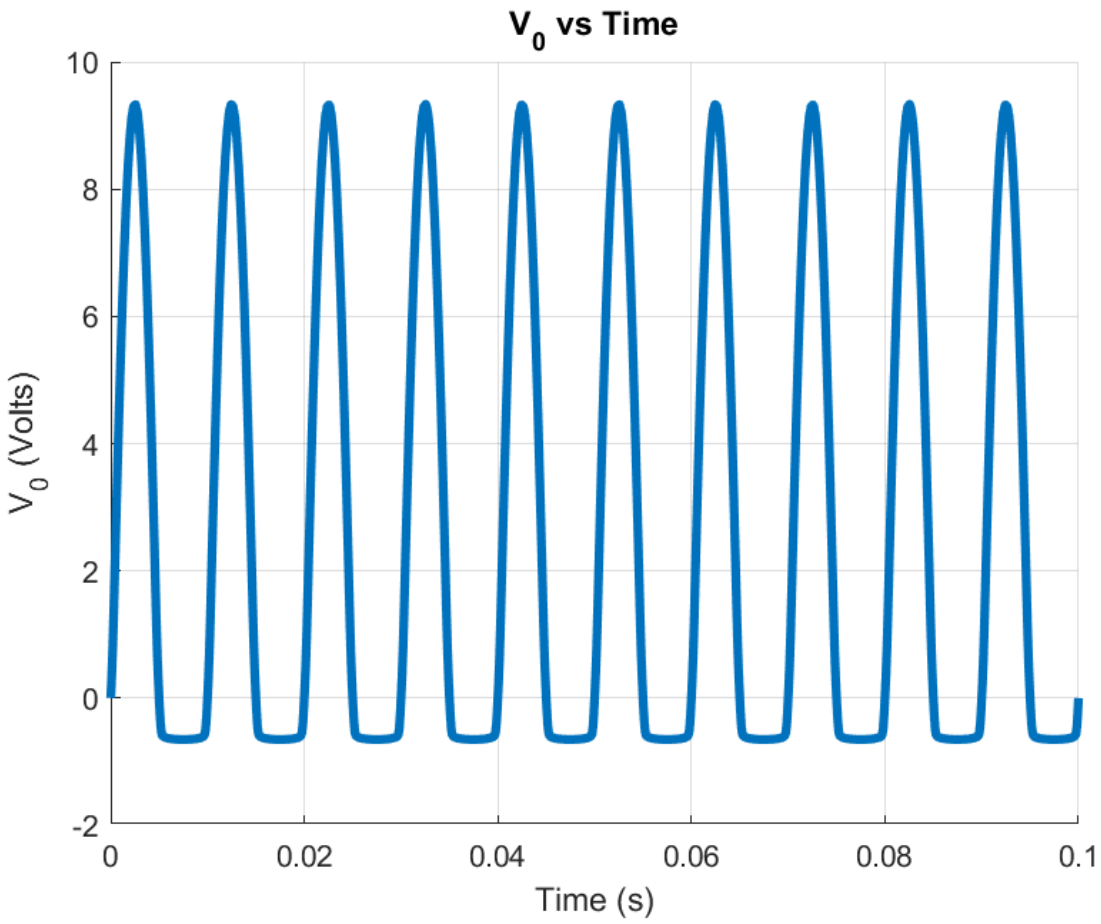

Figure 15: Full-wave rectifier circuit simulation plot V_o —— no capacitor

For the case of 10nF capacitive load the plot in Figure 16 is observed.

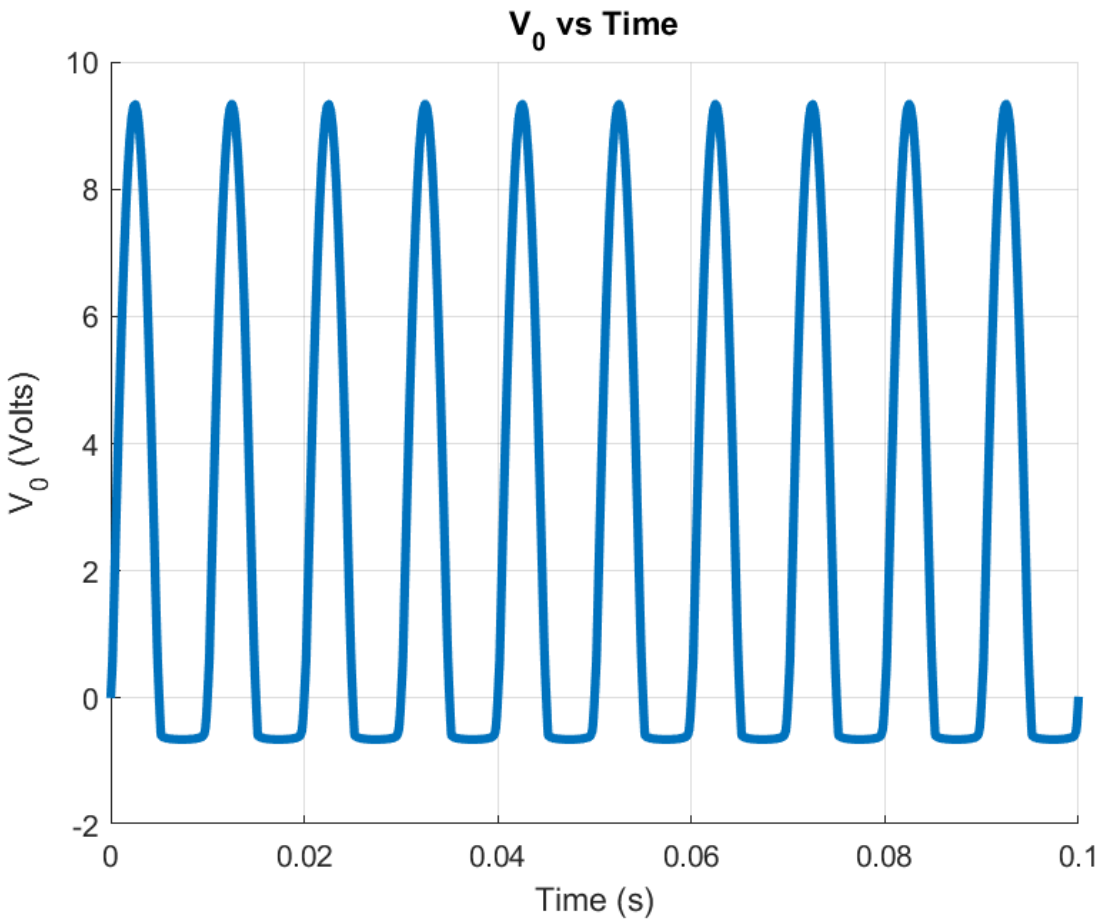

Figure 16: Full-wave rectifier circuit simulation plot V_o —— 10nF capacitor

Lastly the plot in Figure 17 is obtained for the capacitive load of 1uF.

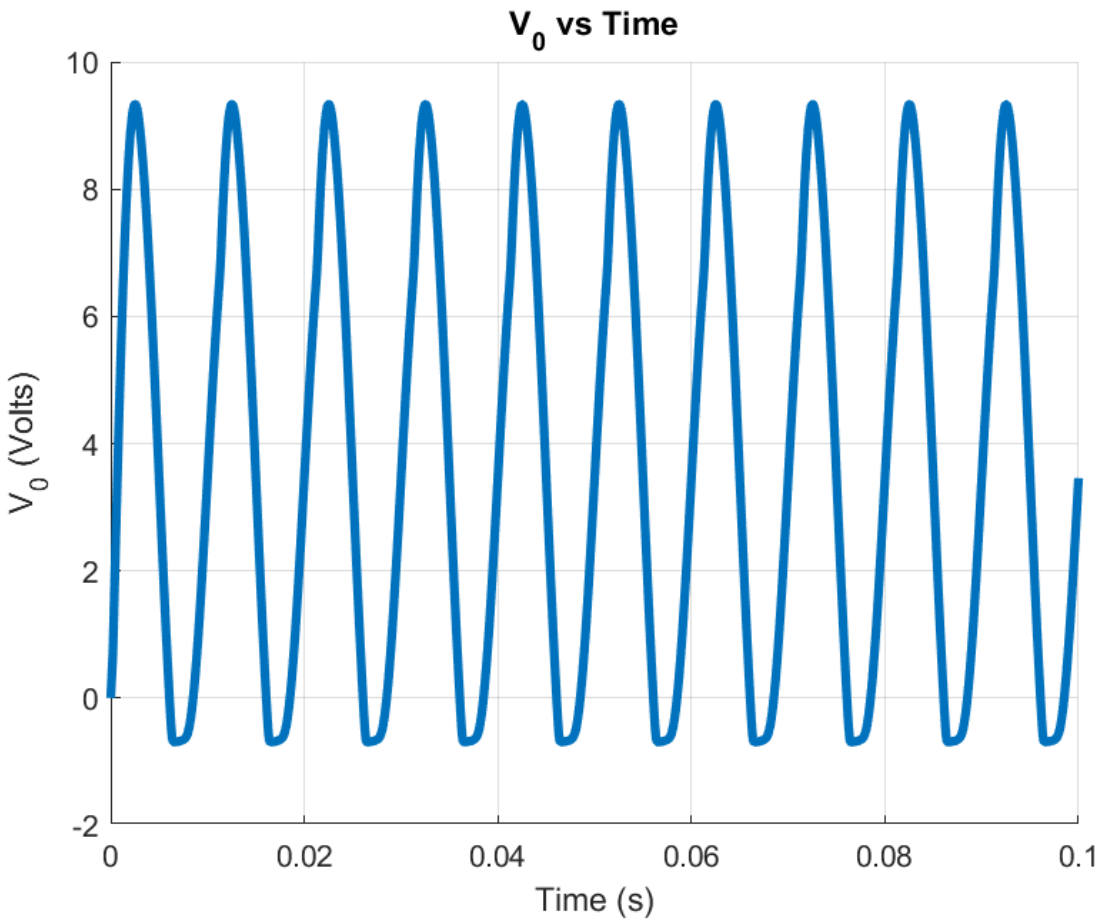

Figure 17: Full-wave rectifier circuit simulation plot V_o —— 1uF capacitor

To sum up , following comments can be made. While there is a slight difference between the cases of not having capacitor and 10nF capacitor, the case of 10uF capacitor shows a significant compansation.

8 Step 8

In this step the piecewise linear model of the zener diodes are investigated. A common piecewise linear model for a zener diode is presented in Figure 18.

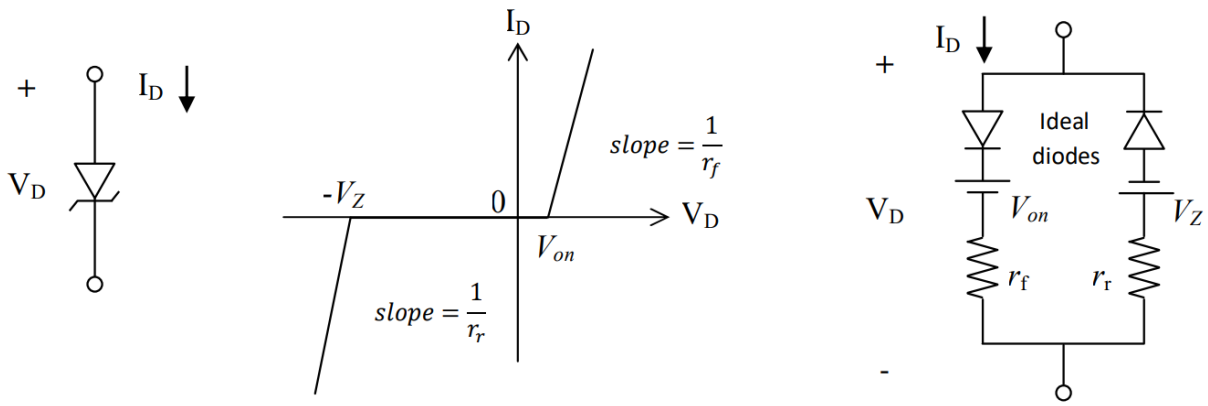

Figure 18: Common piecewise linear model for a zener diode.

As being mentioned in the step 2 , parameters presented in Table 5 are obtained from the datasheet of zener diode BZX55C-6V2 .

Table 5: Parameters from datasheet

Parameter	Value
V_{on}	0.5V
V_z	6.2V
r_f	0.003 Ω
r_r	1 to 10 Ω

9 Step 9

For step 9 DC level shifter circuit given in Figure 19 is investigated.

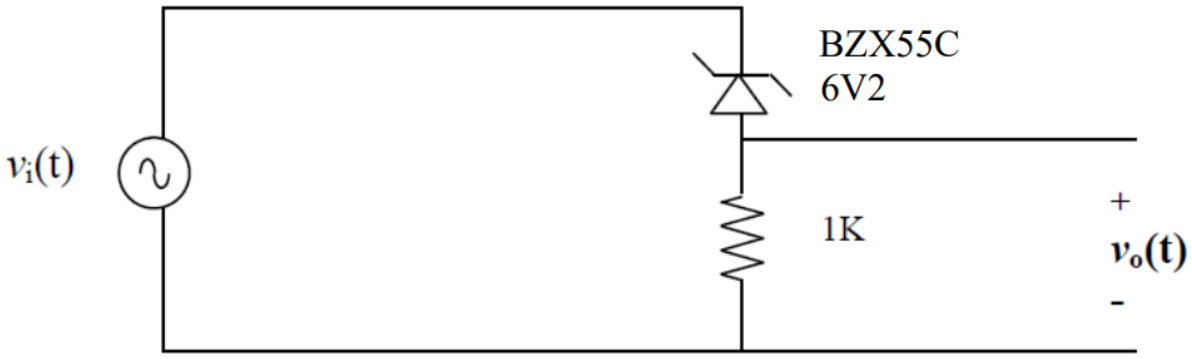

Figure 19: DC level shifter circuit schematic for the Step 9

The circuit given in Figure 20 is constructed in LTSpice environment.

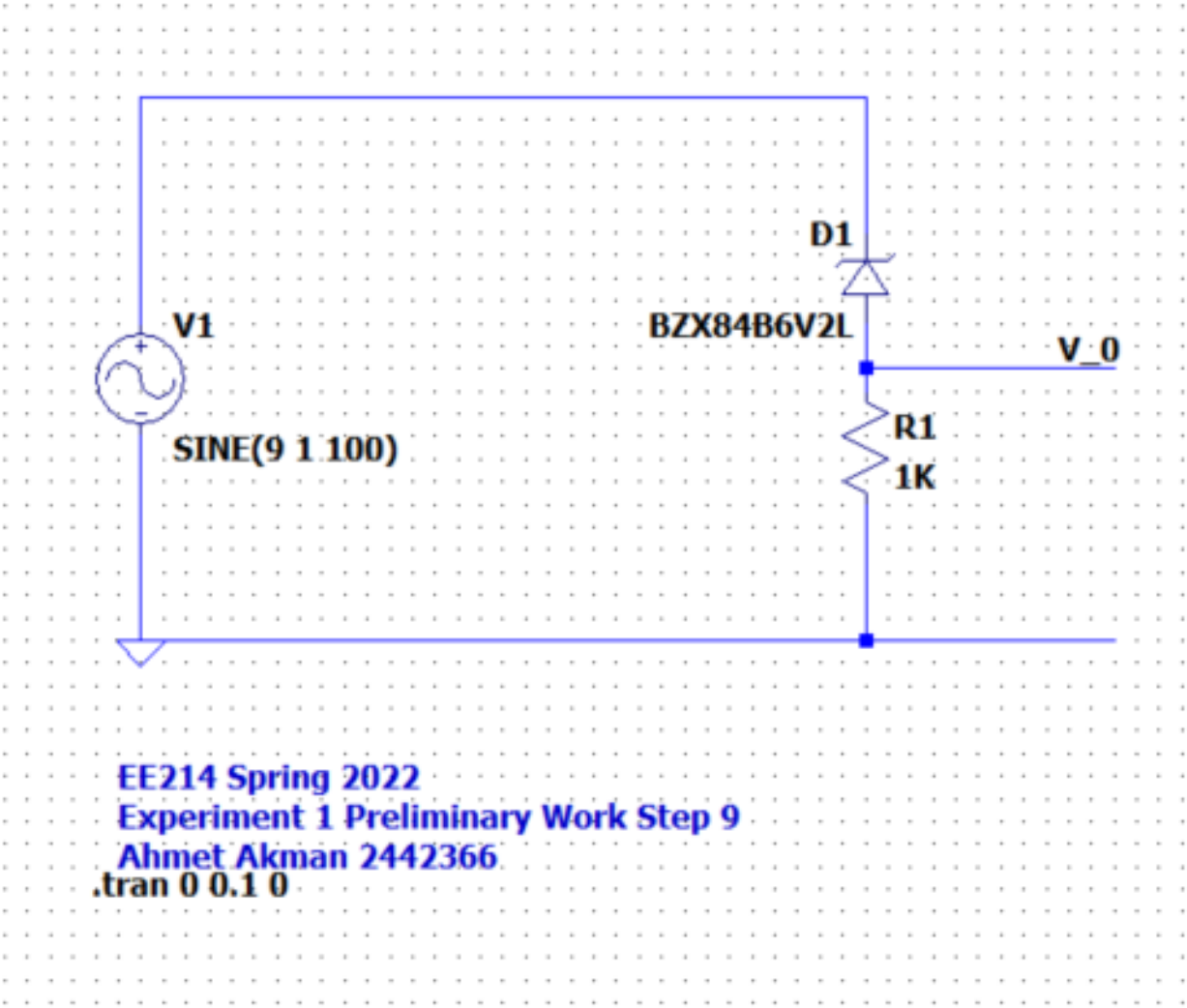

Figure 20: DC level shifter circuit simulation schematic for the Step 9

As the result the plot given in Figure 21 is obtained.

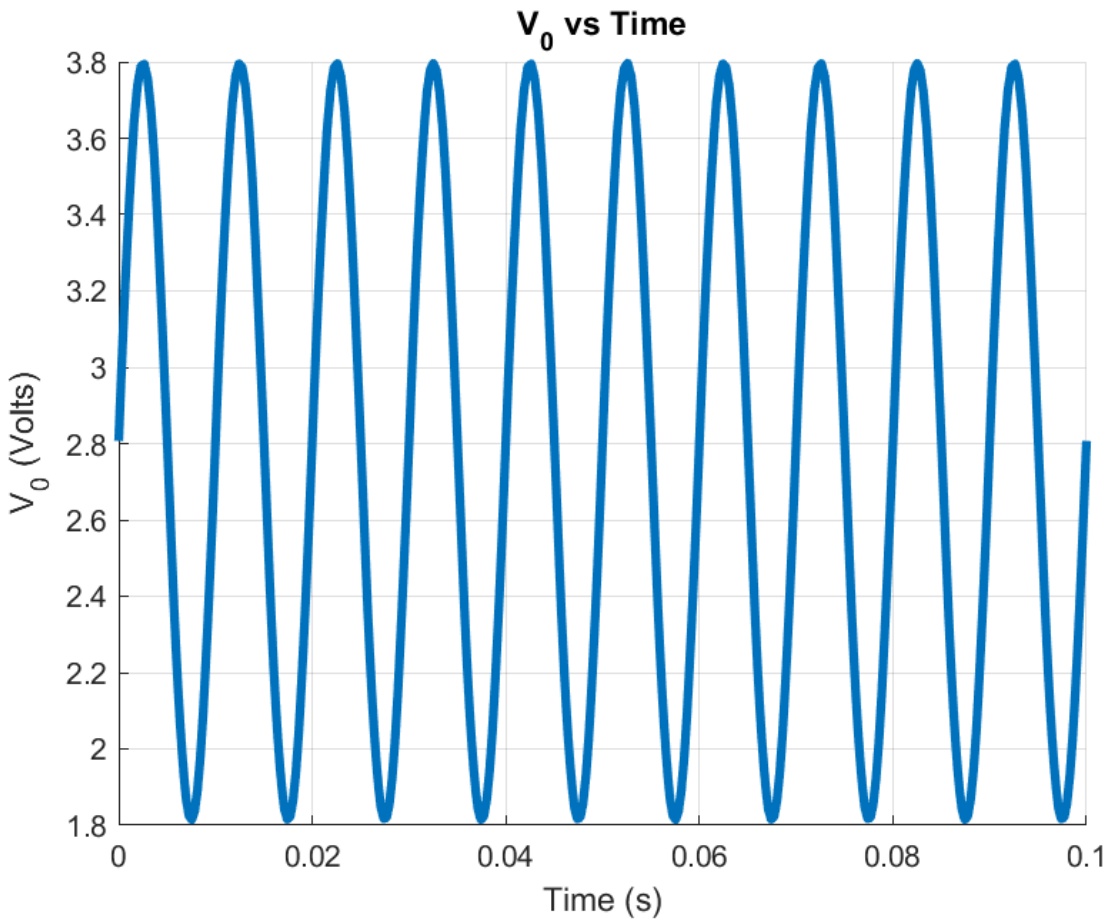

Figure 21: DC level shifter circuit simulation plot V_o

It can be said that the input is shifted appriximately 6 Volts.

10 Step 10

For the steo 10 the circuit given in Figure 22 is taken as a reference.

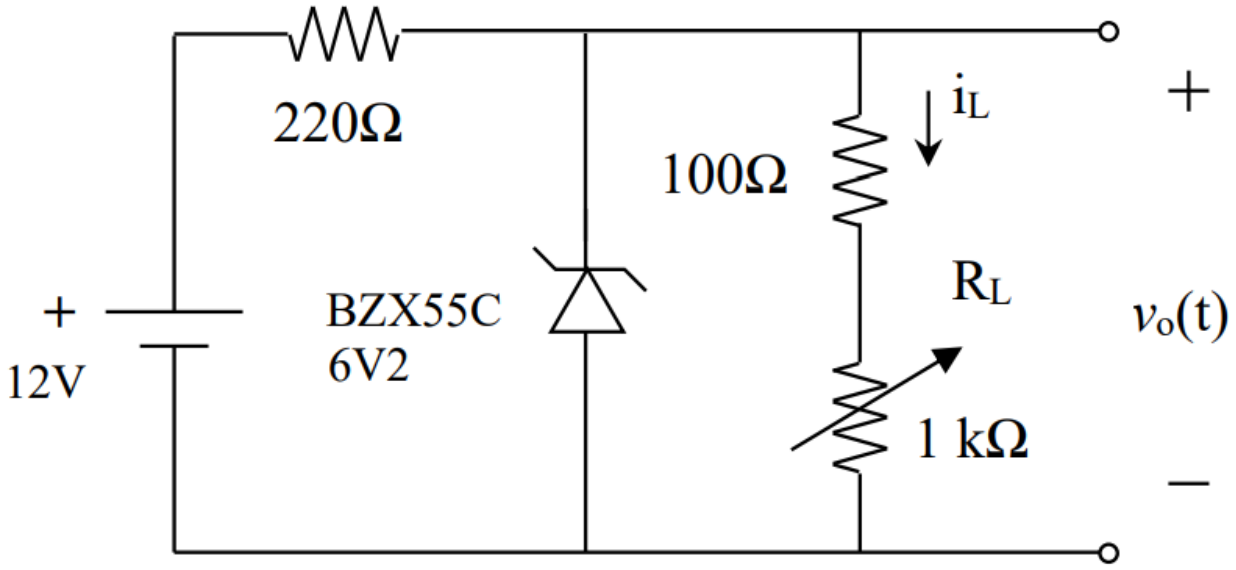

Figure 22: Regulation with zener diode circuit schematic for the Step 10

Then , the circuit given in Figure 23 is set in LTSpice environment.

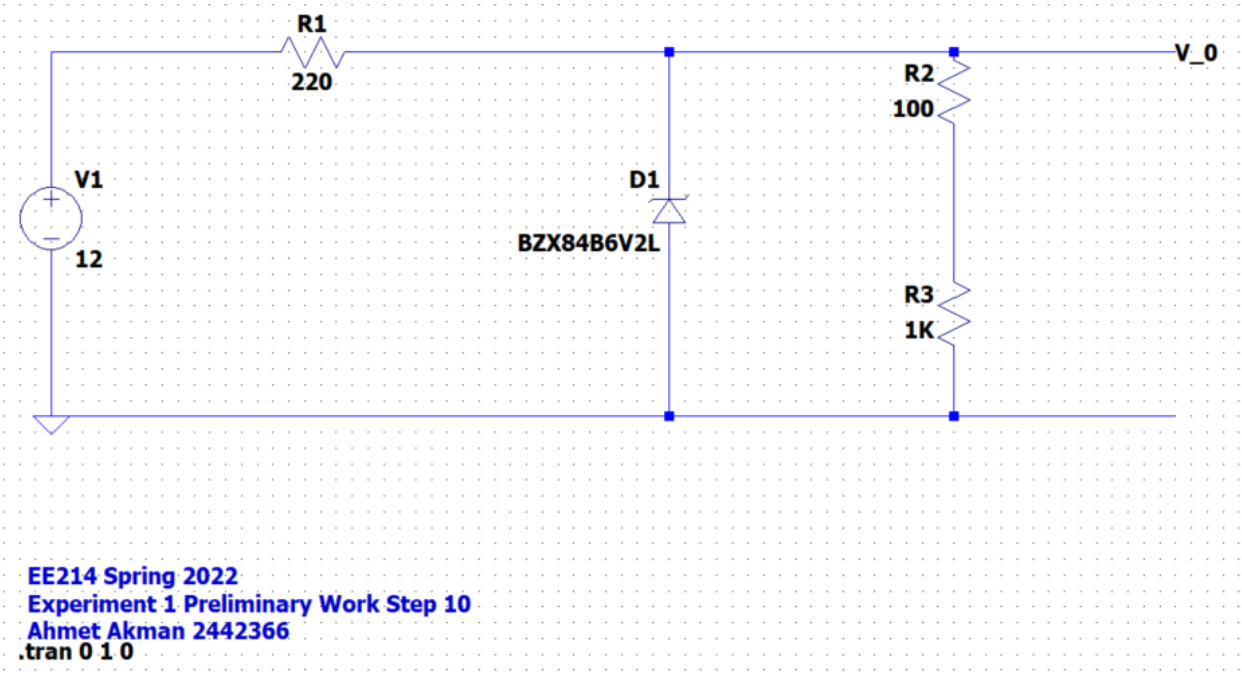

Figure 23: Regulation with zener diode circuit simulation schematic for the Step 10

As the result it can be said that the v_o takes the minimum value of 6.217 Volts and maximumn of 6.221 Volts.

11 Step 11

The clipper circuit given in Figure 24 is considered.

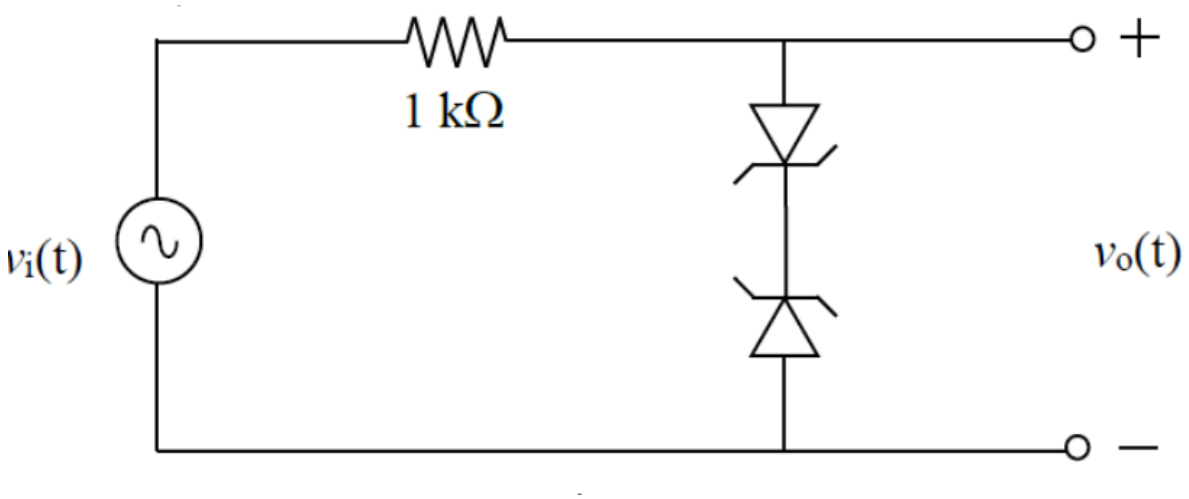

Figure 24: Clipper circuit schematic for the Step 11

The circuit given in Figure 25 is constructed in LTSpice environment.

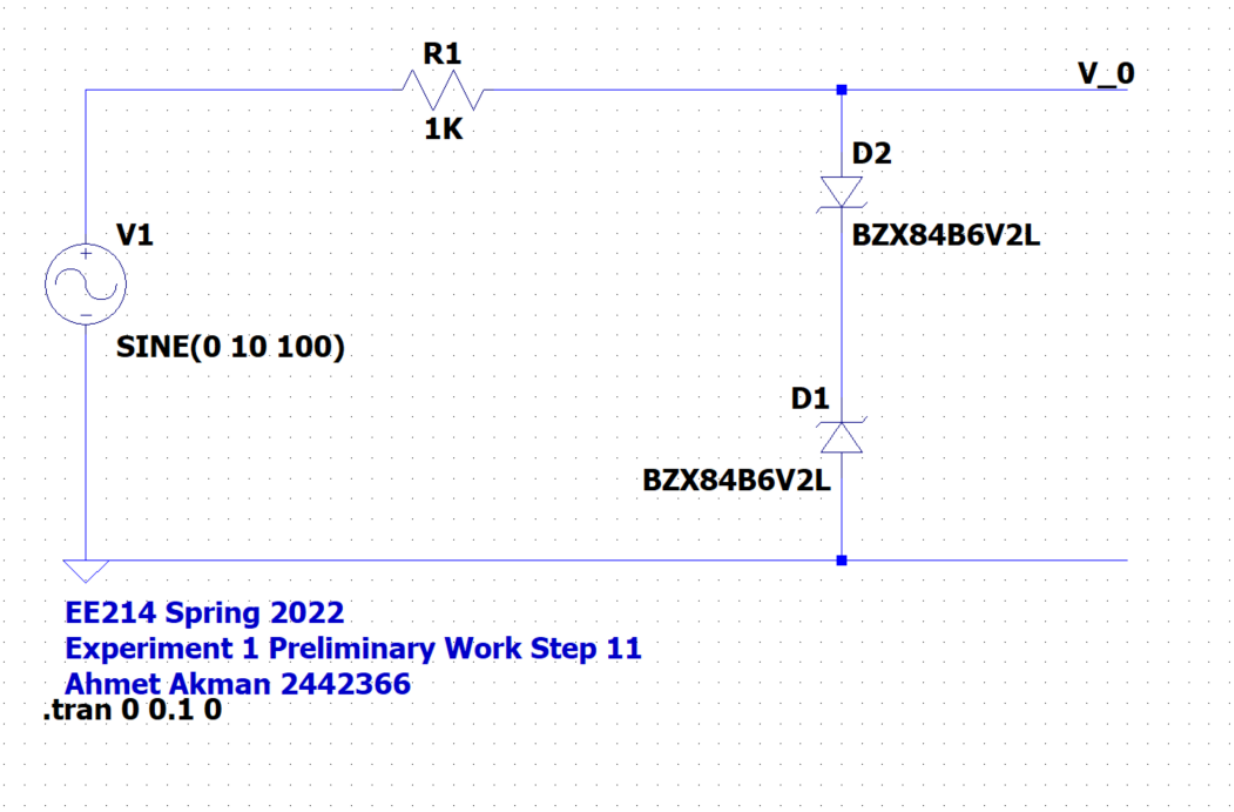

Figure 25: Clipper circuit simulation schematic for the Step 11

As the result the plot given in Figure 26 is obtained.

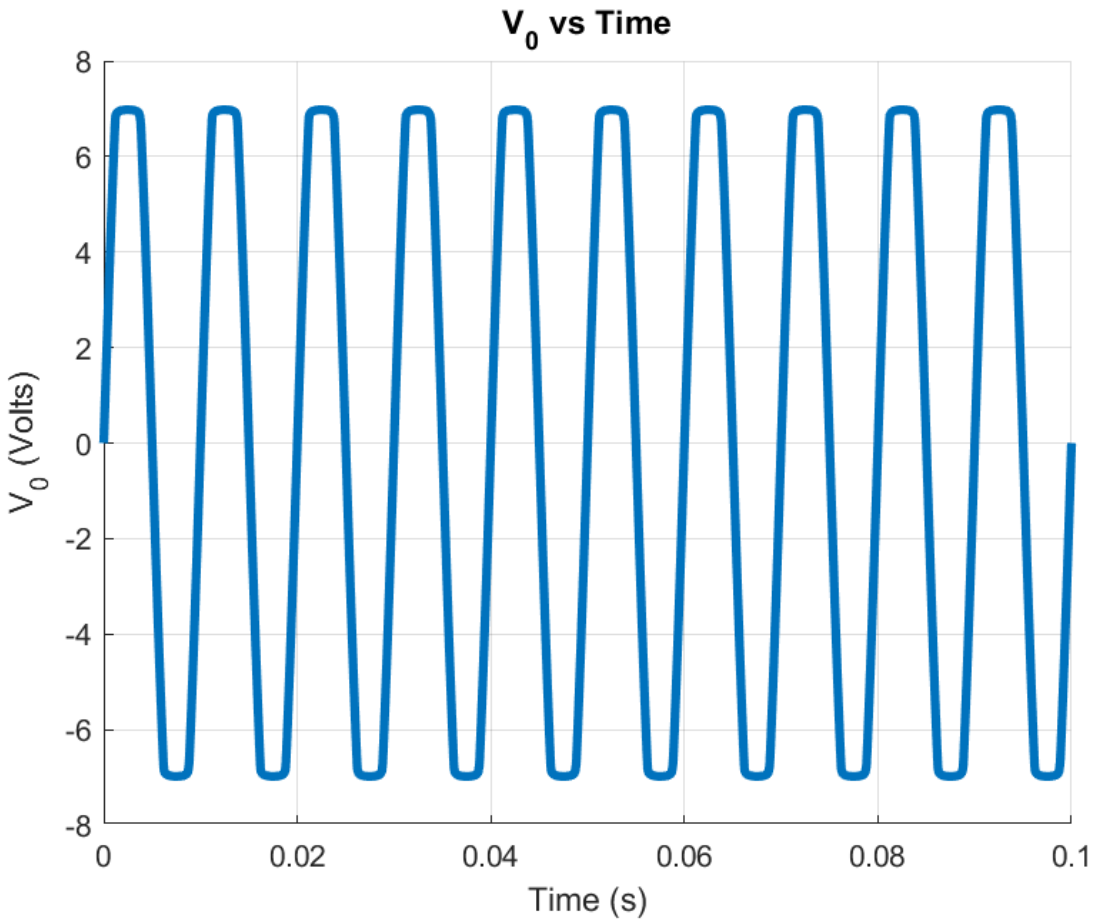

Figure 26: Clipper circuit simulation plot V_o

It can be said that the circuit clips the peaks of the input.

12 Conclusion

In conclusion, as the preliminary work of the first experiment. Some of the rectifier circuts with different diodes are investigated. In this way, various simulations are made. Different kinds of analysis' are done. Therefore their resutls are plotted.

Appendix A

The results of the simulations are fetched from LTSpice and plotted in MATLAB in order to make the plots more readable and convinient.

Appendix B

Figure 27 stands for no capacitor setup.

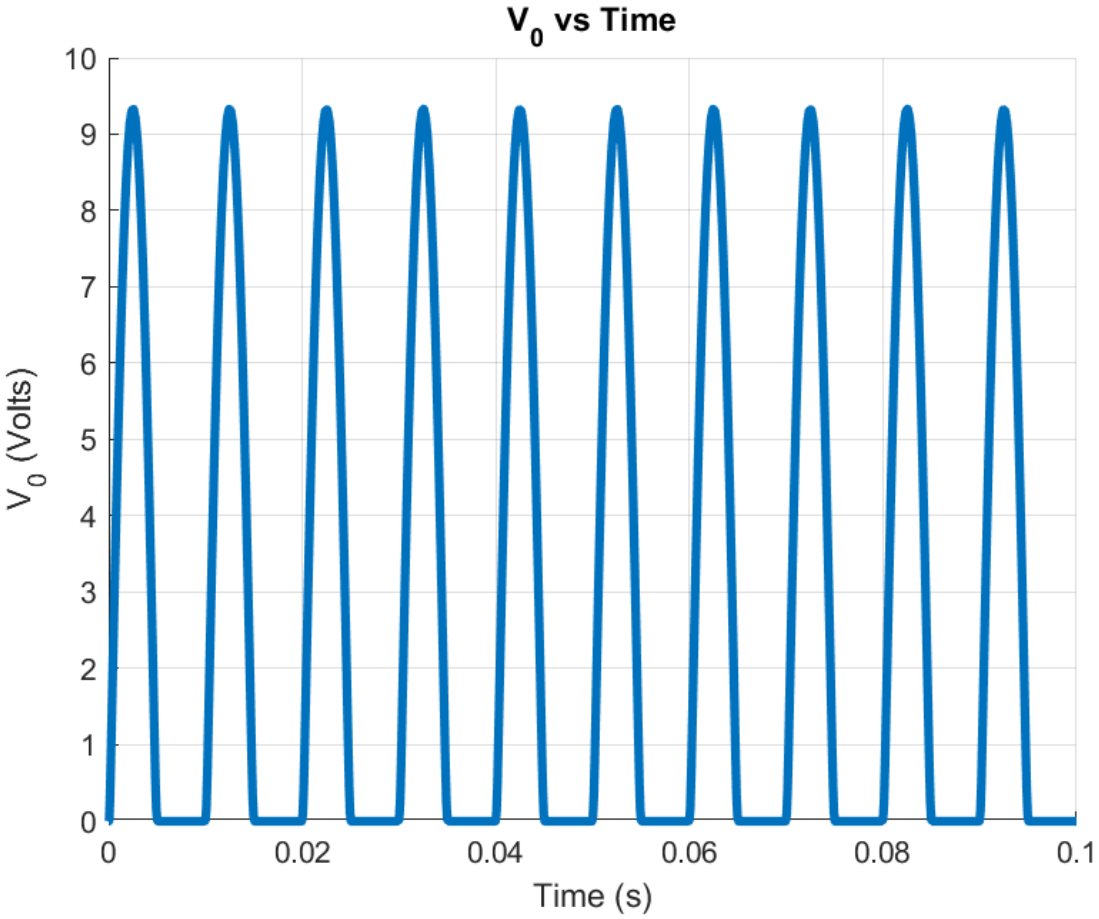

Figure 27: Half wave rectifier circuit simulation plot no capacitor V_o

Figure 28 stands for 10nF capacitor setup.

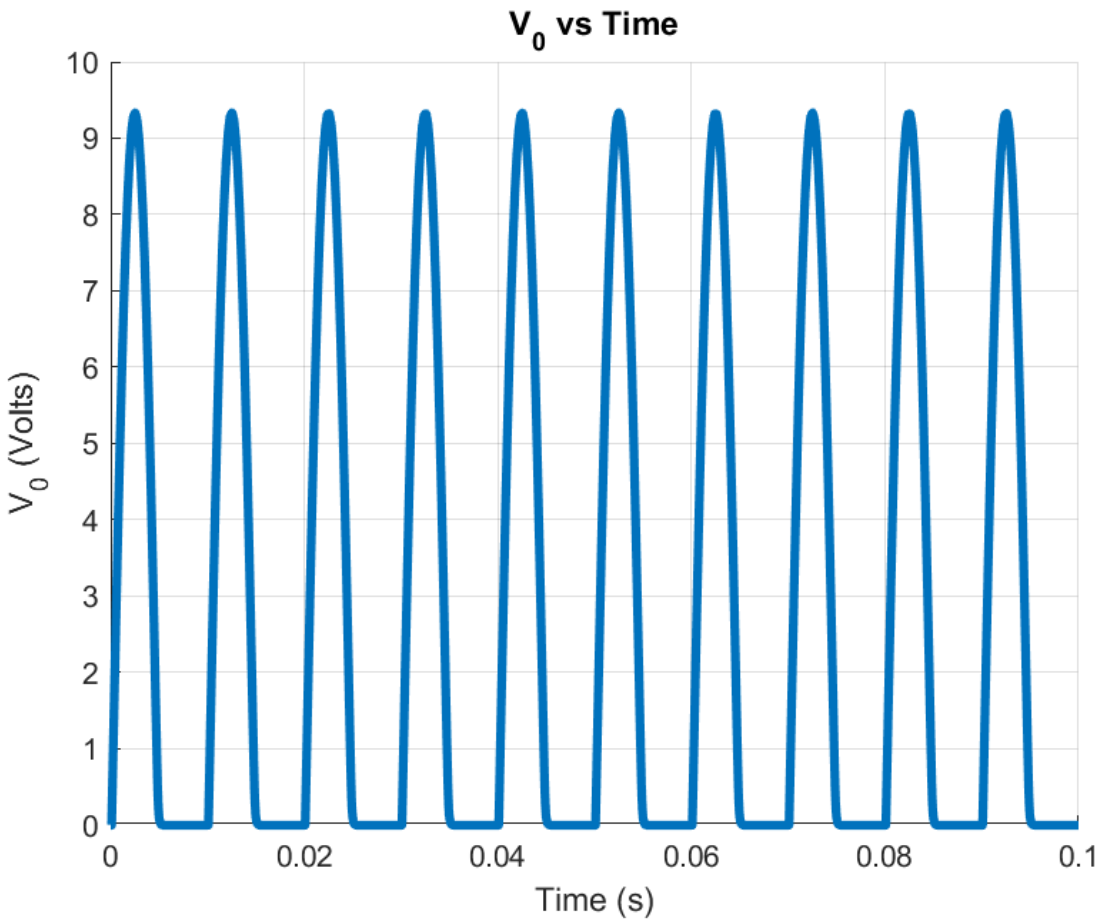

Figure 28: Half wave rectifier circuit simulation plot 10nF capacitor V_o

Figure 29 stands for 1uF capacitor setup.

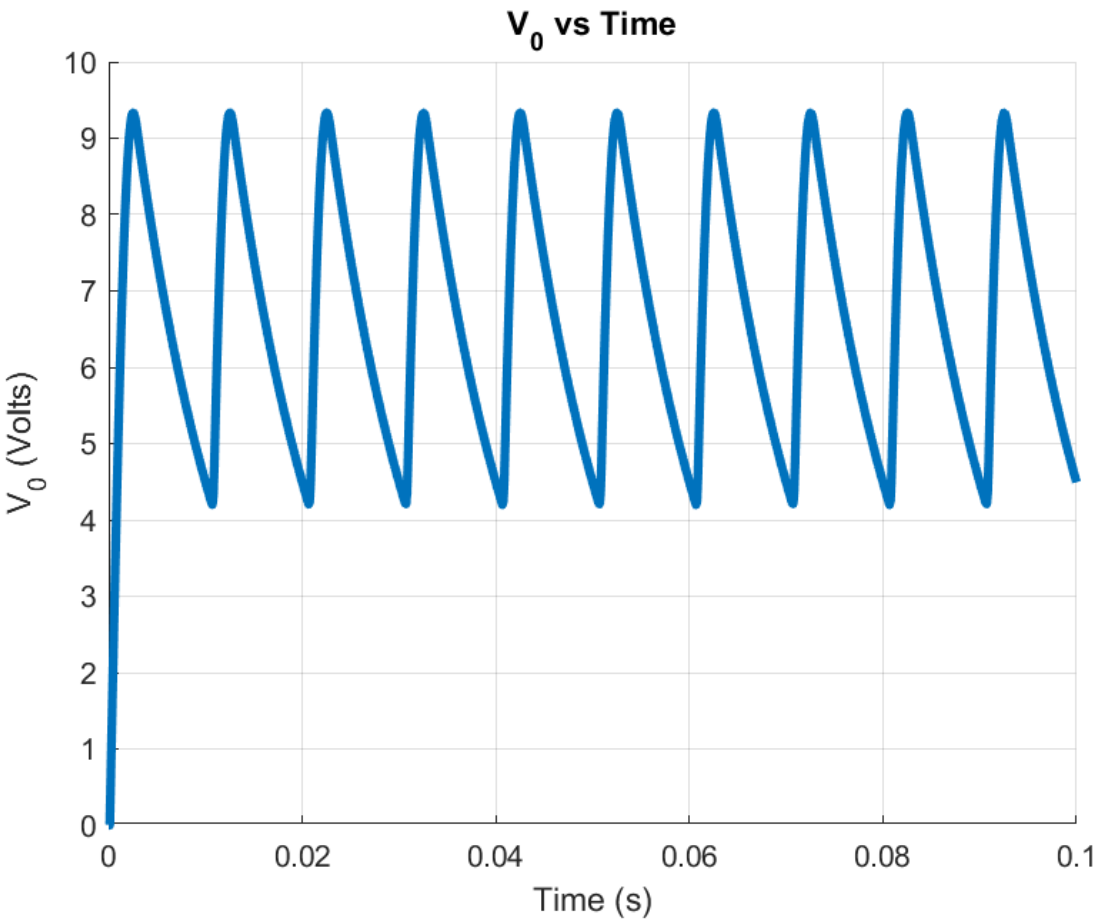

Figure 29: Half wave rectifier circuit simulation plot 1uF V_o