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|  | HACETTEPE UNIVERSITY  ELECTRICAL AND ELECTRONICS ENGINEERING  ELE227 PRELIMINARY WORK #1 |
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1. Convert following decimal numbers to 8-bit binary numbers
2. Convert following 8-bit binary numbers to decimal and hexadecimal

**a.**

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| **RTL SCHEMATIC** |

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| **library IEEE;**  **use IEEE.STD\_LOGIC\_1164.ALL;**  **entity som is**  **Port ( A : in STD\_LOGIC;**  **B : in STD\_LOGIC;**  **C : in STD\_LOGIC;**  **sum : out STD\_LOGIC);**  **end som;**  **architecture Behavioral of som is**  **begin**  **sum <= ((NOT A) AND (NOT B) AND C) OR ((NOT A) AND (B) AND (NOT C)) OR ((A) AND (NOT B) AND (NOT C)) OR ((A) AND (NOT B) AND C) OR((A) AND (B) AND (C));**    **end Behavioral;** |
| **VHDL CODE** |

**b**.

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| **stim\_proc: process**  **begin**  **A <= '0';**  **B <= '0';**  **C <= '0';**  **wait for 100 ns;**  **A <= '0';**  **B <= '0';**  **C <= '1';**  **wait for 100 ns;**  **A <= '0';**  **B <= '1';**  **C <= '0';**  **wait for 100 ns;**  **A <= '0';**  **B <= '1';**  **C <= '1';**  **wait for 100 ns;** | **A <= '1';**  **B <= '0';**  **C <= '0';**  **wait for 100 ns;**  **A <= '1';**  **B <= '0';**  **C <= '1';**  **wait for 100 ns;**  **A <= '1';**  **B <= '1';**  **C <= '0';**  **wait for 100 ns;**  **A <= '1';**  **B <= '1';**  **C <= '1';**  **wait;**  **end process;** |
| **TEST BENCH CODE** | |

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| **TEST BENCH GRAPH** |

**a**.

**b.**

**c.**

**d.**

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| **RTL SCHEMATIC** |

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| **library IEEE;**  **use IEEE.STD\_LOGIC\_1164.ALL;**  **entity cct is**  **Port ( a : in STD\_LOGIC;**  **b : in STD\_LOGIC;**  **c : in STD\_LOGIC;**  **d : in STD\_LOGIC;**  **f1 : out STD\_LOGIC;**  **f2 : out STD\_LOGIC);**  **end cct;**  **architecture Behavioral of cct is**  **begin**  **f1 <= ((c and (not b)) xor a) and ((not a) or c);**  **f2 <= (c and d) or (not d);**  **end Behavioral;** |
| **VHDL CODE** |

**e.**

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| **stim\_proc: process**  **begin**  **-- hold reset state for 100 ns.**  **a <= '0';**  **b <= '0';**  **c <= '0';**  **d <= '0';**  **wait for 100 ns;**  **a <= '0';**  **b <= '0';**  **c <= '0';**  **d <= '1';**  **wait for 100 ns;**  **a <= '0';**  **b <= '1';**  **c <= '1';**  **d <= '0';**  **wait for 100 ns;** | **a <= '1';**  **b <= '1';**  **c <= '1';**  **d <= '1';**  **wait for 100 ns;**  **wait;**  **end process;** |
| **TEST BENCH CODE** | |

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| **TEST BENCH GRAPH** |

**a.**

**b.**

**c.**

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| **RTL SCHEMATIC** |

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| **library IEEE;**  **use IEEE.STD\_LOGIC\_1164.ALL;**  **entity comb\_logic is**  **Port ( x : in STD\_LOGIC;**  **y : in STD\_LOGIC;**  **z : in STD\_LOGIC;**  **a : out STD\_LOGIC;**  **b : out STD\_LOGIC;**  **c : out STD\_LOGIC);**  **end comb\_logic;**  **architecture Behavioral of comb\_logic is**  **begin**  **a <= (x and z) or (y and z) or (x and y);**  **b <= x xor y xor z;**  **c <= not z;**  **end Behavioral;** |
| **VHDL CODE** |

**d.**

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| **stim\_proc: process**  **begin**  **x <= '0';**  **y <= '0';**  **z <= '0';**  **wait for 100 ns;**  **x <= '0';**  **y <= '0';**  **z <= '1';**  **wait for 100 ns;**  **x <= '0';**  **y <= '1';**  **z <= '0';**  **wait for 100 ns;**  **x <= '0';**  **y <= '1';**  **z <= '1';**  **wait for 100 ns;** | **x <= '1';**  **y <= '0';**  **z <= '0';**  **wait for 100 ns;**  **x <= '1';**  **y <= '0';**  **z <= '1';**  **wait for 100 ns;**  **x <= '1';**  **y <= '1';**  **z <= '0';**  **wait for 100 ns;**  **x <= '1';**  **y <= '1';**  **z <= '1';**  **wait;**  **end process;** |
| **TEST BENCH CODE** | |

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| **TEST BENCH GRAPH** |