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**HACETTEPE UNIVERSITY**

**ELECTRICAL AND ELECTRONICS ENGINEERING**

**ELE227 FUNDAMENTALS OF DIGITAL SYSTEMS LABORATORY  
FALL 2019**

**1) Circuit Diagram**

**VHDL Implementation:**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**entity halfAdder is**

**Port ( in1 : in STD\_LOGIC;**

**in2 : in STD\_LOGIC;**

**sum : out STD\_LOGIC;**

**carry : out STD\_LOGIC);**

**end halfAdder;**

**architecture Behavioral of halfAdder is**

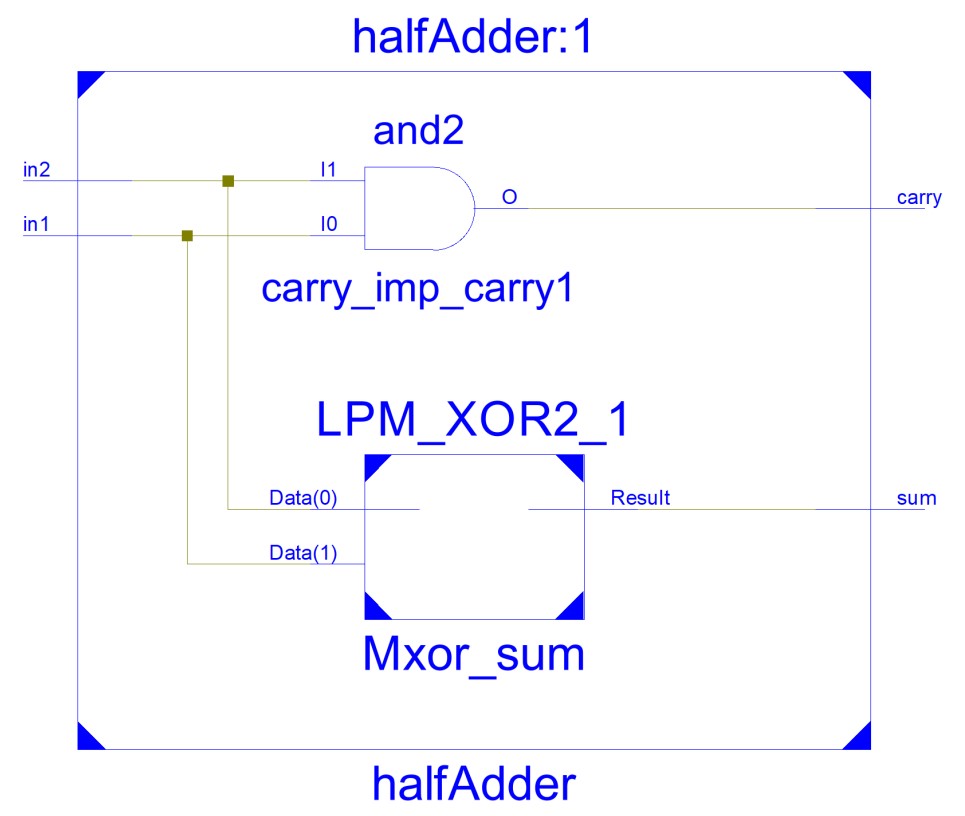
**begin**

**sum <= in1 xor in2;**

**carry <= in1 and in2;**

**end Behavioral;**

**RTL Schematic:**

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**Test Bench Input:**

**begin**

**in1 <= '0';**

**in2 <= '0';**

**wait for 100 ns;**

**in1 <= '0';**

**in2 <= '1';**

**wait for 100 ns;**

**in1 <= '1';**

**in2 <= '0';**

**wait for 100 ns;**

**in1 <= '1';**

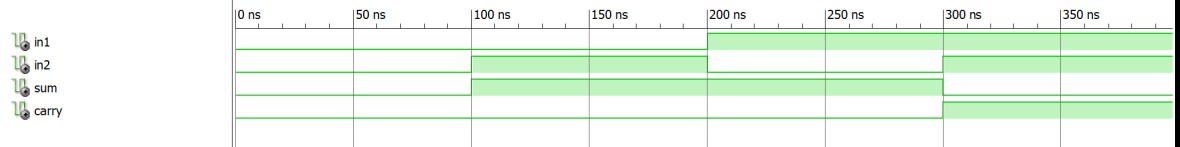
**in2 <= '1';**

**wait for 100 ns;**

**wait;**

**end process;**

**Test Bench Result:**

****

**2) Circuit Diagram**

**VHDL Implementation:**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**entity fullAdder is**

**Port ( in1 : in STD\_LOGIC;**

**in2 : in STD\_LOGIC;**

**cin : in STD\_LOGIC;**

**sum : out STD\_LOGIC;**

**cout : out STD\_LOGIC);**

**end fullAdder;**

**architecture Behavioral of fullAdder is**

**signal sumSign,carrySign1,carrySign2:std\_logic;**

**Component halfAdder is**

**Port ( in1 : in STD\_LOGIC;**

**in2 : in STD\_LOGIC;**

**sum : out STD\_LOGIC;**

**carry : out STD\_LOGIC);**

**end component;**

**begin**

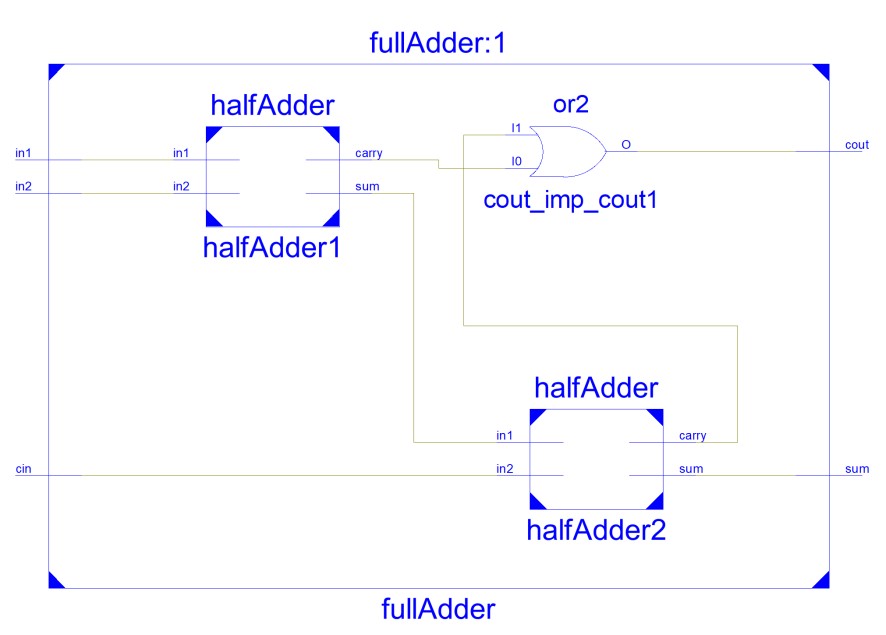
**halfAdder1:halfAdder port map(in1,in2,sumSign,carrySign1);**

**halfAdder2:halfAdder port map(sumSign,cin,sum,carrySign2);**

**cout <= carrySign1 or carrySign2;**

**end Behavioral;**

**RTL Schematic:**

****

**Test Bench Input:**

**stim\_proc: process**

**begin**

**in1 <= '0';**

**in2 <= '0';**

**cin <= '0';**

**wait for 100 ns;**

**in1 <= '0';**

**in2 <= '0';**

**cin <= '1';**

**wait for 100 ns;**

**in1 <= '0';**

**in2 <= '1';**

**cin <= '0';**

**wait for 100 ns;**

**in1 <= '0';**

**in2 <= '1';**

**cin <= '1';**

**wait for 100 ns;**

**in1 <= '1';**

**in2 <= '0';**

**cin <= '0';**

**wait for 100 ns;**

**in1 <= '1';**

**in2 <= '0';**

**cin <= '1';**

**wait for 100 ns;**

**in1 <= '1';**

**in2 <= '1';**

**cin <= '0';**

**wait for 100 ns;**

**in1 <= '1';**

**in2 <= '1';**

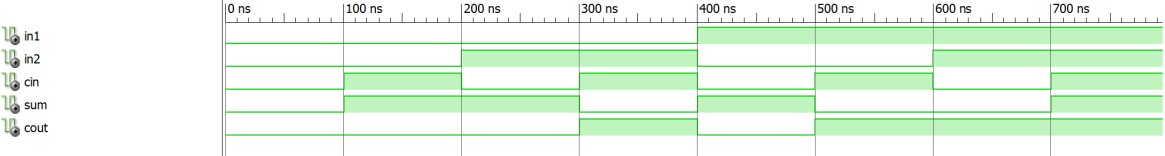
**cin <= '1';**

**wait for 100 ns;**

**wait;**

**end process;**

**Test Bench Result:**

****

**3) Circuit Diagram**

**VHDL Implementation:**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**entity ThreeBitAdderSubtractor is**

**Port ( a : in STD\_LOGIC\_VECTOR (2 downto 0);**

**b : in STD\_LOGIC\_VECTOR (2 downto 0);**

**switch : in STD\_LOGIC;**

**carry : out STD\_LOGIC;**

**result : out STD\_LOGIC\_VECTOR (2 downto 0));**

**end ThreeBitAdderSubtractor;**

**architecture Behavioral of ThreeBitAdderSubtractor is**

**signal aSign1,aSign2,aSign3,carrySign1,carrySign2:std\_logic;**

**component fullAdder is**

**Port ( in1 : in STD\_LOGIC;**

**in2 : in STD\_LOGIC;**

**cin : in STD\_LOGIC;**

**sum : out STD\_LOGIC;**

**cout : out STD\_LOGIC);**

**end component;**

**begin**

**aSign1 <= a(0) xor switch;**

**aSign2 <= a(1) xor switch;**

**aSign3 <= a(2) xor switch;**

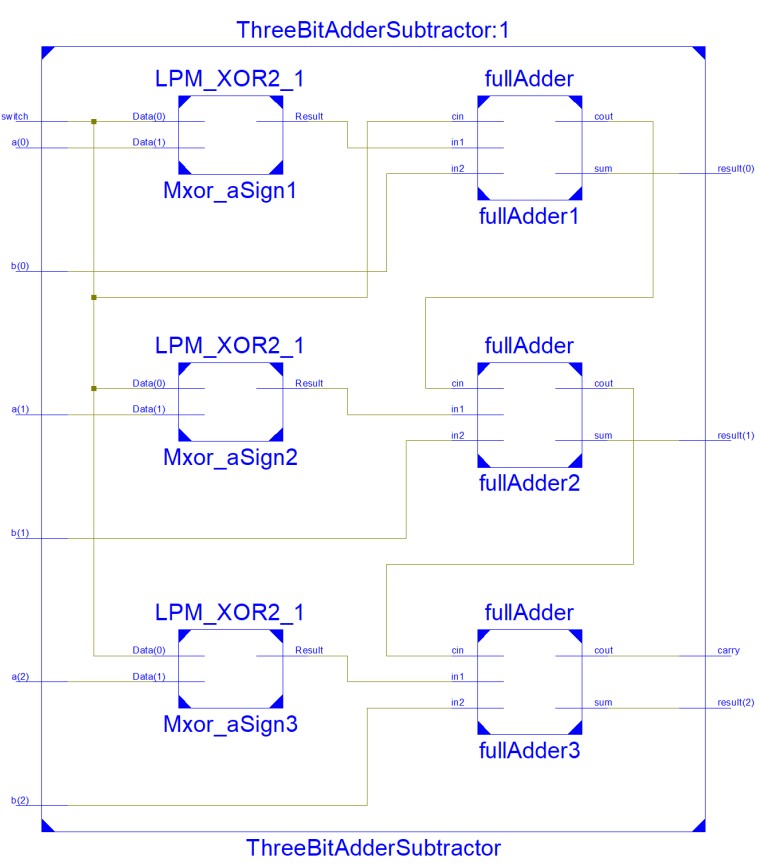
**fullAdder1:fullAdder port map(aSign1,b(0),switch,result(0),carrySign1);**

**fullAdder2:fullAdder port map(aSign2,b(1),carrySign1,result(1),carrySign2);**

**fullAdder3:fullAdder port map(aSign3,b(2),carrySign2,result(2),carry);**

**end Behavioral;**

**RTL Schematic:**

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**Test Bench Input:**

**stim\_proc: process**

**begin**

**a <= "000";**

**b <= "000";**

**switch <= '0';**

**wait for 100 ns;**

**a <= "000";**

**b <= "000";**

**switch <= '1';**

**wait for 100 ns;**

**a <= "011";**

**b <= "001";**

**switch <= '0';**

**wait for 100 ns;**

**a <= "111";**

**b <= "001";**

**switch <= '0';**

**wait for 100 ns;**

**a <= "111";**

**b <= "001";**

**switch <= '1';**

**wait for 100 ns;**

**a <= "100";**

**b <= "111";**

**switch <= '0';**

**wait for 100 ns;**

**a <= "100";**

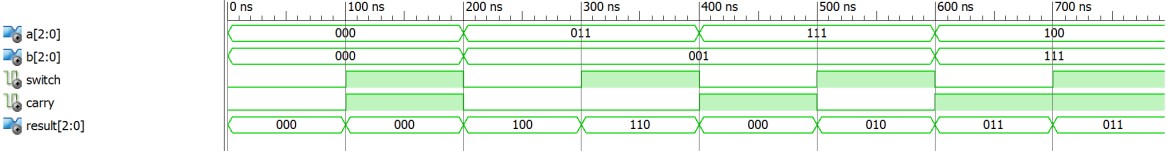
**b <= "111";**

**switch <= '1';**

**wait;**

**end process;**

**Test Bench Result:**

****

**4) Circuit Diagram**

**VHDL Implementation:**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**entity multiplier3Bit is**

**Port ( a : in STD\_LOGIC\_VECTOR (2 downto 0);**

**b : in STD\_LOGIC\_VECTOR (1 downto 0);**

**result : out STD\_LOGIC\_VECTOR (4 downto 0));**

**end multiplier3Bit;**

**architecture Behavioral of multiplier3Bit is**

**signal aSign:std\_logic\_vector(2 downto 0);**

**signal bSign:std\_logic\_vector(2 downto 0);**

**signal carrySign:std\_logic\_vector(1 downto 0);**

**component fullAdder is**

**Port ( in1 : in STD\_LOGIC;**

**in2 : in STD\_LOGIC;**

**cin : in STD\_LOGIC;**

**sum : out STD\_LOGIC;**

**cout : out STD\_LOGIC);**

**end component;**

**begin**

**result(0) <= a(0) and b(0);**

**aSign(0) <= a(1) and b(0);**

**bSign(0) <= a(0) and b(1);**

**fullAdder1:fullAdder port map(aSign(0),bSign(0),'0',result(1),carrySign(0));**

**aSign(1) <= a(2) and b(0);**

**bSign(1) <= a(1) and b(1);**

**fullAdder2:fullAdder port map(aSign(1),bSign(1),carrySign(0),result(2),carrySign(1));**

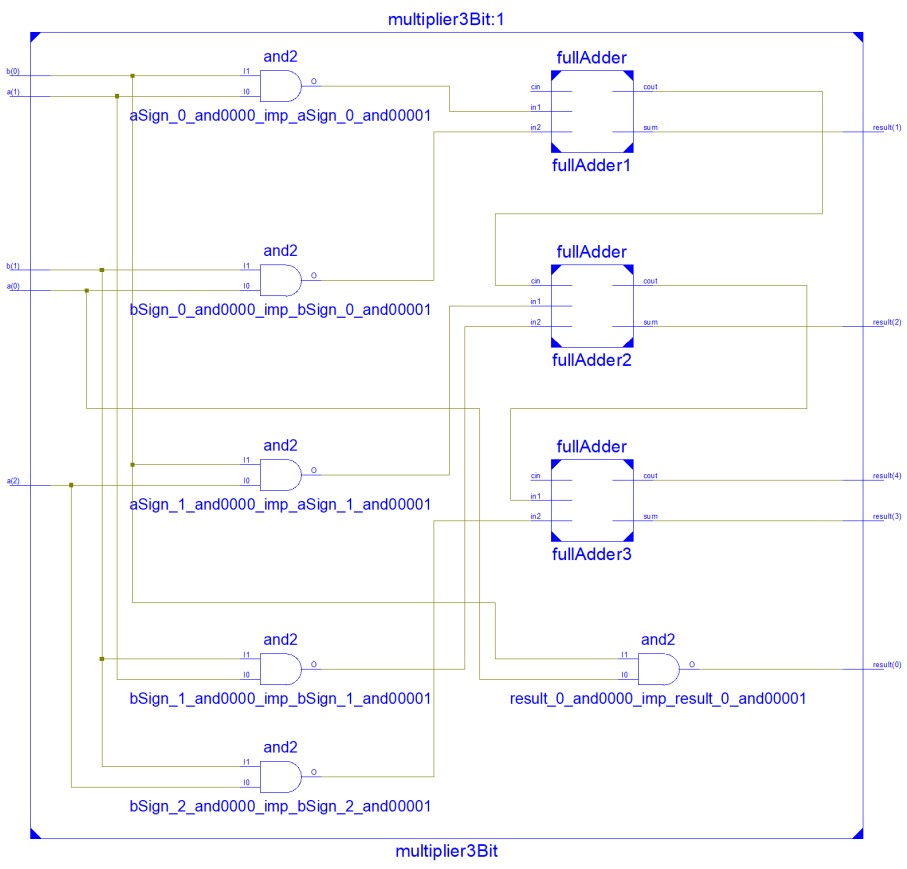
**aSign(2) <= carrySign(1);**

**bSign(2) <= a(2) and b(1);**

**fullAdder3:fullAdder port map(aSign(2),bSign(2),'0',result(3),result(4));**

**end Behavioral;**

**RTL Schematic:**

****

**Test Bench Input:**

**stim\_proc: process**

**begin**

**a <= "000";**

**b <= "00";**

**wait for 50 ns;**

**a <= "000";**

**b <= "01";**

**wait for 50 ns;**

**a <= "000";**

**b <= "11";**

**wait for 50 ns;**

**a <= "001";**

**b <= "01";**

**wait for 50 ns;**

**a <= "001";**

**b <= "10";**

**wait for 50 ns;**

**a <= "001";**

**b <= "11";**

**wait for 50 ns;**

**a <= "011";**

**b <= "01";**

**wait for 50 ns;**

**a <= "011";**

**b <= "10";**

**wait for 50 ns;**

**a <= "011";**

**b <= "11";**

**wait for 50 ns;**

**a <= "111";**

**b <= "01";**

**wait for 50 ns;**

**a <= "111";**

**b <= "10";**

**wait for 50 ns;**

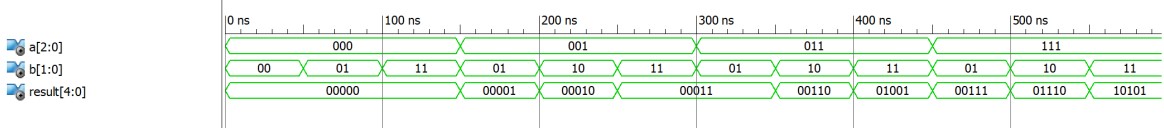
**a <= "111";**

**b <= "11";**

**wait for 50 ns;**

**end process;**

**Test Bench Result:**

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