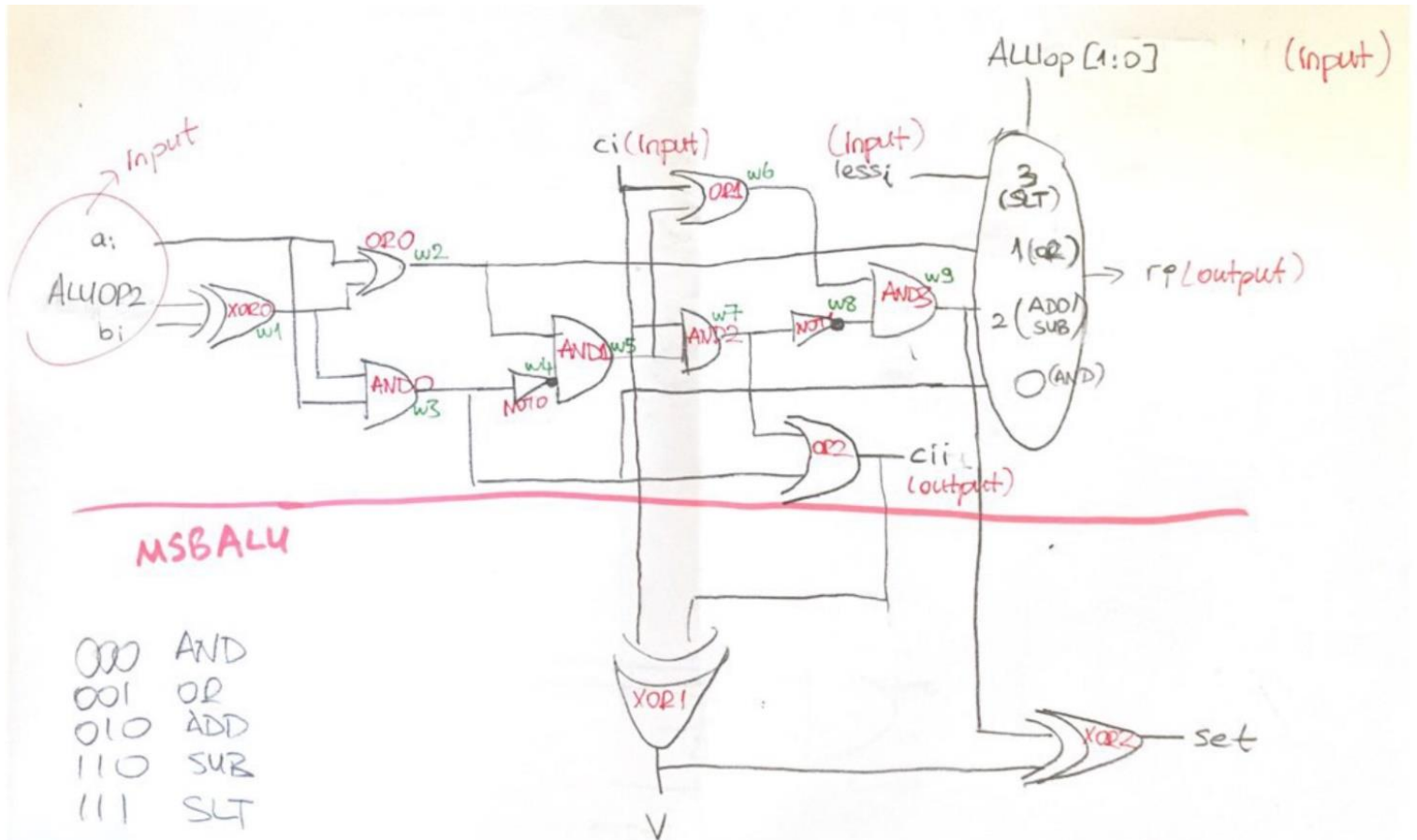


CSE331 COMPUTER ORGANIZATION HW2 REPORT

- I designed my_xor (xor) using 2 not gates, 2 and gates and 1 or gate.
- I designed 2x1 mux using 1 not gate, 2 and gates and 1 or gate.
- I designed 4x1 mux using 3 2x1 muxes.
- I designed alu using 1 my_xor gate, 4 and gates, 3 or gates, 2 not gates, 1 4x1 mux.
- I designed aluMSB using 3 my_xor gate, 4 and gates, 3 or gates, 2 not gates, 1 4x1 mux.
- I designed alu32 using 31 alus, 1 aluMSB.



I tried to show my alu and aluMSB design above so that you can understand the whole verilog code.

Testbench results:

[illegible]