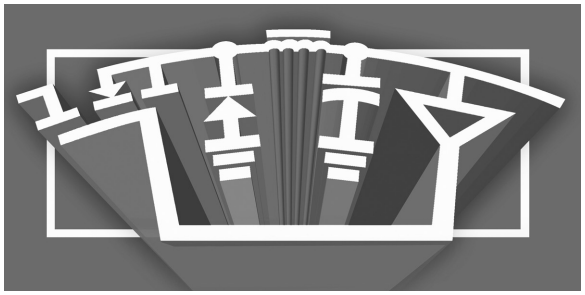

Power Supply Design Seminar

Achieving High-Efficiency with a Multi-Output CCM Flyback Supply Using Self-Driven Synchronous Rectifiers

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Achieving High-Efficiency with a Multi-Output CCM Flyback Supply Using Self-Driven Synchronous Rectifiers

Robert Kollman

ABSTRACT

Broadband access devices are placing high efficiency and low cost requirements on low power, isolated converters. The discontinuous flyback converters has been the traditional choice at these power levels but continuous mode operation is quickly becoming favored as it allows the use of self driven synchronous rectifiers. This paper addresses some of the challenges to CCM operation and their solutions. In particular, the paper discusses the rationale for the selection of the topology. It then provides calculation of circuit stresses and magnetic requirements of the power stage. It also provides analysis and compensation of the power stage with its moving right half plane zero. Finally, measurements of circuit operation are presented to validate the theoretical circuit analysis.

I. INTRODUCTION

High speed internet connections are replacing the traditional telephone connection at customer premise. Voice data can easily be sent over these high speed connections whether it is digital subscriber line (DSL) or cable. However, adding this voice capability has more consequences than just using up some of the available bandwidth because the telephone needs to work even though the power to the customer's premise has been interrupted. In both cable modems and DSLs, two approaches have been implemented; battery back-up at the customer premise or power down the cable/twisted pair. Each approach has it advantages and disadvantages. Battery back-up requires a rather large and expensive battery that is mounted in a controlled environment such as a garage. This requires that the broadband access provider have access to the customer premise for installation and maintenance, which further adds to system cost. In the line powered approach, power is conditioned at a central location and fed down the wire to the customer premise. Since no battery is required, the customer premise equipment can be located outside and access is much easier for the provider. The customer may even be able to handle the installation. However, the provider wants to serve as many customers as possible from a single location so long lengths of wire are used. In the DSL application, this wire can have as much as 1000 ohms of resistance so a relatively high voltage source is required which safety and insulation concerns limit to around 200 V. Adding the fact that the load consumes nearly 10 watts of power further constrains the power supply requirements. Maximum power transfer and system stability both set the minimum usable voltage to one half the source voltage so, in the worst case, only 100 V is available at the customer premise. 100 volts across 1000 ohms of line resistance and 100 volts at the CPE limits the available power to 10 watts so very high power supply efficiencies are required. A similar situation exists in the cable modem systems but is complicated by the use of AC power distribution so power factor becomes an issue.

TABLE 1. MANY BROADBAND ACCESS DEVICES REQUIRE LOW COST AND HIGH EFFICIENCY

	Cable Modem	BNID DSL Modem
Input Voltage	40 Vrms to 90 Vrms Quasi-square wave, 60 Hz or 50 VDC to 150 VDC	100 VDC to 200 VDC
Outputs	5.2 V at 0.6 A, 3.3 V at 0.8 A, 1.8 V at 0.3 A, 1.5 V at 0.2 A, -24 V at 0.12 A, -72 V at 0.1 A	5 V at 0.03 A, 3.3 V at 1.8 A, +/-12 at 05 A, -24 V at 0.12 A, -72 V at 0.1 A
Low Voltage Power (W)	6.6 W	7.3 W
Minimum Efficiency	85%	85%
Isolation	1500 VAC	500 VDC
Cost Target ($)	<$10	<$10

Table 1 presents a summary set of specifications for the customer premise power for these types of systems. Both systems run from a relative high voltage that can have a widely varying source impedance and voltage depending on the distance from the central office or remote terminal and the load demand. In each system, there are a number of output voltages loosely falling into two categories, power for the low voltage electronics and power for the phone. Generating the low voltages efficiently will be the topic of this paper; however, the final power supply will need to address the phone loads also. The power for the low voltage is around 7 watts in both cases and that pushes the efficiency requirement due input power limitations. The peak phone power pushes the output power above 10 watts. The situation is not as bad as it first looks though as the –24 V load does not occur simultaneous with the –72 V. In both cases, the provider is willing to pay for an efficient power supply as this enables him to serve more customers from a single location and limits the power conditioning he has to provide there. Both systems require input to output isolation and both are extremely cost competitive.

II. TOPOLOGY

While the requirements are for a multiple converter, this paper will concentrate on providing the 3.3 volt output only. At these power levels, the flyback topology is very attractive due to its low parts count and good cross regulation of multiple outputs. Synchronous rectification is needed to meet the efficiency goals as a Schottky diode with a 0.45-V forward voltage used on a 3.3-V ouput drop would limit efficiency to 88% just considering the rectification process. Additional circuit losses would probably drop efficiency to the low 80 percent range. At this power level, discontinuous conduction mode (DCM) of operation looks attractive, however, DCM creates an issue in the drive of the synchronous rectifiers. Fig. 1 illustrates the problem. The flyback works by storing energy in the primary of the power transformer while Q1, the primary switch, is on. Current builds in the primary inductance and once an appropriate amount of energy is stored, Q1 turns off. Then the voltage on the transformer reverses and energy is delivered to the secondary through the synchronous rectifier, Q2. Generating the timing of drive for Q1 is not an issue as it is determined by the amount of energy that should be stored in the transformer. The issue is generating the drive waveform for the synchronous rectifier. Turn on can be controlled by the change in polarity on the power transformer, however, turn off can not be controlled in this manner. There are three operational states to this circuit, two of which are not controlled by the control circuits. The primary FET on time is controlled but the synchronous rectifier conduction time and the time when both FET's are off are not controlled. In the non synchronous flyback, once the current has decayed in the transformer secondary magnetizing inductance, the voltage collapses toward zero. However, if a FET was used in place of the diode and its gate was driven from the transformer, the FET would have no turn off command. The secondary current would still decay to zero, gate drive would still be present and then the current would reverse. So a circuit is

required to detect the current reversal and turn the FET off.

An interesting side note is that one can achieve zero voltage switching of both FETs with this approach. The timing would require a delay from the turn off of the primary switch before turning on the secondary switch on the first transition. During the second transition, the secondary circuit would have to generate an appropriate amount of reverse current in the transformer before turning off the synchronous rectifier. This energy could then drive the drain of the primary FET to ground prior to its turn on. The advantages of this mode of operation is zero voltage switching of both FETs. The disadvantages are a relatively complicated control and drive circuit and variable frequency operation.

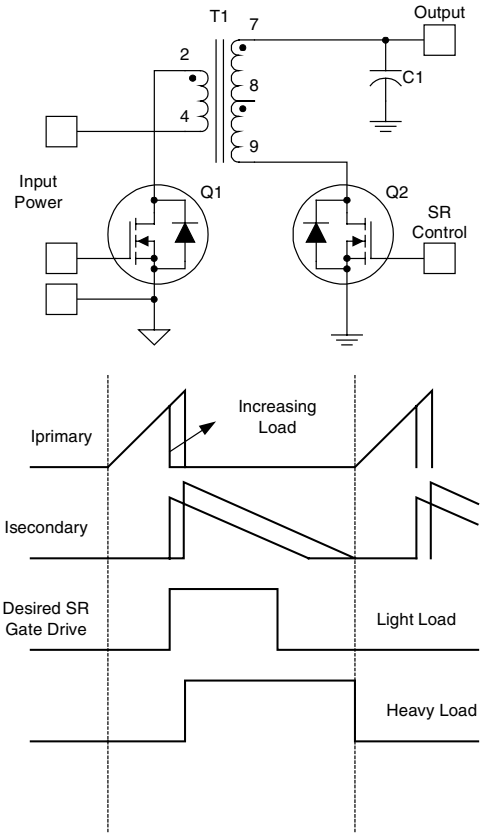

Fig. 1. DCM flyback synchronous rectifiers control needs to sense zero current.

Due to circuit simplicity and low cost, the continuous conduction mode (CCM) flyback is an alternative topology. It is particularly effective for multiple outputs as it improves cross regulation. CCM also reduces circuit stresses significantly. As shown in Fig. 2, current waveforms are trapezoidal rather than triangular. This means that for the same amount of output power, RMS currents are 15% less which means reduced conduction losses (30%) in the power semiconductors and reduced (as much as 50%) filtering requirements in both input and output capacitors. In addition, switching losses could be substantially reduced as peak currents are reduced by a factor of two. However, this is complicated by the fact that a transformer designed for continuous operation will have more leakage inductance than one designed for discontinuous. This inductance must be discharged each switching interval and could lead to significant losses.

Gate drive timing for synchronous rectifiers is simpler because there are two states rather than the three of the discontinuous mode. In fact, the synchronous rectifier can be driven directly from the power transformer. In Fig. 2, Q4, the primary switch is turned on and an incremental amount of energy is added to the power transformer. Q4 is then turned off and the transformer voltage reverses and energy is delivered to the secondary through Q3. When Q4 turns on again, the cycle is repeated. The turn off of Q4 and turn on of Q3 are made with a low voltage present, so they can be termed zero voltage switching. However, the other transition is not as benign as Q4 is turned on with the full input voltage plus the reflected output voltage across it. In addition, it incurs a loss mechanism similar to reverse recovery in an output rectifier, the transformer voltage must collapse to a point to turn the synchronous rectifier off before the synchronous rectifier is disconnected from the circuit. This causes a high current to flow for a brief period in both the rectifier and main switch and leads to switching losses in both of them.

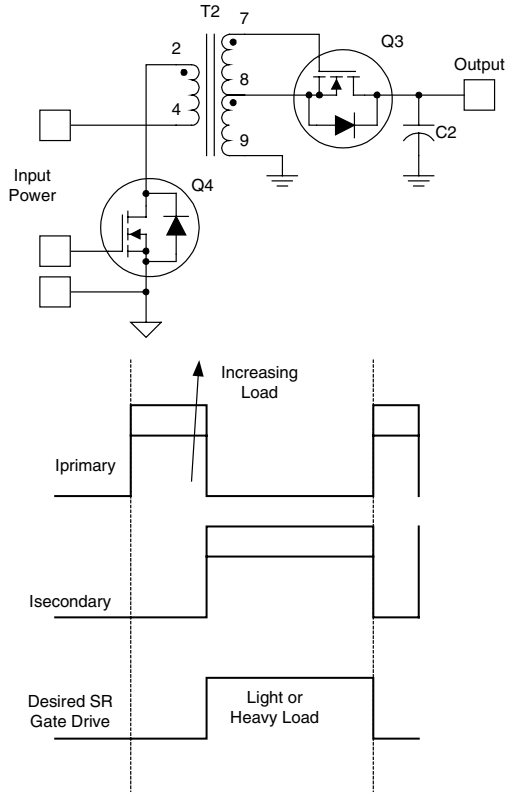

Fig. 2. The CCM flyback can use self driven rectifiers to improve efficiency.

The other significant disadvantage of this approach, is the control characteristics are not as straight forward as the DCM approach. Even with current mode control, this circuit has a right half plane (RHP) zero. In the frequency domain, this RHP zero adds a phase lag to the control characteristics but increases the gain of the circuit. Typical rules of thumb state the highest useable loop crossover frequency is limited to one third the value of the RHP zero. The expression for the location of the RHP zero in a continuous mode flyback is given by:

$$RHPZ = R_l \bullet \frac{(1-D)^2}{2 \bullet \pi \bullet L \bullet D}$$

where R_l is the load resistance, L is the secondary reflected transformer magnetizing inductance and D is the duty factor. The inductance can be minimized to move the RHP. The resulting waveforms are shown in Fig. 3. Rather than having a shallow slope on the current waveform, the slope is similar to the discontinuous flyback. The inductance can even be reduced to the point that the primary switch turns on with reverse current and both transitions could be made with zero switching losses. However, this requires a separate driver with a current sense circuit rather than using the transformer, but results in zero voltage switching and the elimination of the shoot thru current during the turn on of the primary FET.

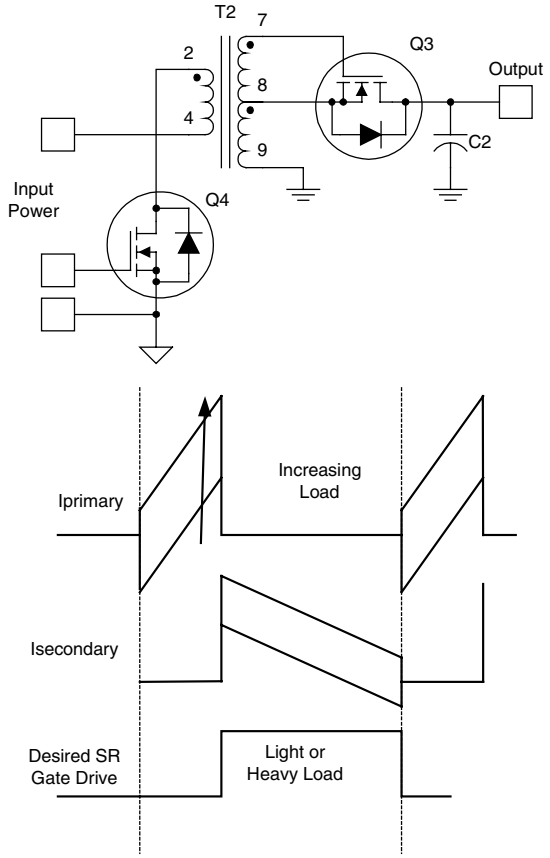

Fig. 3. The synchronous CCM flyback remains continuous regardless of loading.

Reducing the primary inductances, as shown in Table 2, increases the RHP zero location and can result in higher crossover frequencies. This table presents options for the primary inductance of the DSL power supply (refer to Table 1) based on the ratio between the peak-to-peak ripple in the current waveform to its average DC value. The inductance choices start with a relatively high inductance which might be typically chosen for the continuous mode of operation and then progress in octave steps. In this table, the inductance is varied to the point that the waveforms become those of a discontinuous flyback. The RHP zero moves from a low of 5 kHz to over 50 kHz. With the rule of thumb for crossover frequencies being one third the RHP

zero, the crossover frequency can be increased from under 2 kHz to well over 10 kHz with the appropriate choice of inductor. The table also presents the output filter requirements as the inductance is varied. It is interesting to note that the increased ripple current does not significantly impact the value of the output capacitor until the levels of ripple current are quite high. This is due to the fact that the capacitor current does not change polarity during the 1-D state until the ratio of AC to DC current goes above 1.5 to 1. However, the maximum ESR decreases due to the higher ripple current present in the output capacitor.

III. Circuit Stresses and Magnetic Definition

A. Specifying the Transformer

A CCM flyback design starts with a determination of the transformer requirements. The first task is picking turns ratios; this is accomplished by realizing that the volt seconds during the switch on time must equal the volt seconds during the off time. Neglecting the switch drops the expression is:

$$V_{in} \bullet D = V_o \bullet N \bullet (1 - D)$$

Switch drops can be added to the above expression to make them more accurate. Making the assumption of 45% maximum duty factor and solving at the minimum input voltage of 100 volts for the turns ratio yields:

$$N = D\frac{V_{in}}{(1 - D) \bullet V_o}$$

$$N = 0.45\frac{100}{(1 - 0.45) \bullet 3.3}$$

$$N = 24$$

The maximum peak-to-peak ripple current occurs with maximum volt seconds applied to the transformer. This occurs when the output rectifier must conduct for the longest time. Primary inductance can be determined based on the minimum output power by first determining minimum duty at maximum input voltage by the expression:

$$D = \frac{V_o \bullet N}{V_{in} + V_o \bullet N}$$

$$D = \frac{3.3 \bullet 24}{200 + 3.3 \bullet 24}$$

$$D = 0.28$$

Table 2. Reducing Primary Inductance Moves RHP Zero to Higher Frequencies

Primary Inductance (mH)	Ratio Peak-to-Peak Ripple to Max Idc	RHP Zero (kHz)	Required Capacitance (µF)	Maximum ESR
27	0.13	4	200	0.006
16	0.22	6.7	200	0.005
8	0.44	13.3	200	0.005
4	0.9	26.7	200	0.004
2	1.8	72.0	225	0.003

With the minimum duty factor determined at high line, the maximum ripple current can be calculated by equating the input power to the product of duty factor times input voltage times the peak-to-peak ripple current divided by two or:

$$P_{min} = D \bullet V_{in} \bullet \frac{\Delta I}{2}$$

$$\Delta I = 2 \bullet \frac{P_{min}}{D \bullet V_{in}}$$

$$\Delta I = 2 \bullet \frac{0.4}{0.28 \bullet 200} \quad \Delta I = 0.013$$

Again this expression can be refined to include switch drops and power supply efficiency. Once the ripple current has been calculated and an operating frequency selected, the primary inductance is simply calculated. Operating frequency was picked as 166 kHz because this represented a good trade between size and efficiency and it reduced the number of harmonics in the DSL operating frequencies. (6) Solving for primary inductance at 166 kHz yields:

$$e = L \bullet \frac{\Delta I}{\Delta t}$$

$$L = e \bullet \frac{\Delta t}{\Delta I}$$

$$L = V_{inmax} \bullet \frac{D}{f \bullet \Delta I}$$

$$L = V_{inmax} \bullet \frac{D}{f \bullet \Delta I}$$

$$L = 200 \bullet \frac{0.28}{166{,}000 \bullet 0.13}$$

$$L = 0.027 \text{ H}$$

This is used as the starting value of Table 2 and was reduced to move the RHP zero out and to provide zero voltage switching at lighter loads.

Table 3 presents a sample specification for the transformer. It identifies mode of operation and operating frequency. It also specifies a variation in the operating frequency as all control ICs are not perfect and a 30% variation over temperature and tolerances is not uncommon. The spec does not calculate detail RMS currents or exact turns ratio giving the magnetics designer some latitude in volts per turn selection. It also includes some physical requirements including maximum temperature rise and ambient temperature.

TABLE 3. EXAMPLE TRANSFORMER SPECIFICATION

Mode	Continuous flyback
Operating Frequency	150 kHz to 200 kHz
Maximum Duty Factor	45%
Input Voltage	100 VDC to 200 VDC
Output 1	3.3 V at 2.3 A, assume 0.1 V diode drop
Output 2 (Secondary Bias and Gate Drive)	5 V at 0.07 peak, 0.035 A average
Output 3 (Primary Bias)	Pri referenced bias winding, 10 V at 0.01 A
Approximate Turns Ratio, Primary to 3.3 V	24 to 1
Minimum Primary Inductance	6 mH
Leakage Inductance Primary to Shorted Output 1	100 μH
Peak Current	0.11 A
Maximum Height	0.75 inches
Preferred Mounting	SMT
Maximum Ambient Temperature	85°C
Maximum Temperature Rise	45°C, 1500 V isolation
Safety Agency Requirements	CSA, UL, etc.

B. Select the Primary FET

The second step in the power stage design is selecting the primary switch. The voltage on the FET is equal to the maximum input voltage plus the reflected output voltage plus some margin for leakage inductance energy ringing with parasitic capacitances. At low line, the volt seconds on the transformer must balance so the reflected transformer voltage is determined by equating the on time and off time volt-second product or:

$$\frac{D}{f} \bullet V_{inmin} = V_{reflected} \bullet \frac{(1 - D)}{f}$$

$$V_{reflected} = V_{inmin} \bullet \frac{D}{(1 - D)}$$

$$V_{reflected} = 100 \bullet \frac{0.45}{(1 - 0.45)}$$

$$V_{reflected} = 82\ V$$

Some margin needs to be allowed for spiking during turn off. So with a 100 to 200 V input range and a 282 V stress, a 400 V FET should provide ample margin for the spiking.

The next step is to determine the FET resistance which is an iterative process of selection, P-Spice® analysis, and laboratory thermal measurements. A good starting point is to determine an allowable voltage drop during the conduction time and pick a part. This power supply requirement is extremely efficiency conscious so that the FET selection needs to trade switching losses versus conduction losses. If the assumption is made that the allowable efficiency loss is 2%, the optimal loss occurs when switching and conduction losses are equal. 1% conduction loss means the switch drop is 1% of the minimum input voltage or 1 V. One first needs to calculate the DC input current at low line which is:

$$I_{dc} = \frac{P_{max}}{V_{in(min)} \bullet \eta}$$

$$I_{dc} = \frac{3.3V \bullet 2.3A}{100V \bullet 0.85}$$

$$I_{dc} = 0.089\ A$$

Then solve for peak current using duty factor at low line and assuming a rectangular current wave form. Then the needed maximum FET resistance is calculated assuming 1-V switch drop.

$$I_{pk} = \frac{I_{dc}}{D}$$

$$I_{pk} = \frac{0.089}{0.45}$$

$$I_{pk} = 0.2A$$

$$R_{fet} = \frac{1}{I_{pk}}$$

$$R_{fet} = 5$$

This value of on-resistance for 400 V FETs is higher than commonly available so a slightly lower resistance part was chosen as the starting point. This part had an on resistance (R_{ds}) of 3.6 ohms, a total gate charge (Q_g) of 12 nC, gate to drain gate charge (Qgd) of 6.5 nC and an output capacitance (C_{oss}) of 34 pF. Conduction loss at low line is calculated as:

$$P_{condloss} = I_{rms}^2 \bullet R_{ds}$$

$$P_{condloss} = D \bullet Ipk^2 \bullet R_{ds}$$

$$P_{condloss} = 0.45 \bullet 0.2^2 \bullet 3.6$$

$$P_{condloss} = 0.065$$

Next, the available gate drive current is estimated from a typical controller (UCC2809) data sheet using the fall time spec to discharge a 1 nF capacitor in 18 ns.

$$ig = C \bullet \frac{V_{gate}}{T_{fall}}$$

$$ig = \frac{1 \bullet 10^{-9} \bullet 12}{18 \bullet 10^{-9}}$$

$$ig = 0.667$$

This gate drive current is then used to calculate the turn off losses recognizing the fact that the FET conducts until the gate to drain charge is depleted. This turn off time (T_{to}) can be calculated using the gate drain capacitance divided by the drive current. The FET turns off with peak current and charges toward input voltage plus the reflected load voltage (or twice the input voltage in this case). The FET conducts during this period until the drain voltage quits increasing, at which time the current is ramped down rapidly. The switching loss per turn off cycle can be approximated by:

$$E_{to} = T_{to} \bullet I_{pk} \bullet 2 \bullet \frac{V_{in(min)}}{2}$$

Multiply this energy by the switching frequency to calculate loss and substituting to determine turn off time yields:

$$P_{toffloss} = T_{to} \bullet \left(I_{pk} \bullet 2 \bullet \frac{V_{in\,min}}{2} f \right)$$

$$P_{toffloss} = \frac{Q_{gd}}{ig} \bullet I_{pk} \bullet V_{in(min)} \bullet f$$

$$P_{toffloss} = \frac{6.5 \bullet 10^{-9}}{0.67} \bullet 0.2 \bullet 100 \bullet 166 \bullet 10^{3}$$

$$P_{toffloss} = 0.032 \text{ W}$$

A second switching loss occurs when the FET turns on. The FET output capacitance must be discharged and results in loss. Calculating the loss in the output capacitance is complicated by the fact that it is a combination of two non-linear capacitances. One can make a few simplifications to get to a first order solution of the loss. The first assumption is that the drain to source charge is significantly larger than the drain to gate charge. The second assumption is that the drain to source capacitance has the following relationship of a p-n junction:

$$C_{jo} = C_{oss} \bullet (V_{Coss})^{0.5}$$

where V_{Coss} is the voltage at which C_{oss} is specified. With a little manipulation and the simplifying assumption of the FET off voltage equaling twice the low line input voltage, a closed form solution can be developed for this energy loss term as follows, first by determining energy loss (E) per cycle and then multiplying by switching frequency (f):

$$E = \int_0^{2 \bullet V_{in\,min}} C \bullet V dV$$

$$E = \int_0^{2 \bullet V_{in\,min}} \frac{C_{jo}}{V^{0.5}} \bullet V dV$$

$$E = \frac{2}{3} \bullet C_{jo} \bullet (2 \bullet V_{in\,min})^{1.5}$$

$$P_{Cossloss} = E \bullet f$$

$$P_{Cossloss} = \frac{2}{3} \bullet 170\text{pF} \bullet (2 \bullet 100\text{V})^{1.5} \bullet 166\text{kHz}$$

$$P_{Cossloss} = 0.053 \text{ W}$$

This loss is particularly hard to measure as it is all internal to the FET, however, it's measurement can be combined with the turn off loss measurement. Energy delivered into the FET during turn-off is either dissipated in the channel or stored as drain to source charge. Without zero voltage switching of the FET, this stored energy is dissipated at turn on. So the measured turn off loss in reality is turn off loss plus C_{oss} loss. The last significant loss mechanism is the reverse recovery-like loss characteristics of the synchronous rectifier. Estimates could be made based on its turn off times of the synchronous rectifiers but they would be grossly in error as circuit parasitics will, to a large point, determine these losses. The lab is probably the best place to evaluate these losses.

C. Select the Secondary FET

The selection of the secondary FET involves calculation of gate-to-source and drain-to-source voltage stresses and then the determination of allowable on-resistance. The drain to source voltage is determined by the output voltage plus the reflected maximum input voltage or in this case, 3.3 volts plus 200 volts divided by 24 to one which equals 12 volts. A 40 volt was selected to provide significant voltage margin, however, a 20 volt device probably could have been made to work with better efficiency.

The driving of the synchronous rectifier from the transformer requires a judicious selection of turns ratios and FET threshold and gate to source voltage rating. The FET must be fully enhanced for good efficiency but it must not be overstressed at maximum input voltage. A logic level device was picked for the rectifier. The transformer turns ratios were picked to provide approximately 3 volts of drive to enhance the synchronous rectifier. This sets the ratio between drive voltage and output voltage as 1-to-1. The maximum gate to source stress during the secondary off time can be calculated based on the turns ratio. With a 24-to-1 turns ratio and a 200 volt input, gate to source stress is 8.3 volts with almost 4 volts margin over a 12 volt gate to source rating.

The final step involves determining the allowable FET on resistance. A good starting point is allowing a 0.1 volt drop on the rectifier during conduction. This contributes about a 3% reduction in efficiency while not overburdening the cost of the power supply. At this drop, 5-10 amp output currents can be accommodate without the need for heatsinks or specially cooling. The worst case peak current in the rectifier occurs at low line and can be related to the output current and duty factor as:

$$I_{Rect\text{-}pk} = \frac{I_o}{1 - D}$$

$$I_{Rect\text{-}pk} = \frac{2.3}{0.55}$$

$$I_{Rect\text{-}pk} = 4.2A$$

Allowing a 0.1 volt drop in the rectifier fixes the rectifier on resistance to 10 mohms.

$$R_{Rect} = \frac{0.1}{I_{Rect-pk}}$$

$$R_{Rect} = 0.023$$

D. Designing the Output Filter

The simplest filter is a capacitor and determining its specifications is fairly straight forward from circuit stresses and power supply requirements. The current waveform in the capacitor is mostly rectangular in shape with the full load current being drawn from the capacitors during the primary switch on time and sufficient charge to replenish the capacitors being deposited during the off time. The needed capacitor value can be determined from the maximum load current and maximum on time. The change in charge ($I_o \bullet D/f$) and the maximum ripple voltage specification (V_{ripple} = 0.03 V) determines the needed capacitance by the formula:

$$C = I_o \bullet \frac{D}{f \bullet V_{ripple}}$$

$$C = 2.3A \bullet \frac{0.45}{166kHz \bullet 0.03V}$$

$$C = 210\ \mu F$$

ESR is the second needed specification for the capacitor bank. This is calculated by realizing the total change in current results in a ripple voltage that is proportional to the ESR. Making the assumption that the current waveform is rectangular in shape allows the peak-to-peak current (I_{pp}) to be calculated as the average output current divided by (1-D). The required ESR is then obtained from the ripple requirement.

$$I_{pp} = \frac{I_o}{1 - D}$$

$$I_{pp} = 4.2$$

$$R_{esr} = \frac{V_{ripple}}{I_{pp}}$$

$$R_{esr} = 7x10^{-3}$$

The two components of output ripple add in quadature so the total peak-to-peak ripple is the sum of the two. When picking a capacitor based on these calculations, a trade off will be needed to allocate ripple contributions of the two elements. This set of requirements for capacitors is typical of high performance capacitors used in laptop and servers and is much too expensive for commodity applications. A less expensive but more complicated filter is required to be cost competitive. A two stage filter as shown in Fig. 4 is definitely attractive. In this approach, the input capacitor C16 is selected by its ripple current rating and a significant voltage ripple of 300 mV to 500 mV is present. This relatively small amount of capacitance on the filter input is desirable to move the interactions with the remaining output filter components to as high of a frequency as possible. However, it was found in the modelling and later verified in the lab, that the high Q of the ceramic capacitor and its peaking effect with the output inductor caused an unacceptable current loop response. A larger aluminum electrolytic capacitor was therefore added for damping. Inductor L1 and capacitor C17 provide the final filter with approximately 20 dB of attenuation at the switching frequency. C17 is chosen based on several constraints. It should be large enough that it is not significantly impacted by the addition of load capacitance. It also provides damping of the output filter so that a lossy (and cheap) capacitor is desirable. If it were high quality, two very high Q circuits would be formed leading to high output impedances and undesirable control characteristics.

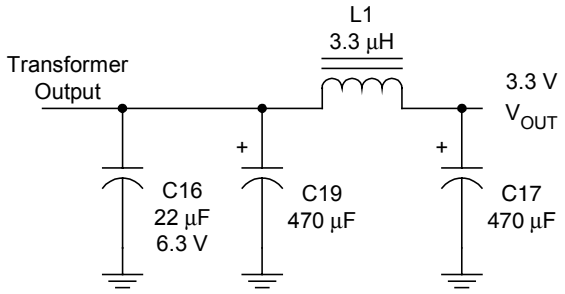

Fig. 4. Two-stage filter is less expensive than single section.

The design process of the filter is to pick first an input capacitor based on ripple current which is calculated by:

$$I_{Cout} = \left(\frac{D}{1-D}\right)^{0.5} \bullet I_o$$

$$I_{Cout} = \left(\frac{0.45}{1-0.45}\right)^{0.5} \bullet 2.3$$

$$I_{Cout} = 2.1A$$

The next step involves the calculation of the ripple voltage based on the chosen ceramic capacitor to determine the ripple present on the filter's first stage. This is used for two things, to check that the damping capacitor ripple current is within its specification and to determine the remainder of filter. With the input ripple amplitude and the output ripple specification, the required attenuation can be calculated. The inductor value can then be determined based on required attenuation. As a final step, the filter response needs to be simulated to check for unacceptable peaking and suitable attenuation which will be discussed in the following paragraphs.

IV. CONTROL

Closing the loop around the power stage is a three step process. The first step models the power stage, the second step adds isolation between the primary and the secondary, and the third step involves the overall loop compensation.

As discussed earlier, judicious choice of the primary inductance and the use of synchronous rectification can move the RHP zero of the control to a relatively high frequency. For instance, in this example, with a primary inductance of the power transformer of 6 mH, the lowest frequency of the RHP zero is around 10 kHz. To understand the loop analysis, a simple MathCad model of the power stage and modulator is used as shown in Fig. 5. For a more accurate model of the power stage and current control loop, refer to the Appendix 1. In the first step in this simplified modeling, the gain of the power stage or the current sense voltage to output current transfer characteristic is calculated by:

$$K \equiv \frac{Io}{Vsense} = \frac{(1-D)N}{Ri}$$

$$K = \frac{(1-0.45)\bullet 24}{2}$$

$$K = 7$$

The next step adds the frequency dependent components to the power train. The RHP zero is calculated per the earlier expression and it is added to the current source expression as shown in Fig. 5. Next the output filter and load are added to finalize the simplified power train model. Two filters are considered, a simple, high quality capacitor design as shown in Figure 5 and the more complex two stage filter approach of Fig. 4.

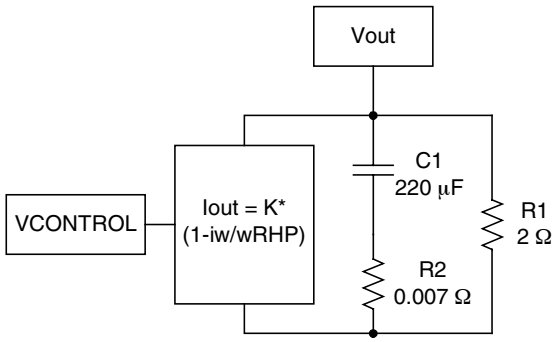

Fig. 5. Simplified power stage model.

Fig. 6 presents the results the results of the modeling efforts for a simple capacitive output filter. The output capacitor used is 220 µF with 7 milliohms of ESR and an output load resistance of 2 ohms. This particular combination of capacitance and very low ESR may be difficult to find and will likely be expensive to implement. The DC gain remains flat to around 300 Hz where the output capacitor begins to shunt the load resistance. This pole is easily calculated from the combination of load resistance and output capacitor. The next inflection point is a zero that is determined by the ESR of the output capacitor and its capacitance around 100 kHz. There is also a second zero around 24 kHz, but this is due to the RHPZ and results in increasing gain and decreasing phase. Closing the gain around this system could be simply done with an integrator with a zero at 300 Hz and a gain of approximately 10 dB at 8 kHz.

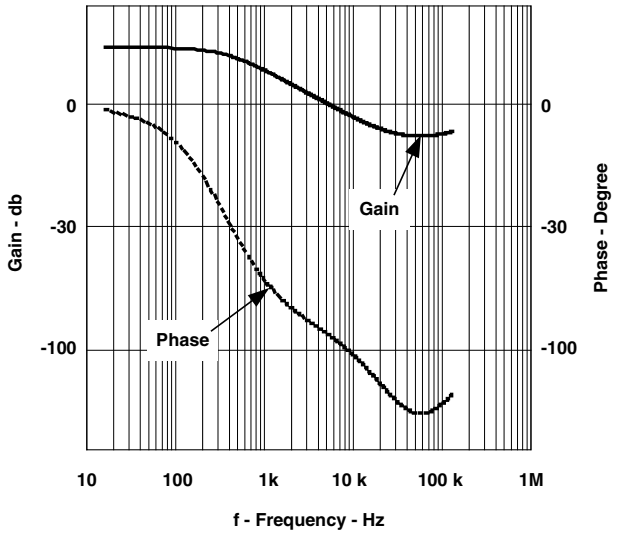

Fig. 6. Modulator/power stage gain with simple filter.

Fig. 7 presents the more complicated modulator/power stage Bode response of the two stage filter of Fig. 4. DC gain is equal to the previous example; however, the design will be much more of a challenge to cross at a similar frequency. The control characteristic has a pole determined by the load resistance and the sum of the two output capacitors or:

$$\text{Pole1} = \frac{1}{2 \bullet \pi \bullet R_{load} \bullet (C17 + C19)}$$

$$\text{Pole1} = \frac{1}{2 \bullet \pi \bullet 2 \bullet (470uF + 470uF)}$$

$$\text{Pole1} = 83$$

The gain falls until the impedance reaches the ESR zero of the electrolytic output capacitor at:

$$\text{Zero1} = \frac{1}{2 \bullet \pi \bullet C16 \bullet ESRC16}$$

$$\text{Zero1} = \frac{1}{2 \bullet \pi \bullet 470uF \bullet 0.3}$$

$$\text{Zero1} = 1.1x10^3$$

Above 10 kHz, two effects are evident, the first being the RHP zero previously discussed and the second caused by the resonance of the output inductor and the high quality ceramic capacitor. If the filter had no loss such as the electrolytic capacitor ESR, the magnitude of the peaking would make the design very bandwidth limited. However, by taking advantage of the inherent damping of the aluminum electrolytic, the amount of peaking can be controlled so a reasonable control bandwidth can be achieved. At high frequencies, we see a total of 270° of phase shift in the circuit; 90° from the ceramic capacitor, 90° from the L-R filter formed by the output inductor and the electrolytic capacitor ESR and 90° from the RHP zero.

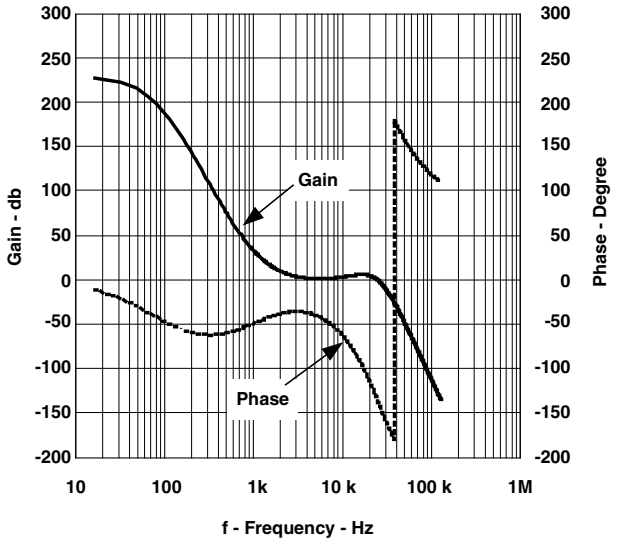

Fig. 7. Reduced cost two section filter uses inexpensive aluminum electrolytic and ceramic capacitors.

With the modulator/filter gain well in hand, the next step adds the error amplifier and isolating opto-coupler as shown in Fig. 8. This circuit uses a shunt regulator to compare the output voltage to a reference and to generate an error voltage. The difference between the error voltage and the output voltage generate a current in the opto-coupler that is used to set the peak current in the primary power switch. If the output voltage goes too high, the error amplifier output goes low to throttle back primary current.

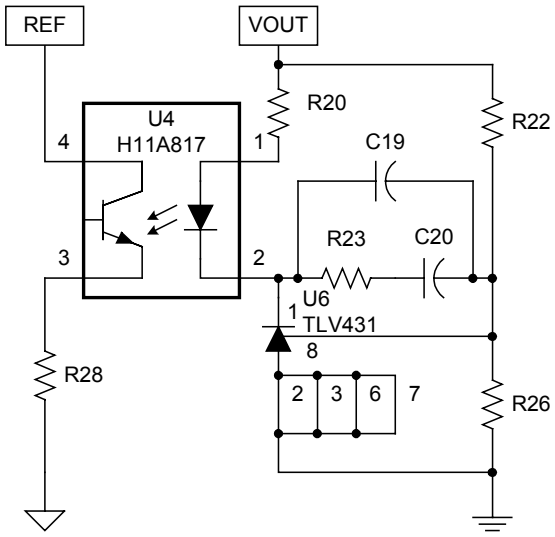

Fig. 8. This optocoupler connection yields a loop within a loop.

What is not very obvious in Fig. 8 is that there are two feedback paths, one through the error amplifier and another through the opto. If the output of the error amplifier were fixed and the output voltage went high, the current in the opto would build to throttle back the primary current just like the error amplifier loop. Therefore, the fixed error amplifier voltage acts as a reference to the inner control loop. This concept is shown in the simplified schematic of Fig. 9. So in reality, there are two loops to compensate: the opto inner loop and then the outer error amplifier loop; and one loop you don't compensate: the current loop.

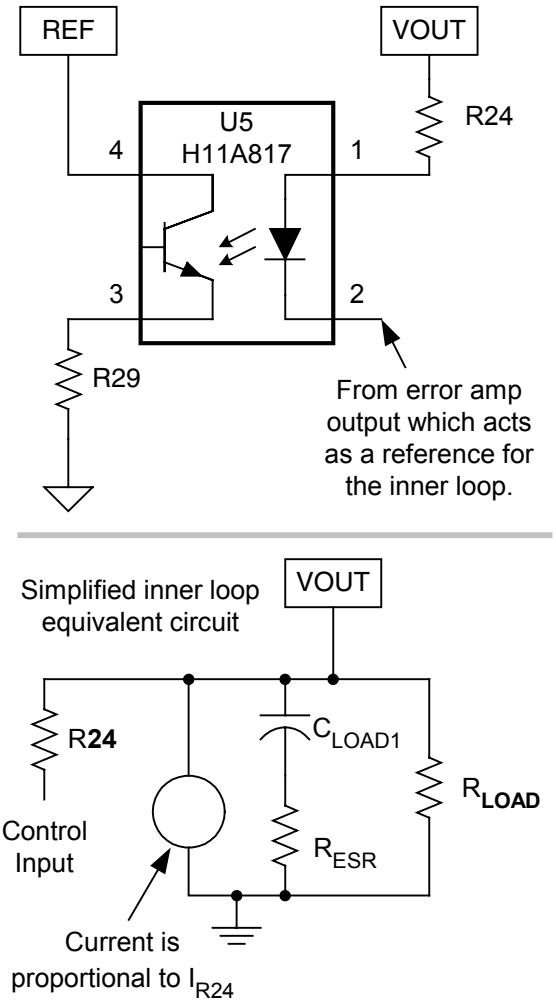

Fig. 9. In the first loop, opto current is set by the output minus a reference.

The strategy for compensating the inner loop is to provide some DC gain and then start rolling it off with a pole at 2000 Hz to provide ample phase and gain margin. For the sake of simplicity, the following assumes that there are no gain variations in the opto and that it has sufficient bandwidth to not enter into the gain expressions. The final circuit design should review these simplifying assumptions. Fig. 10 shows the total open loop gain from adding an opto gain of 1.3 to the modulator/power stage gain of Fig. 7. This inner loop will have a cross over frequency of 2 kHz with ample phase and gain margins. Component count is relatively low since adding a pole to the network just requires a capacitor in parallel with the output of the optocoupler.

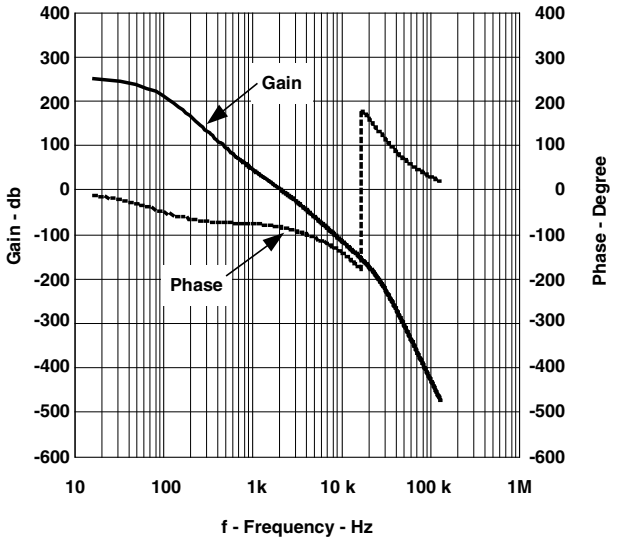

Fig. 10. Inner loop open loop gain.

The next step closes the outer error amplifier loop. First the closed loop response of the inner loop is calculated as shown in Fig. 11. At low frequencies the gain is about 1 as would be expected due to the large gain in the open loop response. At frequencies approaching the cross over, the gain begins to fall. Since the inner loop had good phase margin, no peaking is evident. As in the open loop, at the high frequencies, the control loop exhibits a minus one slope and 270° of phase shift due to the second order filter poles and the RHP zero.

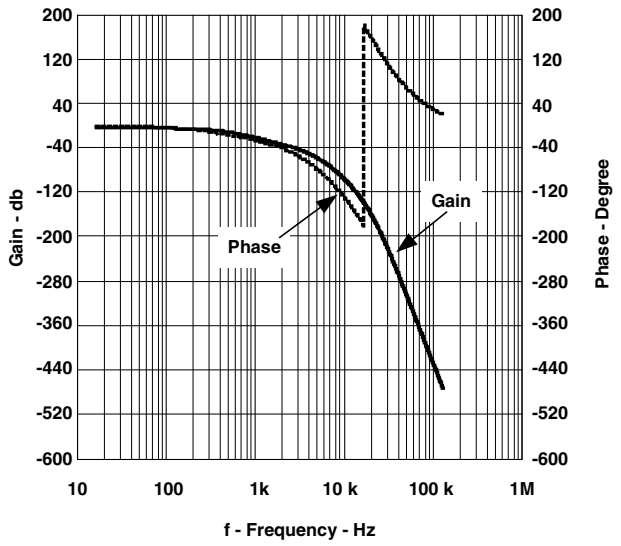

Fig. 11. Inner loop closed loop gain.

With the benign control characteristics of the inner loop, the outer loop compensation is straight forward. The strategy is to use an integrator with a zero at near the desired cross over frequency. Fig. 12 provides the overall loop response. Cross over frequency of the outer loop is around 3 kHz with about 45° of phase margin. Gain margin is about 8 dB. Overall, the result is good in that the design has closed the loop around a RHP zero and a two section filter with a good bandwidth and text book stability.

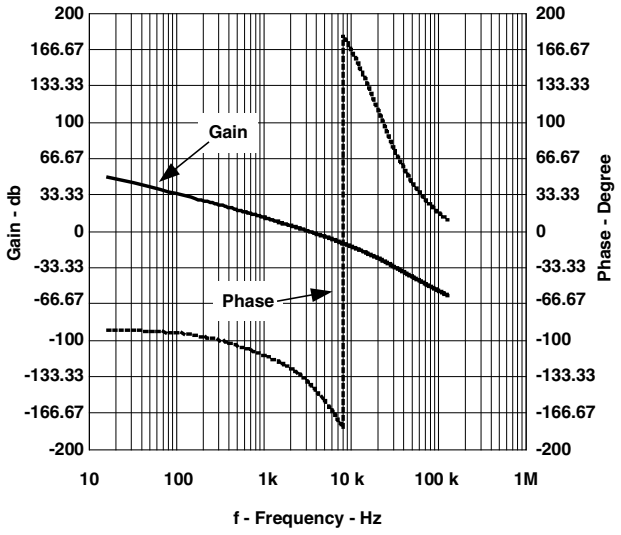

Fig. 12. Outer loop open loop gain shows good stability.

The proceeding analysis was accomplished using a mathematics tool rather than a circuit simulator such as P-Spice®. The circuit of Fig. 13 can be used to perform the same analysis. There are two main subcircuits: a very simple equivalent for the TLV431 shut regulator and a very simplified power stage. In the left block, a voltage controlled current source with a gain of 1 is used to simulate the gain of the ‘431. Since this model is to develop an AC analysis of the control functions, the references and dividers are neglected. These could be added as well as frequency characteristics of the ‘431 and opto. The voltage feedback around the ‘431 turns its output characteristics from a current source to a voltage source. This signal is used to drive a current controlled current source and resistor which simulate the opto, modulator and power stage. The inner loop is obvious from this simplified circuit in that the current in R1, which is the opto current, is set by the difference between the output of the error amplifier and the output of the power supply. More detail can be added to this simple circuit to add the second order effects. First, the gain block, F1, can be devolved into a current controlled current source that simulates the opto and a current controlled current source that simulates the modulator/ power stage. Doing so will allow the insertion of the pole in the control characteristics of the inner loop.

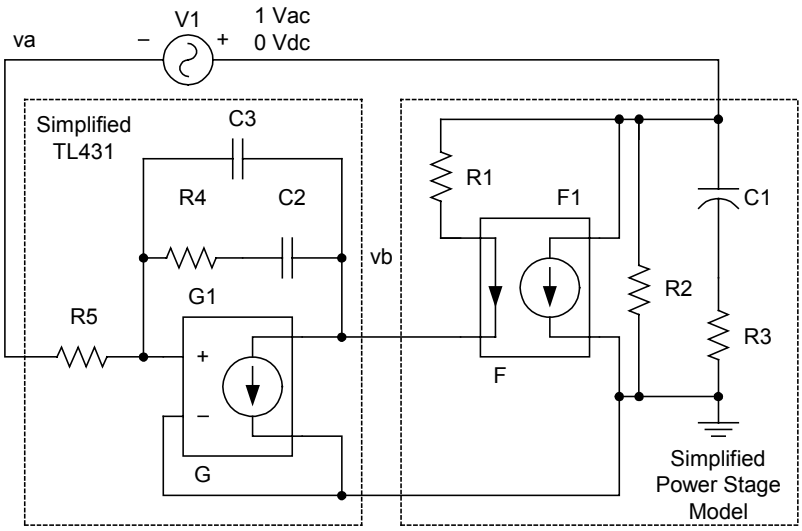

Fig.13. The second loop is formed with the TL431 driving the inner voltage loop.

While not a portion of the actual circuit, the AC source, V1, plays an important role in the simulation. It can be used to measure the loop response of the outer loop by injecting a signal and measuring the return signal. Loop gain and phase can then be readily calculated from the ratios of Vout to Va. A similar method can be used with the inner loop. The error amplifier can be replaced with a fixed voltage connected between Vb and ground. The injection source would be placed between Vout and R1. The inner loop gain can then be measured as Vout divided by the injected voltage (on R1 side of the injection source).

V. EXPERIMENTAL RESULTS

Fig. 14 presents the schematic of the converter. This schematic includes the power stage, feedback circuits, controller and startup circuits. The power stage is the continuous flyback discussed in detail in the preceding sections A UCC2809 controls the primary FET switch Q4 which drives power transformer T2. This control IC was chosen for its simple features and low cost. It does not have the error amplifier and reference that many control ICs have but do not need for isolated power supplies and eliminating these subcircuits provides a cost savings. The transformer includes windings for primary energy storage (10 to 9), primary bias (8 to 7), secondary output power (3 to 5) and secondary synchronous rectifier drive (2 to 3). Q1 acts as the rectifier in the transformer secondary and drives the two section output filter provided by C16, L1, and C17. Output regulation is achieved by comparing the reference within U6 to the output voltage and feeding it back to the primary controller through the optocoupler. Compensation of the inner loop is accomplished with the parallel combination of R19 and C22 who provide a pole around 5 kHz . The outer loop compensation` uses U6 as an operational amplifier with integrator response up until the zero introduced by the series combination of C20 and R22.

When power is first applied to the circuit comparator U3: A is used to provide an undervoltage function by holding down the softstart pin of the UCC2809 controller. Once sufficient voltage is present on the input, D14 forward biases and the comparator releases the soft start pin. Q3 is used to provide start up voltage for the control IC but is disabled once the converter is up and running. The bias developed from the bootstrap winding reverse biases the base emitter junction shutting off current flow from the input and thus saving power that would otherwise be wasted with bleeder resistors. A small transformer is provided to couple an optional sync signal from the secondary back to the primary circuit.

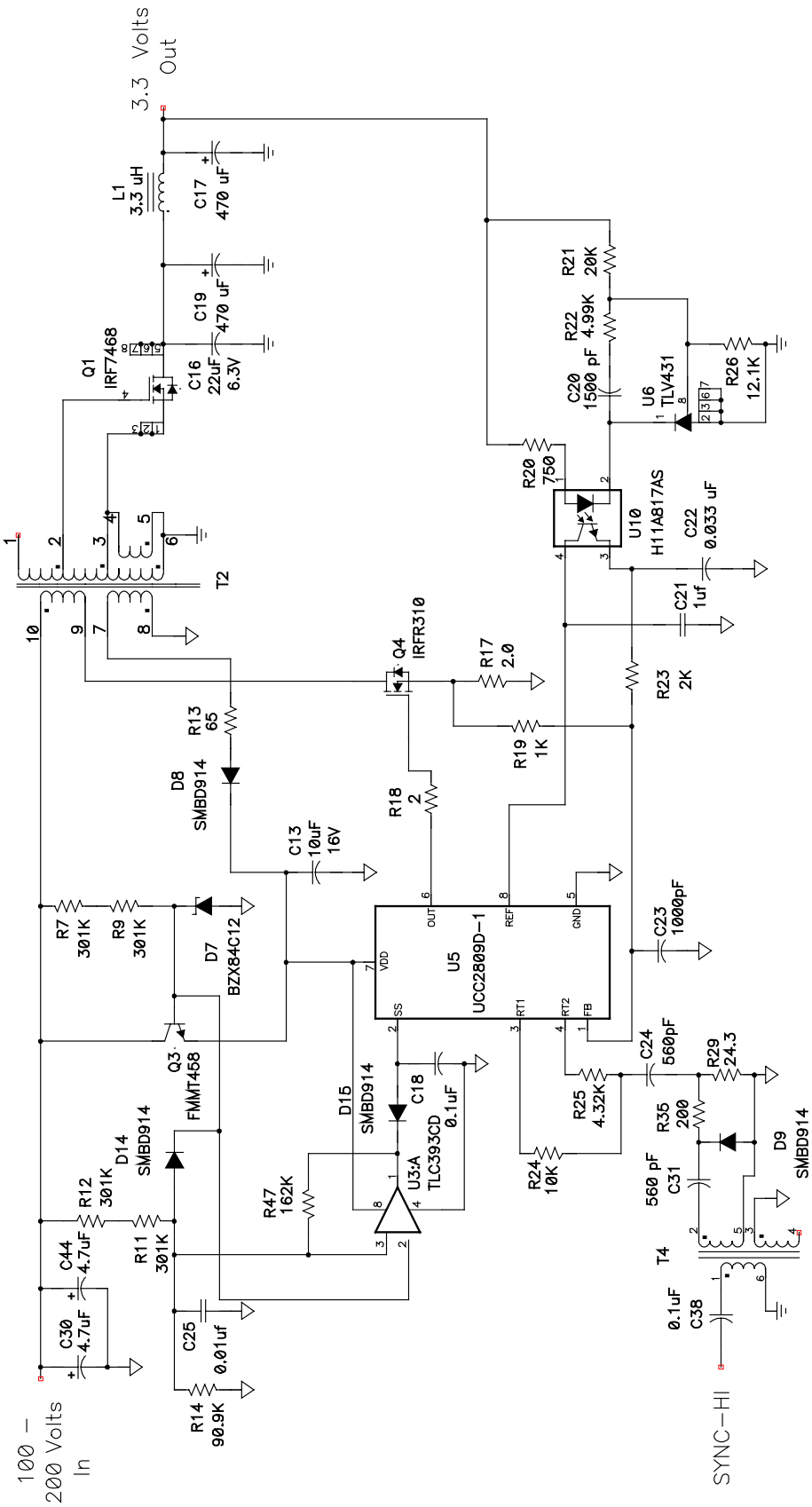

Fig. 14. Prototype converter uses a UCC2809 current mode controller.

Fig. 15 through 20 present some of the converter waveforms during full load operation at 100-V input. These waveforms provide good insight into the actual switching losses. Fig. 15 presents the primary switch drain to source voltage and source current waveforms. The voltage shows the continuous mode of operation with switching between the input voltage plus reflected load voltage to ground. The current waveform also demonstrates the continuous mode of operation with a significant current flow at turn on and a relatively sharp rate of rise of current during the on time. Also, a high current pulse is evident at device turn-on. This current has three parts; capacitive discharge of the power transformer plus board capacitance, gate drive current, and shoot through type losses from the synchronous rectifier. At these low power levels, the capacitive discharge term can be quite significant and resulted in a loss of several percent efficiency in one of the early prototypes of this supply. The excess capacitance was both in the power transformer and the multilayer PWB. A later design minimized the PWB capacitance by separating high voltage traces and minimizing the use of ground planes near these runs.

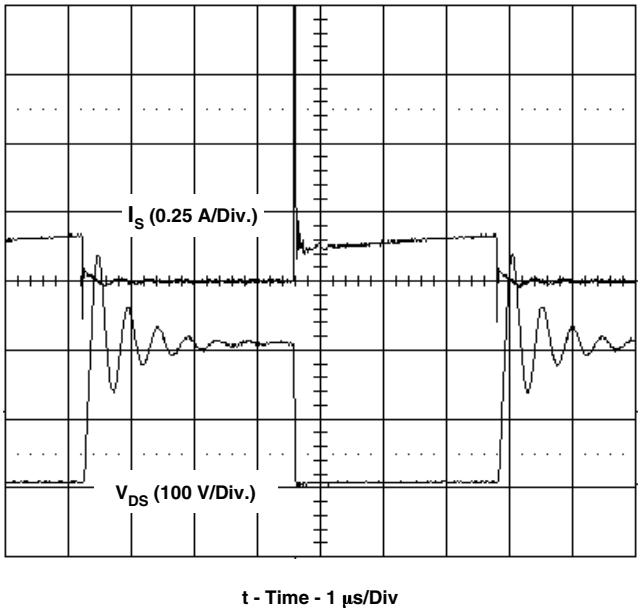

Fig. 15. Power switch current and voltage waveforms.

Fig. 16 shows the very rapid turn on of the power switch at 10 ns per division. The drain voltage is collapsed in 20 ns and the high current spike in the source has almost disappeared in the same time frame. Fig. 17 shows the primary FET source current with no drain voltage present. It accounts for nearly 25% of the high current leading edge spike. The remainder is split between the capacitance and rectifier losses.

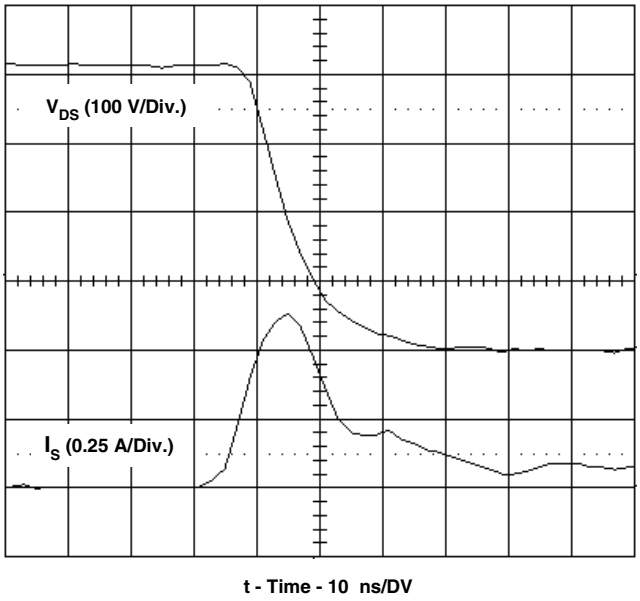

Fig. 16. Low switching losses as synchronous FET is turned off.

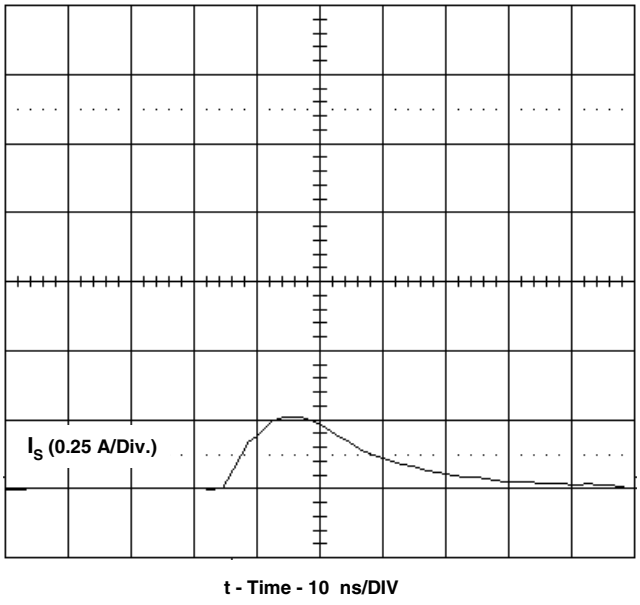

Fig. 17. Significant portion of source current is gate drive.

To further evaluate losses in the rectifier, secondary waveforms were measured. Fig. 18 presents the transformer output voltage during a switching period. The lower magnitude trace is the voltage that is rectified to provide the output power while the larger trace is the gate voltage to the secondary FET. Its gate-to-source voltage is simply the difference between the two traces. The output FET is enhanced with about 5 V of gate-to-source voltage during conduction and reversed biased with about 5 V of negative drive.

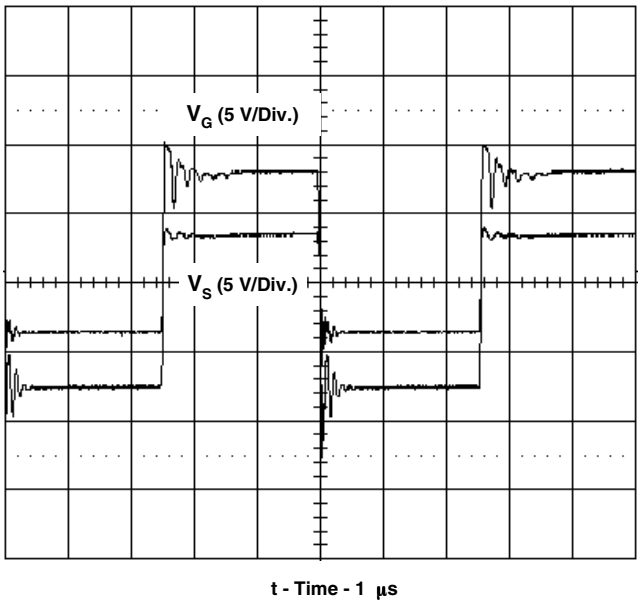

Fig. 18. Synchronous FET voltage waveforms.

Fig. 19 and 20 present expansions of the transformer voltage waveforms. Fig. 19 shows the turn off of the synchronous rectifier at 20 ns per division. Before the gate voltage reaches zero, the synchronous FET remains turned on and connects the 3.3-V transformer winding to the output voltage. When the primary FET turns on, the gate drive waveform collapses to zero volts in about 50 ns at which time the synchronous FET turns off. Then, the power winding on the transformer collapses and the voltage reverses. During the time when the synchronous is turning off, leakage inductance is the main limiter of current flow in the power transformer, however, based on the primary current waveforms, this is not a significant loss due to the short shoot through times and limited amount of current.

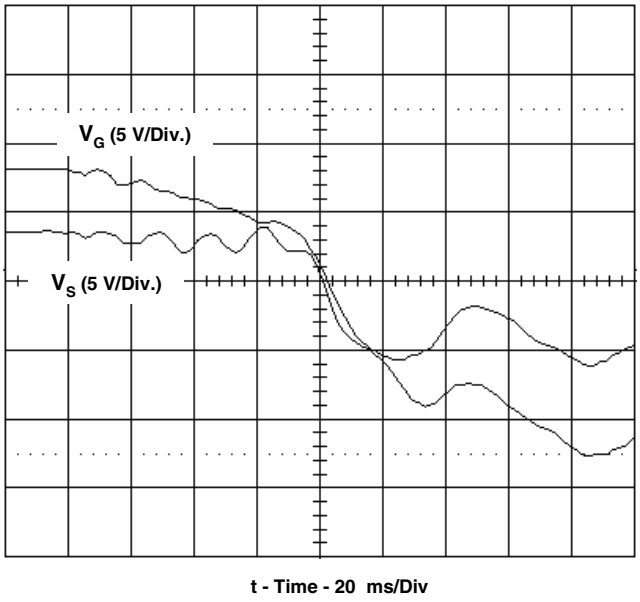

Fig. 19. Synchronous FET is turned off in 50 nanoseconds.

Fig. 20 shows the transformer waveforms at turn on. This is a much more docile edge. Gate and drain voltage rise gradually and turn on of the synchronous FET is accomplished smoothly. These traces do not show the high frequency content that occurs at turn off where the primary FET and synchronous rectifiers are trying to push currents in opposite directions.

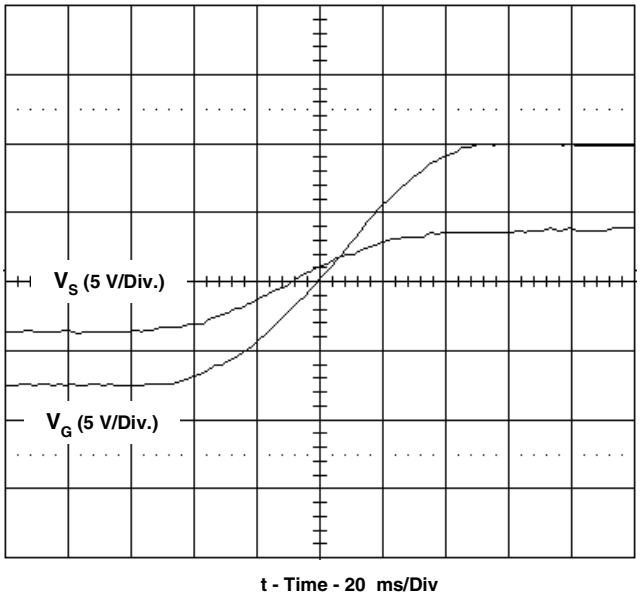

Fig. 20. The synchronous FET is turned on quickly and smoothly.

Fig. 21 presents efficiency of the converter versus output current and input voltage. At 100 input voltage, this 3.3 V, 7 watt output power supply reaches almost 90% efficiency and losses are dominated by losses associated with high currents. At the higher input voltages, efficiency is somewhat degraded due to switching losses from the active components as well as losses due to circuit parasitic capacitances. In this particular application, efficiency was critical at the low input voltages so the degradation at the higher voltages was acceptable. To gauge the effectiveness of the synchronous rectifier, a Schottky was substituted and it resulted in about a 4% efficiency loss.

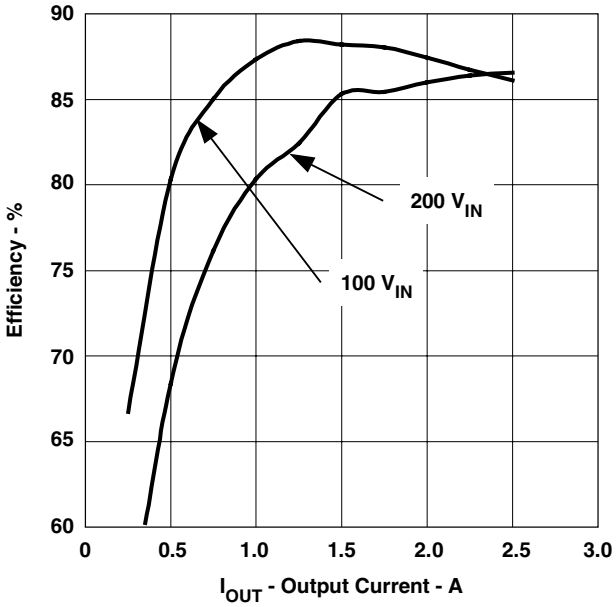

Fig. 21. Efficiency is high for this low power, offline design.

TABLE 4. LOSS BUDGET SUMMARY SHOWS GOOD CORRELATION WITH EFFICIENCY MEASUREMENTS

Loss Element	100 V Loss	200 V Loss
T2 Leakage	0.256	0.036
Q4 Turn On	0.166	0.199
T2 Capacitance	0.160	0.360
Q1 Conduction	0.136	0.101
Q4 Coss	0.053	0.097
Q4 Conduction	0.065	0.044
Q4 Turn Off	0.032	0.032
R17 Conduction	0.068	0.050
U5	0.024	0.024
T2 Core	0.020	0.030
Q1 Gate	0.018	0.018
C19 Conduction	0.014	0.025
T2 Conduction	0.014	0.009
R11,12	0.013	0.059
R7,9	0.013	0.059
Total	1.045	1.143
Measured Loss	0.943	1.074
Difference	0.108	0.069

Table 4 presents a detail accounting of the various losses within the power supply. With an output of just 6.6 watts of power, every milliwatt of loss is important in maximizing efficiency. 75% of the loss is in just 4 elements and they represent the key to further efficiency improvements. The transformer has the biggest effect on overall efficiency in two areas, the first is the losses as the leakage inductance is discharged each switching interval. The second is in its interwinding capacitance that is also discharged each switching interval. While the leakage inductance of the transformer was only 80 µH referred to the primary, this amount to 0.25 watts of dissipation. And with the capacitance of the transformer of 50 pF, this introduced about 0.16 watts of the total loss. Unfortunately, reducing one of these parasitic elements usually increases the other if the core size and primary inductance is maintainted. If cost were not an aspect in the design of the power supply, an increase in core size might allow a reduction in both of these loss elements. The other alternative is one that we eluded to earlier. The power supply can be run with even less

primary inductance on the transformer which can lead to both reduced leakage and reduced capacitance. The next element to address to improve the efficiency is the turn on loss of the primary FET. Since this is a self driven design, there is some turn-on losses caused by the secondary FET shorting the transformer. A better drive circuit could reduce this loss by turning the secondary FET off prior to primary turn on. This could be done with an additional drive transformer and delay circuits or could be accomplished with an adaptive circuit. The last significant loss element is the conduction loss of the secondary FET. This can be improved with a lower resistance part with additional cost. So with additional cost, this design can be pushed over 90% efficiency, however, the design was implemented with the lower cost components and circuitry due to high cost pressures.

Fig. 22 through 24 present various loop measurements and they show good correlation with the analysis presented. Fig. 22 is the open loop gain from the input of the opto to the output of the power supply open loop. To make this measurement, the opto was disconnected from the output and its anode was connected to a lab supply through a 750 ohm resistor while grounding the cathode. The opto was then driven with a signal source, and the transfer function from the opto to the output voltage was measured. Fig. 23 shows the closed loop response of the opto. It was made by connecting the opto through a 750 ohm resistor to the power supply output and then measuring the response from the opto input to the power supply output. Fig. 24 shows overall gain of the outer control loop. It was made by connecting the TLV431A and its compensation components to the opto input and then injecting an AC signal between the power supply output and the TLV431 circuit input. All measurements were made with a Venable Network Analysis System.

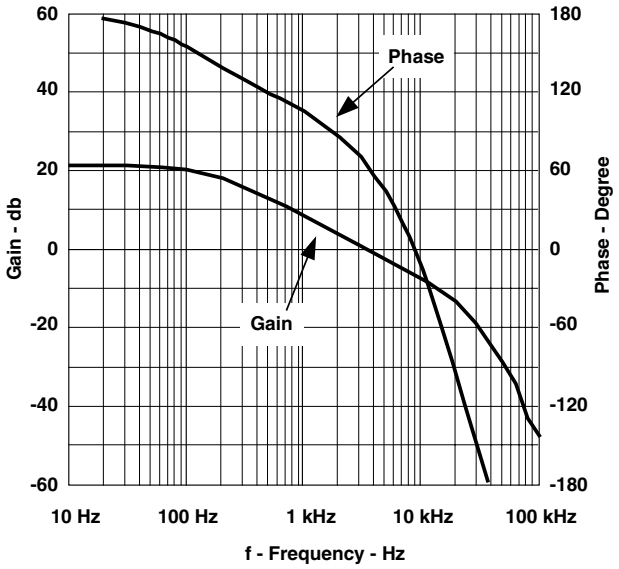

Fig. 22. Opto voltage to output voltage response (corresponds to Fig. 10).

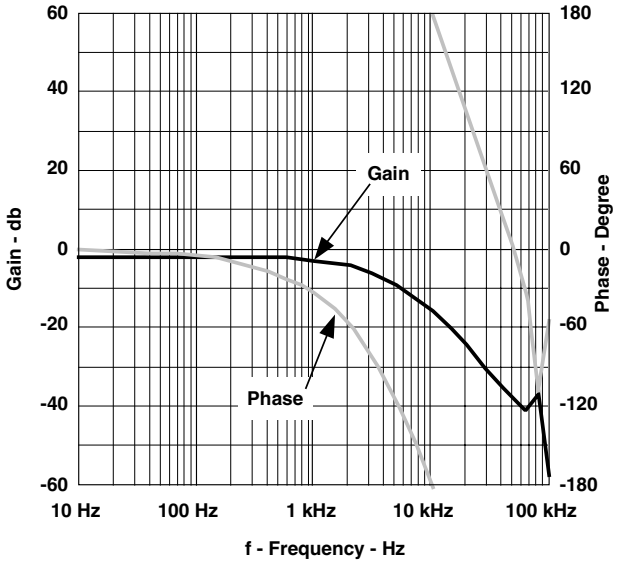

Fig. 23. Closed inner loop transfer (corresponds to Fig. 11).

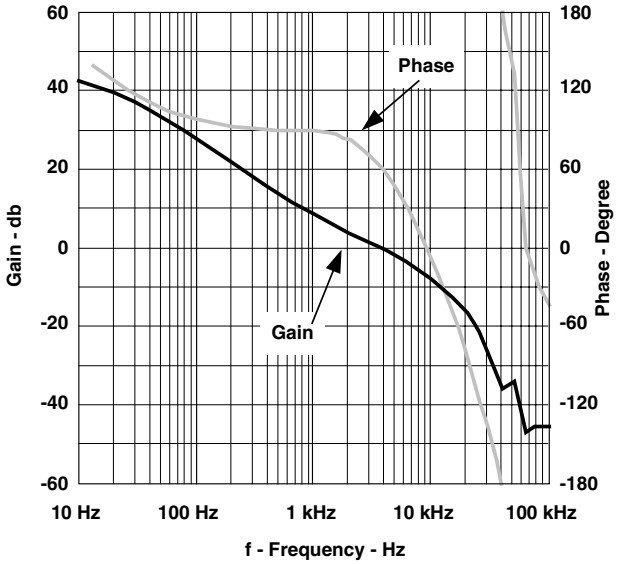

Fig. 24. Overall loop open loop response (corresponds to Fig. 12).

VI. SUMMARY

The design procedure for a low power continuous flyback converter with synchronous rectifiers has been presented. The design was based on the requirements of low cost and high efficiency as required by line powered DSL and cable modem customer premise equipment. Circuit stress calculations and magnetic requirements definitions have been outlined. Control loop analysis of a nested loop and a two section filter has been presented. Finally, all calculations have been verified with lab results from a prototype converter.

VII. REFERENCES

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[5] Ridley, Ray; *A New Small-Signal Model For Current Mode Control*, Ph. D. Dissertation, Virginia Polytechnic Institute and State University, Blacksburg, VA, November 1990.

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APPENDIX. DERIVATION OF CURRENT LOOP CONTROL CHARACTERISTICS

The flyback converter can be modeled as a buck boost converter when the primary circuit is reflected to the secondary side as shown in Fig. 1. To do so requires reflecting input voltage and transformer magnetizing inductance through the transformer turns ratio.

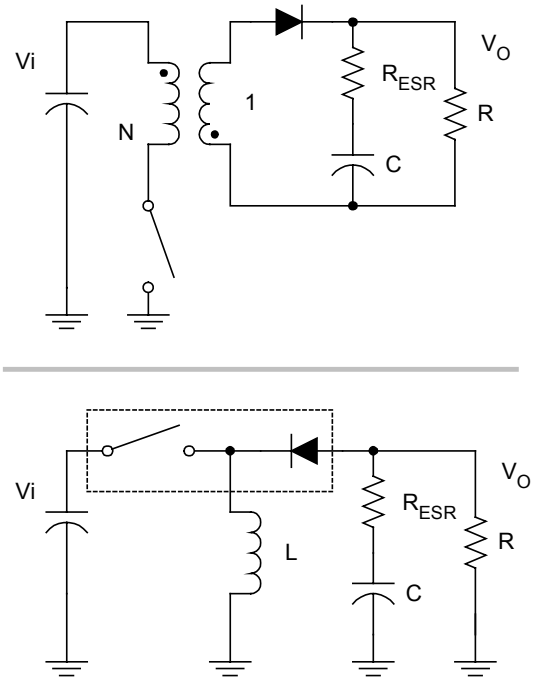

Fig. 1. The flyback can be simplified to a buck-boost converter for analysis.

The next step in the process is to add the simplified average PWM switch model developed by Vorperian and the model extension to current mode developed by Ridley Engineering. Fig. 2 shows the small signal equivalent circuit for the current mode controlled flyback converter. This figure shows the power stage, as well as the gain blocks for the current loop within the power stage. Fm, the modulator gain, is calculated as:

$$Fm = \frac{1}{\left(\frac{V_{in}}{L} \bullet F_s + ExtRamp\right)}$$

where Fs is the switching frequency and ExtRamp is the value of externally added ramp. He(s) models the instability of the current loop as the duty factor approaches 50%. Ridley Engineering has numerous references on the He(s) term, if a person wants to include the complexity of this term in their analysis. Finally, Ri models the conversion of the inductor current to a sense voltage.

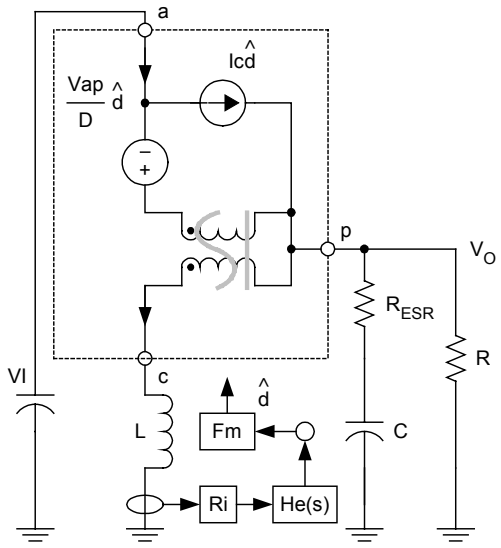

Fig. 2. Vorperian buck-boost equivalent model.

Using the small signal model of Fig. 2, the open loop control to output transfer can be derived to be the following. This is the transfer function that would characterize voltage mode control. The transfer function shows an ESR zero (ωz1), a right half plane zero (ωz2), and double pole at ωo.

$$Gv(s) = \frac{\hat{v}o(s)}{\hat{d}(s)} = Kv\frac{\left(1+\frac{s}{\omega z1}\right)\left(1-\frac{s}{\omega z2}\right)}{1+\frac{s}{\omega oQ}+\frac{s^2}{\omega o^2}} \quad \omega z1 = \frac{1}{R_{esr}C}$$

$$\omega z2 = \frac{R(1-D)^2}{DL}$$

$$Kv \approx \frac{Vi}{(1-D)^2}$$

$$\omega o \approx \frac{1-D}{\sqrt{LC}}$$

$$Q \approx \frac{(1-D)R}{\sqrt{L/C}}$$

Also, using the small signal model of Fig. 2, the open loop control to inductor current transfer function is derived to be the following. This transfer function is needed to complete the control to output transfer function for current mode control.

$$Gi(s) = \frac{\hat{i}\ell(s)}{\hat{d}(s)} = Ki\frac{\left(1+\frac{s}{\omega p}\right)}{1+\frac{s}{\omega oQ}+\frac{s^2}{\omega o^2}}$$

$$\omega p \approx \frac{1+D}{RC}$$

$$Ki \approx \frac{Vo(1+D)}{RD(1-D)^2}$$

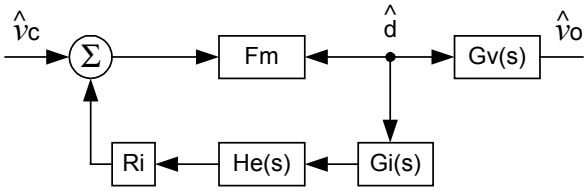

Fig. 3. Control loop block diagram showing current loop.

With these two gain blocks calculated, one can use the block diagram of Fig. 3 to calculate or simulate the gain from the control to output voltage transfer function. The solution with the current loop closed is:

$$\frac{\hat{V}o}{\hat{V}c} = \frac{FmGV(s)}{1+FmGI(s)RiHe(s)}$$

From the transfer function expression, it can be observed that when the current loop has large gain, the double poles of the open loop control to output transfer function, Gv(s), and the open loop control to inductor current transfer function, Gi(s), almost cancel and results in the following approximate transfer function.

$$T(s) \approx \frac{\hat{V}o}{\hat{V}c} \approx K\frac{\left(1+\frac{s}{\omega z1}\right)\left(1-\frac{s}{\omega z2}\right)}{1+\frac{s}{\omega p}}$$

By making the assumption that current loop has high gain at DC, K can be simply calculated as:

$$K \approx \frac{ViR}{(Vi+2Vo)Ri}$$

Note that in practice the current sense resistor will need to be reflected back through the transformer turns ratio.

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