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A New Strategy for Detection and Management of Faults in High Power NPC Converter Systems

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Abstract **Neutral Point Clamped (NPC) converter is often used in high power medium voltage industrial applications. This paper proposes a new fault detection and management method for NPC converters, able to detect any type of power semiconductor device fault and to allow the continuity of operation in case of fault. The fault detection, which is very fast, is based on the measurements of load and clamp-diode legs currents. The fault management strategy is suitable for NPC inverters feeding both passive and active load (such as a three-phase asynchronous motor) supplied by Active Front End (AFE) or Diode Front End (DFE). Finally, a comparison among three different reconfiguring modulations, with special regard to the evaluation of harmonic distortion of the line-to-line voltages and phase currents, is suggested.**

Keywords**: Fault tolerance, NPC converter, multilevel converter, space vector modulation (SVM).**

I. INTRODUCTION

In recent years, the multilevel converters [1]-[7] diffusion in high power medium voltage industrial plants is growing fast; they constitute an excellent solution that allows to overcome significant troubles in power electronics converters, such as operating at voltages higher than the blocking voltage of the existing power semiconductor devices and the need to reduce the size of filter elements, which are required when dv/dt of the output waveforms is very high.

Other significant advantages deriving from multilevel voltage source conversion systems are in lower harmonic distortion of voltage waveforms generated and in reduced common mode voltages, if compared with the voltages that can be obtained by using conventional two-level converters.

The achievement of a high number of generated voltage levels implies an increasing of the number of static semiconductor devices in the converter system, which results in a higher fault probability with a consequent reliability reduction. The reduction in converter reliability implies, in absence of a suitable counteraction, a higher probability of the industrial or transport application stop, which may cause, in almost the totality of the cases, very high economic losses. The continuation of operation, although at a lower performance, is of course better than the complete stop of the whole plant. Two main strategies can be adopted to improve the reliability of multilevel converters. One is the reduction of the electrical stress applied to the passive component of the converter, that is, the capacitor cell. This was done by injecting a suitable second harmonic circulating current in [8]-[11], with no reduction of the converter efficiency. The second strategy is to make the converter fault-tolerant, i.e. capable of operating after a loss of a semiconductor device due to a fault. In recent years, in response to the market request for continuous service, a research effort towards the realization of fault-tolerant multilevel conversion structures has been made [12]-[20].

One of the most widespread multilevel conversion architectures is the Neutral Point Clamped (NPC) converter structure [1]; this is the first topology that has been considered for a real development, and nowadays represents a milestone in some important high power applications. The main drawback of NPC converters, when target is fault tolerance ability, is the great energy stored in the dc-link capacitors that can create dangerous short-circuit currents in case of fault [13].

In this paper, a new strategy is proposed to identify any power semiconductor fault type and to manage the fault transition into a reconfigured operating way that guarantees the fault tolerance with both passive and active load (such as three-phase asynchronous motor), without significantly increasing the cost of the converter. The proposed method allows detecting any kind of power semiconductor device fault in the shortest possible time, in order to manage a suitable reconfiguration of the converter control system and to guarantee, even if at a reduced voltage level, the continuity of operations.

Until now, power electronics researchers have shown that NPC converters can be fault tolerant only if many additional components are used or if the power semiconductor devices are oversized [21], [22], while the already installed converter systems are usually equipped only with overvoltage and overcurrent protections [13]. In the technical literature, the most important contributions are related to NPC converters equipped with additional devices and/or controlled with strategies that make possible the service continuation once the fault is detected and extinguished: the only papers found, related to fault detection strategies deal with open-circuit fault detection are [23]-[26]. Among them, an often used open-circuit fault detection method relies on the analysis of the current distortion typical of that operating condition [25],[26]. However, as explained in [27], with these techniques it is

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difficult to identify precisely which switch has failed in case of grid-connected operation of the converter. Moreover, finding papers regarding the converter fault tolerance with passive load is quite simple [21]-[23], while it seems not so easy discovering papers that refer to the converter fault tolerance in motor drives applications.

In this work, new strategies are proposed, which permits to achieve the fault tolerance of the whole system with both passive and active load, without over-sizing the semiconductors. The proposed reconfiguration strategy is different in case of external or internal switch fault, and depends also on the fault type (open-circuit or short-circuit fault).

II. Power Semiconductor Faults in NPC Converters

A. Fault Types

The power semiconductor devices that make up the NPC converter in medium-voltage high-power applications are usually the Insulated Gate Bipolar Transistors (IGBT), the Integrated Gate Commutated Thyristors (IGCT) and the Injection Enhancement Gate Transistors (IEGT).

These devices can be built using the press-pack technology, which represents a key aspect for the evaluation of failure behavior.

The cases of switch failures considered for the NPC converter, are:

- Short-circuit (SC) fault, if the switch remains in the "on-state";
- Open circuit (OC) fault, if the switch remains in the "off-state".

When a SC fault occurs, a press-pack device remains in short circuit for an undefined time, with the possibility to consider the switch as an "ideal" short circuit that guarantees the current flowing in both directions. This condition, named "short circuit failure mode", has been verified through power semiconductor manufacturers tests and is reported in [28], [29]. The NPC converter structure, which is represented in Fig. 1, is most stressed when a SC fault occurs: the simultaneous on-state of three consecutive switches causes a short circuit of a semi dc-link capacitor, and a great overcurrent in the converter is generated [13, 30].

Instead, the OC fault creates several problems to the reconfiguration strategy, after the fault transition: the available Voltage Space Vectors are not so many and guaranteeing a satisfactory output voltage is not easy, as shown in [30].

III. Fault Detection Method

In order to identify each type of failure, two sensors for each leg of the inverter have been inserted, as shown in Fig. 2 and analyzed in [30]. Thus, detecting any type of fault (SC and OC) of any switch and managing the transition becomes possible.

Placing six Rogowski coils, one for each clamp-diode leg, as shown in Fig. 2, in addition to the three current sensors that usually equip the converters, to detect any kind of fault is possible. In the following, with reference to Fig. 1, Sx1 and Sx4 are defined "external switches", while Sx2 and Sx3 are defined "internal switches", where x = a, b, c is the leg index.

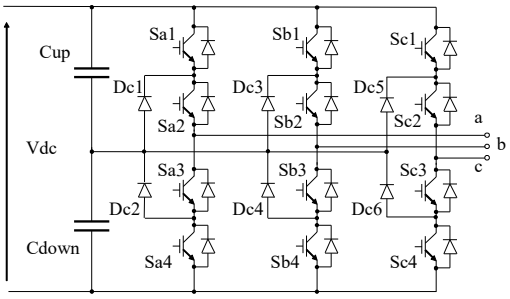

Fig. 1. Neutral Point Clamped architecture.

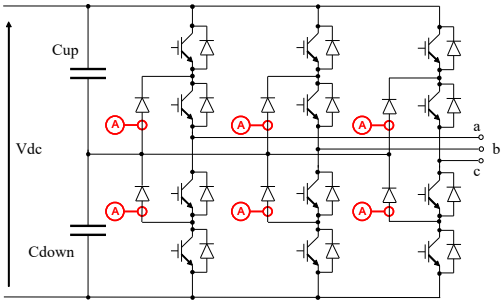

Fig. 2. Additional current sensors disposition for faults detection.

1) Short-circuit fault detection

The SC fault in NPC converter, as already explained, leads to the upper or lower capacitor short-circuit, as shown in [13]; this short-circuit happens when a row of three consecutive switches (of the same inverter branch) are in on-state at the same time: this situation is possible with Sx1, Sx2 and Sx3 or Sx2, Sx3 and Sx4 switched on at the same time.

The external switch SC fault is detected by comparing the clamp diode current to the related phase load current when the branch is in the state 0 (Sx2 and Sx3 ON), (Fig. 3).

The internal SC fault (Sx2 or Sx3) is identified by comparing the clamp diode current to zero during the branch state P (Sx1 and Sx2 ON) or state N (Sx3 and Sx4 ON). Both cases have been better described in [32].

2) Open-circuit fault detection

The OC fault does not generate any overcurrent in the NPC, and then, waiting for one or two load current electrical cycles, in order to identify the faulty switch, is possible. Fault detection is based on a principle very similar to the SC one, as better described in [32]. The identification of a Sa1 OC fault is shown for example in Fig. 4.

IV. Fault Transition Management

In this section two different strategies, which allow managing any kind of fault, are proposed:

A. The first strategy can be implemented without using additional components in the converter and, at this time, is practicable only in case of passive load;

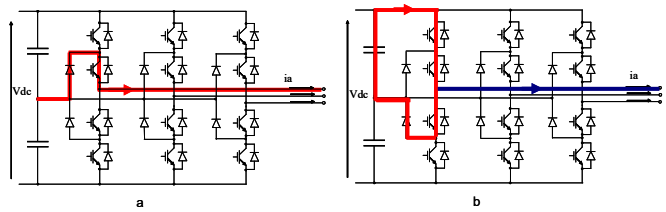

Fig. 3. Phase "a" load current path (0-state) in healthy configuration (a) and Sa1 short circuit fault (b) when ia is positive.

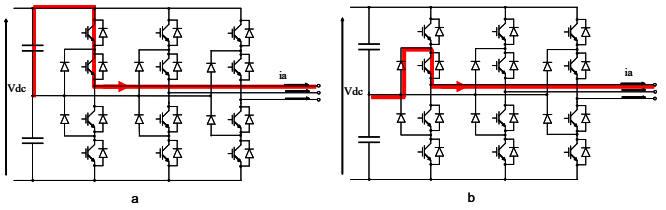

Fig. 4. Phase "a" load current path (P-state) in healthy configuration (a) and Sa1 OC fault (b) when ia is positive.

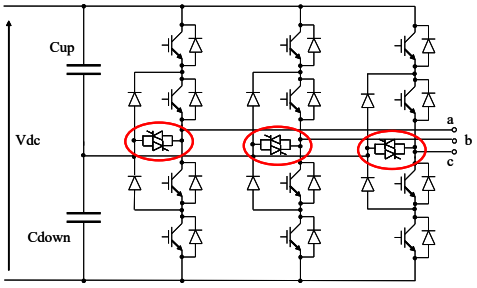

Fig. 5. NPC architecture with BCT.

B. Another strategy, based on the addition of a Bidirectional Controlled Thyristor (BCT) or, alternatively, of a pairs of Silicon Controlled Thyristors (SCR) in each leg, as shown in Fig. 5, is proposed [31, 32]: this strategy is practicable with all types of load but is recommended, and at this time compulsory, to guarantee the fault tolerance when the NPC converter feeds an active load (e.g., asynchronous motor). The use of bi-directional switches has been generalized for use with *any-level* NPC inverters in [33].

Another essential distinction, in order to better define the fault transition strategy, has to be made between drives supplied with AFE converters, with the possibility of feeding back the energy into the grid, and drives fed by DFE converters, which do not permit bidirectional power flows. The unidirectional case presents more criticality than the bidirectional one, but managing dangerous fault transitions through the proposed solution is possible in both cases (especially in case of SC fault), avoiding high overcurrent flowing in the NPC converter.

A. Simulation Environment

The simulations results that will be presented in the next sections are based on a Matlab/SIMULINK environment and PLECS circuital simulator [34-35]. The main data of the induction motor used during the research activity are reported in Table I. The load torque is applied proportionally to the square of the speed, so as to obtain the nominal torque at rated speed. A NPC inverter with a nominal power equal to 5 MVA has been implemented, equipped with IEGTs Toshiba ST2100GXH24A and EUPEC D1331 SH freewheeling diodes, switching at a frequency equal to 1 kHz, and with a dc-link nominal voltage of 5200 V. The ABB 5STB 25U5200 BCTs have been selected to implement the proposed strategies.

TABLE I
MOTOR DATA

Symbol	Quantity	Value
P_n	Nominal power	5 MW
V	Nominal voltage (rms)	3000 V
T	Nominal torque	70 kN·m
ω	Nominal speed	750 rpm
$2p$	Numbers of poles	8
J	Moment of inertia	500 kg·m^2
R_s	Stator resistance	13.7 mΩ
L_s	Stator inductance	0.51 mH
$cos\varphi$	Power factor	0.87
η	Nominal efficiency	0.96

Supply stage has been modeled with a three phase generator with a three-winding, three-phase transformer: in case of DFE there is a couple of three-phase diode rectifiers, while in the case bidirectional power flow an AFE converter identical to NPC inverter is utilized on the line-side. Control strategy is implemented in ANSI C code through S-Function [36].

B. Short-Circuit fault transition

The principal goal of the transition phase (from pre-fault to reconfigured system) is avoiding dangerous switch overvoltages and further overcurrents inside the converter.

With reference to the "a" branch, if during a commutation between commanded states 0 and P the Sa1 SC fault is detected, the short-circuit condition is removable by turning off Sa3, forcing the "a" leg to state P. Owing to the need of avoiding the overvoltage on Sa2, imposing the state N would not be possible: indeed, if the related load current was positive, it would flow into freewheeling diodes 3 and 4, as depicted in Fig. 6, and then Sa2 would block the full dc-link voltage. In the case that a passive load is supplied, a fault transition management approach without using additional devices is proposed, which is aimed to maintain the converter operations, even if at a reduced performance: the overall dc-link voltage can be halved, in order to avoid the voltage oversizing of power semiconductor devices, using for instance a NPC AFE rectifier suitably designed, which is a stage that often feeds the NPC inverters dc-link [36, 37].

If no additional components are used and only with passive load, the transition in case of external switch in SC fault can

be managed by maintaining the P state in all the three legs if the faulty switch is Sa1, while with Sa4 SC fault the transition can be managed by maintaining N state; after dc-link voltage transient, fault tolerance is guaranteed by properly modifying the modulation strategy, as it will be shown in the next section.

The internal switch SC fault can be extinguished using the external component involved in the mesh failure. In presence of faulty switch Sa2, the healthy configuration is reached by turning off Sa4; in case of Sa3 fault, Sa1 must be turned off. In this case it is simple to clamp the faulty leg to the 0 state by forcing the healthy internal switch to be ON and then to implement a reconfiguration strategy is possible also without changing the dc-link voltage value, as shown in [31] and [32].

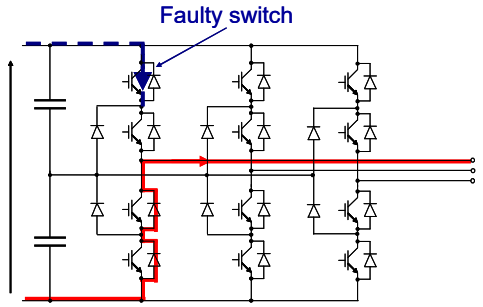

Fig. 6. Voltage stress on Sa2 with Sa1 on SC fault and "a" leg on state N.

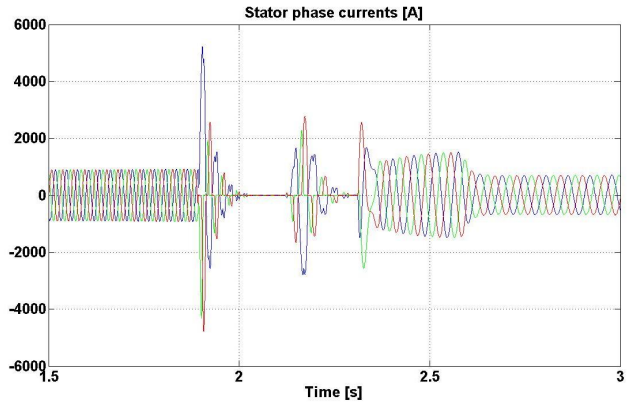

Fig. 7. External switch SC: current transient with AFE converter and FOC.

If the system feeds an active load (e.g., ac motor), managing the transition into a reconfigured state is possible only by equipping the converter with three BCTs (Bidirectional Controlled Thyristors) [31], as shown in Fig. 5 and as discussed in details by the authors in [32].

The transition, in case of an external switch in SC fault, is performed by connecting, during fault transition, the faulty branch at neutral point through the BCTs and maintaining all switches of healthy branches in the OFF state. This way it is possible to extinguish the transient motor currents, and to reconfigure the system when the voltages and currents reach values that are sustainable by the converter.

The use of an AFE converter as rectifier stage and the implementation of a suitable drive control strategy, such as Field Oriented Control (FOC), permit to obtain a smooth current transient, and to guarantee good voltage and current profiles during the fault management and the subsequent drive reconfiguration. A traditional FOC scheme has been used for this test, whose structure is described in [38]. Fig. 7 shows the stator current profile in the best solution proposed in [32]. Fig. 8 shows the motor speed and dc-link voltages behaviors (V_{DCup} and V_{DCdown}) during the three subsequent stages, fault extinction, dc-link voltage halving and motor restart through field oriented control system. Note that, in order to keep a voltage level sustainable by the converter in reconfigured operation, the dc-link voltage has to be reduced to half of its previous value by the AFE control system. As the currents are extinguished during the transition, the torque is equal to zero and the rotor decelerates with inertial trend.

C. Open-Circuit fault transition

The OC fault causes less problems to the converter than short-circuit (SC) fault. In OC fault case no overcurrents appear; in the worst instance an overvoltage condition may occur, but featuring a very slow dynamics, if compared to short-circuit overcurrents dynamics. In case of OC fault, if it is not possible to transform an open-circuit fault into a short-circuit fault, as shown in [14], the transition into the reconfigured strategy is made opening all the switches of the faulty leg. Exactly in the same way as in the SC event, in the case of OC faults there are two possible occurrences, external switch or internal switch in OC fault.

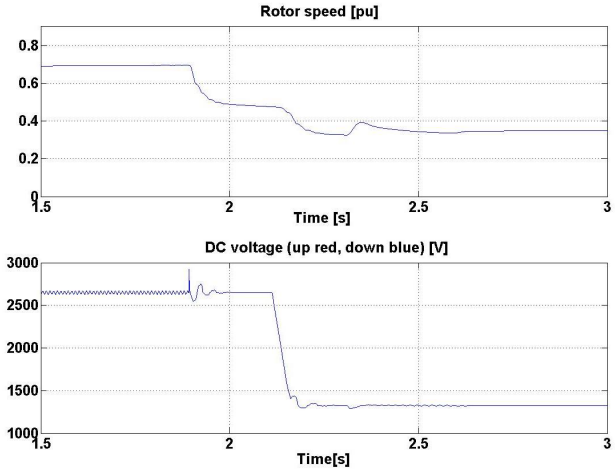

Fig. 8. Speed and dc-link voltage transient with AFE converter and FOC.

The external switch OC fault transition, e.g., Sx1 or Sx4 (where x = a, b, c is leg index), is managed by turning on the two internal switches of faulty leg, Sx2 and Sx3 (that is equivalent to turning on the related BCTs), and then proceeding with the modified modulation strategy in the two healthy legs, as will be explained in the next section: this solution would be feasible without additional components in converter architecture. Instead, the internal switch OC fault is handled by connecting the faulty leg to the Neutral Point (NP) through the related BCT turn-on: even in this case, adopting the "two-phase" modulation strategy shown in [31] and [32] is possible. Figs. 9 and 10 show the behavior of some

quantities during a Sx3 OC fault when the converter supplies an active load. The motor phase currents transient, which is shown in Fig. 9, proves the absence of overcurrents during the OC fault management. This simulations have been performed with an open-loop controlled motor, therefore a higher speed reduction can be appreciated in Fig. 10, with respect to the case represented in Fig. 8 that refers to a motor controlled with a FOC strategy. In order to supply again the motor after the transition, the complete rotor demagnetization is mandatory.

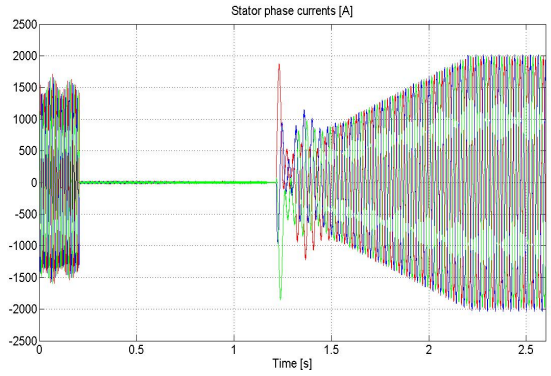

Fig. 9. Current transient with DFE converter in case of Sx3 in OC fault.

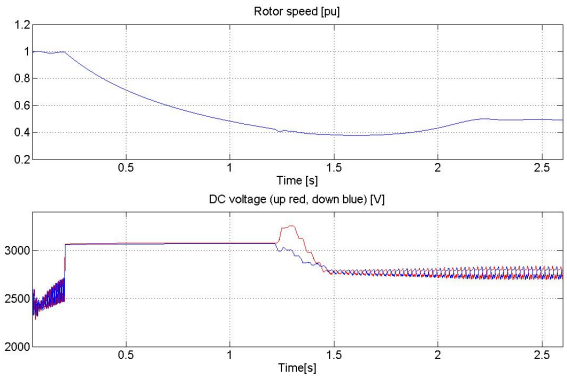

Fig. 10. Speed and dc-link voltage transient with DFE converter in case of Sx3 in OC fault.

The better solution is achievable with a closed-loop strategy like FOC that permits to reactivate the whole regulation system a few ms after the fault detection. The proposed approach is explained in greater details in [30], where all kinds of transitions and reconfiguration strategies derived considering any fault type are described, in both cases of passive and active load connected to the AC side of the NPC inverter.

V. Reconfiguration Methods

After the fault transition, if connecting the faulty leg to the Neutral Point is possible, it is simple to recreate a three-phase line-to-line voltage by imposing to the healthy legs a couple of reference signals presenting a phase displacement of 60°, as shown in [31]. With this strategy the NPC output line-to-line voltage has a reduction of $1/\sqrt{3}$, if compared to the maximum value reachable on healthy configuration. This solution is feasible in each fault case (both OC and SC) when NPC converter is equipped with BCTs.

Conversely, in case of converter without additional components, the reconfiguration strategies are different depending on the fault case: it is possible to clamp the faulty branch at NP, as stated above, in case of Sa2 or Sa3 in SC fault and also when an OC fault in Sa1 or Sa4 occurs. In presence of an internal switch OC fault, it is possible to turning off all the switches of faulty leg, and to modulate the remaining two legs. Instead, in case of external switch SC fault (and inverter without additional components) it is necessary to halve dc-link voltage in order to guarantee fault tolerance and a suitable reconfiguration: this way the output voltage (and, as a consequence, the output power) has a reduction of 50% referring to the pre-fault condition.

In this case the reconfiguration is different from all already explained solutions, because it is not possible to clamp the faulty leg at NP (in this case a semi dc-link short circuit would appear): the impossibility to impose state 0 implies that the faulty leg has only the states P and N available, once dc-link voltage is halved. The simplest way to reconfigure the converter is a 2-level modulation where, on each NPC branch, the upper switches and the lower ones are powered together; however, this strategy has many disadvantages in term of output voltage quality and stress on the power semiconductor devices during commutations: for these reasons two different modulation strategies are proposed, in order to improve the harmonic content of output voltage.

The proposed strategies, that are implementable without additional components, are feasible only if the drive is equipped with a four-quadrant converter (AFE and inverter) that allows the DC-Link voltage halving: this aspect is fundamental, as already explained, in order to avoid the oversizing of each power semiconductor switch.

The first proposed strategy is a modified Sine Pulse Width Modulation (SPWM), defined as “hybrid PWM”, in which the faulty leg (with an external switch in SC fault) is 2-level modulated, with only state P and N available, and the remaining two legs are 3-level modulated (Fig. 11). The “hybrid PWM” uses a third harmonic injection, as shown in Fig. 11, in order to allow a maximum modulation index value equal to the one reachable with the classic Space Vector Modulation (SVM). In Fig. 12 related phase and line-to-line voltage waveforms can be observed. Load voltages compensation strategies have been also developed, in order to attenuate the effects of the greater dc-link voltages fluctuations due to the reconfigured modulation strategy. It is simple to notice that the line-to-line voltage Vbc is not affected by the fault and therefore has the best shape and the lower harmonic content if compared with Vab and Vac, as shown in Fig. 12b and in the next sections.

The alternative proposed strategy is based on a three-level SVM properly designed in order to avoid the forbidden states within the faulty leg (the state 0 in case of external switch in SC fault) and to guarantee a reasonable dc-link voltage

balancing during fault tolerant mode: this strategy is defined as “hybrid SVM” and the output voltage obtained with this approach will be compared with those obtained using “hybrid PWM” and 2-level modulations, in which each leg is 2-level modulated.

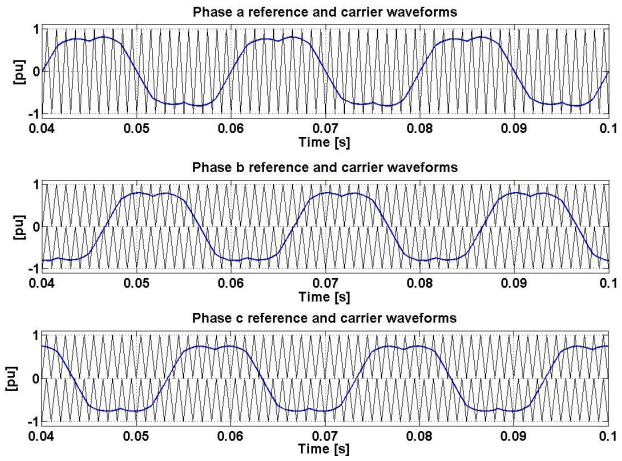

Fig. 11. Modulating and carrier signals in hybrid PWM with external switch SC fault in leg “a”, and third harmonic injection.

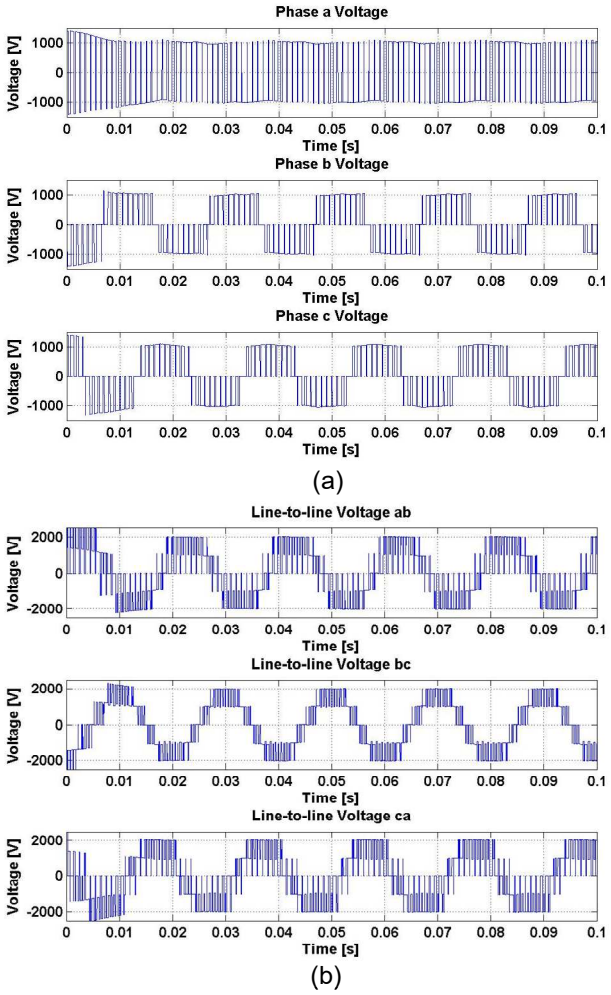

Fig. 12. Phase voltage (a) and line-to-line voltage (b) with “hybrid PWM” method and external switch SC fault.

Fig. 13a shows the set of 19 available space vectors and the 27 possible switching states on healthy configuration while in Fig. 13b the unavailable states when an external switch of phase “a” is in SC fault are deleted (with a red filled box). This fault type (the external one) eliminates each redundancy and the switching states number has a reduction from 26 to 18.

The proposed “hybrid SVM” is developed in order to reduce the harmonic content of output line-to-line voltage with respect to the 2-level modulation one, and to minimize the Neutral Point voltage oscillation. In Fig. 14 a classic modulation strategy principle [39] is traced on space vector diagram: the three level modulation is simplified into several 2-level modulations centered at the six apexes of the inner hexagon. In Fig. 15 the two modulation strategies, mixed in order to obtain the previously mentioned targets of “hybrid SVM”, are traced on the space vector diagram: the first proposed strategy shown in Fig. 15a is very similar to the previously explained classic SVM, but differs from it owing the modulation adopted inside the striped zones, because of the vectors lack,

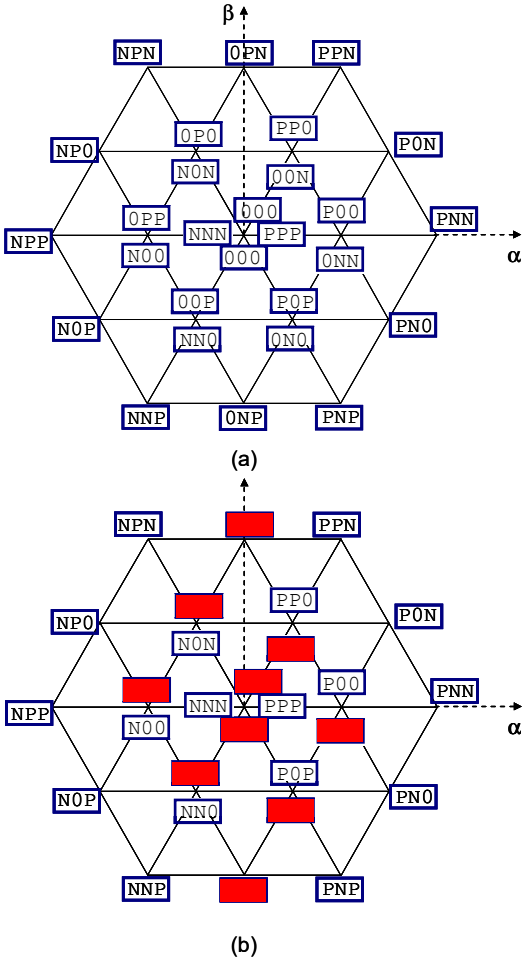

Fig. 13. Space vector diagram of NPC converter on healthy condition (a) and external switch SC fault (b) in phase “a”.

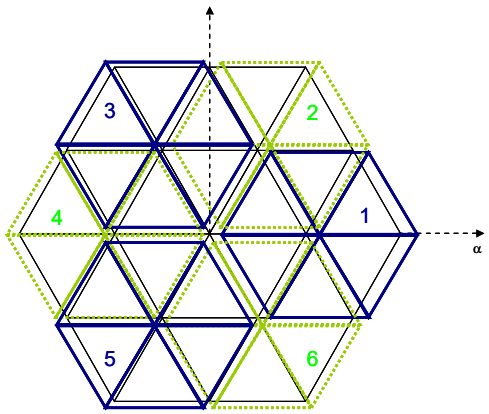

Fig. 14. Classic three level modulation: Space Vector diagram.

shown in Fig. 13b, due to the fault: inside the striped zone only the vectors at the apexes of these triangles are used for modulation.

The second proposal, mixed to the first one in order to maintain a restrained DC-Link voltage ripple, is based on a principle similar to a classical 2-level SVM, and it is shown in Fig. 15b: this modulation, centered at the middle of the external hexagon, utilizes only the active vectors located on the hexagon contour, and the zero vectors at the axis origin; this way is possible to avoid the clamping of a leg to the upper or to the lower capacitor, for a semi electrical voltage period.

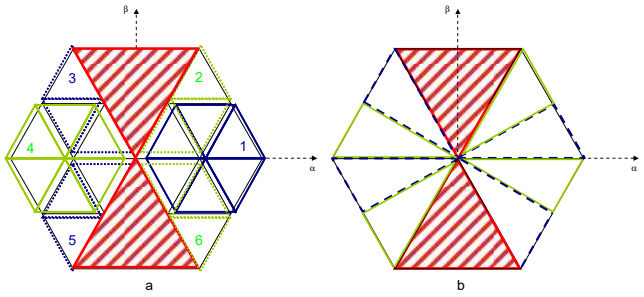

Fig. 15. Modified Space Vector diagram of NPC converter with external switch SC fault in phase "a": first (a) and second (b) proposed modulation strategies.

Without mixing the first explained modulation (Fig. 15a) with the second proposed one, the DC-Link voltage fluctuations can become very wide; in fact, as it is possible to see in Fig. 13b, when an external switch SC fault on the phase "a" occurs, the right half of hexagon has only configurations with the branch "a" in state P available, while the other (left) half has only the state N available for phase "a".

The way to balance Neutral Point is the modulation with zero vectors at the centre of hexagon (Fig. 15b), in which for example it is possible to compensate the P state of phase "a" in the right half of hexagon by imposing, as zero vector, the NNN configuration; similarly the compensation of N state in the left side is possible by imposing the PPP configuration as zero state; during each SVM period, when this strategy is implemented, two active vectors of hexagon contour and one zero vector will be imposed. By implementing alternatively the modulation strategy proposed in Fig. 15a and the one represented in Fig. 15b is possible to obtain the wanted line-to-line output voltage features. In Fig. 16 simulation results of phase and line-to-line voltage waveforms obtained with the above described "hybrid SVM" strategy are shown.

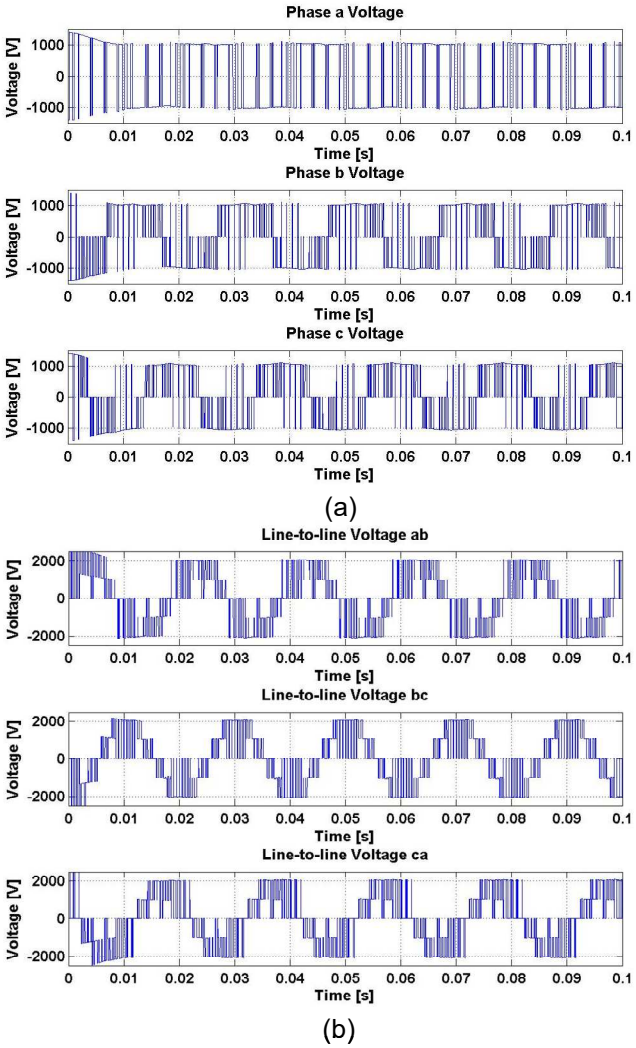

Fig. 16. Phase voltage (a) and line-to-line voltage (b) with hybrid SVM method and external switch SC fault.

Fig. 17 shows the dc-link capacitor voltages in the three modulation cases: the 2-level modulation has the smallest DC-Link voltage fluctuation but a higher harmonic content in output voltage generated, as will be highlighted in the next paragraph. The DC-Link voltage ripple of the other two proposed strategies ("hybrid PWM" and "hybrid SVM") is similar.

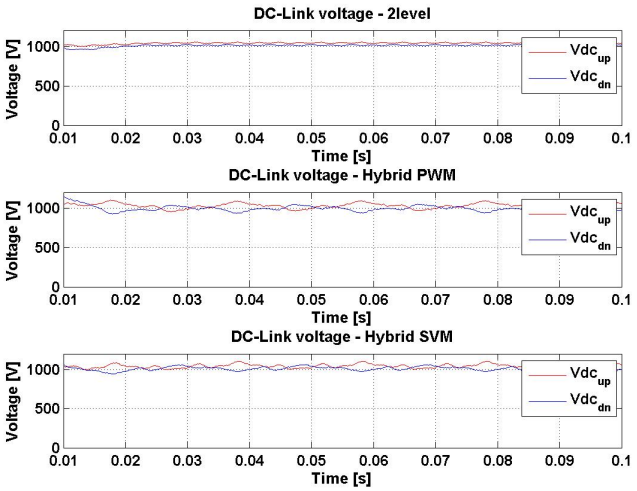

Fig. 17. Dc-link capacitor voltages using the three modulation strategies.

Table II summarizes the THD, THD_W (THD harmonic index Weighted) and percent THD values that have been computed using the three modulation strategies.

TABLE II
HARMONIC DISTORTION COMPARISON AMONG THE THREE MODULATION STRATEGIES

Symbol	Two level SVM	Hybrid PWM	Hybrid SVM
Fundamental – Vab [V]	1731,88	1760,64	1750,46
Fundamental - Vbc [V]	1732,00	1752,07	1770,09
Fundamental - Vca [V]	1731,65	1740,81	1664,89
THD Vab [V]	1250,53	969,26	1074,35
THD Vbc [V]	1246,29	620,36	903,98
THD Vca [V]	1250,80	957,22	1014,71
THD_W Vab [V]	170,93	149,60	195,90
THD_W Vbc [V]	170,93	89,26	158,44
THD_W Vca [V]	170,95	143,72	176,34
THD% Vab	0,521	0,303	0,377
THD% Vbc	0,518	0,125	0,261
THD% Vca	0,522	0,302	0,371

In term of harmonic content the "hybrid PWM" is better than the other two strategies, and the DC-Link voltage fluctuations are acceptable, if compared with the competitor solutions.

As already depicted, for the two proposed strategy (and not in 2-level SVM where all legs are modulated in the same manner), in this particular fault case the "best" line-to-line voltage in term of THD is the Vbc one, in fact the phases "b" and "c" are not affected by the fault. Fig. 18 shows the comparison among the spectrums of the three strategies in Vab line-to-line voltage (Fig. 18a) and Vbc one (Fig. 18b): these simulation results confirm the better response of "hybrid PWM" solution with respect to the 2-level SVM and the "hybrid SVM".

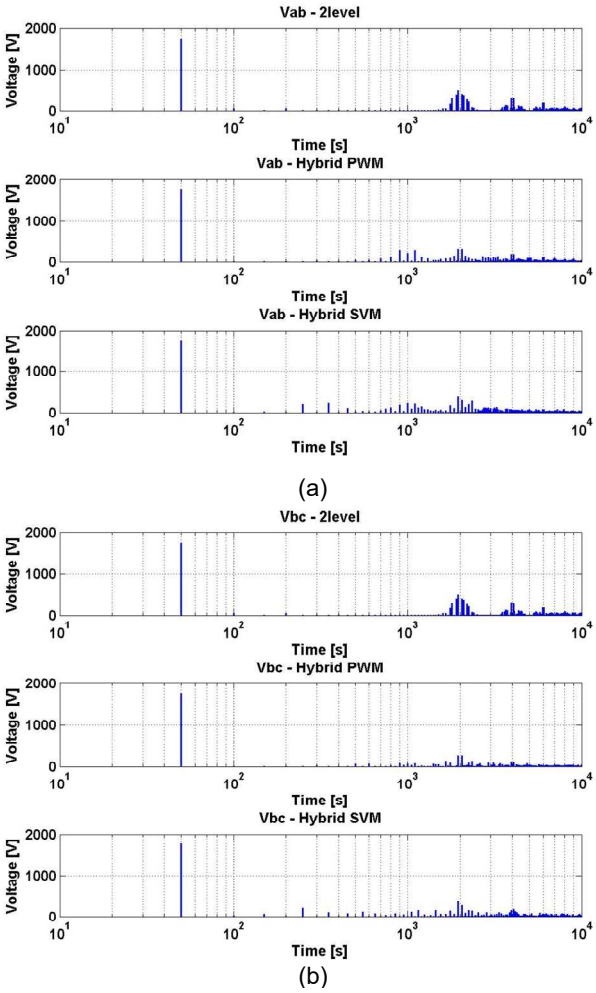

Fig. 18. Line-to-line Vab (a) and Vbc (b) voltage spectrum with the three proposed methods.

VI. CONCLUSION

A new approach to detect power semiconductor device faults and to manage the fault transition into a reconfigured situation for NPC inverter systems has been proposed.

The presented solutions consider any type of fault (Open Circuit and Short Circuit) and any type of load (passive and active), and allow to detect and extinguish the fault; furthermore a comparison among three different modulation strategies is proposed, in order to guarantee the fault tolerance and to maintain the Total Harmonic Distortion factor as little as possible. All cases are considered also regarding the supply stage on the line side: both the configuration with DFE or AFE are taken in account. The cost of the proposed solution is not negligible but it can be accepted if compared with the overall converter cost. The installation of all the presented solutions in an existing converter is possible and quite simple.

Simulation results referring to fault extinguish and transition management showing that power semiconductor devices are maintained below their rated values have been

presented. Another set of simulation results show the quality of output voltage generated when the proposed reconfiguration strategies are implemented.

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