

DC-LINK CAPACITOR SIZING OF THREE-LEVEL NEUTRAL POINT
CLAMPED VOLTAGE SOURCE INVERTERS FOR VARIABLE SPEED DRIVES

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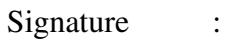
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ABSTRACT

DC-LINK CAPACITOR SIZING OF THREE-LEVEL NEUTRAL POINT CLAMPED VOLTAGE SOURCE INVERTERS FOR VARIABLE SPEED DRIVES

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A three-level neutral point clamped (NPC) voltage source inverter (VSI) topology can be advantageous in electric vehicles with a high DC-link voltage and a high switching frequency due to the flexibility in power switch selection. However, the potential oscillations in neutral point must be handled to guarantee an efficient operation of this topology. A bulky DC-link capacitor is not an option for EV applications; thus, the sizing of the DC-link capacitor considering the traction system characteristics is an important design step. This thesis investigates the effect of PWM modulation methods on the DC-link capacitor size of a three-level neutral point clamped voltage source inverter. Five PWM methods, from which three methods have an active neutral point potential control, are compared in terms of their neutral point potential (NPP) oscillations at various operating conditions. Since the operating conditions in a vehicle traction system depend on the traction motor, the worst-case NPP oscillation condition of each PWM method is determined based on the operation characteristics of a reference electric machine. Then, the size of the DC-link capacitor is determined for each PWM method so that NPP ripple is kept under desired limits under

its worst-case operating condition. It is shown that both the modulation technique and the electric machine characteristics are effective on the capacitor size. A 1 kVA prototype three-level neutral point clamped inverter is designed and used to experimentally verify the results of capacitor sizing. Carrier-based PWM method required significantly smaller capacitors than other methods; however, this method had disadvantage of higher switching losses.

Keywords: Three-level Neutral Point Clamped Inverter, Capacitor Sizing, Electric Vehicle, PMaSynRM Drive, Neutral Point Potential Ripple, Nearest Triangle Vector Method, Carrier Based Method, Numeric Modeling, Printed Circuit Board Design

ÖZ

DEĞİŞKEN HIZLI SÜRÜCÜLERDE KULLANILACAK ÜÇ DÜZEYLİ NÖTR NOKTASI BAĞLANTILI GERİLİM KAYNAK EVİRİCİLERİ İÇİN DOĞRU AKIM BAĞLANTI SIĞACI BOYUTLANDIRILMASI

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Üç seviyeli nötr nokta bağlantılı gerilim kaynağı evirici topolojisinin, güç anahtarları seçimindeki esneklik nedeniyle yüksek doğru akım bağlantı gerilimine ve yüksek anahtarlama frekansına sahip elektrikli araçlarda avantajlı olması beklenmektedir. Bununla birlikte, bu topolojinin verimli çalışmasını sağlamak için nötr noktadaki potansiyel salınımları incelenmelidir. Yüksek hacimli bir doğru akım bağlantı siğacı, elektrikli araçlar için uygun bir seçenek değildir; bu nedenle, doğru akım bağlantı siğacının, çekiş sistemi özellikleri dikkate alınarak, olabildiğince küçük boyutlandırılması önemli bir tasarım adımıdır. Bu tez, darbe genişlik modülasyonu yöntemlerinin, üç seviyeli nötr nokta bağlantılı gerilim kaynağı eviricisinin doğru akım bağlantı siğaci boyutu üzerindeki etkilerini araştırmaktadır. Çalışma dahilinde üçü aktif nötr nokta potansiyel kontrolüne sahip olmak üzere, toplam beş darbe genişliği modülasyon yönteminin, çeşitli çalışma koşullarında nötr nokta potansiyeli salınım performansları karşılaştırılmaktadır. Cer motorunun evirici üzerindeki etkileri göz önünde bulundurularak, referans bir motor için her bir darbe genişlik modülasyon yönteminin

en kötü nötr nokta potansiyel salınım durumu tespit edilmiştir. Nötr nokta potansiyel dalgalanmasının en kötü çalışma koşulu altında istenen sınırlar altında tutulması için her darbe genişlik modülasyon yöntemi için doğru akım bağlantı sığacının boyutu belirlenmiştir. Modülasyon tekniğinin ve elektrik makinesi özelliklerinin sığaç boyutu üzerinde etkili olduğu gösterilmiştir. Sonuçların deneysel olarak doğrulanması için 1 kVA güç seviyesine sahip prototip üç seviyeli nötr nokta bağlantılı evirici tasarlanmıştır. Deneysel doğrulamalar başarılı bir şekilde tamamlanmıştır. Çalışma sonucunda, taşıyıcı sinyal tabanlı darbe genişlik modülasyon yönteminin, diğer yöntemlerden çok daha küçük sığaçlar gerektirdiği gözlemlenmiştir; ancak, bu yöntemin anahtarlama kayıpları üzerindeki olumsuz etkileri göze çapmaktadır.

Anahtar Kelimeler: Üç Seviyeli Nötr Nokta Bağlantılı Evirici, Sığaç Boyutlandırma, Elektrikli Araç, Sürekli Mıknatıs Destekli Senkron Relüktans Motor Sürüşü, Nötr Nokta Salınımı, Yakın Üçgen Vektör Metodu, Taşıyıcı Tabanlı Metot, Sayısal Modelleme, Baskı Devre Kartı Tasarımı

To my lovely family...

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LIST OF ABBREVIATIONS

Si	Silicon
DC	Direct current
AC	Alternative current
MOSFET	Metal oxide semiconductor field effect transistor
IC	Integrated circuit
PCB	Printed circuit board
VSI	Voltage source inverter
EMI	Electromagnetic interference
PWM	Pulse width modulation
GND	Ground
FFT	Fast fourier transform
DSP	Digital signal processor
EV	Electric Vehicle
NPC	Neutral Point Clamped
PV	Photovoltaic
THD	Total harmonic distortion
TDD	Total demand distortion
NPP	Neutral point potential
ESR	Equivalent series resistance
SPWM	Sinusoidal pulse width modulation
SVPWM	Space vector pulse width modulation
NTV	Nearest Triangle Vector
CB	Carrier based
IGBT	Insulated gate bipolar transistor

RMS	Root mean square
PM	Permanent magnet
IM	Induction machine
PMaSynRM	Permanent magnet assisted synchronous reluctance machine
PMSM	Permanent magnet synchronous motor
RPM	Revolutions per minute
NA	Not applicable
SPI	Serial Peripheral Interface
ADC	Analog to Digital Conversion
RAM	Random access memory

LIST OF VARIABLES

V_{ds}	Drain-to-source voltage
V_{gs}	Gate-to-source voltage
Q_{GS}	Gate-to-source charge
Q_{GD}	Gate-to-drain charge
I_G	Gate current
V_{gd}	Gate-to-drain voltage
R_{on}	On-state resistance
V_{th}	Threshold voltage
f_{sw}	Switching frequency
T_j	Junction temperature
T_a	Ambient temperature
I_{load}	Load current
V_{REF}	Reference voltage
R_{J-C}	Junction to case thermal resistance
R_{HS-A}	Heat sink to ambient thermal resistance
m_i	modulation index
v_{out}	output voltage
V_{DC}	DC voltage
S_x	Switch state of phase x
ω	Electrical angular frequency
I_o	Peak load current
φ	phase angle between phase voltage and phase current
v_{np}	Neutral point voltage

i_{np}	Neutral point current
T	Switching period
u'_k	First modulation signal
u''_k	Second modulation signal
i_{cmp}	Compensation current
f_{fund}	Fundamental frequency
C_s	Snubber capacitance
L_{on}	On-state inductance
V_F	Forward voltage
R_s	Snubber resistance
S	Apparent power
P	Real power
P_{con}	Conduction loss
$P_{LossPDiode}$	Power diode loss
$P_{CONMOSD}$	MOSFET diode loss
P_{RRMOSD}	MOSFET diode reverse recovery loss

CHAPTER 1

INTRODUCTION

Electric vehicle (EV) market is expected to grow in the following decades due to environmental concerns. This growth rises the interest in designing traction systems with better performance for EVs. Two-level three-phase voltage source inverters (VSIs) with a DC-link voltage around 300-400 V are commonly used to drive the traction electric machines in EVs [1]. This topology is favorable due to its high efficiency and low cost. However, the industry is demanding drive systems with higher power density and higher efficiency. Two of the most common trends to achieve these goals are to increase the rotational speed of the traction electric machine [2] and to increase the DC-link voltage level to 800 V levels [3, 4]. Both of these changes can increase the stress on the power electronic switches. Moreover, another future need is the fast charging of the batteries in EVs. Using a higher DC-link voltage level is considered as a solution to shorten the charging times [3]. Porsche and Fisker proposed to use 800 V DC-link voltage level to achieve faster charging in electric vehicles [1].

In order to satisfy these needs and requirements, three-level neutral point clamped (NPC) VSIs can be examined as an alternative topology. Three-level NPC VSI was first introduced in 1981. The aim of the topology was to achieve higher output voltage quality with lower harmonics [5]. Later, the topology was used in many medium voltage applications including laminators, mills, compressors, fans etc. [6]. Moreover, the topology is becoming attractive for photovoltaic (PV) applications [7].

Semiconductors of the three-level NPC inverter block half of the DC-link voltage [8, 9, 10]. So, this topology supports higher DC-link voltages compared to its two-level counterpart with the same semiconductor voltage rating. Hence, the topology becomes more attractive with increasing DC-link voltage [1, 11, 12]. Moreover, three-

level NPC VSI is a better alternative while using GaN based semiconductor devices since this technology can only provide limited blocking voltage. Three-level topology is also preferable because of its lower switching losses compared to a two-level VSI [13, 14, 15, 16]. Due to this property, even though the conduction losses of three-level NPC VSIs are higher than that of the two-level VSIs, its total semiconductor losses in higher switching frequencies are lower than two-level VSI [17]. Another benefit of three-level NPC VSI for motor drive applications, is its lower total harmonic distortion (THD) of the output voltage due to lower harmonic content [8, 18]. Lower THD leads to lower harmonic losses in the electric machines; hence, less heating of the machines. Moreover, due to lower switching losses, it is suggested that gate units of the semiconductors can be adjusted to get a lower dv/dt [14]. Lower dv/dt is beneficial, since in high dv/dt cases, unexpected shaft voltages may occur which causes EMI problems [19].

An important drawback of three-level NPC VSIs is the need for neutral point potential (NPP) control. Phase currents connected to neutral point depletes one capacitor, while charging the other. This asymmetrical usage of capacitor charge results in a ripple at neutral point of the inverter [1, 12]. Having voltage ripple at the neutral point causes distorted waveforms at the output voltage [20, 21]. Voltage ripple, if left unchecked, may cause high voltages across the power switches, which may decrease the efficiency and may even cause permanent damage to the inverter [22, 23]. One other problem is that, loss distribution of the semiconductors in three-level neutral point clamped inverter depends on PWM strategy [24, 25].

Furthermore, DC-link capacitor losses increase due to low frequency capacitor current ripple [13]. The DC-link capacitors are under constant stress due to the ripple current, which increases the core temperature, internal self-heating, and equivalent series resistance (ESR) of the capacitors [26]. Thus, capacitor lifetime is affected from the NPP ripple [27].

In order to limit NPP ripple, simplest way is to increase the size of DC-link capacitors. However, this solution leads to higher volume and additional weight of the DC-link capacitors. Another method of controlling NPP is to use pulse width modulation (PWM) methods with NPP control property. These methods first measure the NPP

and then, adjust the switch states and duty cycles of semiconductors to reduce the NPP ripple. Two main groups of these methods are space vector and carrier-based methods [28], or there are some works that uses a hybrid strategy between these groups [29]. These PWM methods have different NPP ripple limiting performances. Therefore, in order to obtain the same NPP ripple, size of the DC-link capacitors must be adjusted for each PWM method individually.

In this study, sizing of DC-link capacitors of a three-level NPC type VSI is performed for five different PWM methods. In addition to the PWM methods with no NPP control that are sinusoidal PWM (SPWM) and space vector PWM (SVPWM), three PWM methods with NPP control, that are the nearest triangle vector (NTV) method, the symmetric space vector PWM (symmetric SVPWM) method [30] and the carrier-based method [28] are selected. Each modulation technique is examined for two types of NPP ripple. First one is the high frequency or switching frequency NPP ripple. The frequency of this ripple type is in the range of switching frequency of the inverter. Therefore, this ripple type is beyond the control bandwidth of the inverter. Second NPP ripple type is the low frequency NPP ripple. Frequency of this ripple type is three times the fundamental frequency of the inverter [31]. Therefore, this ripple type is within the control bandwidth of the inverter.

Most PWM methods have a self balancing effect on NPP as explained in [32]. However, this effect is slow and needs to be fastened.

In the literature, there are papers that makes DC-link capacitor sizing for two-level inverters [33]. However, a comprehensive comparative study on the DC-link capacitor sizing for a three-level NPC VSI considering different operating points for variable speed drive applications is not present. Indeed, one of the most important contributions of this study is the fact that the electric machine characteristics such as the phase voltage, current and power factor are used to identify the worse NPP ripple case for each modulation type. Therefore, this study is expected to increase the understanding of the effect of different PWM methods and the electric machine characteristics on the DC-link capacitor sizing.

Outline

The most common electric drive system and the used modulation techniques are discussed in Chapter 2. Moreover, three-level NPC type VSI is introduced and application of SPWM and SVPWM techniques in such an inverter is explained in detail. This chapter also includes the analytical NPP ripple derivation for SPWM method.

Three PWM methods for three-level NPC VSI with NPP ripple control are explained in Chapter 3. A model that can be used to estimate the low frequency NPP ripple is introduced and its results are used to compare the effectiveness of each method. The PWM methods with NPP control are also compared with classical PWM methods.

The used electric machine characteristics are given at the beginning of Chapter 4 and 20 operating points are selected for NPP ripple evaluations. DC-link capacitor sizing algorithm considering both the low frequency and high frequency NPP ripple is presented for the selected drive system characteristics.

The design of a small scale three-level NPC inverter with 1kVA rating is explained and finally, test results are given in Chapter 5. The test results are compared with simulations to show the validity of used numeric analysis.

CHAPTER 2

STATE OF ART ELECTRICAL DRIVE SYSTEMS IN ELECTRIC VEHICLES

Electrical drive system of state of art battery electric vehicles composes of battery system, one or more inverter(s) and AC machine(s). As 3-phase AC machines are implemented in the vast majority of EVs, 3-phase voltage source inverters are used in the drive systems. In all the EVs on market, 3-phase two-level VSIs are used. In this chapter, first, two-level voltage source inverter is explained and the two most common PWM methods to drive this inverter are presented. Then, three-level neutral point clamped inverter is introduced and its two most common PWM drive methods are explained.

2.1 Two-Level Voltage Source Inverter

The most common DC-AC converter in EVs is a three-phase two-level voltage source inverter. Rising popularity of this system was due to its simple structure. Topology of the circuit consists of six power switches and six reverse diodes. In order to provide stability at the input voltage, a high voltage DC-link capacitor is added to DC-link input. Fig. 2.1 shows the circuit structure of a three-phase two-level voltage source inverter.

This topology is called voltage source inverter because its input is a DC voltage source [34]. Other type of inverters is current source inverters which is not used commonly in electric vehicles.

There are different PWM methods used to control the turn on time of the power semi-

conductors. These methods aim to obtain sinusoidal voltage waveform at the output. Simplest of PWM methods is SPWM method. In this method reference voltage signals for each phase is compared with a triangular carrier signal. When the voltage reference signal for a phase is larger than the carrier signal, upper power switch of the corresponding phase is turned on while the bottom power switch is turned off. In this case, voltage output of the corresponding leg is equal to DC-link voltage, V_{DC} . When carrier signal is larger than voltage reference signal, bottom power switch of the corresponding phase is turned on. In this case the output voltage of the corresponding leg will be zero. By changing the output voltage according to voltage reference value, this PWM method obtains AC sinusoidal signal at the output terminals.

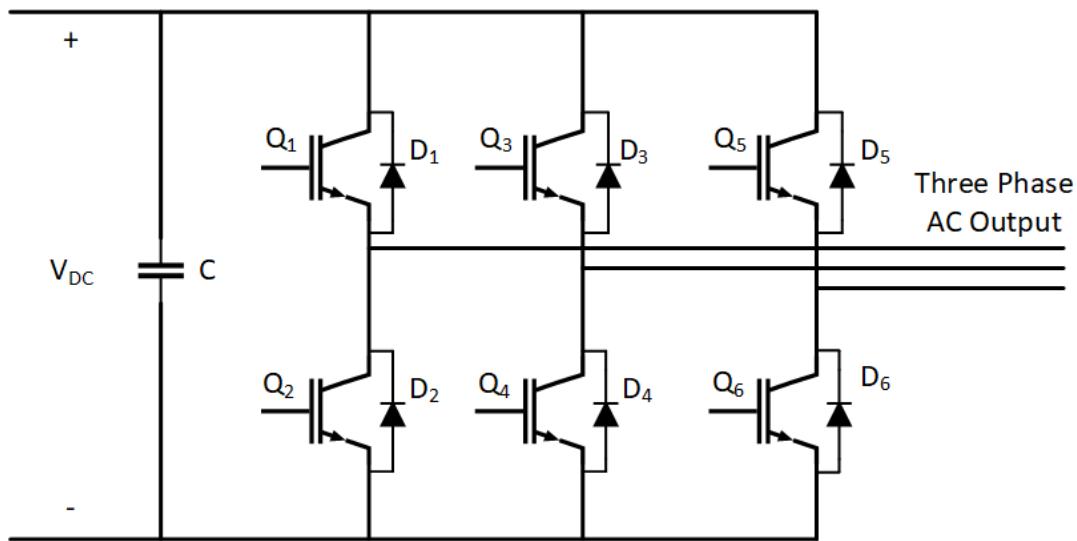


Figure 2.1: Circuit Topology of Three Phase Two Level Voltage Source Inverter

In SPWM method, modulation index, which is the proportion of peak phase voltage to half of DC-link voltage, is limited to one. The relationship between modulation index, DC-link voltage and line-to-line output rms voltage is provided in (2.1).

Note that, in all parts of the thesis, modulation index is considered as proportion of peak phase voltage to half of DC-link voltage.

$$v_{outlinetoline(RMS)} = \frac{m_i V_{DC} \sqrt{3}}{2\sqrt{2}} \quad (2.1)$$

Fig. 2.2 shows the voltage reference and triangular carrier signals. Red line given

in upper graph represents phase voltage reference signal while blue line represents carrier signal. Modulation index (m_i) is selected as 0.8, fundamental frequency of sinusoidal waveform is 50Hz and the switching frequency is 1kHz. Graph given on the bottom represents the gate signals provided to corresponding phase. When voltage reference signal is larger than carrier signal, top switch is turned on and bottom switch is turned off, which corresponds to 1. When voltage reference signal is smaller than carrier signal, top switch is turned off and bottom switch is turned on, which corresponds to 0.

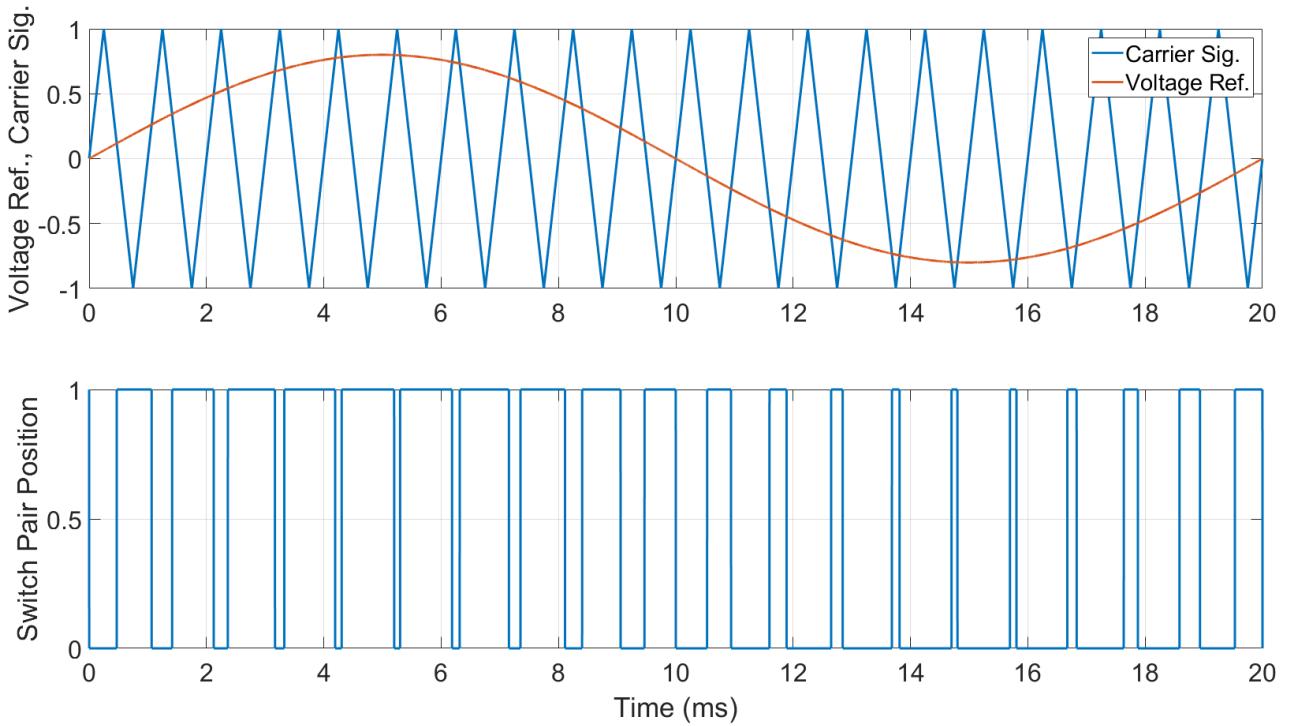


Figure 2.2: Illustration of Comparison Step of SPWM Method

Another common PWM method is space vector PWM (SVPWM) method. In this method, voltage reference signals are not solely regarded as scalar quantities. The reference signals are regarded as vectors, meaning that the positions of the reference signals on space are used in application of the method.

Each phase of a three-phase two-level voltage source inverter has one power switch pair. Letter S is used to define the state of a switch pair. State value 1 means the top switch of the corresponding phase is turned on while the bottom switch is turned off.

Value 0 means the bottom switch is turned on while the top switch is turned off. S_a , S_b , S_c represent the state of switch pair in corresponding phase leg. Due to 2 possible positions for each phase and 3 different phases, there are a total of 8 switch states that can be applied to the inverter. These switch states are shown in Table 2.1. Moreover, voltage values between each phase and load neutral point are shown. Notice that this neutral point is at neutral point of Y connected load, so it is different than DC-link neutral point.

All switching states of the inverter can be represented as vectors. These vectors are shown in Fig. 2.3. There are two zero vectors [000] and [111] that are located at the center of the hexagon. Other 6 vectors are non zero vectors and located at the corners of the hexagon.

Table 2.1: Two-Level SVPWM Possible Switching States

S_a	S_b	S_c	V_{an}	V_{bn}	V_{cn}
0	0	0	0	0	0
0	0	1	$\frac{-V_{DC}}{3}$	$\frac{-V_{DC}}{3}$	$\frac{2V_{DC}}{3}$
0	1	0	$\frac{-V_{DC}}{3}$	$\frac{2V_{DC}}{3}$	$\frac{-V_{DC}}{3}$
0	1	1	$\frac{-2V_{DC}}{3}$	$\frac{V_{DC}}{3}$	$\frac{V_{DC}}{3}$
1	0	0	$\frac{2V_{DC}}{3}$	$\frac{-V_{DC}}{3}$	$\frac{-V_{DC}}{3}$
1	0	1	$\frac{V_{DC}}{3}$	$\frac{-2V_{DC}}{3}$	$\frac{V_{DC}}{3}$
1	1	0	$\frac{V_{DC}}{3}$	$\frac{V_{DC}}{3}$	$\frac{-2V_{DC}}{3}$
1	1	1	0	0	0

In order to use the vectors, three phase voltage reference should be represented in terms of these vectors. Convenient way of representation starts with Clarke transformation. Purpose of Clarke transformation is to change the reference frame of voltage reference signals. Initial reference frame is a rotating three axis reference frame. Axes of this frame is aligned with A, B and C phases of the inverter. The final reference frame is again a rotating frame. However, there are two axes in the final reference frame. The axes are orthogonal to each other. The axes are named alpha (α) and beta (β). The reference frames are illustrated in Fig. 2.4. Blue lines represent α and β

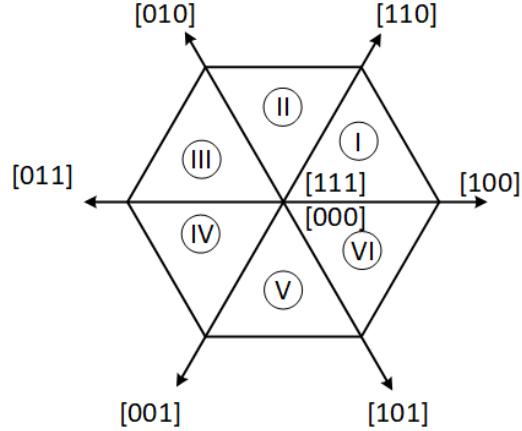


Figure 2.3: Two Level Inverter Vectors of Switching States

axes. Letter v represents equivalent reference voltage vector, ω represents electrical angular frequency and t represents time.

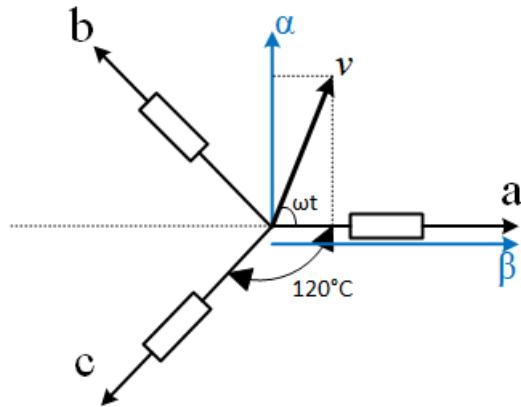


Figure 2.4: Clarke Transformation

An equivalent voltage reference vector represented in abc frame can be converted into $\alpha\beta$ reference frame by Clarke transformation matrix provided in (2.2). Multiplier $\frac{2}{3}$ is added to keep amplitude of voltage reference vectors the same.

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \quad (2.2)$$

There are six regions on the space vector plane. In order to represent the voltage reference in terms of vectors, region number which contains the voltage reference should be found. By using $\alpha\beta$ coordinate information, it is possible to obtain region number. Table 2.2 shows $\alpha\beta$ range of different regions.

After the determination of the region, reference voltage should be represented in terms of zero vectors and two non-zero vectors that are creating the borders of the corresponding region by vector summation. An example vector summation is provided in Fig. 2.5. Multipliers t_1 and t_2 are used to determine dwell times of the corresponding vectors. Relationship between t_1 , t_2 , v_α and v_β are shown for different regions in Table 2.3.

Table 2.2: Two-Level SVPWM Switching States

$-\alpha > \frac{\beta}{\sqrt{3}}$	$\beta > 0$	$\alpha > \frac{\beta}{\sqrt{3}}$	Region
x	1	1	1
0	1	0	2
1	1	x	3
x	0	0	4
1	0	1	5
0	0	x	6

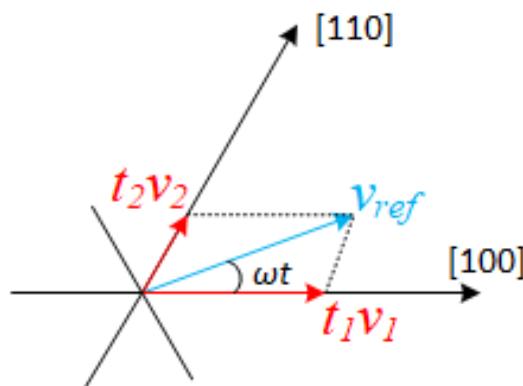


Figure 2.5: Two Level Inverter Vectors of Switching States

After finding t_1 and t_2 , t_0 should be found by subtracting t_1 and t_2 from the total

Table 2.3: Two-Level SVPWM Possible Switching States

Region	Turn On Time Expression
1	$t_1 = \frac{1}{2}(\sqrt{3}\alpha - \beta)$ $t_2 = \beta$ $t_0 = T - t_1 - t_2$
2	$t_1 = \frac{1}{2}(-\sqrt{3}\alpha + \beta)$ $t_2 = \frac{1}{2}(\sqrt{3}\alpha + \beta)$ $t_0 = T - t_1 - t_2$
3	$t_1 = \beta$ $t_2 = \frac{1}{2}(\sqrt{3}\alpha + \beta)$ $t_0 = T - t_1 - t_2$
4	$t_1 = -\beta$ $t_2 = \frac{1}{2}(-\sqrt{3} + \beta)$ $t_0 = T - t_1 - t_2$
5	$t_1 = -\frac{1}{2}(\sqrt{3}\alpha + \beta)$ $t_2 = \frac{1}{2}(\sqrt{3}\alpha - \beta)$ $t_0 = T - t_1 - t_2$
6	$t_1 = \frac{1}{2}(\sqrt{3}\alpha + \beta)$ $t_2 = \frac{1}{2}(\sqrt{3}\alpha - \beta)$ $t_0 = T - t_1 - t_2$

switching period T . As a result, all the dwell times of the vectors are known. At the next step, dwell times should be applied to power switch gates. In order to limit the switch state change to one switch at a time, two zero vectors [000] and [111] are used at the beginning and ending of each switching period and other two vectors are applied between zero vectors. In the most commonly applied SVPWM method, dwell times of zero vectors are set to be equal to each other. An example of gate signal production is illustrated in Fig. 2.6 for region number one. Time spent in each vector is provided in bottom row. First vector applied to the inverter is a zero vector [000]. After $\frac{t_0}{4}$ duration, vector [100] is applied to inverter for $\frac{t_1}{2}$. Then vector [110] is applied for $\frac{t_2}{2}$. Lastly, vector [111] is applied for $\frac{t_0}{4}$. Then the applied vectors are applied in reverse sequence. Notice that with this sequence only one phase leg is switched during vector change.

Time Axis								
S_A	0	1	1	1	1	1	1	0
S_B	0	0	1	1	1	1	0	0
S_C	0	0	0	1	1	0	0	0
Vector	v_0	v_1	v_2	v_7	v_7	v_2	v_1	v_0
Time Duration	$\frac{t_0}{4}$	$\frac{t_1}{2}$	$\frac{t_2}{2}$	$\frac{t_0}{4}$	$\frac{t_0}{4}$	$\frac{t_2}{2}$	$\frac{t_1}{2}$	$\frac{t_0}{2}$

Figure 2.6: Two-Level Inverter SVPWM Example Switching Sequence For Region One

Voltage reference within the vector hexagon can be obtained by SVPWM method. However, not every voltage reference amplitude can be obtained at every angle. Therefore, during a constant amplitude operation, voltage reference is limited within the blue circle provided Fig. 2.7. The maximum radius of the circle is $\frac{V_{DC}}{\sqrt{3}}$. It is possible to reach $\frac{V_{DC}}{2}$ with SPWM; thus, it is possible to obtain 15% higher AC voltage with SVPWM compared to SPWM method with the same input DC voltage. Therefore, DC-link utilization of SVPWM is better than SPWM. On the other hand, applying SVPWM requires higher computational power than SPWM.

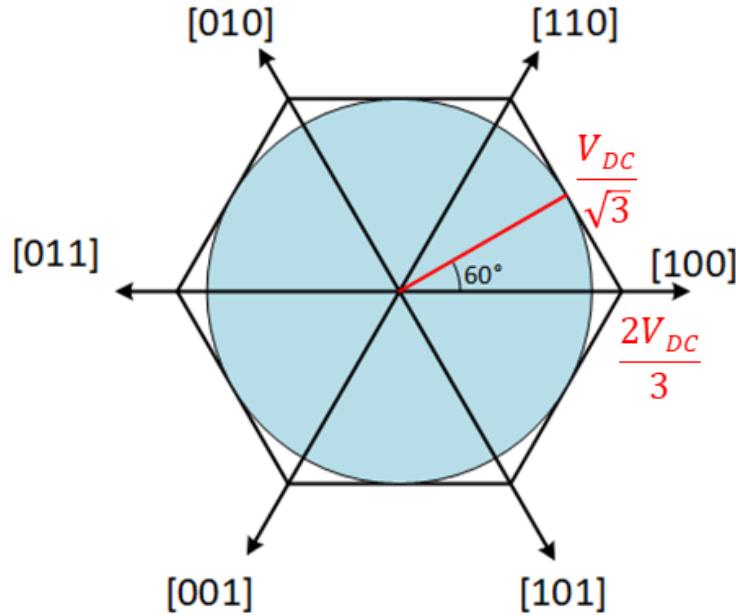


Figure 2.7: Vector Diagram of Two Level SVPWM Method

2.2 Three-Level Neutral Point Clamped Inverter

Three-phase three-level neutral point clamped inverter is a circuit topology consisting of twelve power switches and six power diodes as shown in Fig. 2.8. As the name suggests neutral point of the circuit is clamped by power diodes. In order to obtain neutral point, two capacitors with the same size are used at the DC-link. Power semiconductors should be able to conduct current in reverse direction, so, if the power switches are selected as IGBT, reverse diodes should be added.

Three-level NPC VSI topology has several advantages compared to two-level voltage source inverter. Firstly, for the same DC-link voltage level, semiconductors with lower voltage rating can be used. This is because of the fact that 4 power semiconductors are connected in series at each phase. Hence, two switches should endure the entire DC-link voltage; in other words, each power switch should endure half of DC-link voltage. This is illustrated in Fig. 2.9.

Line-to-line output voltage waveform of three-level neutral point clamped inverter

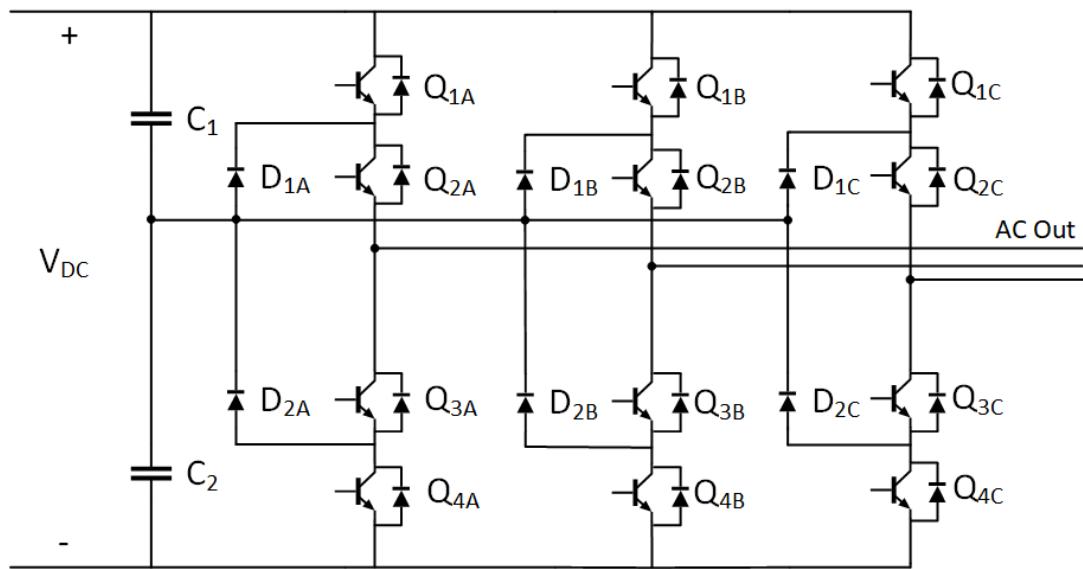


Figure 2.8: Three-Level Neutral Point Clamped Inverter

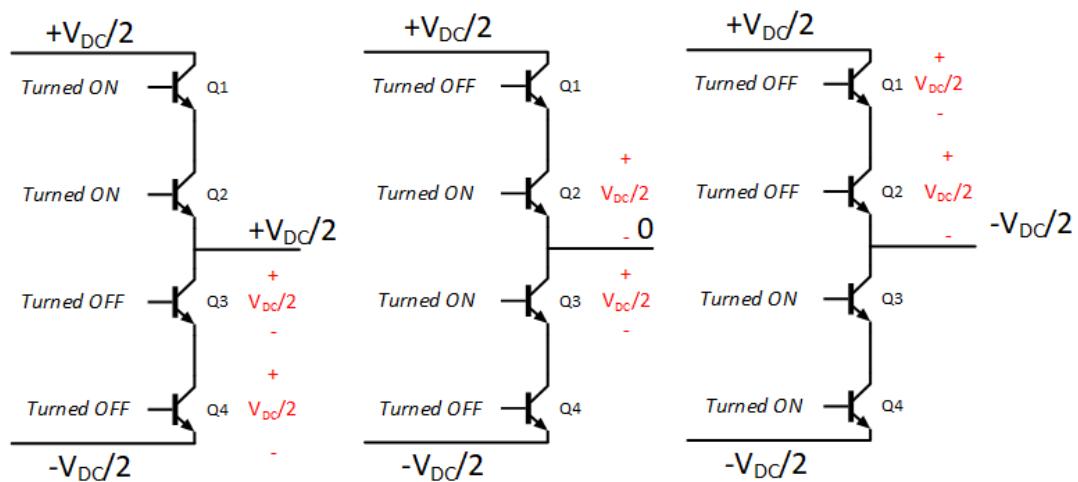


Figure 2.9: Voltage Distribution Across Power Semiconductors of Three-Level NPC Inverter

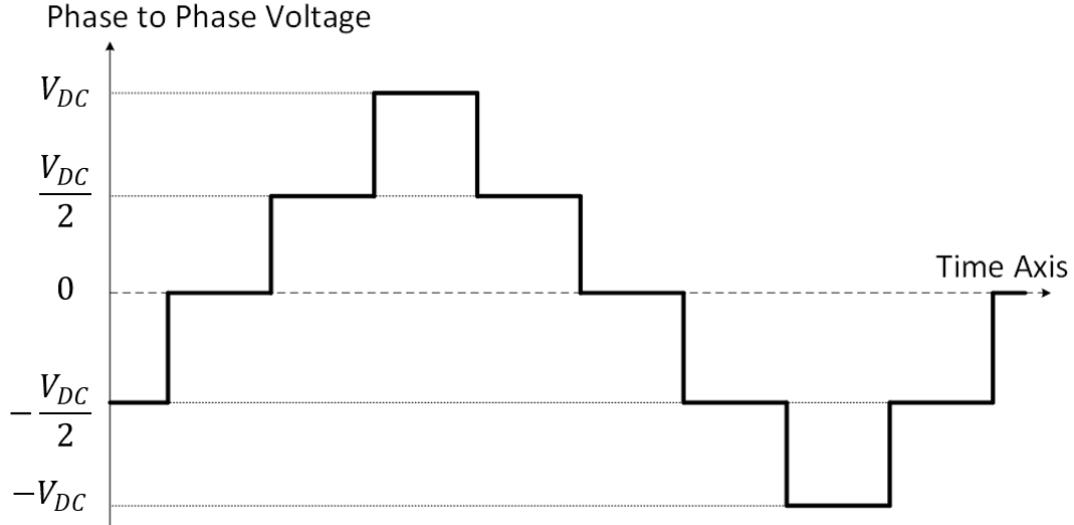


Figure 2.10: Output Line-to-Line Voltage of Three-Level NPC Inverter

has a staircase waveform. There are 5 instantaneous discrete voltage values that can be obtained at line-to-line voltage. These values are $\pm V_{DC}$, $\pm \frac{V_{DC}}{2}$ and 0. Line-to-line output voltage waveform of the three-level inverter is given in Fig. 2.10.

In three-level NPC inverter, changing output of each phase voltage requires only one switch position to change. Since the switch has only $\frac{V_{DC}}{2}$ voltage, energy loss due to switching is lower than two-level voltage source inverter. This difference makes three-level neutral point clamped inverter more efficient than two-level voltage source inverter at high switching frequencies.

One benefit of using three-level neutral point clamped inverter is to have lower output current total demand distortion (TDD). Having high harmonics is problematic for motor drive applications because harmonics cause higher losses, excessive heating and disturbed torque in motors [35]. In standard IEEE-519-1999, current THD and TDD are defined as in (2.3) [36]. Variable I_1 is the fundamental frequency current and I_L is the maximum demand load current. All variables are in root-mean-square. It is observed that, having higher current THD leads to higher current TDD when load current is high and it leads relatively lower TDD when load current is low. In other words, keeping current THD low decreases the current TDD.

$$I_{THD} = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \dots}}{I_1} \quad (2.3)$$

$$I_{TDD} = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \dots}}{I_L}$$

It is shown in [37] that, for the same operating conditions three-level NPC inverter can provide lower current THD than its two-level counterpart. Therefore, three-level inverter is a better alternative than two-level VSI in terms of keeping current TDD under desired limits.

It should be noted that three-level NPC inverter has several disadvantages compared to its two-level counterpart. Firstly, this topology has 12 power switches while two-level VSI has only 6 power switches. Since higher number of power switches requires additional control, three-level NPC inverter has more complex control structure than two-level inverter; therefore, it requires higher computational power for the same operation. Moreover, having additional 6 power switches and 6 power diodes makes this topology more expensive than a two-level inverter. However, power switches of three-level inverter blocks half the voltage blocked by switches of two-level inverter. Hence, individual power switches of three-level NPC inverter is expected to cost less than individual power switches of two-level inverter.

An important disadvantage of three-level NPC inverter is having unequal power loss between power semiconductors [25]. This problem is caused by having different switching and conduction losses for power semiconductors. Loss distribution depends on the operating conditions. In other words, modulation index, power factor, PWM method are effective on distribution of losses. Unequal loss distribution may cause more complex and; therefore, costly cooling systems for three-level NPC inverters.

Another common multilevel inverter type multilevel inverter type is the T-type three-level inverter. Similar to NPC inverter, T-type inverter provides smaller output voltage steps and lower harmonic content at the output. Main difference between T-type and NPC inverter is their efficiency. NPC inverter is more efficient than T-type at higher switching frequencies [38]. In this study, NPC inverter topology is studied because it provides better efficiency at higher switching frequencies.

Sections below explains two common PWM methods used in three-level NPC inverter. These methods do not include any neutral point potential control. Therefore, their neutral point oscillations will be taken as reference when the effectiveness of neutral point potential controlling methods are evaluated.

2.3 Sinusoidal PWM

Sinusoidal PWM (SPWM) is the simplest common PWM method to drive three-level neutral point clamped inverter.

Application of SPWM method firstly requires phase voltage reference signals provided in (2.4), where m_i corresponds to modulation index and ω corresponds to electrical angular frequency which is equal to $2\pi f$ while f is the electrical frequency. Two triangular carrier signals per phase should be obtained. Minimum and maximum value of the two signals are $[0, V_{DC}/2]$ and $[-V_{DC}/2, 0]$. Frequency of the triangular signals is equal to f_{sw} . Then, voltage reference signals are compared with two triangular carrier signals. Every reference signal of each phase is compared with carrier signals independently. Given that a reference signal is larger than both of the carrier signals, Q1 and Q2 switches are turned on at the related phase of the inverter while turning Q3 and Q4 off, this switch state is denoted as S_1 . If the reference signal is smaller than first carrier signal and larger than second carrier signal, Q2 and Q3 are turned on while turning Q1 and Q4 off, this switch state is denoted as S_2 . If the reference signal is smaller than both carrier signals, then Q3 and Q4 are turned on while Q1 and Q2 are turned off, this switch state is denoted as S_3 . Maximum modulation index for this method is limited at one. Which means peak amplitude of the output sinusoidal signal is limited by $\frac{V_{DC}}{2}$ similar to two-level VSI case.

$$\begin{aligned} v_a(t) &= m_i \cos(\omega t) \\ v_b(t) &= m_i \cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_c(t) &= m_i \cos\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{2.4}$$

The method does not control neutral point potential, which means that this method

does not require a voltage sensor at the neutral point. This property provides a cost benefit. However, since the method does not control neutral point potential, large capacitors should be used in the DC-link. It is possible to calculate low frequency neutral point potential voltage by using load current and phase voltage expressions with the following steps. Neutral point current flows from a phase only if the phase state is S_2 . Dwell time of S_2 state, which is denoted as d_{2x} , is given in (2.5) with x corresponding to related phase. As shown in the expression, sign of the second term depends on the sign of the corresponding phase voltage reference. In order to combine two conditions, absolute value of the second term is used and the result is given in (2.6).

Since fundamental period of the phase current is many times larger than switching period, phase current can be assumed constant within a switching period. In this case, neutral point current flowing to each phase will be the product of dwell time of state S_2 and corresponding phase current. Summation of current flowing to each phase will be equal to average neutral point current for that switching period as given in (2.7).

Load current for each phase is provided in (2.8). Peak value of phase current is denoted as I_o and phase difference between phase voltage and phase current is denoted as φ . Combining phase current information with (2.7), neutral point current i_{np} that flows from neutral point to the diodes of each phase can be obtained as in (2.9).

$$\begin{aligned}
& \text{if } v_a(t) > 0 \text{ then } d_{2a} = 1 - m_i \cos(\omega t), \\
& \text{if } v_a(t) < 0 \text{ then } d_{2a} = 1 + m_i \cos(\omega t), \\
& \text{if } v_b(t) > 0 \text{ then } d_{2b} = 1 - m_i \cos\left(\omega t - \frac{2\pi}{3}\right), \\
& \text{if } v_b(t) < 0 \text{ then } d_{2b} = 1 + m_i \cos\left(\omega t - \frac{2\pi}{3}\right), \\
& \text{if } v_c(t) > 0 \text{ then } d_{2c} = 1 - m_i \cos\left(\omega t - \frac{4\pi}{3}\right), \\
& \text{if } v_c(t) < 0 \text{ then } d_{2c} = 1 + m_i \cos\left(\omega t - \frac{4\pi}{3}\right)
\end{aligned} \tag{2.5}$$

$$\begin{aligned}
d_{0a} &= 1 - m_i |\cos(\omega t)|, \\
d_{0b} &= 1 - m_i \left| \cos\left(\omega t - \frac{2\pi}{3}\right) \right|, \\
d_{0c} &= 1 - m_i \left| \cos\left(\omega t - \frac{4\pi}{3}\right) \right|
\end{aligned} \tag{2.6}$$

$$i_{np}(t) = d_{0a}i_a(t) + d_{0b}i_b(t) + d_{0c}i_c(t) \tag{2.7}$$

$$\begin{aligned}
i_a(t) &= I_o \cos(\omega t - \varphi) \\
i_b(t) &= I_o \cos\left(\omega t - \frac{2\pi}{3} - \varphi\right) \\
i_c(t) &= I_o \cos\left(\omega t - \frac{4\pi}{3} - \varphi\right)
\end{aligned} \tag{2.8}$$

$$\begin{aligned}
i_{np}(t) = -mI_o \left[&|\cos(\omega t)| \cos(\omega t - \varphi) + \right. \\
&\left| \cos\left(\omega t - \frac{2\pi}{3}\right) \right| \cos\left(\omega t - \varphi - \frac{2\pi}{3}\right) + \\
&\left. \left| \cos\left(\omega t - \frac{4\pi}{3}\right) \right| \cos\left(\omega t - \varphi - \frac{4\pi}{3}\right) \right]
\end{aligned} \tag{2.9}$$

$$i_{np}(t) = 2C \frac{dV(t)}{dt} \tag{2.10}$$

$$\Delta V_{np}(t) = \frac{1}{2C} \int_{-\infty}^t i_{np}(t) dt \tag{2.11}$$

NPP ripple ΔV_{np} can be obtained by using (2.11). The total capacitance is $2C$, since neutral point current flows from two DC-link capacitors. It can be concluded that, $\Delta V_{np}(t)$ is a periodic signal with the same frequency as neutral point current. Moreover, since neutral point current is linearly related with both modulation index m_i and peak load current I_o , NPP ripple is also linearly related with these two parameters.

Period of i_{np} in (2.9) is one third of the fundamental period of the voltage references. This is because three terms in (2.7) are symmetric to each other with 120° phase

difference. Therefore, i_{np} frequency depends on the fundamental frequency of AC voltage. Due to relation (2.11), given the peak value of i_{np} is constant, frequency of i_{np} is inversely proportional with NPP ripple.

To understand NPP ripple relation with power factor, numeric integral of (2.9) is provided in Fig. 2.11 for $m_i = 1$, $f = 50 \text{ Hz}$, $I_o = 1 \text{ A}$. This graph shows that lagging phase angle between current and voltage signals has monotonically increasing effect on positive half cycle integral of i_{np} . Hence, NPP ripple increases with phase angle.

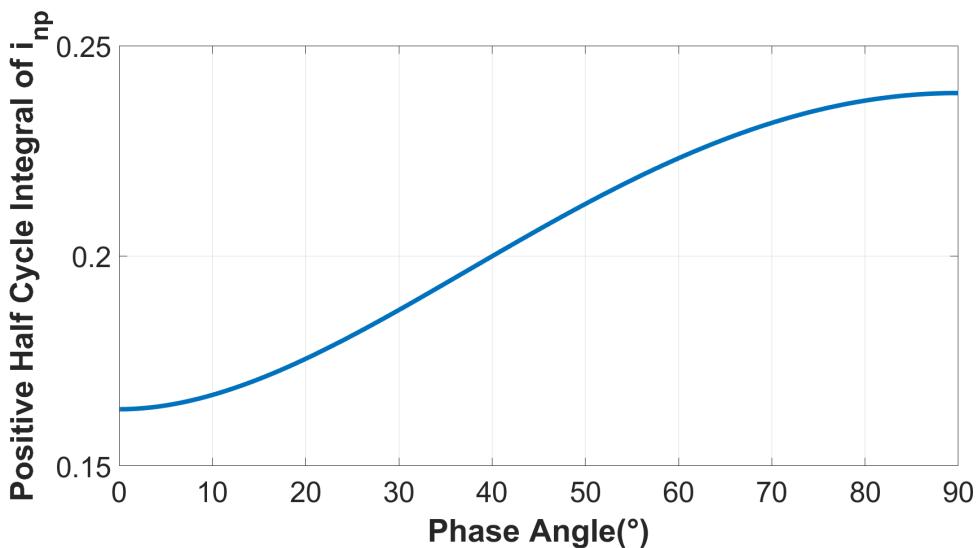


Figure 2.11: Positive Half Cycle Integral of i_{np} vs Phase Angle

Based on these findings, worse case for low frequency NPP ripple can be expected at high modulation index, high load current, low fundamental frequency and low power factor for SPWM modulation.

2.4 Space Vector PWM

Space vector PWM (SVPWM) method is also applicable to three-level NPC inverter. However, due to higher number of power switches, application of the method is more complex than two-level inverter case.

In order to have three different voltage values at the phase voltage, three different

switching states are used. First switching state is obtained by turning on top two switches while turning bottom two switches off. This state is denoted as P state. In this state output voltage corresponding to related state is obtained as $\frac{V_{DC}}{2}$. Note that this voltage is the voltage difference between phase node and neutral point of the DC-link. Second state is obtained by turning middle two switches on while keeping top and bottom switch turned off. This state is denoted as O state. In this state, output voltage corresponding to related state is obtained as 0. Lastly, bottom two switches can be turned on while keeping top two switches turned off. This state is denoted as N state. In this state, output voltage corresponding to related state is obtained as $-\frac{V_{DC}}{2}$. State definitions are summarized in Table 2.4. These states are previously called as S_0 , S_1 and S_2 in SPWM explanations, respectively. The P, O and N notation is commonly used for SVPWM literature, that is the reason behind the notation change.

Table 2.4: SVPWM Switching States

S1	S2	S3	S4	State
On	On	Off	Off	P (S_1)
Off	On	On	Off	O (S_2)
Off	Off	On	On	N (S_3)

Since there are three switching states for three phases, there are totally 27 switching states for the inverter. All possible switching states of the inverter are represented on a space vector field in Fig. 2.12. Different from two-level SVPWM case, in three level case, vectors have different lengths. Largest vectors are obtained when all phases have non-O states. Middle vectors are obtained when one phase has O state and other phases have non-O states. Small vectors are obtained when one phase is in a non-O state and others have O state. It is important to mention that there are two alternatives for each small vector. In the figure, zero vectors are denoted with red color, small vectors are denoted with blue color, middle vectors are denoted with green color and large vectors are denoted with purple color.

The algorithm to obtain duty cycles of switches starts by obtaining voltage reference signals similar to SPWM case. By using reference signals, position of reference volt-

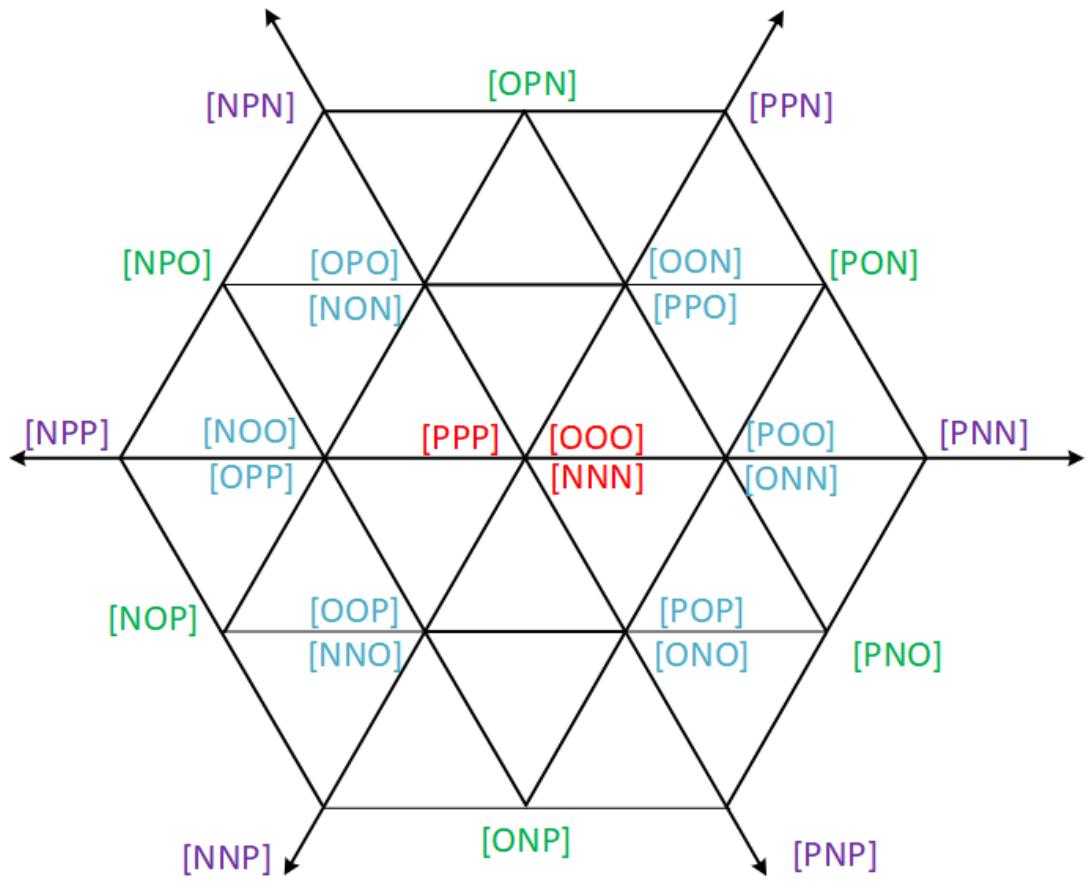


Figure 2.12: Three-Level NPC Inverter Space Vector Plane

age vector on the space vector diagram is found. Similar to two-level SVPWM case, Clarke transformation is performed on voltage reference signal. Then, similar to two-level SVPWM case, four different vectors are used to obtain required output voltage. Four vectors should be determined according to position of voltage reference vector. In order to determine vectors, space-vector plane is divided into six major regions and each major region is divided further into six subregions.

Major regions of space vector plane are provided in Fig. 2.13. It is possible to determine which major region contains the reference vector by using abc reference frame coordinate information. Table 2.5 shows major regions and their corresponding abc coordinate values.

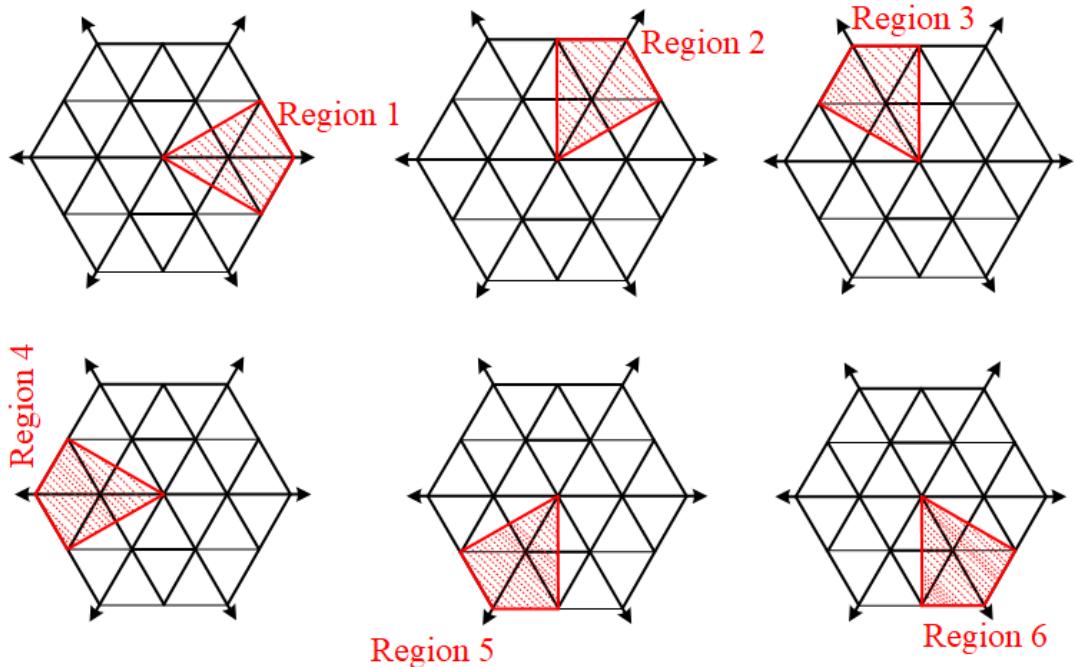


Figure 2.13: Six Major Regions [39]

Major regions of space vector plane are divided into subregions. Every subregion is cornered with at least four vectors. These vectors are summed to obtain the required output voltage. Fig. 2.14 shows the subregions of major region 1. Notice that space vector hexagon of two-level inverter and subregions of major region are similar. If the center of major region is regarded as center of two-level inverter hexagon, representation of voltage reference vector in terms of space vectors is possible. Notice

Table 2.5: Assigning Main Region for SVPWM Method

V_a	V_b	V_c	Main Sector No
>0	<0	<0	1
>0	>0	<0	2
<0	>0	<0	3
<0	>0	>0	4
<0	<0	>0	5
>0	<0	>0	6

that in Fig. 2.14, all the vectors that are used to represent reference voltage vector are given. Vectors given before the comma are vectors of three-level inverter. Vectors given after the comma are corresponding two-level inverter vectors. Since the geometric relationship between voltage reference vector and space vectors are the same for two-level inverter and three-level inverter cases, expressions used in two-level inverter SVPWM also can be used to obtain t_1 and t_2 in three-level SVPWM.

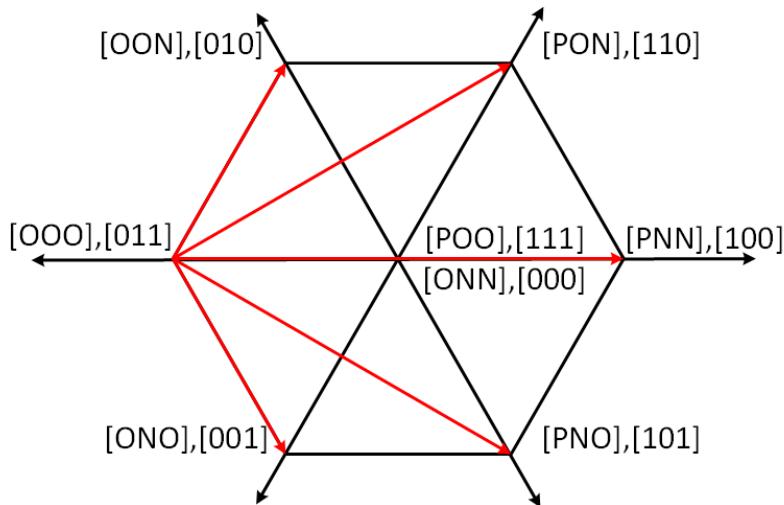


Figure 2.14: Subregions of Major Region 1 [39]

The origin of the space vector plane is transferred to center of major region by subtracting the coordinates of center of the major region from alpha-beta parameters of the voltage references. Subtraction step is provided in Table 2.6 for different major

regions. In the expressions, α' and β' denotes the transferred coordinate information. Then in the next step, subregions that contains voltage reference vector is determined.

Table 2.6: Transferring Origin Point to Center of Corresponding Major Region

Major Region Number	Required Computation
1	$\alpha' = \alpha - \frac{V_{DC}}{3}$ $\beta' = \beta$
2	$\alpha' = \alpha - \frac{V_{DC}}{6}$ $\beta' = \beta - \frac{V_{DC}}{\sqrt{3}}$
3	$\alpha' = \alpha + \frac{V_{DC}}{6}$ $\beta' = \beta - \frac{V_{DC}}{\sqrt{3}}$
4	$\alpha' = \alpha + \frac{V_{DC}}{3}$ $\beta' = \beta$
5	$\alpha' = \alpha + \frac{V_{DC}}{6}$ $\beta' = \beta + \frac{V_{DC}}{\sqrt{3}}$
6	$\alpha' = \alpha - \frac{V_{DC}}{3}$ $\beta' = \beta + \frac{V_{DC}}{\sqrt{3}}$

By using alpha beta parameters centering major region and geometric expressions, it is possible to obtain duty cycle for each switch. Computation includes vector summation that was shown in Fig. 2.5. Since the vectors and geometric relations are the same with two-level SVPWM case, same expressions can be applied to find t_1 and t_2 .

Now the dwell times of the vectors are known. Next step is to decide the vectors and their switching sequence. In order to limit the switch position change to one phase and one level, first center vector is selected as initial vector. Then, other two vectors are applied. Lastly, second center vector is applied. Vectors are applied in the reverse order to reach the initial vector. In Fig. 2.15 vector sequence is illustrated for major region 1 and subregion 1. First vector is selected as [ONN] and its dwell time is $\frac{t_0}{4}$, then state of phase A is changed and [PNN] vector is applied for $\frac{t_1}{2}$. Next vector is [PON] and it is applied for $\frac{t_2}{2}$. Last vector is [POO] and it is applied for $\frac{t_0}{4}$. After this point same vectors are applied in reverse order and switching is completed. Notice

that, in each vector change only one phase changed its state. Considering this fact, Table 2.7 shows the switching vector sequences that are used for major region 1.

Time Axis								
S_A	O	P	P	P	P	P	P	O
S_B	N	N	O	O	O	O	N	N
S_C	N	N	N	O	O	N	N	N
Vector	v_0	v_1	v_2	v_7	v_7	v_2	v_1	v_0
Time Duration	$\frac{t_0}{4}$	$\frac{t_1}{2}$	$\frac{t_2}{2}$	$\frac{t_0}{4}$	$\frac{t_0}{4}$	$\frac{t_2}{2}$	$\frac{t_1}{2}$	$\frac{t_0}{2}$

Figure 2.15: Three-Level NPC Inverter SVPWM Switching Sequence

Table 2.7: Three-Level SVPWM Vector Sequence for Major Region 1

Sub Region	Vector Sequence
1	ONN-PNN-PON-POO-POO-PON-PNN-ONN
2	ONN-OON-PON-POO-POO-PON-OON-ONN
3	ONN-OON-OOO-POO-POO-OOO-OON-ONN
4	ONN-ONO-OOO-POO-POO-OOO-ONO-ONN
5	ONN-ONO-PNO-POO-POO-PNO-ONO-ONN
6	ONN-PNN-PNO-POO-POO-PNO-PNN-ONN

Analytical calculation of low frequency neutral point potential is complex for SVPWM method. Therefore, in the following chapters low frequency NPP ripple is examined with numeric methods.

Chapter Summary

In this chapter, topology of two-level voltage source inverter (VSI) is presented. Two most common PWM methods used in two-level VSI are introduced. Then three-level neutral point clamped inverter topology is explained. Two PWM methods, SPWM and SVPWM which do not have NPP control are shown in detail. An analytical expression of low frequency NPP ripple is obtained for SPWM method.

CHAPTER 3

DC-LINK CAPACITOR VOLTAGE BALANCING OF THREE-LEVEL NPC INVERTERS

An important drawback of three-level NPC VSI, is the need for neutral point potential (NPP) control. Phase currents connected to neutral point depletes one capacitor, while charging the other. This asymmetrical usage of capacitor charge results in a ripple at neutral point of the inverter as illustrated in Fig. 3.1. In figure on the left, neutral point current i_{np} is flowing from neutral point to the phases of inverter. In this case, capacitor on the top is charged while the capacitor on the bottom is depleted. In the figure on the right, neutral point current is flowing from phases of the inverter to the neutral point. In this case, capacitor on the top is depleted while the capacitor on the bottom is charged.

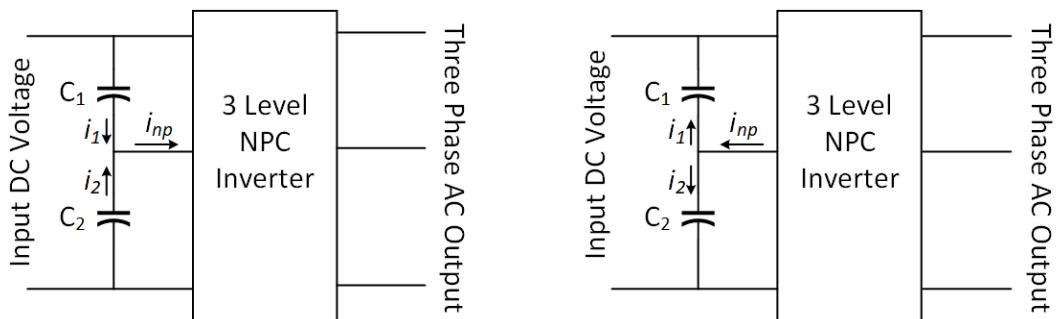


Figure 3.1: Three-Level Neutral Point Clamped Inverter Asymmetrical Capacitor Usage

There are two components of NPP ripple. First is the low frequency NPP ripple. This ripple type has frequencies comparable to fundamental output frequency of the inverter. Low frequency NPP ripple has largest component at three times the fundamental frequency. This is because neutral point current has three times the funda-

mental frequency. Low frequency NPP ripple can be controlled with control loops in the PWM method. This is because switching frequency is many times larger than low frequency NPP ripple frequency. The other component of NPP ripple is high frequency NPP ripple. This ripple type has frequencies comparable with switching frequency. Hence, this ripple type can not be controlled with closed loops added to PWM method. In this study, frequencies larger than 10 times the fundamental frequency is considered as high frequency.

Voltage ripple, if left unchecked, may cause high voltages across the power switches, which may decrease the efficiency and may even cause permanent damage to the inverter. This is because capacitor voltage is directly transferred to two power switches on the phase. If the voltage of the top DC-link capacitor is $\Delta v\%$ higher than $\frac{V_{DC}}{2}$, then voltage on the power switch is $\Delta v\%$ higher than $\frac{V_{DC}}{2}$. In this case if the switch is selected only for $\frac{V_{DC}}{2}$, then there can be a device failure. Voltage division in case of capacitor unbalance for O state is illustrated in Fig. 3.2.

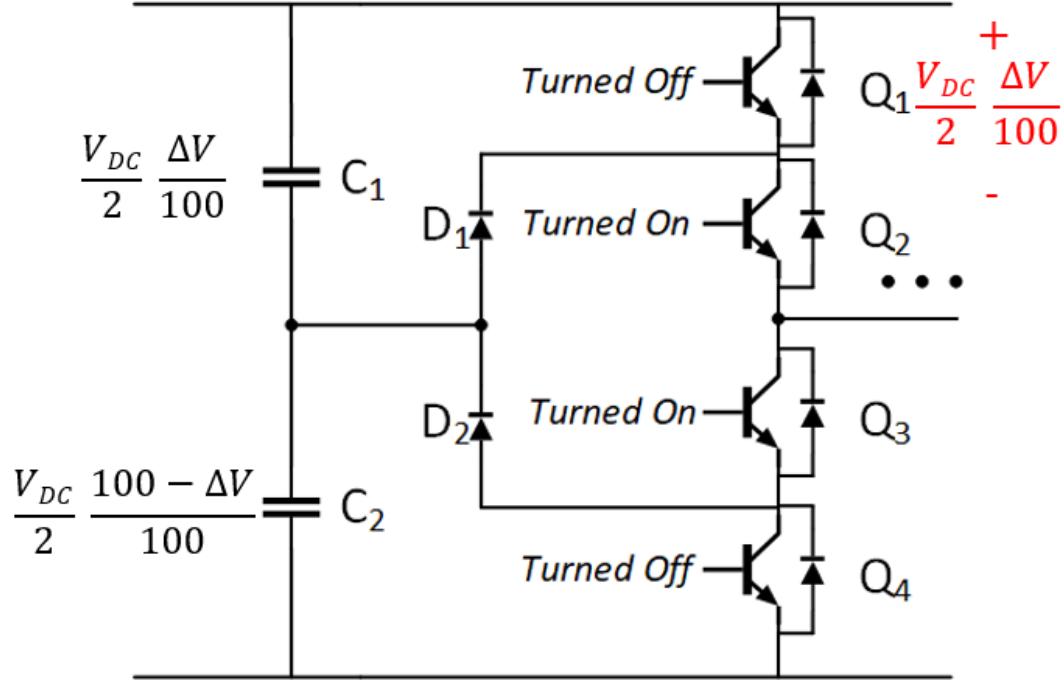


Figure 3.2: Voltage on Power Switches on O State in Case of Voltage Unbalance

Furthermore, DC-link capacitor losses increase due to low frequency capacitor current ripple [13]. This ripple results in a need for larger cooling systems. Moreover,

Orfanoudakis [13] points out that, capacitor health is negatively affected by high ripples which eventually cause capacitor failure or degrading. Main cause of capacitor loss is the Equivalent Series Resistance (ESR) of the capacitor. Especially, electrolytic capacitors have high ESR values and this property causes higher losses limiting the capacitor lifetime. Figure 3.3 shows the ESR component of a regular capacitor.

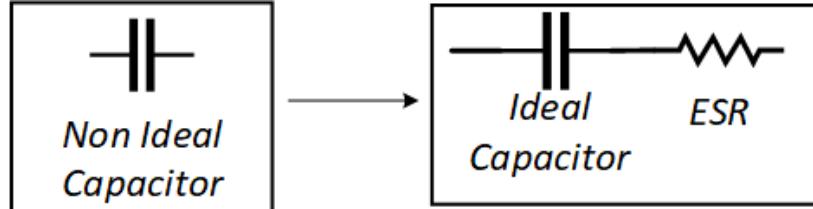


Figure 3.3: Illustration of ESR

3.1 Presented PWM Method Solutions to NPP Ripple

There are several solutions provided in the literature to reduce NPP ripple. One solution is to design PWM methods which can measure NPP and act to reduce the ripple. In this section, three PWM methods which has NPP control are introduced.

3.1.1 Nearest Triangular Vector Method (NTV)

Nearest Triangular Vector Method is a PWM method with neutral point potential control. The method uses space vector diagram. However, unlike regular SVPWM method, vector selection and duty cycle calculation do not solely depend on voltage references but also depend on neutral point potential. When the neutral point potential is higher than desired value, small vectors on the space vector diagram that results in a current flow from neutral point to phase outputs are selected. When the neutral point potential is lower than desired value, the other small vectors on the space vector diagram that results in a current flow from phase outputs to neutral point are selected. By using this effect, it is possible to control neutral point potential. Nearest Triangle Vector Method (NTV) provided in [30] and [40] is used in this study and details of

this method are explained in this section.

In this method, space vector plane is divided into six main triangular regions. Then, each of these six main regions are further divided into four small triangular regions. Therefore, there are totally twenty-four different small triangular regions. Space vector diagram showing the main triangular regions and small triangular regions of NTV method is illustrated in Fig. 3.4. First step of applying NTV method is to find which small triangular region contains the voltage reference vector. Same method that is used to determine position of voltage reference in SVPWM method can be used in NTV method because borders of small triangular regions are the same for two methods. However, notice that vector sequences are different for two methods.

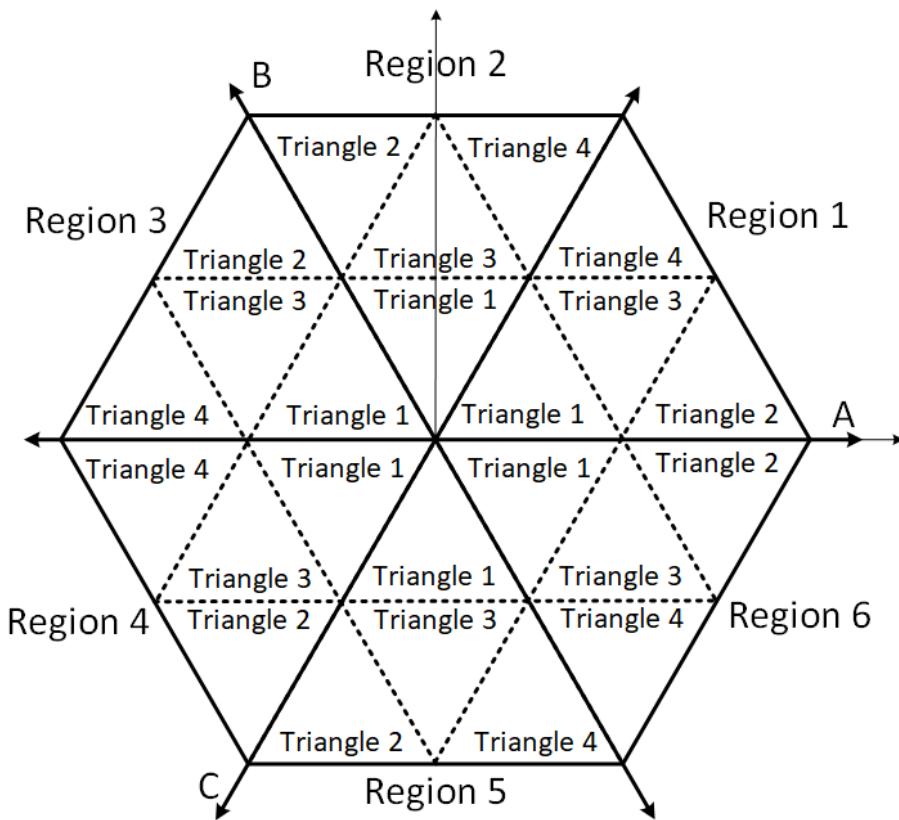


Figure 3.4: Triangular Regions Used In NTV Method [41]

In NTV method, vectors on the space vector plane are grouped according to two properties. The first property is their geometric property on space vector diagram and the second one is the effect on neutral point voltage. First vector group is denoted with a , vectors on this group are [PNN, NPN, NNP]. These vectors are large vectors that

are aligned with abc phase positions on the space vector diagram. Vectors in group a has no effect on neutral point voltage balance, because neutral point current is zero when these vectors are applied. Second vector group is denoted with b , vectors on this group are [PPN, NPP, PNP]. Vectors of group b are large vectors that are aligned with negative abc phase positions on the space vector diagram. Vectors in group b have no effect on neutral point voltage balance, since neutral point current is zero when these vectors are applied. Third group is denoted with c . Vectors on group c are middle vectors and they are [OPN, NPO, PON, NOP, PNO, ONP]. Vectors on this group has a non-zero neutral point current. Fourth group of vectors is denoted with a_p , vectors in this group are [OPO, OOP, POO]. Fifth group of vectors is denoted with a_n , vectors in this group are [NON, ONN, NNO]. Sixth group of vectors is b_p , vectors in this group are [OPP, PPO, POP]. Seventh group is denoted with b_n , vectors in this group are [OON, ONO, NOO]. Vectors on groups a_p , a_n , b_p and b_n are small vectors on the space vector diagram. Other groups are denoted with o_p , o_o , o_n . Vectors in these groups are [PPP, OOO, NNN] respectively and they are all zero vectors on the space vector diagram.

Neutral point current depends on the selected vector. Equivalent neutral point current for each vector is provided in Table 3.1 and Fig 3.5. Notice that in terms of Small Triangular Regions, Region 1 and Region 2 are symmetric to each other along the phase B line. This is because of the symmetric behaviour of the inverter in terms of neutral point current.

After main triangle region and small triangle region are decided, dwell times of each vector are obtained according to the Table 3.2. On time of the vectors are denoted with t_0 , t_1 , t_2 , t_3 , t_5 , switching period is denoted with T ; angle of voltage reference is denoted with θ and modulation index is denoted with m_i . These expressions are obtained from vector summations. Notice that, some vector groups have the same dwell time calculation. This is because of the fact that their effect on output voltage is the same. If two vectors have the same effect on the output voltage, then decision between these two vectors are made according to their effect on neutral point voltage.

After the dwell times are calculated, vector sequence should be decided. Vector sequence is decided according to phase currents and neutral point voltage. Since there

Table 3.1: Equivalent Neutral Point Current of Vectors

Vector	Equivalent i_{np}
[NPN,NPP,NNP,PNP,PNN,PPN,PPP,OOO,NNN]	0
[OPN,ONP,ONN,OPP]	i_a
[POO,NOO]	$-i_a$
[PON,NOP,POP,NON]	i_b
[OPO,ONO]	$-i_b$
[POO,NOO]	$-i_a$
[NON,PON,POP,NOP]	i_b
[OPO,ONO]	$-i_b$
[NNO,PNO,NPO,PPO]	i_c
[OOP,OON]	$-i_c$

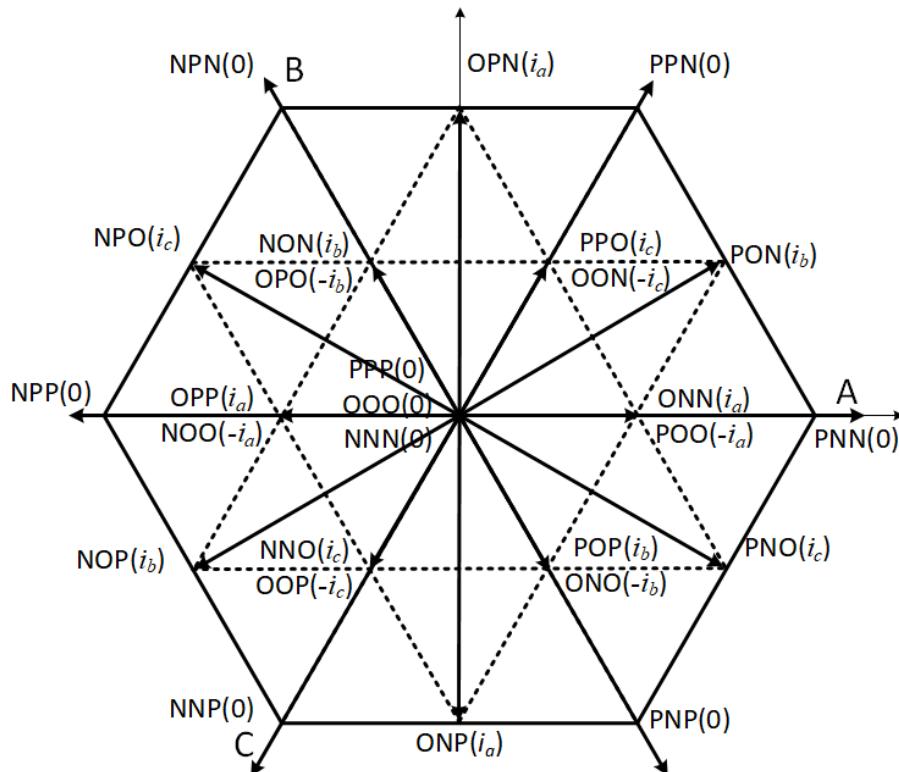


Figure 3.5: Equivalent Neutral Current of Each Vector

Table 3.2: NTV Dwell Time Expressions [41]

Region	NTV	Time Length of NTV
Small Triangle 1	o_p, o_o, o_n	$t_0 = T(1 - 2m_i \sin(\theta + \frac{\pi}{3}))$
	a_p, a_n	$t_1 = 2m_i T \sin(\frac{\pi}{3} - \theta)$
	b_p, b_n	$t_2 = m_i T \sin(\theta)$
Small Triangle 2	a_p, a_n	$t_1 = 2T(1 - m_i \sin(\theta + \frac{\pi}{3}))$
	c	$t_3 = 2m_i T \sin(\theta)$
	a	$t_4 = T(2m_i \sin(\frac{\pi}{3} - \theta) - 1)$
Small Triangle 3	a_p, a_n	$t_1 = T(1 - 2m_i \sin(\theta))$
	b_p, b_n	$t_2 = T(1 - 2m_i \sin(\pi/3 - \theta))$
	c	$t_3 = T(2m_i \sin(\theta + \frac{\pi}{3}) - 1)$
Small Triangle 4	b_p, b_n	$t_2 = 2T(1 - m_i \sin(\theta + \frac{\pi}{3}))$
	c	$t_3 = 2m_i T \sin(\frac{\pi}{3} - \theta)$
	b	$t_5 = T(2m_i \sin\theta - 1)$

is a symmetry between the regions of space vector plane, adding additional variables to the algorithm simplifies the process. These additional variables are i_X , i_Y and i_Z . Depending on the main triangle region, i_X , i_Y and i_Z are equal to different phase currents. Their relationship with phase currents are provided in Table 3.3.

In order to determine the vector sequence, two more variables are defined. These variables are X_{s0} and X_{s1} . The variables are determined according to direction of i_X , i_Y , i_Z and value of neutral point potential v_{np} . Calculation process of X_{s0} and X_{s1} is provided in Table 3.4.

The vector selection depends on position of voltage reference vector and parameters of X_{S0} and X_{S1} . This selection is done so that if the NPP is larger than zero, then neutral point current will flow from neutral point to output of the inverter or if the NPP is smaller than zero then, neutral point current will flow from output of the inverter to neutral point of the inverter.

Example vector selection for main triangular region 1 is given in Table 3.5. At the

Table 3.3: NTV Variables of i_X, i_Y, i_Z [41]

Region Number	Expression
1	$i_X = i_a$ $i_Y = i_c$ $i_Z = i_b$
2	$i_X = i_b$ $i_Y = i_c$ $i_Z = i_a$
3	$i_X = i_b$ $i_Y = i_a$ $i_Z = i_c$
4	$i_X = i_c$ $i_Y = i_a$ $i_Z = i_b$
5	$i_X = i_c$ $i_Y = i_b$ $i_Z = i_a$
6	$i_X = i_a$ $i_Y = i_b$ $i_Z = i_c$

Table 3.4: NTV Variables of X_{s0} and X_{s1}

NPP	Current State	Parameter
$NPP > 0$	$i_X > 0$	$X_{SO} = 1$
$NPP > 0$	$i_X > 0$	$X_{SO} = -1$
$NPP > 0$	$i_Y < 0$	$X_{S1} = 1$
$NPP > 0$	$i_Y > 0$	$X_{S1} = -1$
$NPP < 0$	$i_X > 0$	$X_{SO} = 1$
$NPP < 0$	$i_X > 0$	$X_{SO} = -1$
$NPP < 0$	$i_Y < 0$	$X_{S1} = 1$
$NPP < 0$	$i_Y > 0$	$X_{S1} = -1$

last column step number is provided. Step number is defined as total switch position change of the inverter in one switching period. Notice that a change of one state for one phase and one level ($P \rightarrow O$, $O \rightarrow P$, $N \rightarrow O$, $N \rightarrow O$) means one step change. In NTV method, step number is either 4 or 8 in each switching cycle.

One drawback of NPP control with NTV method is the need for neutral point potential measurement. This necessity adds one more sensor to the inverter. Therefore, increases the cost and complexity.

Analytical neutral point current calculation is complex for NTV method. Therefore, neutral point voltage is analyzed numerically at the following chapters.

3.1.2 Symmetric SVPWM Method

Similar to NTV method, symmetric SVPWM method uses space vector plane and uses small vectors to regulate NPP. However, unlike NTV method, number of steps in one switching cycle is fixed to 6. Vectors are selected so that each vector change causes maximum one step. This is achieved by restricting the selection of vectors. This difference causes higher low frequency NPP ripple in symmetric SVPWM method compared to NTV method; on the other hand, having a fixed step size at

Table 3.5: NTV Sequence Selection Guide for Region 1 [30]

Triangle Number	X_{S0}	X_{S1}	Switching Sequence	Steps
Tr1	+1	x	100-200-210-200-100	4
Tr1	-1	x	200-210-211-210-200	4
Tr2	+1	+1	100-210-221-210-100	8
Tr2	+1	-1	210-211-221-211-210	4
Tr2	-1	+1	210-211-221-211-210	4
Tr2	-1	-1	110-210-211-210-110	4
Tr3	x	+1	210-220-221-220-210	4
Tr3	x	-1	110-210-220-210-110	4
Tr4	+1	+1	100-111-221-111-100	8
Tr4	+1	-1	100-110-111-110-100	4
Tr4	-1	+1	111-211-221-211-111	4
Tr4	-1	-1	110-111-211-111-110	4

switching cycle causes better output voltage waveform. Symmetric SVPWM method application provided in [30] is used in this study and explained in this section.

Application of symmetric SVPWM algorithm starts with Clarke transformation as given in (2.2). Then main triangular region that contains voltage reference is found using the same method with NTV method. Related expressions were provided in Table 2.5 . Then the main triangular regions are divided into subregions. Subregions of Symmetric SVPWM method are $1, 2L, 2H, 3, 4L, 4H$ as provided in Fig. 3.6.

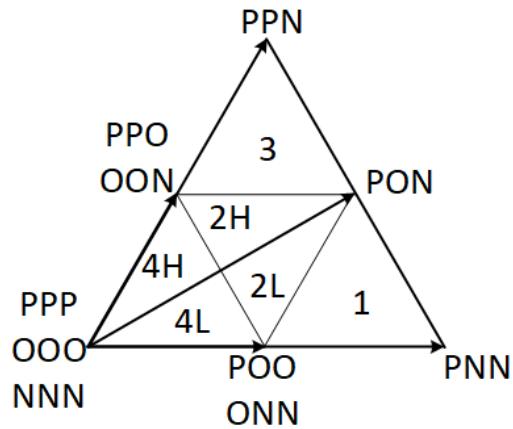


Figure 3.6: Symmetric SVPWM Sub-Regions [30]

In this method, NPP information is not used to select vectors, but instead, dwell time of the vectors are increased or decreased according to NPP value. To achieve this control, PID controller is applied to NPP value. Diagram of PID controller is provided in Fig. 3.7. Output of this PID structure is named x variable. The x variable is used to modify dwell times of the vectors. An example of dwell time control is given in Fig. 3.8. In this example, dwell time of vector POO is reduced by variable x , and the dwell time of vector ONN is increased by variable x . When Fig. 3.5 and Table 3.1 are examined, it can be observed that POO makes i_{np} equal to $-i_a$ and ONN makes i_{np} equal to i_a . Therefore, by increasing x it is possible to provide a longer positive i_{np} current given that $i_a > 0$.

Sequence of vectors for main triangular region 1 is provided in Table 3.6. According to this table, switching in each cycle has constant 6 steps, which means that the states of phases switches only once at each vector change. Because of constant step number,



Figure 3.7: Symmetric SVPWM NPP Control PID

Time Axis								
S _A	O	P	P	P	P	P	P	O
S _B	N	N	O	O	O	O	N	N
S _C	N	N	N	O	O	N	N	N
Time Duration	$\frac{t_1}{4} \left(\frac{1+x}{2} \right)$	$\frac{t_4}{2}$	$\frac{t_3}{2}$	$\frac{t_1}{4} \left(\frac{1-x}{2} \right)$	$\frac{t_1}{4} \left(\frac{1-x}{2} \right)$	$\frac{t_3}{2}$	$\frac{t_4}{2}$	$\frac{t_1}{4} \left(\frac{1+x}{2} \right)$

Figure 3.8: Example Vector Sequence of Symmetric SVPWM Method

symmetric SVPWM method provides better THD than NTV method [30].

Table 3.6: Symmetric SVPWM Vector Sequence for Main Triangular Region 1 [30]

Sub-Regions	Vector Sequences	Steps
1	ONN-PNN-PON-POO // POO-PON-PNN-ONN	3//3
2L	ONN-OON-PON-POO // POO-PON-OON-ONN	3//3
2H	OON-PON-POO-PPO // PPO-POO-PON-OON	3//3
3	OON-PON-PPN-PPO // PPO-PPN-PON-OON	3//3
4L	ONN-OON-OOO-POO // POO-OOO-OON-ONN	3//3
4H	OON-OOO-POO-PPO // PPO-POO-OOO-OON	3//3

3.1.3 Carrier Based Method

This method is selected from the carrier based methods class as an alternative to other methods. The method presented in [28] is implemented in this study. Unlike previous methods, vector position information is not used in carrier based method. Therefore, space vector plane is not used.

Important benefit of this method is that, the method can provide zero low frequency

NPP ripple for all operating points of an inverter. This is done by following a couple of rules. Switching times are controlled so that, turn on time of middle two switches are equal at each switching cycle. In other words, state of each phase is O, for equal amount of time. Since for one switching cycle total of phase currents is zero ($i_a + i_b + i_c = 0$), total charge leaving the neutral point is always zero in this PWM method.

Application of the method starts by obtaining voltage reference signals given in (2.4). The principle of keeping dwell time of state O equal for each phase is presented in (3.1). Notice that in (3.1), d denotes dwell time, first letter of subscript denotes phase and second letter denotes state position. Next, voltage references of each phase are reordered according to their magnitude. New variables are denoted with u and they are sequenced to have u_1 as largest. Their relationship is provided in (3.2).

Another rule of this method is to keep dwell time of N state of phase u_1 and dwell time of P state of phase u_3 zero. This principle is based on the fact that, largest of the voltage reference signals is always positive. Therefore, N state for this phase should have zero dwell time. Moreover, smallest of the voltage reference signals is always negative. Therefore, P state for this phase should have zero dwell time. Mathematical expression of this principle is provided in (3.3).

$$d_{a1} = d_{b1} = d_{c1} \quad (3.1)$$

$$u_1 > u_2 > u_3 \quad (3.2)$$

$$d_{10} = d_{32} = 0 \quad (3.3)$$

Dwell times for each phase and each state are decided according to voltage differences of voltage references as shown in (3.4). These expressions are based on the fact that having state N provides zero voltage difference between phase and negative node of DC-link voltage. Moreover, having state O provides $\frac{V_{DC}}{2}$ voltage difference and having state P provides V_{DC} voltage difference.

$$\begin{aligned}
d_{12} + 0.5d_{11} + 0d_{10} - d_{22} - 0.5d_{21} - 0d_{20} &= \frac{u_1 - u_2}{u_{dc}} \\
d_{22} + 0.5d_{21} + 0d_{20} - d_{32} - 0.5d_{31} - 0d_{30} &= \frac{u_2 - u_3}{u_{dc}} \\
d_{32} + 0.5d_{31} + 0d_{30} - d_{12} - 0.5d_{11} - 0d_{10} &= \frac{u_3 - u_1}{u_{dc}}
\end{aligned} \tag{3.4}$$

In this method, dwell times of switches are decided by comparing two modulation signals with triangular carrier waves. In order to find these modulation signals, expressions (3.1), (3.2), (3.3) and (3.4) are combined. Two modulation waves, u'_k and u''_k are found and their expressions are provided in (3.5), where phase number is denoted with k .

$$u'_k = \frac{u_k - u_3}{2}, \quad u''_k = \frac{u_{dc} - u_1 - u_k}{2}, \quad k = 1, 2 \tag{3.5}$$

Until this point, neutral point potential was not used to control the duty cycles. At the next step, modulation signals are adjusted so that switches operate in a way to eliminate neutral point potential. A change in duty cycle Δd will be included to eliminate neutral point potential. This change makes a difference in output voltages. However, since the change affects all P, O, N states, final phase voltage reference remains the same. Expression in (3.6) shows the adjusted voltage reference. Notice that the adjusted voltage is the same with original voltage.

$$u_{k,adj} = 2u_{dc}(d_{k2} - \Delta d_k) + u_{dc}(d_{k1} + 2\Delta d_k) + 0(d_{k0} - \Delta d_k) = u_k \tag{3.6}$$

By using the adjustment of dwell times, it is possible to increase or decrease the state O time of middle phase, u_2 , without changing the output voltage. The adjustment is illustrated in Fig. 3.9. Since O state connects neutral point to the corresponding phase, by changing Δd , it is possible to have control on neutral point potential.

Next step is to determine Δd . Sign of Δd is decided by the sign of i_{cmp} , which is the compensation current. This variable is calculated from neutral point potential deviation Δu_{NP} , capacitance of DC-link capacitors C_1 and C_2 and switching period

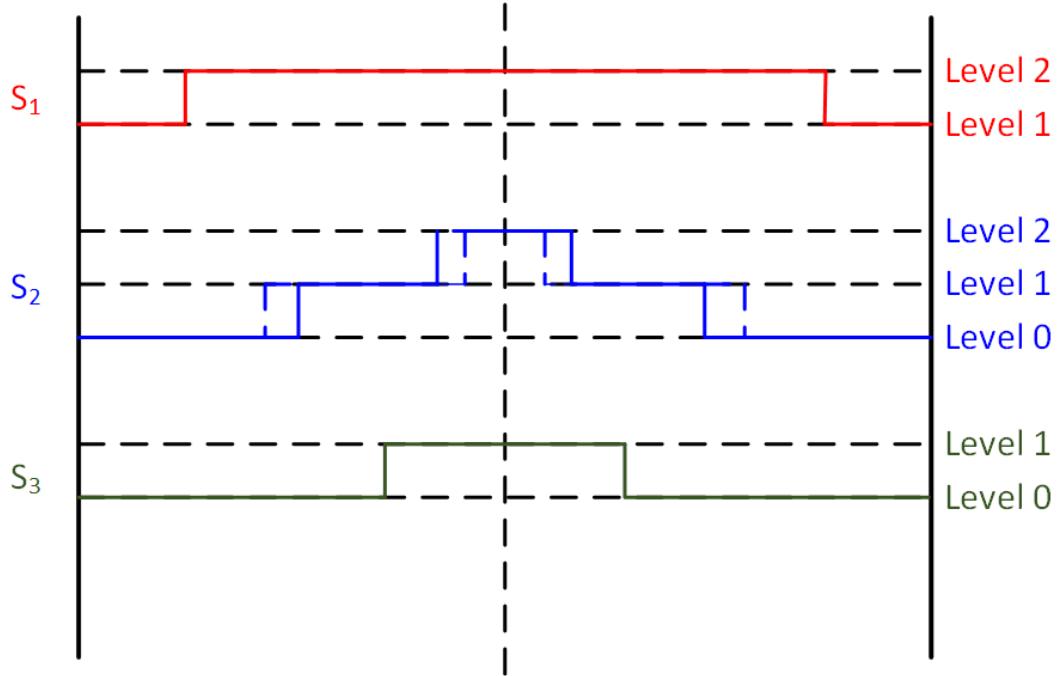


Figure 3.9: Application of Adjustment [28]

T . Expression of i_{cmp} is given in (3.7). Relationship between Δd and i_{cmp} depends on phase current of phase 2. The relationship is given in (3.7).

$$i_{cmp} = \frac{\Delta u_{NP}(C_1 + C_2)}{T_S} \quad (3.7)$$

$$i_{cmp} = 2\Delta d_2 i_2 \quad (3.8)$$

The carrier based method has better control on neutral point potential than other methods. However, this comes with a price. Due to the higher step numbers compared to other PWM methods, the carrier based method has higher losses than other PWM methods [28].

3.2 Effects of PWM Methods on Low Frequency Neutral Point Potential (NPP) Ripple

The low frequency neutral point potential ripple in a three-level NPC type VSI must be limited by a proper sized capacitor and if possible with additional neutral point voltage control. In this section, previously explained five modulation techniques are analyzed to identify their NPP values as a function of modulation index, power factor, fundamental frequency and load current. First two techniques that are SPWM and SVPWM do not have an active NPP control, whereas the other three that are symmetric space vector PWM, nearest triangle vector method and carrier based method have neutral point potential control.

In order to examine the low frequency neutral point potential ripple, the method presented in [30] is used. In this method, load current amplitudes, phase difference between current and voltage, modulation index and capacitor size are provided as input to the model. The model uses algorithms to obtain neutral point current, then by using neutral point current, voltage ripple on the neutral point is obtained. In [30], model is designed to find ripple for NTV method. In this study, model is extended for all five PWM methods previously introduced. Block diagram of the model is provided in Fig. 3.10.

The model is implemented in MATLAB Simulink environment for each PWM method. In the model, input parameters are selected as given in Table 3.7. By using low frequency neutral point potential model, low frequency neutral point potential ripple is investigated under varying modulation index, fundamental frequency, load current and power angle with different PWM methods. Results of these simulations are provided in Fig. 3.11a, Fig. 3.11b, Fig. 3.12a, Fig. 3.12b, Fig. 3.13a, Fig. 3.13b, Fig. 3.14a, Fig. 3.14b, Fig. 3.15a and Fig. 3.15b. In Fig. 3.11a, Fig. 3.12a, Fig. 3.13a, Fig. 3.14a and Fig. 3.15a power factor is kept constant at 0.75 and modulation index is kept constant at 0.85, while fundamental frequency is kept constant at 50Hz and load current is kept constant at $100A_{RMS}$ in the other ones. Moreover, NPP Ripple is normalized with DC-link voltage, V_{DC} , which is 800V. These results suggest the followings:

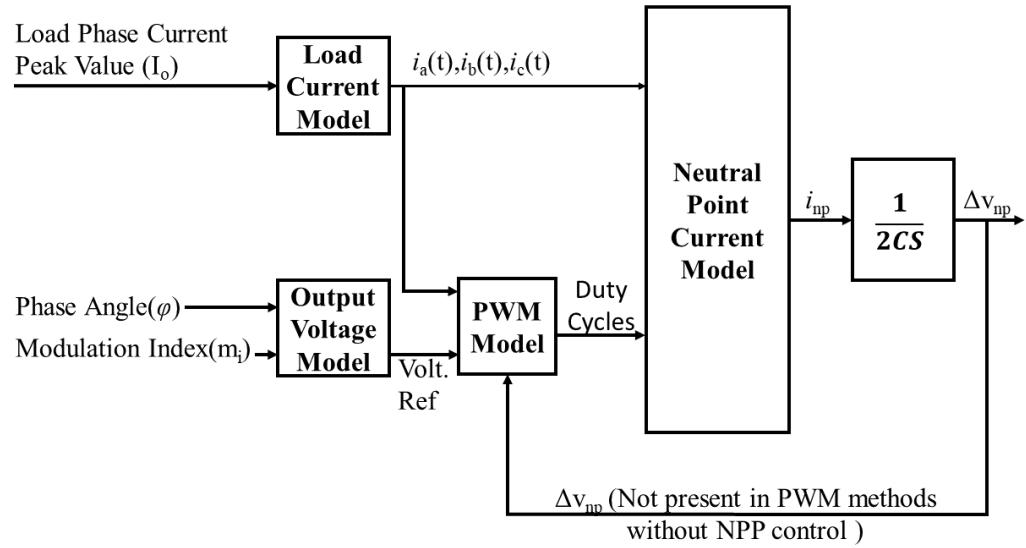


Figure 3.10: Low Frequency Neutral Point Potential Model [30]

Table 3.7: Input Parameters Used Low Frequency NPP Ripple Models

Parameter	Value
Maximum Modulation Index, m_i	1
DC-link Capacitors Size	$500 \mu F$
DC-link Voltage, V_{DC}	800V
Maximum Fundamental Frequency, f_{fund}	300 Hz
Minimum Fundamental Frequency, f_{fund}	30 Hz
Switching Frequency, f_{sw}	20 kHz
Maximum Load Current Amplitude, I_o	200 A _{RMS}
Maximum Power Factor	0.9
Minimum Power Factor	0.1
Time Step	1 μs

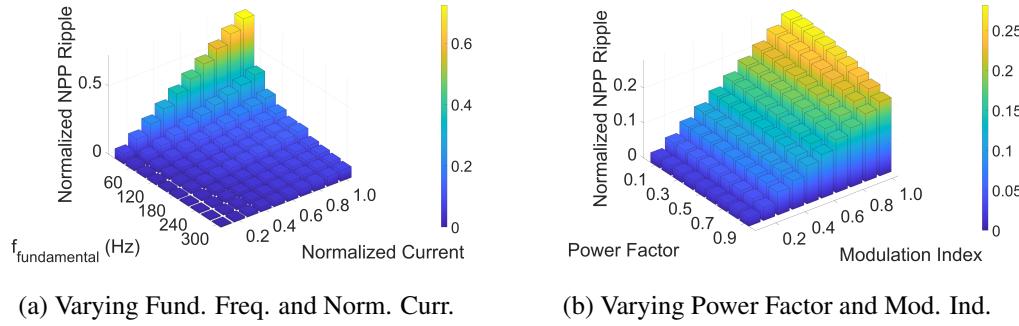


Figure 3.11: SPWM Low Frequency NPP Ripple

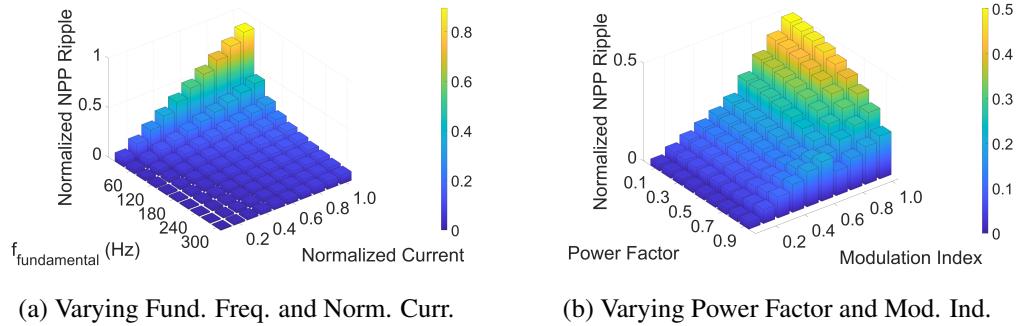


Figure 3.12: SVPWM Low Frequency NPP Ripple

- In SPWM case, results are consistent with analytical expectations obtained from (2.9) and (2.11). Low frequency neutral point potential ripple increases with falling fundamental frequency, increasing load current, falling power factor and increasing modulation index.
- In SVPWM case, results are similar to SPWM case. Low frequency neutral point potential ripple increases with increased power angle, increased load current, lower fundamental frequency and higher modulation index.
- In NTV case, different than previous methods, low frequency NPP ripple is very low for low modulation index operating points. This is because NTV method is able to completely eliminate low frequency NPP ripple for some operating regions. Therefore, in Fig. 3.13a, all low frequency ripple is zero. For this operating condition, only remaining ripple type is high frequency ripple, which is not effected by fundamental frequency. It only increases when load current

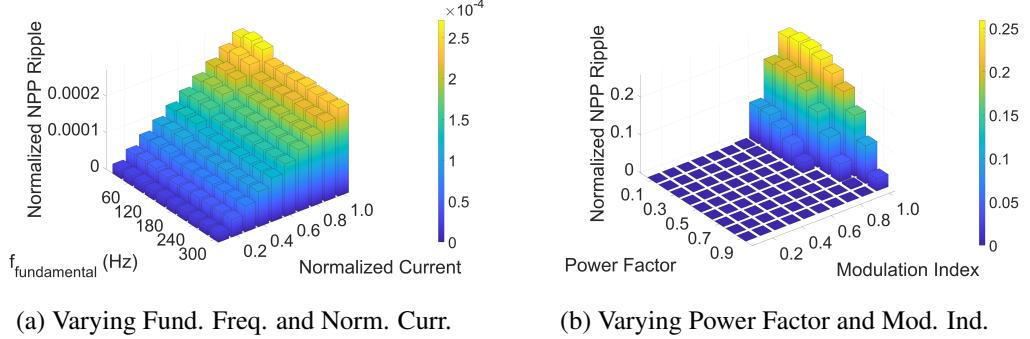
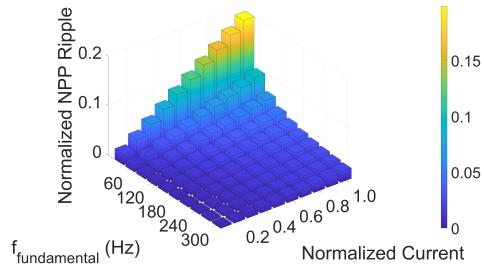


Figure 3.13: NTV Low Frequency NPP Ripple

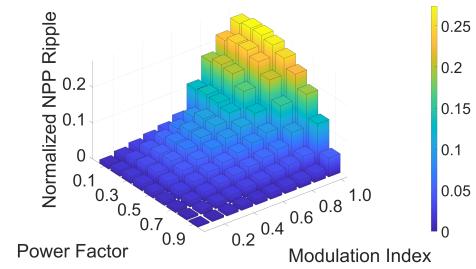
increases.

- In symmetric SVPWM case, low frequency neutral point potential ripple is significantly smaller in low modulation index operating conditions compared to high modulation index conditions. This is because symmetric SVPWM method eliminates low frequency NPP ripple better in low modulation index and high power factor cases.
- It is verified that both in NTV and symmetric SVPWM cases, highest low frequency NPP ripple is observed when fundamental frequency and, power factor are low, whereas modulation index and load current are high.
- In carrier based method case, low frequency NPP ripple is completely eliminated for all operating conditions. Only remaining component is high frequency NPP ripple, which is not affected by fundamental frequency, power factor or modulation index. Only if load current increases the NPP ripple of the carrier based method rises.

Three PWM methods used to reduce the NPP ripple are detailly explained in this chapter. The effect of the PWM method on the DC-link capacitor sizing is investigated in the next chapter.

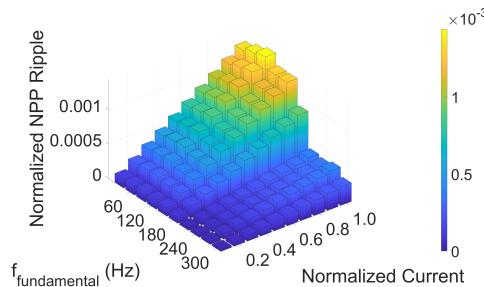


(a) Varying Fund. Freq. and Norm. Curr.

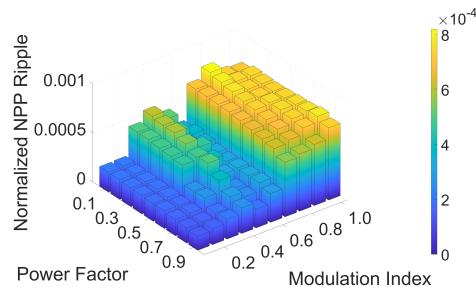


(b) Varying Power Factor and Mod. Ind.

Figure 3.14: Symmetric SVPWM Low Frequency NPP Ripple



(a) Varying Fund. Freq. and Norm. Curr.



(b) Varying Power Factor and Mod. Ind.

Figure 3.15: Carrier Based Method Low Frequency NPP Ripple

Chapter Summary

In this chapter, NPP ripple problem of three-level neutral point clamped inverter is explained with its reasons and negative consequences. Three PWM methods, NTV method, symmetric SVPWM method, carrier based method that are used to suppress NPP ripple are explained in detail. Low frequency NPP ripple model is introduced in order to investigate the relationship between operating conditions of the inverter and low frequency NPP ripple for different PWM methods. Lastly, by using NPP ripple model, low frequency NPP ripple is numerically observed for all five PWM methods introduced.

CHAPTER 4

SIZING OF DC-LINK CAPACITORS

This chapter explains method of finding correct DC-link capacitor size for three-level neutral point clamped inverter of a motor drive application. Reference motor characteristics and specifications are provided at the beginning. Then, numeric models and algorithms of capacitor selection procedure are explained. Selected capacitor size is provided for different PWM methods. Lastly, capacitor sizes are compared with that of a two-level inverter.

4.1 Capacitor Types

It is stated in [42] that, most common capacitor types used in the market for inverters are electrolytic capacitors, ceramic capacitors and film capacitors. Between these capacitor types, film capacitors can work better with higher frequency and they are affected less from the temperature change. Moreover, film capacitors provide less capacitance per volume compared to ceramic or electrolytic capacitors. Although provides less capacitance than other capacitor types, film capacitors are most commonly used DC-link capacitor type in electric vehicles because of their long life span and reliability [42].

In this study, DC-link capacitor is mostly considered as an ideal capacitor since focus of the study is on examining low frequency NPP ripple. However, while implementing the results on a traction drive system, film capacitors should be used.

4.2 Electric Machine Specifications

Both inverter and the electric machine operating conditions are important for neutral point potential ripple. A permanent magnet (PM) assisted synchronous reluctance machine (PMaSynRM) with ferrite permanent magnets is selected as the traction motor in this study. This electric machine type is gaining popularity for EV applications due to the absence of rare-earth materials. Moreover, this machine type is known to have a lower power factor than permanent magnet synchronous machines (PMSM) and induction machines (IM), hence expected to cause higher stress on the inverter. This fact makes the investigation of the PMaSynRM even more interesting.

Specifications of an exemplary 100kW PMaSynRM with the torque and rotational speed specifications provided in Table 4.1 is taken as reference for the analysis. The phase voltage limit is specified for the 0.95 modulation index with SPWM modulation with wye-connected stator terminals for 800V DC-link voltage.

Table 4.1: Specifications of the Drive System

Parameters	Values
DC-Link voltage	800 V
Pole number	4
Rated power	100 kW
Base speed	4000 rpm
Maximum speed	12000 rpm
Rated phase current	184 Arms
Rated phase voltage	266 Vrms
Rated torque	275 Nm

The stator and rotor structures of the selected electric machine is shown in Fig. 4.1. As can be seen, a four-pole, 48 slot machine with 4 flux barriers is chosen to start with. Moreover, the finite element analysis results for its electromagnetic power output, power factor, phase current and phase voltage characteristics are given in Fig. 4.2 and Fig. 4.3. It is important to mention that the machine has power factor values around

0.75 in most of the base speed region, which is expected to be 0.85-0.90 for PMSMs. Those characteristics specify the operating conditions of the drive system and are crucial for the specification of the DC-link capacitor size.

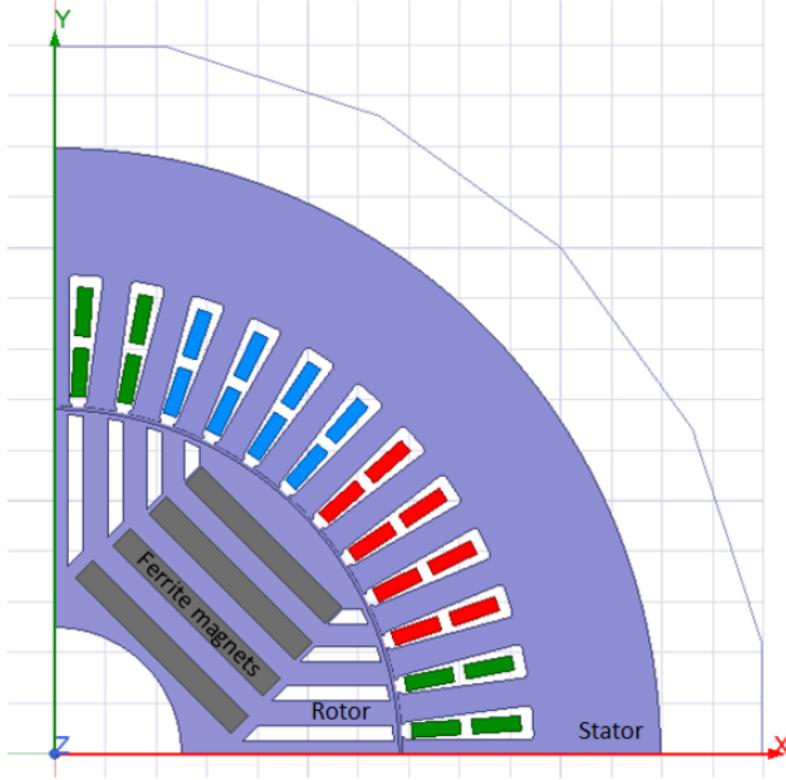


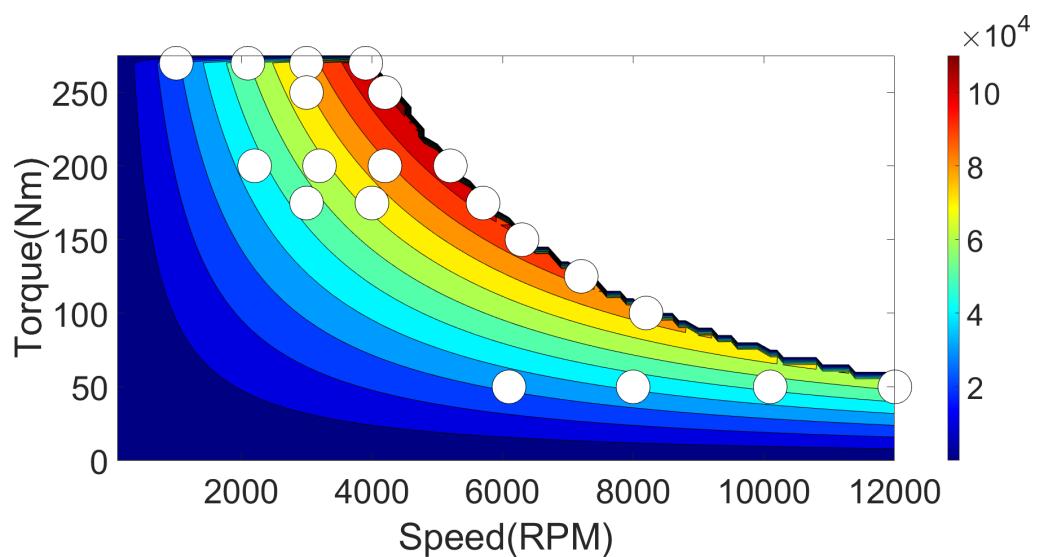
Figure 4.1: Structure of the PMaSynRM

4.3 Determining Worst Case by Considering Electric Machine Characteristics

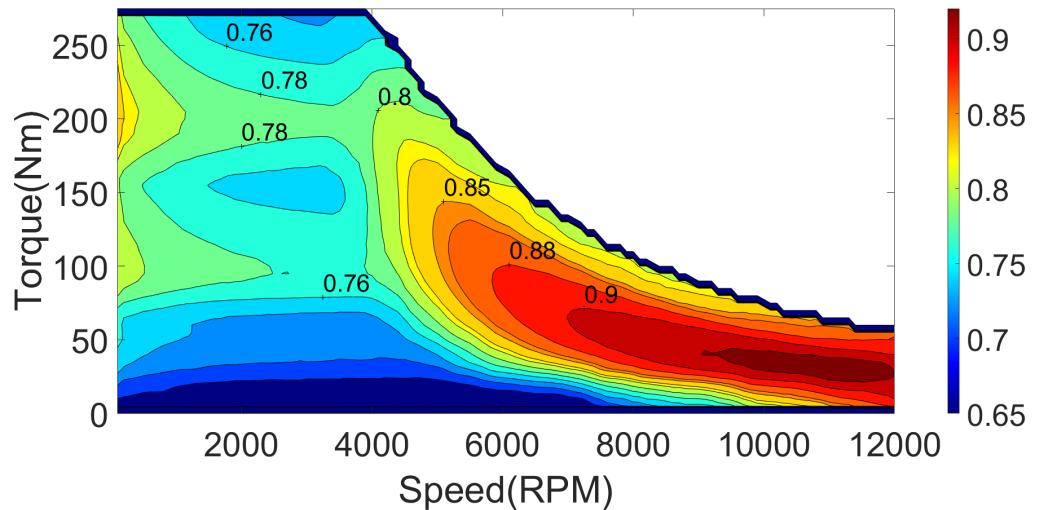
In order to decide the correct capacitor size, operating point with the maximum low frequency NPP ripple should be found on the electric machine characteristics.

To find worst case, firstly, the effect of phase current is examined. In Chapter 3, it is observed that, all PWM methods have increasing NPP ripple with increasing load current. Therefore, worst cases of all methods are expected to be in high load current regions. From the current map in Fig. 4.3a, it is observed that highest load currents are observed in high torque regions.

Secondly, the effects of m_i and fundamental frequency are investigated. All inspected

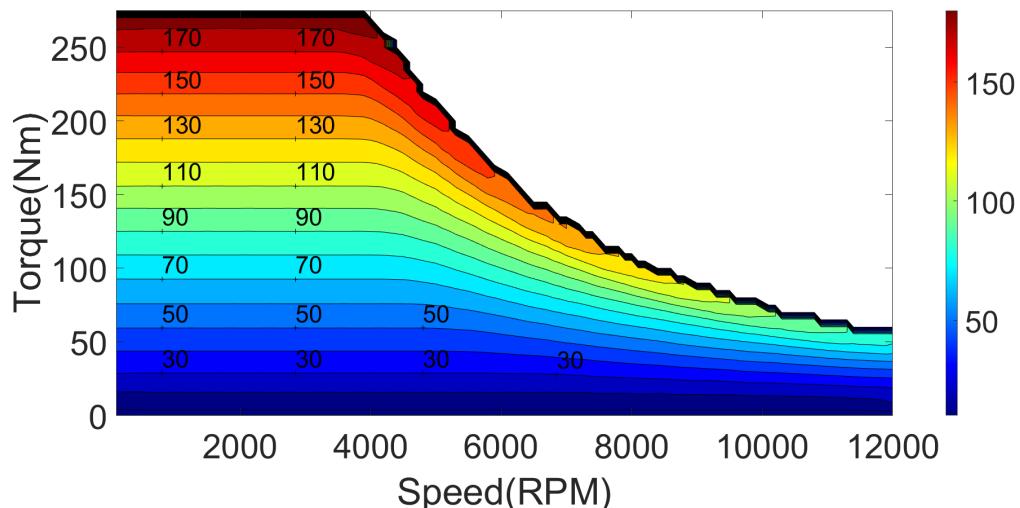


(a) Output Electromagnetic Power

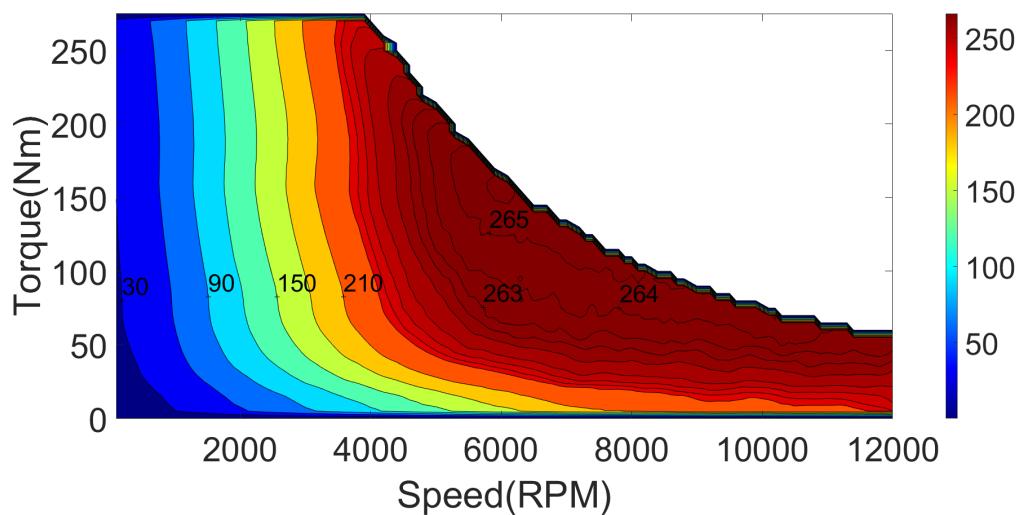


(b) Power Factor

Figure 4.2: Power and Power Factor Characteristics of the PM Assisted Synchronous Reluctance Motor



(a) Phase Current (rms)



(b) Phase Voltage (rms)

Figure 4.3: Phase Current and Voltage Characteristics of the PM Assisted Synchronous Reluctance Motor

methods except for carrier based method have a rising low frequency NPP ripple with increasing modulation index. However, at constant torque operation, increased modulation index is correlated with increased speed and consequently increased fundamental frequency which has a lowering effect on NPP ripple. Therefore, in operation regions with speed lower than base speed, 4000rpm , change in modulation index and fundamental frequency are expected to compensate for each other. On the other hand, at field weakening region, correlation between high modulation index and fundamental frequency gets weaker, where, although speed of the machine increases, modulation index is almost constant. Therefore, lower low frequency NPP ripple is expected in this region.

Thirdly, the effect of power factor is investigated. All inspected methods except for carrier based method have a rising low frequency NPP ripple with reducing power factor at operating regions with high modulation index. As can be seen in machine characteristics, regions with low torque and low speed have lowest power factor values. However, these regions should have small low frequency NPP ripple because they have considerably low load current. Next lowest power factor regions occur at high torque low speed operations. These regions are expected to have higher low frequency NPP ripple since load current is around its maximum value at these regions.

By considering these effects, several candidates for maximum low frequency NPP ripple operating point are decided. Decided points are shown with white circles in Fig. 4.2a and also provided in Table 4.3. On these operating points, NPP ripple value is obtained by using system simulation with each PWM method. The full simulation models and results are explained in following section in detail.

4.4 Full Simulation Models

Low frequency neutral point potential ripple model that is used to examine only low frequency ripple on NPP is introduced in Section 3.1. In order to investigate the effect of high frequency NPP ripple and also to verify the results of low frequency NPP ripple model, Matlab Simulink Simulation Models for each modulation technique are built. In these full simulation models, parameters given in Table 4.2 are used.

Note that, step time selected for full simulations and low frequency models is $1\mu s$. Selected switching frequency for the numeric models is either 10kHz or 20kHz. This means lowest switching period is equal to 50 times the step time. This proportion is adequate to simulate switching effects properly.

Table 4.2: Parameters Used in Simulations

Parameters	Values
DC-Link voltage, V_{DC}	800V
Modulation Index, m_i	1
Load Current, I_{RMS}	10A _{RMS}
Switching Frequency, f_{SW}	20kHz
Power Factor, $\cos(\varphi)$	0.90
Simulation Time Step	$1\mu s$
Dead Time	$2\mu s$

Full Simulation Model for SPWM

As can be seen in Fig. 4.4, this model consists of mainly three parts. These three parts are gate signal control, power circuit and ripple measurement parts. Gate signal control takes three reference sinusoidal signals, then multiplies the signals with modulation index. As the SPWM method suggests, these signals are compared with two triangular carrier waves. Output of gate signal control is twelve gate drive signals for twelve power switches of the inverter. Second part of the simulation is power circuit. This part includes an independent voltage source to represent the DC input. Two capacitors of DC-link are added and their voltages are measured.

IGBTs with diodes are used to build inverter stage as seen in Fig. 4.5. IGBT with diode block is used to obtain three-level neutral point clamped inverter. Internal resistance R_{on} is selected as $1m\Omega$, snubber resistance R_s is selected as $1k\Omega$ and snubber capacitance C_s as infinite. In order to connect the neutral point, diodes are used. Inductance of the diode L_{on} is selected as zero, On state resistance R_{on} , as $10\mu\Omega$,

forward voltage V_F is selected as $0.8V$, snubber resistance R_s as $1M\Omega$ and snubber capacitance C_s as infinite.

Output of inverter stage is connected to current measurement block. After the measurement block, RL load is connected. In order to obtain different power factor and load current parameters, resistance and inductance of the RL load are adjusted.

Full Simulation Model for SVPWM

Part that generates voltage reference signals, power circuit part and ripple measurement part are the same as SPWM full simulation model. The control part is added to apply the SVPWM method explained in Section 2.4. Figure 4.6 shows the functions used to obtain PWM signals of SVPWM method. In the first function, three phase voltage reference signals and DC-link voltage are obtained as input. By using trigonometric functions given in Table 2.6, major region number, subregion number, α and β are obtained. In the second function, output signals of first function are obtained as input and by using calculations given in Table 2.3 dwell times of the semiconductors are obtained. Then these dwell times are fed to power circuit.

Full Simulation Model for NTV Method

Part that generates voltage reference signal, power circuit part and ripple measurements part are the same as previous models. The control part is adjusted to apply NTV method explained in Section 3.1.1. Block diagram of the control algorithm of the model is provided in Fig 4.7. The first function of the algorithm is the same with SVPWM method. Then in the second function, triangle number and region number are found. Third function is used to obtain voltage reference angle and power factor that are used in function four. The fourth function finds dwell times of vectors by using space vector position information, θ and modulation index. Fifth function obtains i_X and i_Y variables according to Table 3.3. These variables represent the effect of phase currents on the neutral point current. Sixth function determines X_{s0} and X_{s1} variables. These variables are decided according to Table 3.4 and they determine which vectors are going to be used to obtain reference voltage. The last function com-

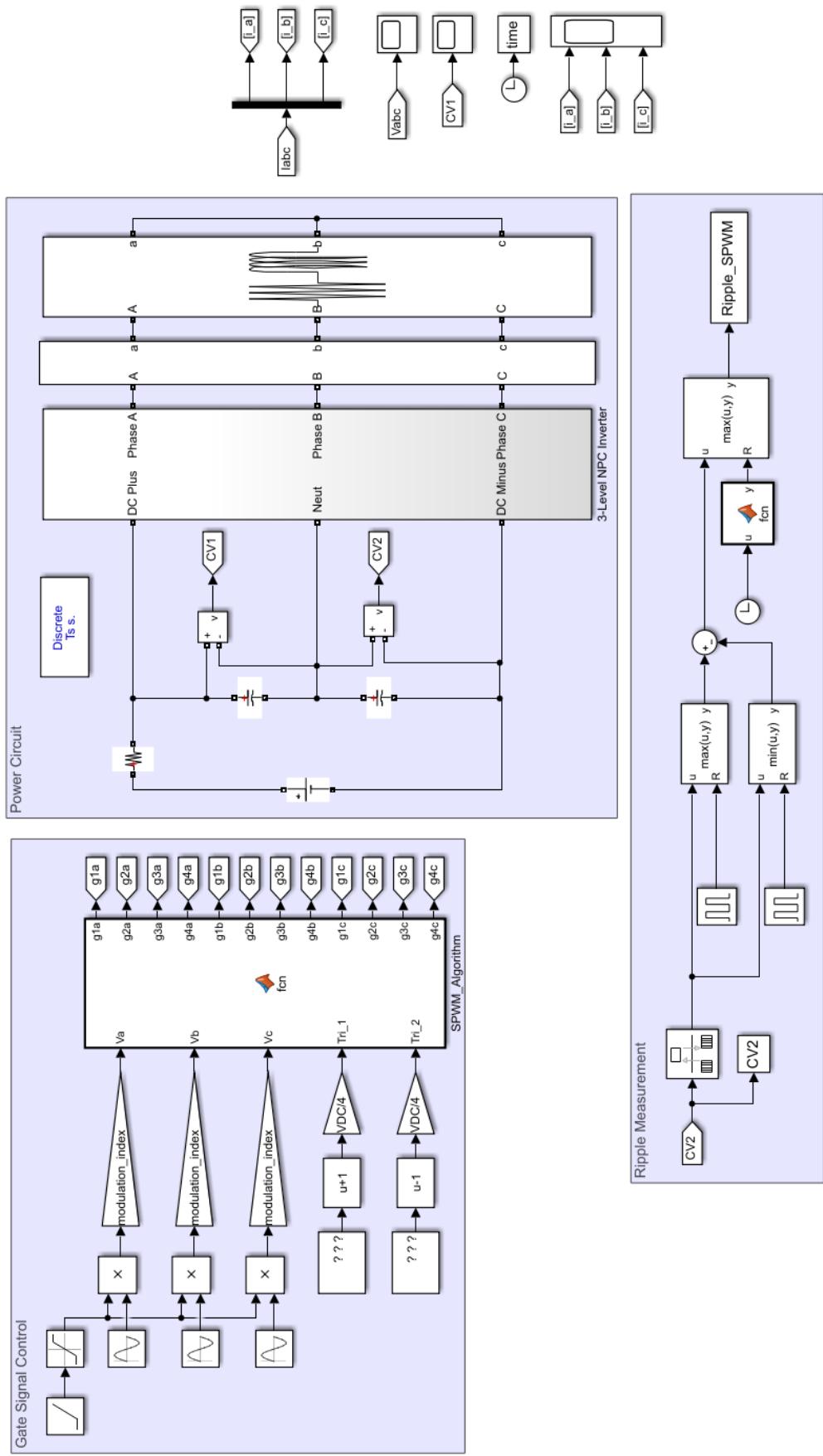


Figure 4.4: Full Simulation Model for SPWM Method

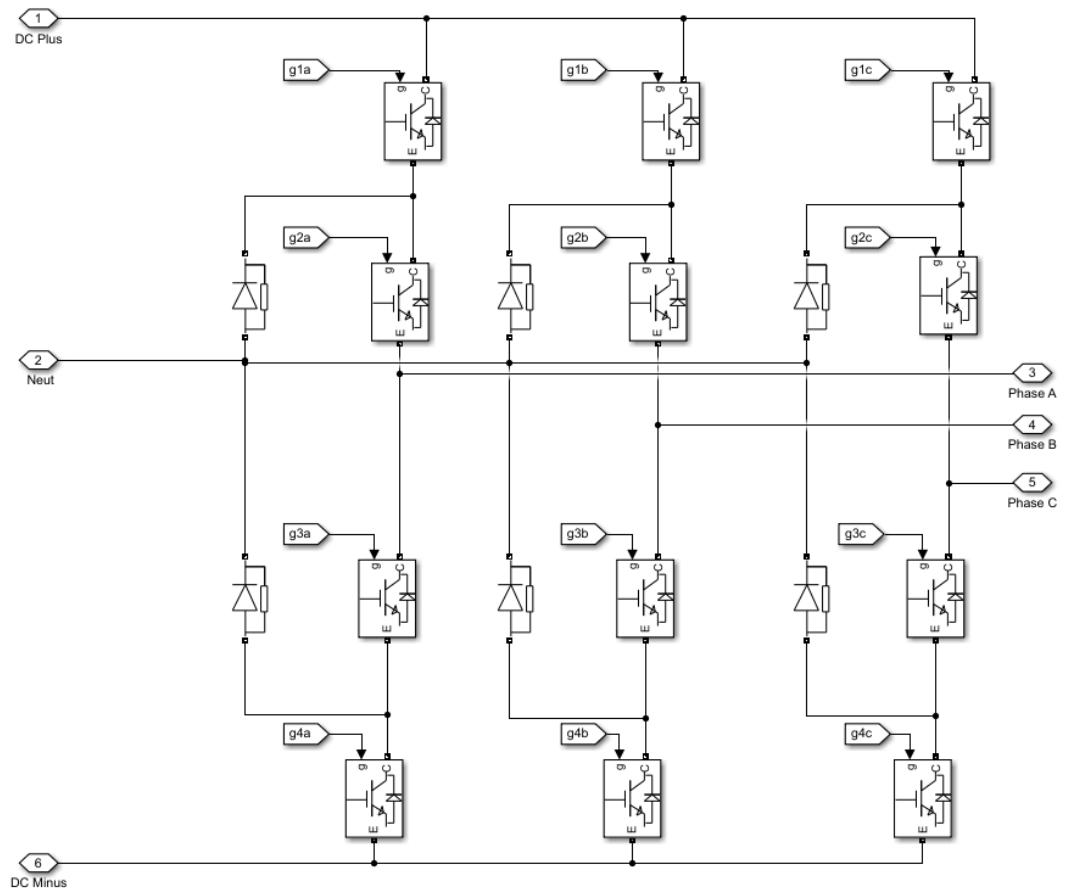


Figure 4.5: Power Switches of Full Simulation Model

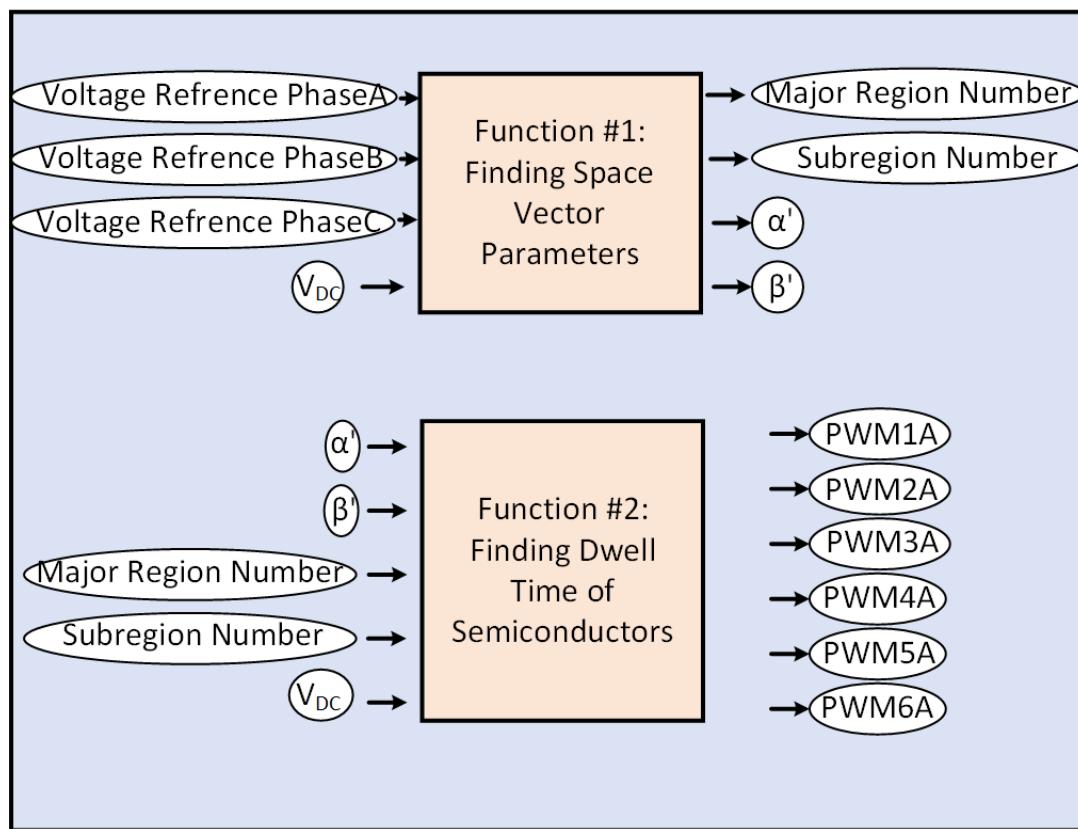


Figure 4.6: SVPWM Method Full Simulation Block Diagram

bines variables and uses a look-up table to decide on switching sequence and to find the comparison signals. The signals are then compared with triangular carrier signals and the resulting gate signals are sent to power circuit.

Full Simulation Model for Symmetrical SVPWM

Part that generates voltage reference signal, power circuit part and ripple measurements part are the same as previous models. The control part is adjusted to apply the symmetric SVPWM method explained in Section 3.1.2. Block diagram of the control algorithm of the model is provided in Fig. 4.8. First three functions are the same as NTV method. By using region number, major region number, subregion number and a look-up table spec position variable is found. Spec position explains which of the four regions represents position of the reference vector in Fig. 3.6. In order to find the x variable, a PI controller and a saturation block are applied to neutral point potential. Large triangle number is another parameter used to define the position of voltage reference vector and it is obtained from major region number and subregion number. Lastly, by using x variable, dwell times of different vectors, large triangle parameter, spec position and phase currents, comparison signals for all switches are obtained. These comparison signals are than compared with triangle carrier signal and the result is provided to power circuit.

Full Simulation Model for Carrier Based Method

The control part is adjusted to apply carrier based method explained in Section 3.1.3, other parts of the simulation model are the same with previous models. Block diagram of the control algorithm of the model is provided in Fig. 4.9. Functions in Part 1 are used to obtain u_1, u_2, u_3 and Case G from voltage reference signals according to (3.2). Case G is the variable that defines the sequence of phases according to their value. Functions in Part 2 are used to obtain $d_{11}, d_{21}, d_{31}, d_{12}, d_{22}, d_{32}$ and Δd by using u_1, u_2, u_3 and V_{NP} . In Part 3, $d_{12}, d_{22}, d_{32}, d_{31}, \Delta d$ are used to obtain comparison signals. Then these signals are compared with triangular carrier signal to obtain gate drive signals which are sent to power circuit.

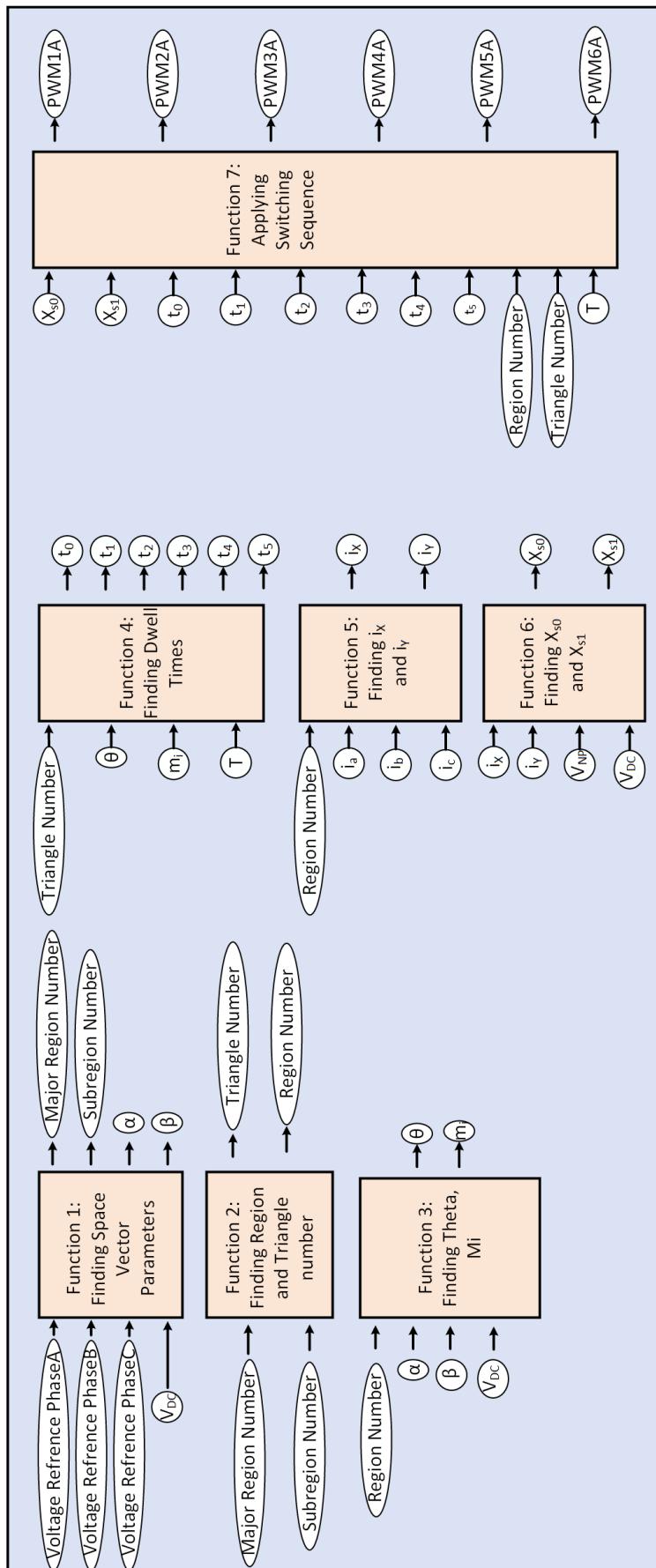


Figure 4.7: Controller Structure of NTV Method

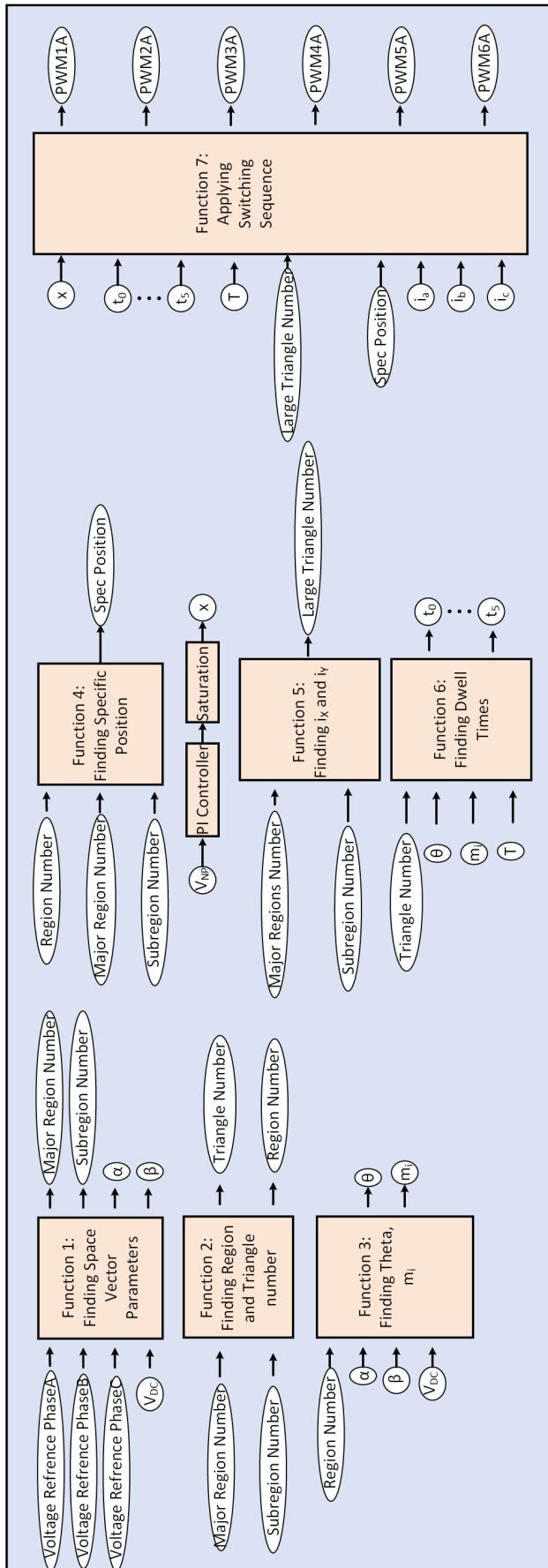


Figure 4.8: Full Simulation Model Blocks for Symmetric SVPWM Method

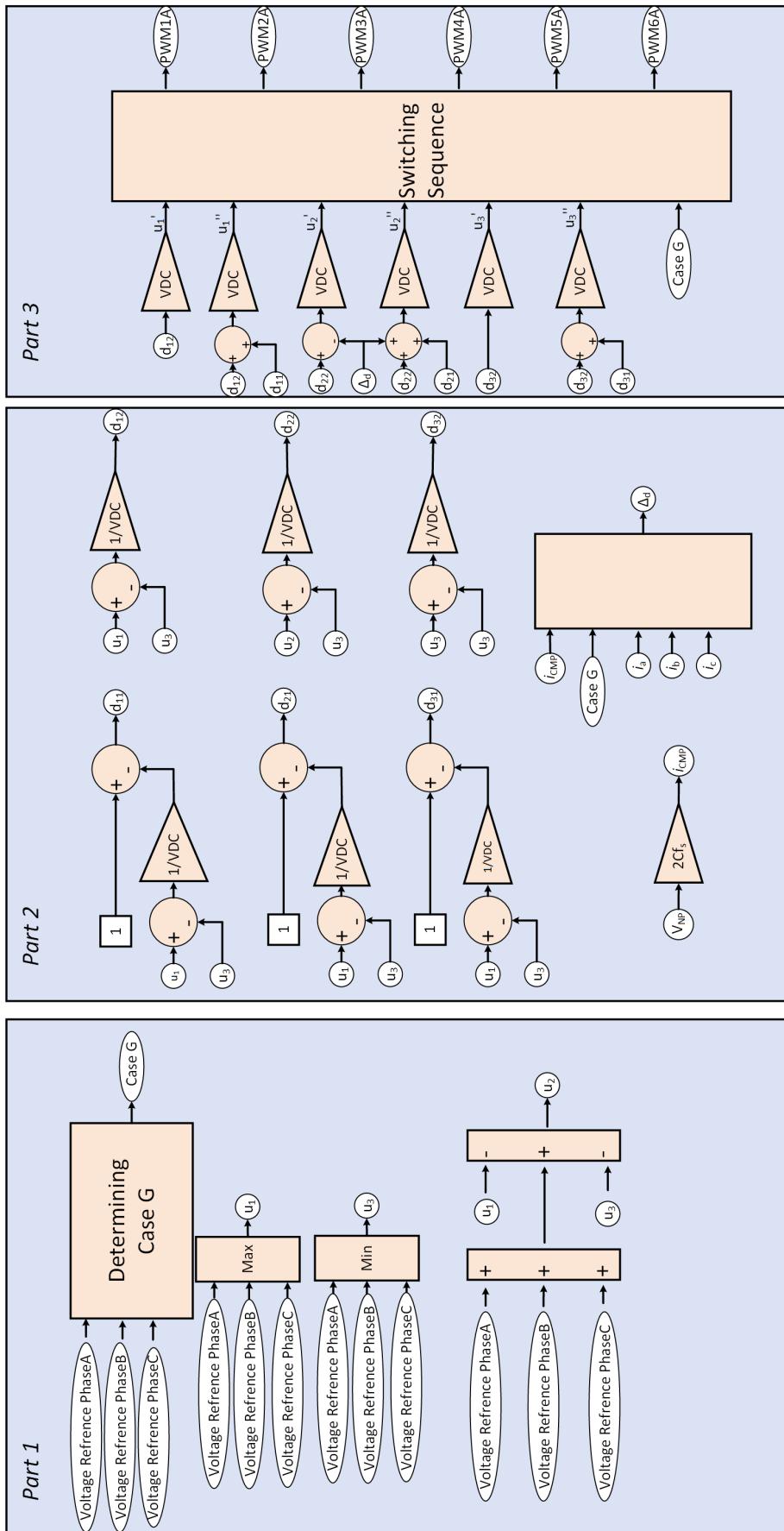


Figure 4.9: Controller Structure of Carrier Based Method

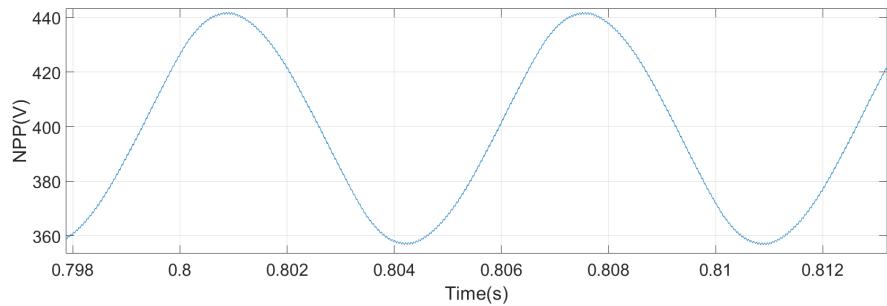
NPP ripple waveforms are examined in each simulation. Simulation conditions are specified in Table 4.2. The waveform for different methods are given in Fig. 4.10, Fig. 4.11 and Fig. 4.12. It is observed that low frequency neutral point potential ripple is dominant for all cases except for carrier based method. High frequency ripple is around 1V for all cases. For SPWM and SVPWM methods, the waveform is mostly sinusoidal. In NTV and symmetric SVPWM, there are time intervals at which low frequency NPP ripple is completely eliminated and there are time intervals in which low frequency ripple could not be eliminated, whereas in carrier based method, low frequency NPP ripple is completely eliminated.

Table 4.4 provides NPP ripple results for selected worst case operating candidates. Accordingly, worst case for SPWM method is the case number 3, for SVPWM the case number 2, for symmetric SVPWM the case number 1, for NTV the case number 5 and for carrier based method the case number 2. These worst cases for each PWM method is used at capacitor sizing section.

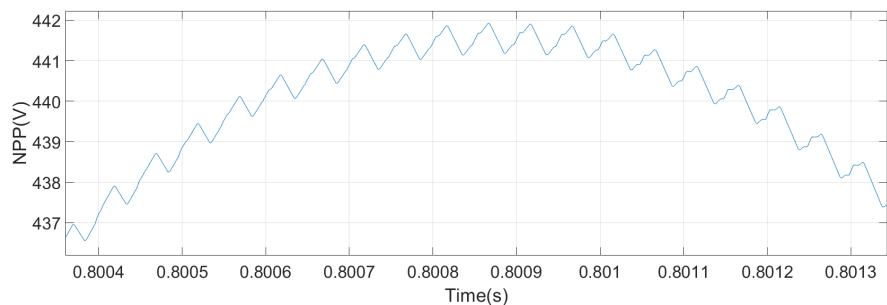
4.5 Capacitor Sizing

Purpose of capacitor sizing is to determine a capacitor with minimum capacitance that can keep the NPP ripple under desired limits. In this study, the desired limit is selected as 5% of the V_{DC} , which means peak to peak NPP ripple should not exceed 40V. Capacitor sizing is done in two steps. In the first step, low frequency NPP ripple calculation model given in Fig. 3.10 is used. Since this model does not include any real circuit component and it is a simpler model compared to alternative simulations provided in Section 4.4, this modeling takes less time than alternative simulations.

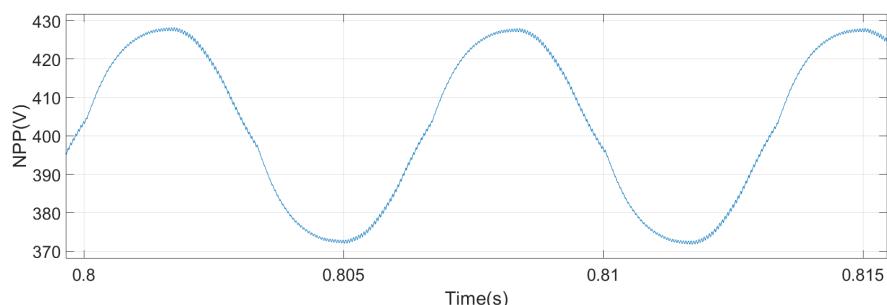
Worst cases selected in the previous sections are modelled using low frequency NPP ripple model. In order to find the correct size for the DC-link capacitor, modeling started with a very low capacitance value that is $10\mu F$. Capacitor size is adjusted first with $1mF$ steps then, $100\mu F$ steps and lastly $10\mu F$ steps until peak to peak ripple of NPP is below 5% of the total DC-link voltage. Block diagram of this algorithm is given in Fig. 4.13. If the ripple decreases below the limit value algorithm adjusts the capacitance to its previous value and continues with a smaller incremental step.



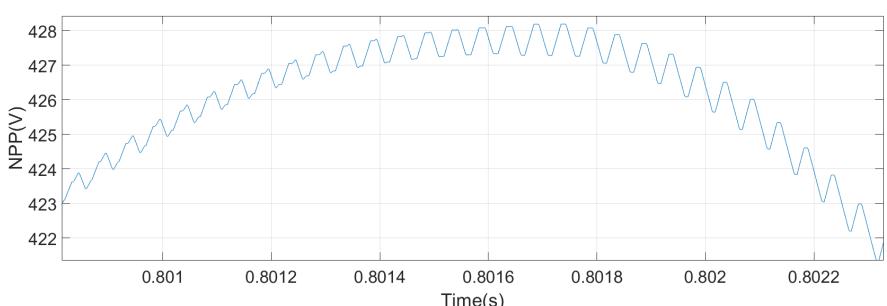
(a) SPWM Method NPP Waveform



(b) SPWM Method NPP Waveform a Closer Look

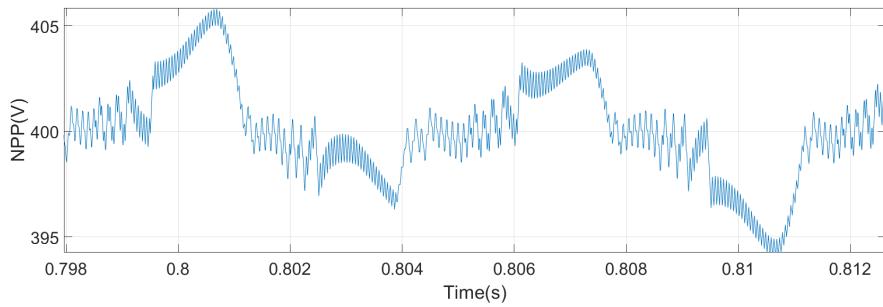


(c) SVPWM Method NPP Waveform

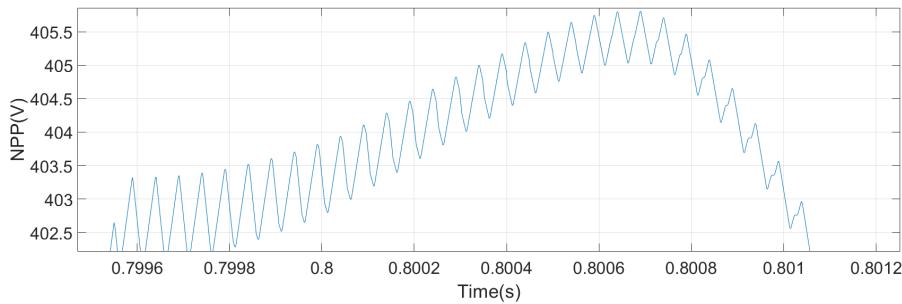


(d) SVPWM Method NPP Waveform a Closer Look

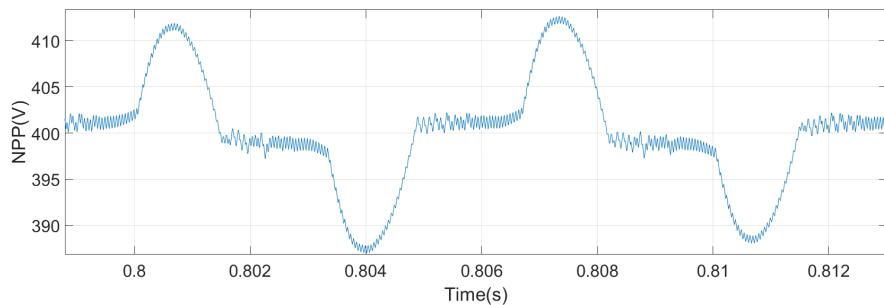
Figure 4.10: NPP Waveform of SPWM and SVPWM Methods



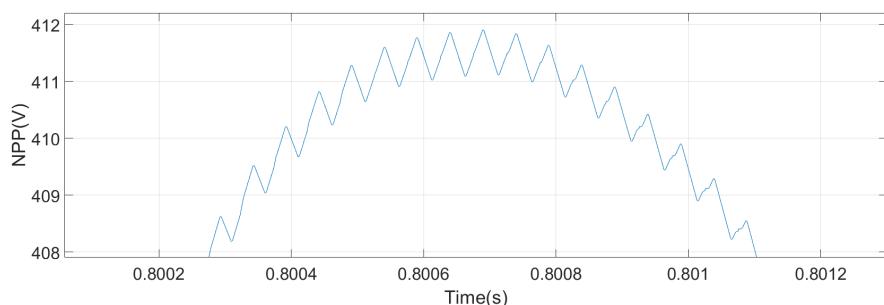
(a) NTV Method NPP Waveform



(b) NTV Method NPP Waveform a Closer Look

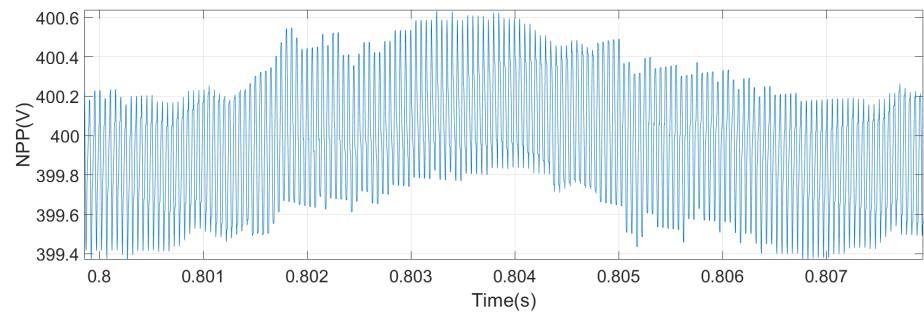


(c) Symmetric SVPWM Method NPP Waveform

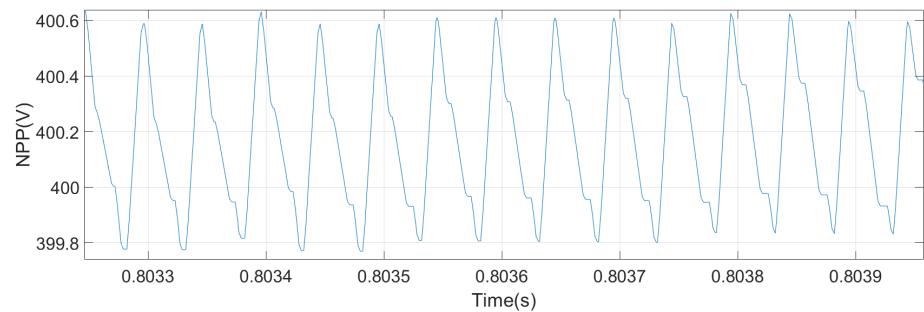


(d) Symmetric SVPWM Method NPP Waveform a Closer Look

Figure 4.11: NPP Waveform of NTV and Symmetric SVPWM Methods



(a) Carrier Based Method NPP Waveform



(b) Carrier Based Method NPP Waveform a Closer Look

Figure 4.12: NPP Waveform of Carrier Based Methods

Table 4.3: Selected Operation Points

Case No	Torque (Nm)	Speed (RPM)	f (Hz)	Current (A)	Voltage (V)	MI (%)	PF
1	270	3900	130	183.84	248.97	0.88	0.75
2	270	3000	100	182.86	213.16	0.75	0.74
3	270	2100	70	182.83	150.73	0.53	0.74
4	270	1000	33	182.89	78.85	0.28	0.76
5	250	4200	140	177.27	255.57	0.90	0.77
6	250	3000	100	172.03	210.60	0.74	0.75
7	200	5200	173	162.80	264.00	0.93	0.80
8	200	4200	140	141.67	258.70	0.91	0.81
9	200	3200	107	137.72	211.58	0.75	0.78
10	200	2200	73	137.74	146.81	0.52	0.79
11	175	5700	190	156.01	265.47	0.94	0.81
12	175	4000	133	122.14	252.15	0.89	0.80
13	175	3000	100	121.87	199.70	0.71	0.77
14	150	6300	210	144.76	265.91	0.94	0.82
15	125	7200	240	139.87	265.61	0.94	0.81
16	100	8200	273	125.85	265.22	0.94	0.82
17	50	12000	400	81.34	263.37	0.93	0.88
18	50	10100	337	72.62	263.27	0.93	0.90
19	50	8000	267	56.67	262.35	0.93	0.91
20	50	6100	203	46.33	259.66	0.92	0.85

Table 4.4: NPP Ripple for Selected Operation Points with $C_1 = C_2 = 500\mu F$

Case No	Ripple (SPWM)	Ripple (SVPWM)	Ripple (NTV)	Ripple (Sym SVPWM)	Ripple (Carrier Based)
1	123.10	88.84	28.89	56.33	4.32
2	137.08	94.83	21.71	51.85	5.56
3	143.12	88.59	15.81	47.94	5.33
4	138.00	93.63	9.24	42.06	2.76
5	115.33	80.13	32.65	55.28	4.16
6	128.45	84.77	20.36	48.96	4.97
7	85.90	60.65	32.52	44.41	3.86
8	89.26	59.38	22.21	35.02	3.70
9	94.28	63.57	15.71	33.52	3.96
10	91.97	74.44	12.62	28.69	4.25
11	75.22	56.43	28.57	39.40	3.63
12	78.92	58.50	17.01	33.32	2.91
13	84.81	54.31	13.70	29.92	3.83
14	64.97	45.79	24.30	32.98	3.42
15	53.28	37.84	22.92	32.52	3.26
16	43.50	30.20	19.82	25.76	2.77
17	18.36	15.32	9.49	10.20	1.92
18	19.92	14.79	8.53	9.69	1.93
19	17.97	13.73	6.62	6.48	1.17
20	19.49	13.51	5.96	6.98	1.18

Selected capacitor size for each PWM method with low frequency neutral point potential is given in Table 4.5. Note that carrier based method has no result for low frequency capacitor sizing. This is because theoretically, carrier based method has always zero low frequency NPP ripple. It is observed that required DC-link capacitance value to keep the NPP ripple in the desired limits is higher in PWM methods without NPP control. Between NTV and symmetric SVPWM methods, symmetric SVPWM needs larger DC-link capacitance because it has more constraints on small vector selection compared NTV method.

Results given in the first column of Table 4.5 considers only low frequency NPP ripple. However, NPP ripple contains both low frequency and high frequency components. Since the frequency of high frequency ripple exceeds the control bandwidth of the controller, the PWM methods do not aim to control this ripple type. In order to examine the effects of high frequency NPP ripple, full simulation models explained in previous section are used. In this part, initial capacitor values are obtained from the first column of Table 4.5 since these should be the minimum DC-link capacitance values. Similar to low frequency case, capacitance value is adjusted with steps, where first $1mF$ steps, and then $100\mu F$ steps and, then $10\mu F$ steps are used. The results are provided in the second column of Table 4.5.

All inspected PWM methods except for carrier based method are expected to have a dominant low frequency NPP ripple, which means most of the NPP ripple is caused by the low frequency component. Due to this reason, final capacitance values are expected to be close to the values in first column of Table 4.5. This expectation holds for SPWM and SVPWM cases. However, in NTV and symmetric SVPWM cases, performance of NPP ripple control is reduced due to high frequency ripple component on the NPP. Therefore, larger capacitors are needed for NTV and symmetric SVPWM cases. Carrier based method requires the smallest DC-link capacitor among all PWM methods; but, this benefit comes with a cost of lower efficiency [28].

One important outcome of analysis in this section is that the NPP voltage measurement and control loops must be designed carefully.

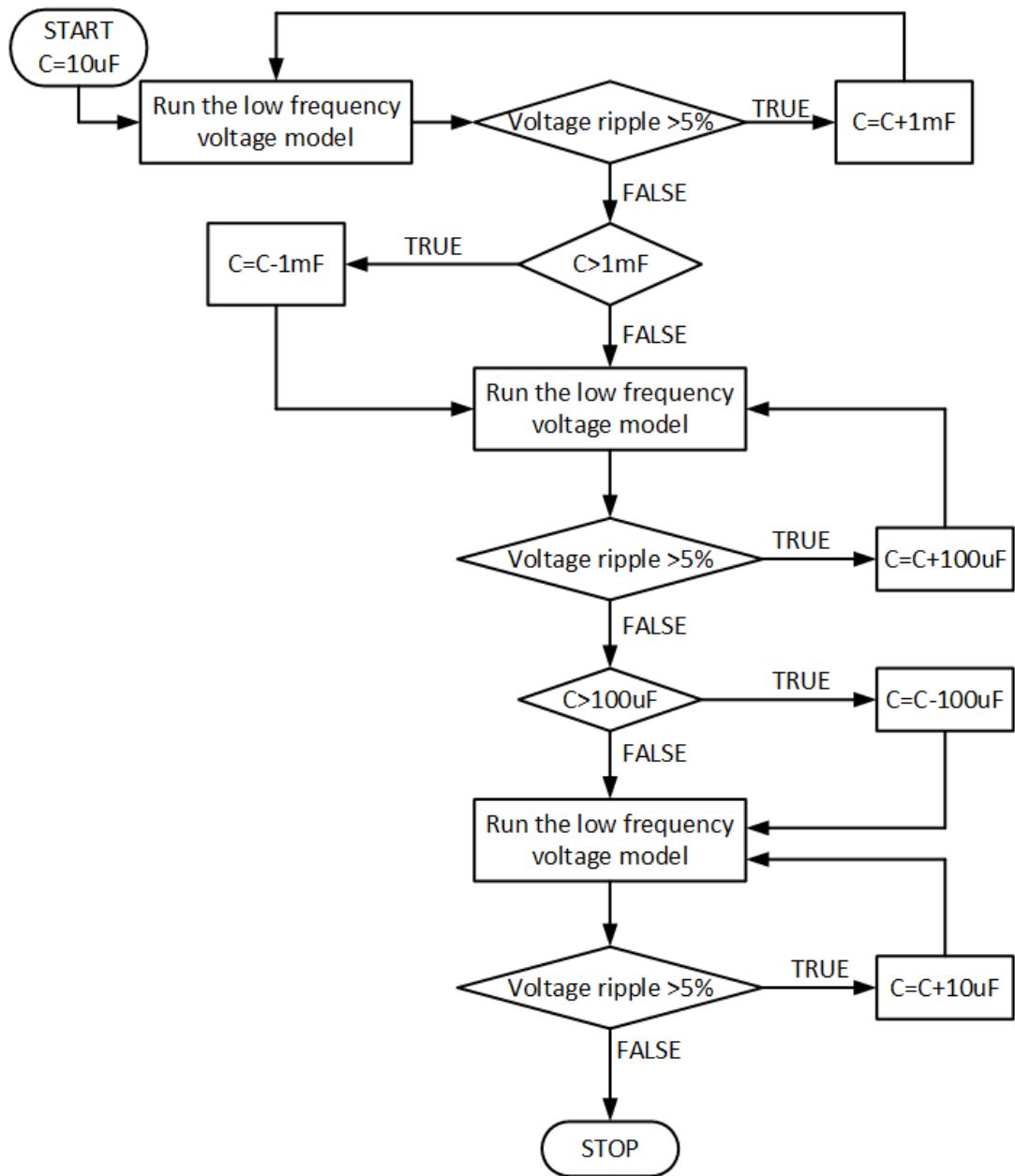


Figure 4.13: Capacitor Sizing Algorithm Low Frequency NPP Part

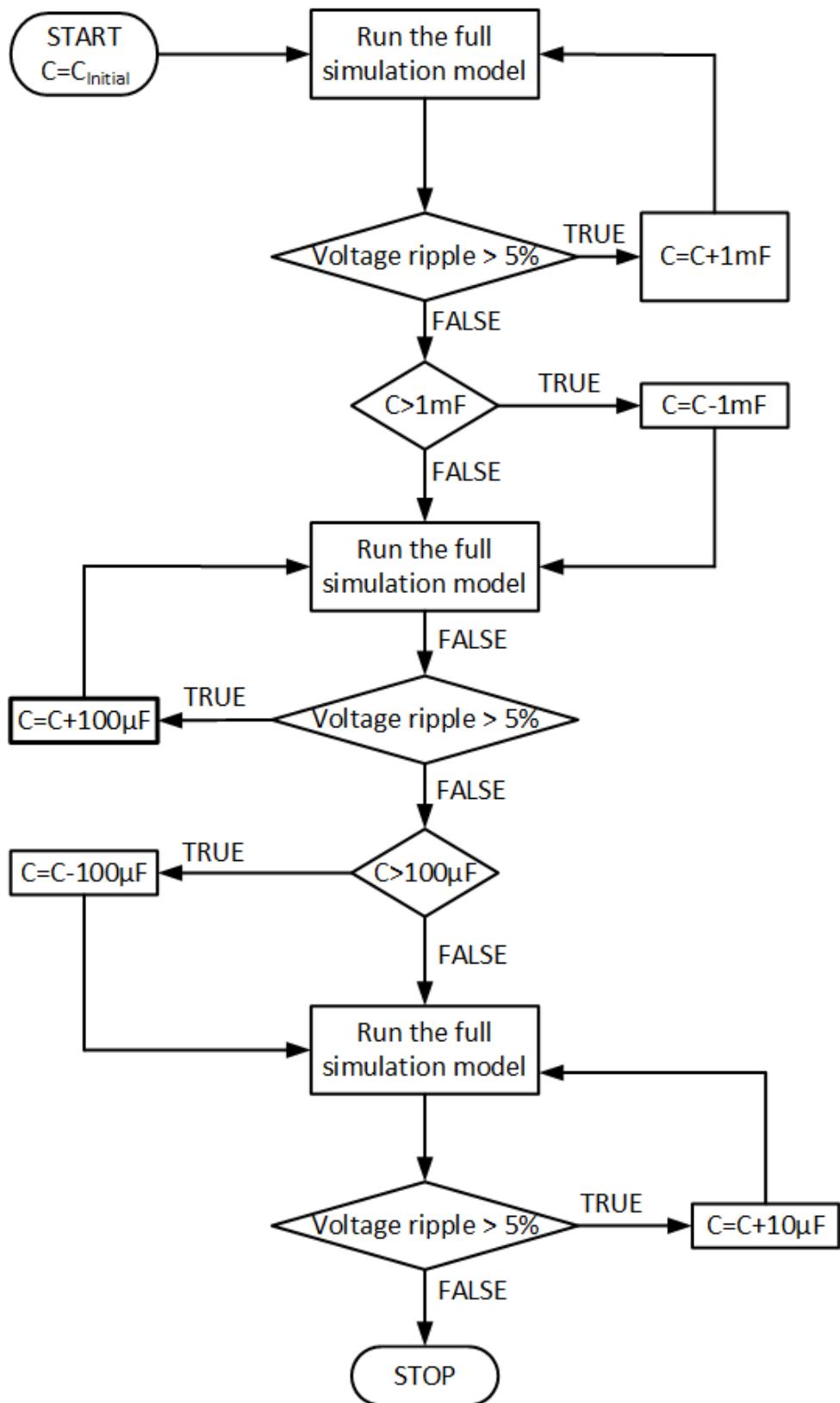


Figure 4.14: Capacitor Sizing Algorithm High Frequency NPP Part

Table 4.5: Capacitor Sizing Results for One DC-link Capacitor

PWM Method	Low Frequency	Final
SPWM	1.7mF	1.7mF
SVPWM	1.0mF	1.2mF
NTV	$120\mu F$	$340\mu F$
Symmetric SVPWM	$460\mu F$	$670\mu F$
Carrier Based Method	NA	$70\mu F$

4.6 Comparison with Two-Level VSI Case

Capacitor size is obtained for three-level NPC inverter. For comparison, two-level VSI counterpart of the same system is examined. In two-level VSI system, limitation of capacitor size is due to capacitor voltage ripple. If the ripple increases, this may damage the components. Simulation model for two-level VSI is built and provided in Fig. 4.15. In this model, SPWM control method is used as the PWM method. Power circuit has an high inductance between independent DC source and DC-link capacitor. This component is added to observe DC-link voltage ripple under constant input current. Parameters of the model are provided in Table 4.6. Same capacitor selection algorithm was used as the three-level NPC inverter.

Table 4.6: Two-Level VSI Simulation Model Parameters

Parameter	Value
DC-Link Voltage	800V
Modulation Index	0.9
Load Current	$182A_{RMS}$
Power Factor	0.74
Fundamental Frequency	100Hz
Simulation Time Step	$1\mu s$

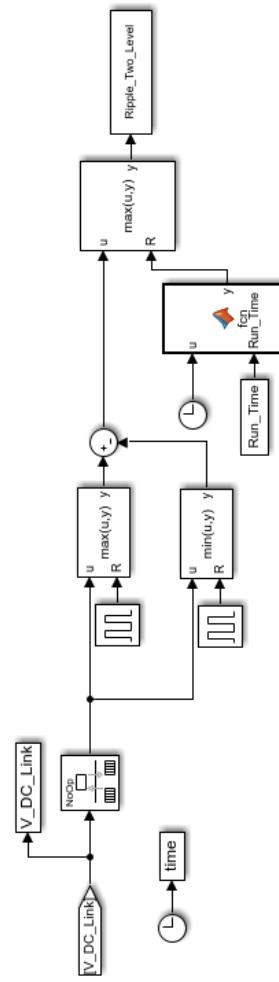
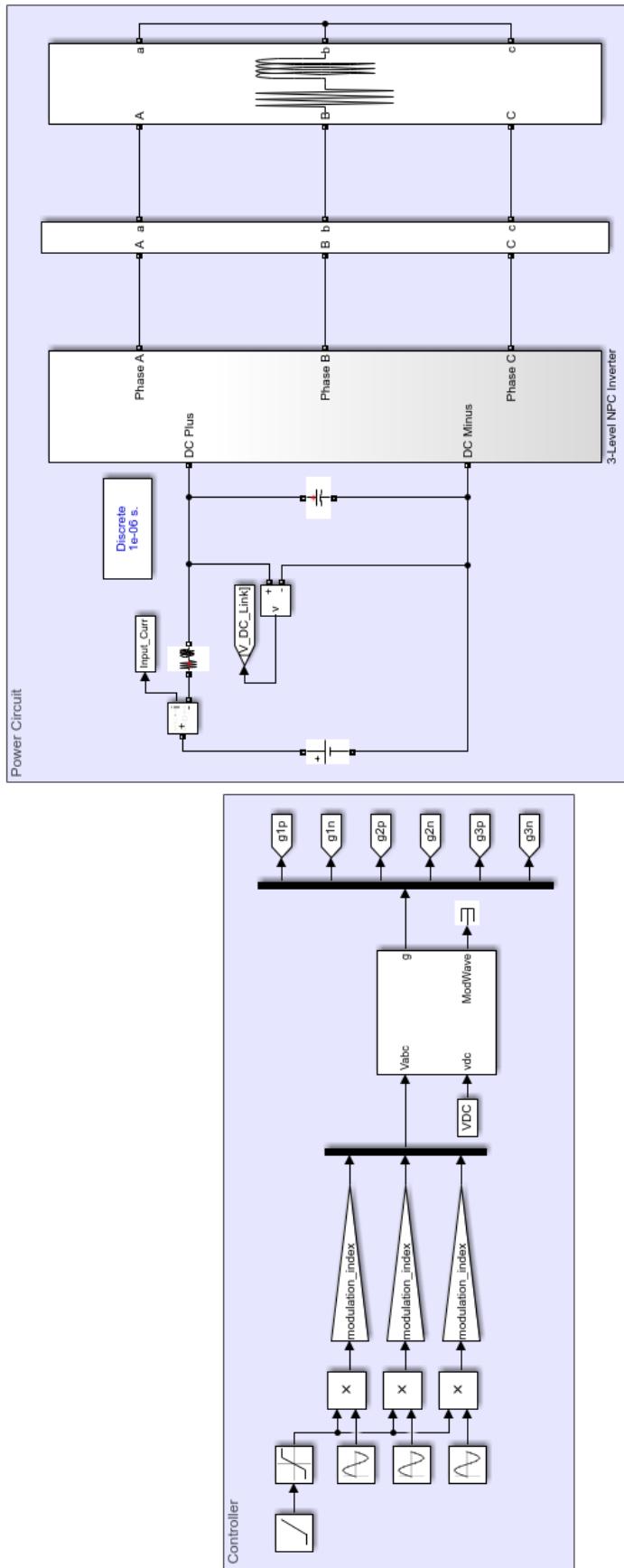
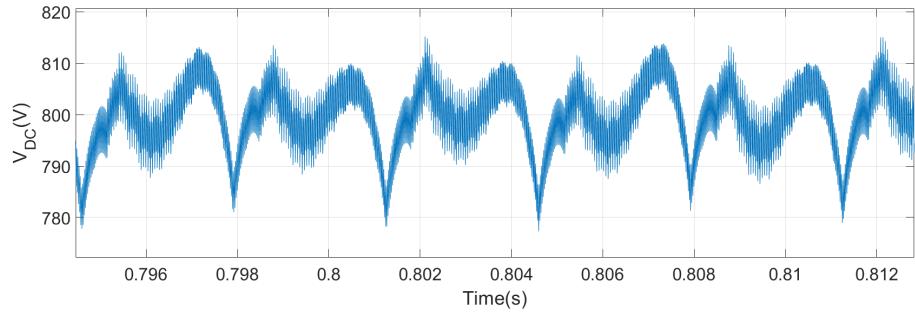
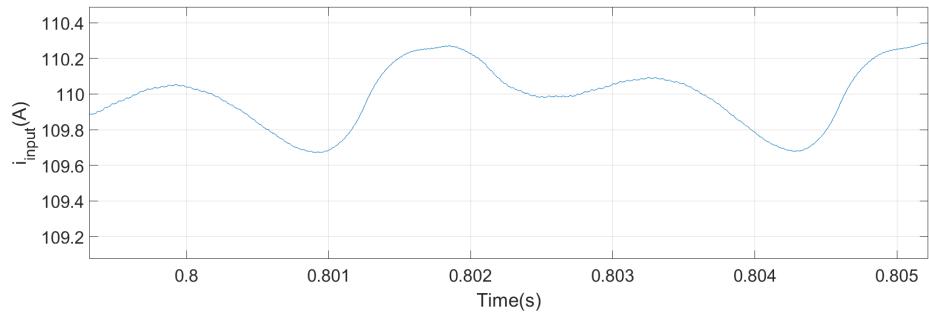


Figure 4.15: Two-Level VSI Simulation Model



(a) Two-Level VSI DC-Link Voltage



(b) Two-Level VSI Input Current

Figure 4.16: Input Current and DC-link Voltage Waveform of Two-Level VSI

Selected capacitor is $120\mu F$. Input current waveform of the simulation is provided in Fig. 4.16b and DC-link voltage waveform of the simulation is provided in Fig. 4.16a.

It is observed that, required DC-link capacitor is larger in three level NPC inverter case.

Chapter Summary

In this chapter, characteristics of the drive system is introduced. Possible operating conditions for highest NPP ripple are determined. Full simulation models that can simulate both low frequency and high frequency NPP ripple are introduced. By using full simulation models and possible operating conditions for highest NPP ripple, operating points with maximum NPP ripple are obtained for each PWM method. Then, capacitor sizing for each PWM method is done first considering only low frequency

NPP ripple. Later, high frequency NPP ripple is also taken into consideration by using full simulation models; therefore, capacitor selection is finalized. Lastly, capacitor size of three-level NPC inverter is briefly compared to capacitor size of two-level VSI.

CHAPTER 5

EXPERIMENTAL VERIFICATION

To test the analytical and numeric results of previous chapters a 1kVA three-level neutral point clamped inverter is designed and NPP is observed under different operating conditions. In this chapter experimental setup and experimental results are presented. The measured NPP waveforms are compared with the simulation results to show the validity of the numeric analysis.

In the experiment, $380V_{DC}$ input voltage is inverted into a three phase AC output voltage with varying frequency and amplitude. The inverter is loaded by various RL type loads to imitate motor driving conditions. In order to obtain different operating conditions, inductance and resistance of RL loads are changed in each case. Block diagram and the photo of the experimental setup are presented in Fig. 5.1 and Fig. 5.2, respectively.

There are several equipment used on the experiment to make measurements and provide power. DC input of the inverter is provided with Keysight RP7972A Regenerative Power System which is able to provide stable DC voltage up to 1000V with 60A [43]. Figure 5.4a shows the power supply.

Waveform measurements of neutral point potential, output current and output voltage are obtained with digital oscilloscope LeCroy Waverunner 6050A shown in Fig. 5.4b [44].

Control circuit of the PCB is supplied with Gw Insteck GPS-3303 which is shown in Fig. 5.4e [45].

Loading of the PCB circuit is done with passive RL loads. Resistor part of the load

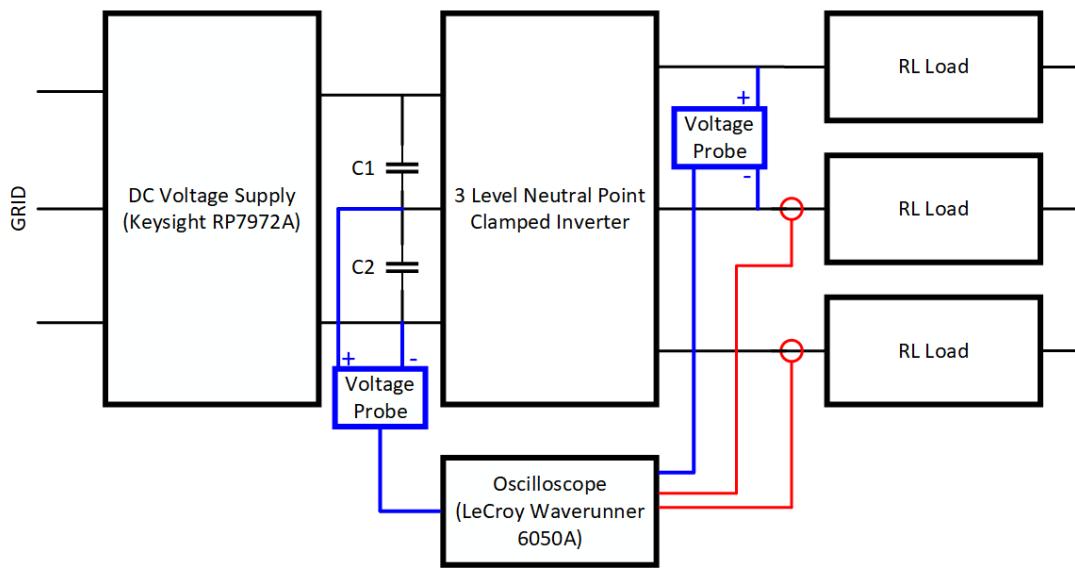


Figure 5.1: Block Diagram of the Experimental Setup

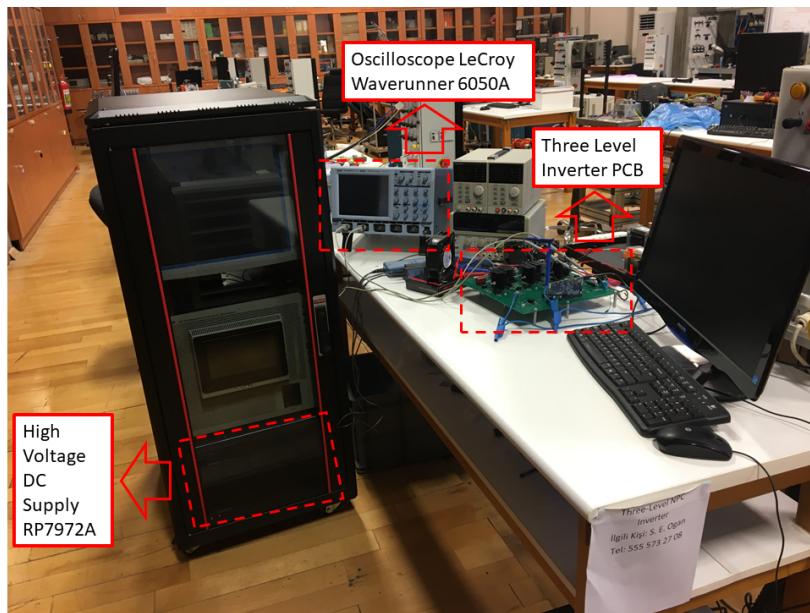


Figure 5.2: Experimental Setup

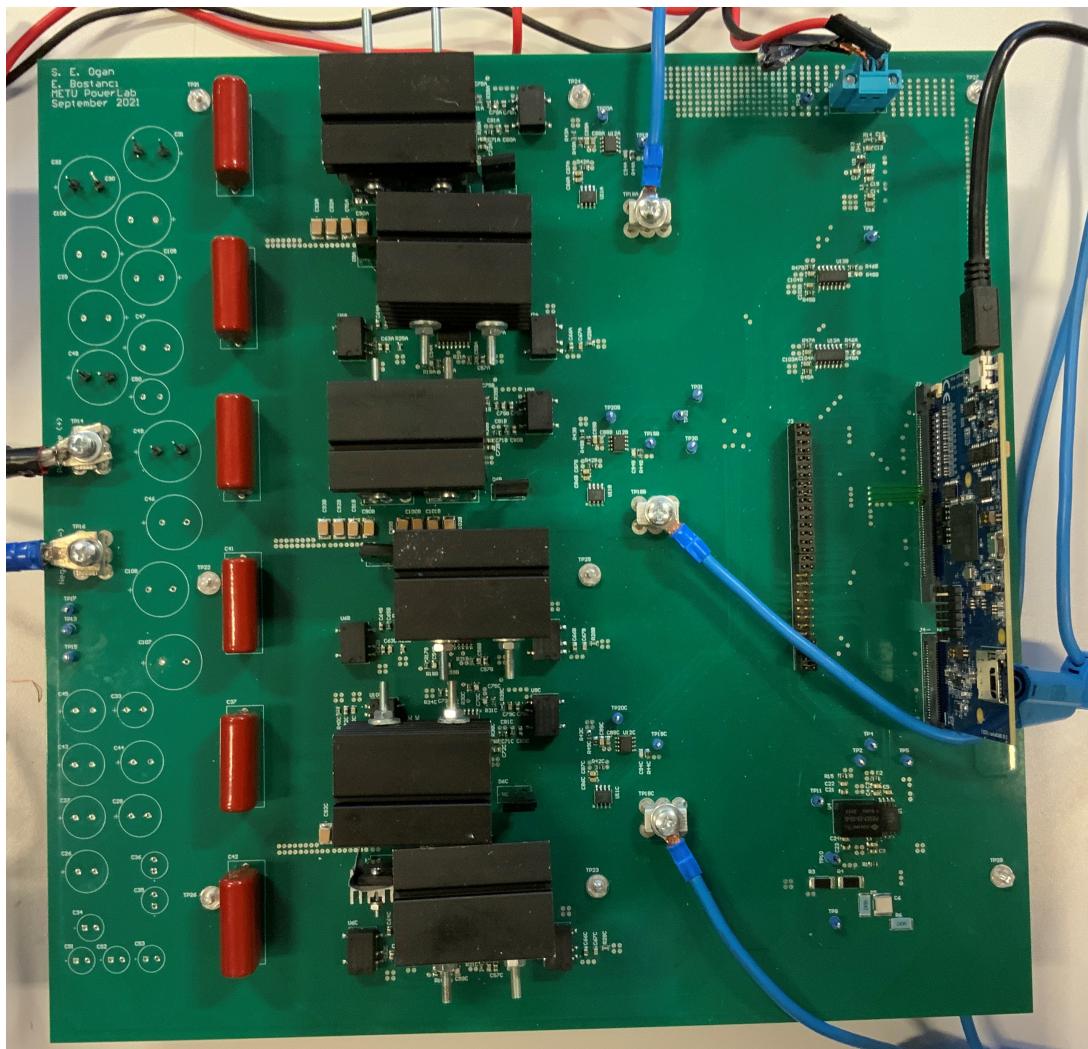


Figure 5.3: Prototype 1 kVA Three-Level Neutral Point Clamped Inverter

is three rheostats with varying resistance. Rheostats are shown in Fig. 5.4c. Inductor part of the load, is obtained with varying inductors shown in Fig. 5.4d.

5.1 Prototype Three-Level NPC Inverter

In the experiment, relationships between NPP ripple, PWM method, modulation index, load current and fundamental frequency are investigated. For this reason, a 1 kVA three-level NPC inverter is designed. This is a downscaled version of the driver investigated in the Chap 4. In the downscaled version, DC-link voltage is decreased from $800V_{DC}$ to $400V_{DC}$ and output voltages are halved. Load current is decreased from $250A_{peak}$ to $3A_{RMS}$. Original version of the driver would have more design concerns due to higher parasitic and EMI/EMC effects. However, although the design of initial drive system and downscaled drive system are different from each other due to rated power difference, the downscaled system is adequate to investigate the relationship between NPP ripple and other parameters. Hence, the experimental setup can be used to make proof of concept for results obtained in the previous chapters. A top view photo of the prototype is shown in Fig. 5.3. Basic design parameters of the prototyped three-level NPC inverter are given in Table 5.1. The components of the prototype are briefly discussed in the following text.

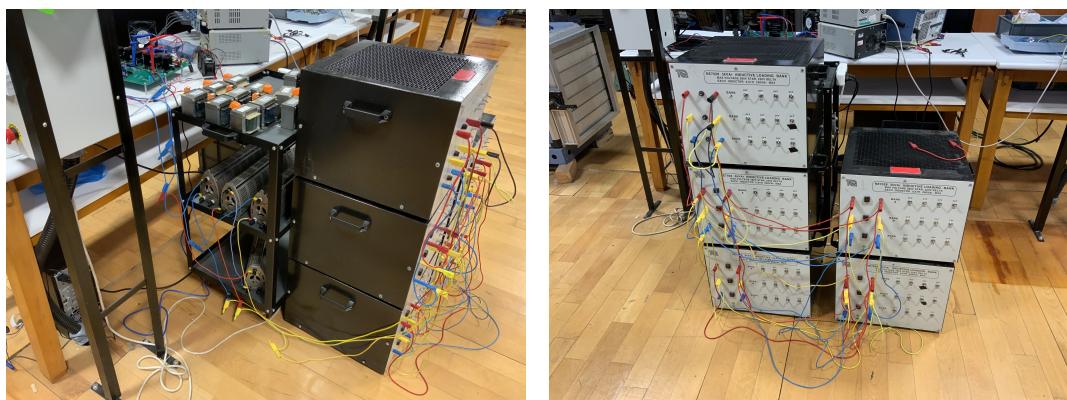
Table 5.1: Specifications of the Three-Level Neutral Point Clamped Inverter

Parameters	Values
Maximum Input Voltage	$400V_{DC}$
Maximum Line Current	$3A_{RMS}$
Rated Apparent Power	$1kVA$
Switching Frequency	$10kHz$



(a) Keysight RP7972A [43]

(b) LeCroy Waverunner 6050A [44]



(c) Load Rheostats

(d) Load Inductors



(e) Low Voltage DC Supply

Figure 5.4: Equipment of the Experiment

Power Switch and Diodes

An N-channel MOSFET with a device ID of IXTH30N60P [46] is selected. MOSFETs are preferred because of high switching speed and simple drive system. Main parameters of the switch is provided in Table 5.2.

Table 5.2: Specifications of Power MOSFET

Parameters	Values
Drain to Source Voltage, V_{dss}	600V
Continuous Drain Current	30A
Drive Voltage	10V
Package Type	TO – 247
Maximum Junction Temperature	150°C

Power diodes selected for the design are SCS208AMC, which is a Silicon Carbide Schottky diode with no reverse recovery time; therefore, allows fast switching [47]. Main parameters of the diode are provided in Table 5.3.

Table 5.3: Specifications of Power Diode

Parameters	Values
DC Reverse Voltage, V_r	650V
Average Rectified Current, I_o	8A
Package Type	TO – 220

Gate Drive System

Gate drive system of the MOSFETs contains isolated gate drivers and isolated voltage supplies. The system uses 1W isolated DC-DC voltage supply PDS1-S5-S12-M-TR, which can provide 12V DC voltage output with 5V DC input [48]. SI8275GB-IS1R gate drivers from Skyworks are used [49]. Each gate driver drives two power switches

and each isolated power supply drives one power switch. As a result, 12 isolated DC supplies and 6 gate driver integrated circuits are used in the PCB. Block diagram of the gate drive circuit is provided in Fig 5.5.

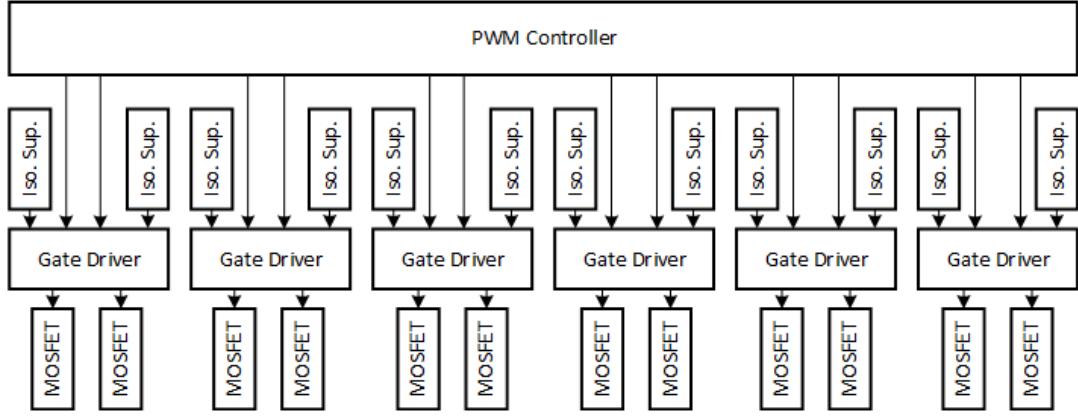


Figure 5.5: Power Switch Gate Drive Block Diagram

Voltage Sensing System

There are two voltage sensors on the PCB. The first one measures the voltage difference between neutral point and negative input of the input DC voltage. The other sensor measures the input DC voltage of the inverter. Two sensors have a similar structure. Firstly, voltage is divided by resistors. Then isolation amplifier AMC1301 is used to galvanically isolate high voltage and low voltage sides of the circuit [50]. The measurements are obtained separately.

Current Sensing System

Since the algorithms use output current to make NPP control, three phase currents are measured on the PCB. TMCS1101A4BQDRQ1 current sensor integrated circuit is used to measure the current. This is a one channel hall effect sensor [51]. Then, the output of sensor is connected to integrated circuit TSA7887BRZ that is an Analog to Digital converter [52]. The integrated circuit is placed near to the current sensor. By this method, signal is transferred in digital format to increase the immunity against noise. A Single Serial Peripheral Interface (SPI) communication hardware was used

to communicate with all three current sensing systems. Figure 5.6 shows the connection of SPI communication.

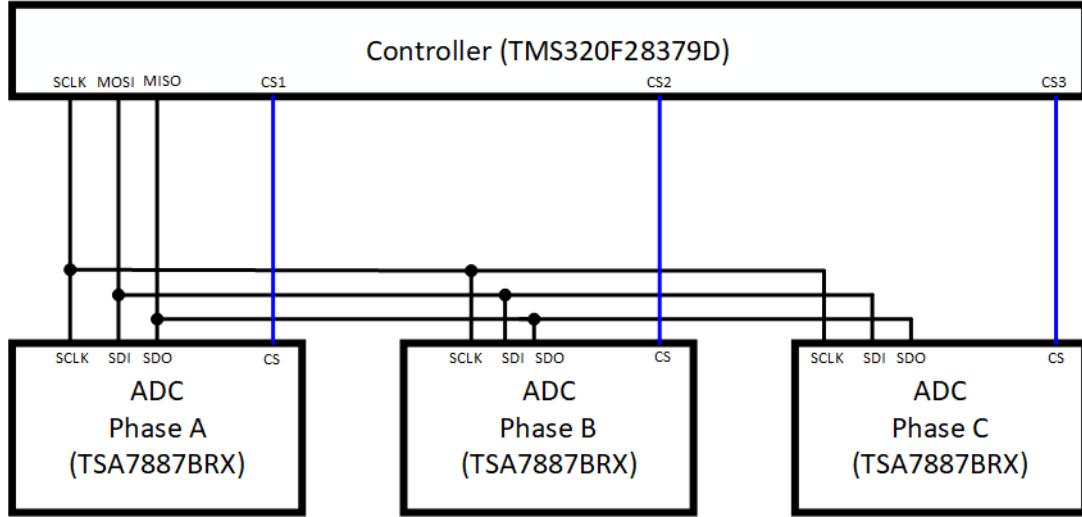


Figure 5.6: SPI Connection Block Diagram

5.1.1 Digital Controller

In order to sense current and voltage, run the control algorithm and generate the PWM signals, a digital signal processor is used. The processor TMS320F28379D [53] is selected and used on a control card TMDSCNCD28379D [54] to ease the connection of ADCs, PWMs and communication interfaces. A photo of the control card is shown in Fig. 5.7.



Figure 5.7: Digital Control Card (TMDSCNCD28379D)[54]

Programming of the DSP is done on Code Composer Studio environment using C programming language. After debugging of the code, the code was uploaded to RAM or FLASH memory of the DSP. Uploading is done by using the emulator that is integrated on the control card. One of the PWM algorithms was uploaded on the RAM; however, for other algorithms, there were long functions which consumes a lot of memory. Therefore, other three algorithms were uploaded to FLASH memory of the DSP.

In order to run the algorithms in 10kHz frequency, Timer module of the DSP is used. This module uses system clock of DSP to make interrupts at every $100\mu s$. Code is programmed so that after initialization of all modules and variables, every Timer interrupt triggers algorithm to run one time and change the duty cycle of PWM modules.

ADC module of the DSP is used to measure DC-link voltage and neutral point voltage. The module receives a trigger from the Timer module in every $100\mu s$. The module obtains a differential signal and converts the signal into 16 bit digital signal.

PWM module of the DSP is used to control the gate drivers. The module has a counter working with 50MHz frequency. The counter is programmed to count until 2500 and then count back to zero. Control algorithm of the DSP provides a compare value to the PWM module. Then the compare value is compared with counter of PWM module. If the compare value is higher than counter, then output pin of the PWM module is set high. If the compare value is lower than counter, then output pin of the PWM module is set low. Advantage of PWM module is being able to operate PWMs independent of the DSP.

Serial peripheral interface module of the DSP is used to set communication with current sensors. Serial peripheral interface is a short distance communication protocol developed by Motorola. Four pins are used in this protocol. One device on the communication line should be set up as a master and other devices should be set up as slaves. In this study DSP on the control card is programmed to behave as a master and integrated ADC circuit of the current sensor is programmed as a slave. Since there are three current sensors, there are three slaves on the communication line. DSP is communicating with three slaves one by one. In every $100\mu s$, DSP is communi-

cating with the next slave. By following this pattern, DSP is obtaining every current measurement in ever $300\mu s$

5.1.2 DC-Link Capacitors

Three different capacitor types are used in the DC-link. Ceramic capacitors are placed closest to the switches so that high frequency signals are exposed to ceramic capacitors with minimum distance. Then after approximately 60-70 mm distance, film capacitors are added. Then after approximately 80-100 mm, electrolytic capacitors are added. Electrolytic capacitors are best working with low frequency signals.

5.1.3 Isolation

Low voltage control part of the circuit is isolated from the high voltage power part. This isolation is important as high voltage switching causes reduced signal quality on the control part. This reduced signal quality decreases the accuracy of the sensors, interrupts communication lines and may cause undesired turn ons or turn offs of the power semiconductor switches.

Isolation is achieved by removing conductive layers between control parts and high power parts of the PCB. Connection between control parts and high power parts are only made with isolated integrated circuits. There are four different components with isolation on the PCB that are the gate driver integrated circuit, the voltage supplies of the gate drivers, the hall effect current sensor and the isolated voltage sensors.

5.2 Thermal Design

Thermal design is carried out to ensure the successful operation of the inverter. Main power loss of the inverter occurs on power MOSFETs and power diodes. Therefore, these losses are considered for thermal design.

There are two main types of losses affecting MOSFETs. First is the conduction loss. This type of loss occurs when the MOSFET is turned on and conducting cur-

rent. Turned on MOSFET has a conducting channel between drain and source. The channel has an electrical resistance. This resistance is named drain-source on resistance $R_{DS(on)}$. The resistance depends on voltage and current ratings of the device. Moreover, resistance increases with increasing temperature due to reduced electron and hole mobility of the conduction channel. Conduction loss is proportional with $R_{DS(on)}$ and square of on time current. Its expression is provided in (5.1) [55].

$$P_{con} = R_{DS(ON)} I_{QSW(RMS)}^2 \quad (5.1)$$

The other main loss of the MOSFET is switching loss. When a MOSFET is turned on or turned off, switching does not occur instantly. Instead, certain amount of time is necessary to completely form up or eliminate the conductive channel. While forming the conductive channel up, voltage on the device will gradually decrease and current flowing through the device will gradually rise up. This coexistence of voltage and current causes a loss known as switching loss. Switching loss of the MOSFET occurs both at turn on and at turn off. Therefore, it is proportional to the number of switching in a unit amount of time; in other words, switching frequency. It is also proportional to off time voltage and on time conduction current of the MOSFET. Lastly, the loss is proportional with turn on and turn off time of the MOSFET. Switching loss expression is provided in (5.2). Variable V_{MOS} is the voltage on the MOSFET, I_{MOS} is the current of the MOSFET, f_{sw} is the switching frequency, Q_{GS} is the gate source charge, Q_{GD} is the gate drain charge and I_G is the gate current.

$$P_{sw} = V_{MOS} I_{MOS} f_{sw} \frac{(Q_{GS} + Q_{GD})}{I_G} \quad (5.2)$$

Power diode used in the design is SCS208AM which is a SiC Schottky Barrier Diode. This diode causes forward conduction loss. When diode is turned on, there is a voltage drop on its junction. The junction voltage is expressed in two parts. One part is constant and does not change with current flowing through the diode. This part of voltage is expressed with V_{T0} . Other part of voltage depends on current flowing through the diode; in other words, forward current. Proportion of this voltage type to

forward current is shown with dynamic resistance which is denoted with R_D . Overall, forward characteristic of the diode voltage is given in (5.3).

$$V_F = V_{T0} + R_D I_{F1} \quad (5.3)$$

Forward conduction loss of the power diode is calculated with average current and rms current flowing through the diode as is given in (5.4).

$$P_{LossPDiode} = V_{T0} I_{ave} + R_D I_{RMS}^2 \quad (5.4)$$

Since the power diodes are SiC Schottky Diodes, there is almost no reverse recovery loss for the power diodes.

Last main reason for the loss, is source drain diode of the MOSFET. Silicon technology is used in these diodes; therefore, these diodes have reverse recovery loss and conduction loss. Conduction loss of the diodes are calculated as given in (5.5). Variable V_{SD} is the voltage between source and drain, I_{ave} is the average current flowing through the MOSFET. Reverse recovery loss of the diode is calculated as given in (5.6). Variable V_R is the reverse voltage, I_{RM} is the peak reverse recovery current, t_{rr} is the reverse recovery time and f_{sw} is the switching frequency.

$$P_{CONMOSD} = V_{SD} I_{ave} \quad (5.5)$$

$$P_{RRMOSD} = V_R I_{RM} t_{rr} f_{sw} \quad (5.6)$$

While calculating the total loss of the inverter, it is assumed that half of the devices are in conduction since only 2 device can be conducting current for each phase. Moreover, conduction time is spread equally between MOSFET and source-drain diode of the MOSFET. Every component is switched with 10 kHz. Then, $R_{DC(ON)}$ is obtained as $240m\Omega$ from the datasheet, I_{QSW} is selected as $2.5A_{rms}$, V_{MOS} is $200V$ since

MOSFETs are switched under this voltage, I_{MOS} is 2.25 since this is the average current, $Q_{g(on)}$ is obtained as $82nC$ from the datasheet, I_G is calculated as $3A$, V_{T0} is obtained as $1.63V$ from the datasheet, R_D is calculated as $39.8m\Omega$. Under these conditions total expected loss of the inverter is calculated as given in (5.7).

$$P_{CONMOSFET} = 240m\Omega \cdot 2.5^2 A_{RMS}$$

$$P_{CONMOSFET} = 1.5Watt$$

$$P_{SWMOSFET} = 200V \cdot 2.25A \cdot 10kHz \cdot \frac{82nC}{3A}$$

$$P_{SWMOSFET} = 123mW$$

$$P_{RRMOSD} = 100V \cdot 8A \cdot 100ns \cdot 10kHz$$

$$P_{RRMOSD} = 0.8W$$

$$P_{CONMOSD} = 1.5V \cdot 2.25A$$

$$P_{CONMOSD} = 3.38W$$

$$P_{LossPDiode} = 1.63V \cdot 2.25A + 39.8m\Omega \cdot 2.5^2 A_{RMS}$$

$$P_{LossPDiode} = 3.92W$$

$$P_{InvTotal} = 3P_{CONMOSFET} + 3P_{CONMOSD} + 6P_{RRMOSD} + 6P_{SWMOSFET} + 3P_{LossPDiode}$$

$$P_{InvTotal} = 3 \cdot 1.50W + 3 \cdot 3.38W + 6 \cdot 0.8W + 6 \cdot 0.123W + 3 \cdot 3.92W$$

$$P_{InvTotal} = 31.94W$$

(5.7)

The expected efficiency of the inverter is calculated by adding the expected losses to output power. Expression for expected efficiency is provided in (5.8).

$$\begin{aligned} \eta &= \frac{P_{Out}}{P_{Out} + P_{Loss}} \%100 \\ \eta &= \frac{1000Watt}{1000Watt + 31.94Watt} \%100 \\ \eta &= \%96.90 \end{aligned} \quad (5.8)$$

In order to keep the temperature under desired limits, heat-sinks are placed on each power semiconductor. The ambient temperature is considered as $30^\circ C$. The maximum allowed temperature is $120^\circ C$. Selected heat-sink for MOSFETs is a vertical

type with the component ID of M46162B021000G [56]. This heat-sink has ambient to surface thermal resistance of $10^{\circ}C/W$. In this case, maximum junction temperature is calculated under full load operating condition as given in (5.9). Notice that, each heat-sink is connected to two MOSFETs.

$$\begin{aligned}
 P_{LossMosfet} &= 0.25P_{CONMOSFET} + 0.25P_{CONMOSD} + P_{RRMOSD} + P_{SWMOSFET} \\
 P_{LossMosfet} &= 2.14W \\
 T_j &= 2 R_{th(JC)} P_{LossMosfet} + 2 R_{th(CS)} P_{LossMosfet} + 2 R_{th(AC)} P_{LossMosfet} + T_a \\
 T_j &= 2 0.23^{\circ}C/W 2.14W + 2 0.21^{\circ}C/W 2.14W + 2 10^{\circ}C/W 2.14W + T_a \\
 T_j &= 75^{\circ}C
 \end{aligned} \tag{5.9}$$

Selected heat-sink for power diodes is given in [57]. Ambient to case thermal resistance of the heat-sink is $8^{\circ}C/W$. Junction temperature calculation s given in (5.10).

$$\begin{aligned}
 T_j &= R_{th(AC)} P_{LossPDiode} + R_{th(JC)} P_{LossPDiode} + T_a \\
 T_j &= 8^{\circ}C/W 3.92W + 4^{\circ}C/W 3.92W + 30^{\circ}C \\
 T_j &= 77^{\circ}C
 \end{aligned} \tag{5.10}$$

These results suggest that junction temperature of MOSFETs are expected to be less than $75^{\circ}C$ and that of the power diodes to be less than $80^{\circ}C$. Hence, the thermal design of the inverter is expected to work properly.

5.3 Measurement Results

In the previous chapters, capacitor selection was made for a $100kW$ drive system. 20 operating points were selected in previous analysis as in Table 4.3. In order to verify the findings of simulations, similar operating conditions are tested in the experimental setup. These cases are obtained by proportionally reducing examined voltage and current. Voltages are reduced while keeping modulation index constant. The currents are reduced while keeping maximum current at $2.5A_{rms}$. The operating points determined for experimental verification are shown in Table 5.14. Output voltage was

obtained by multiplying modulation index with DC-link voltage as given in (5.11). Power factor is calculated by using measured load inductance, measured load resistance and fundamental frequency as given in (5.12). Resistive and inductive loads are measured by LCR meter and digital micro ohm meter and added to Table 5.14. Expected apparent power and real power are calculated according to (5.13), (5.14). Simulation and experimental results are obtained for all cases with the different PWM methods: SPWM, SVPWM, NTV and carrier based method.

Observation of harmonic content is done for Case #2. Case is given in Table 5.14. This case is selected because of high load current, medium fundamental frequency, medium modulation index and medium power factor.

$$V_{out,phpeak} = m_i \frac{V_{DC}}{2} \quad (5.11)$$

$$\cos(\phi) = \frac{R}{\sqrt{R^2 + 2\pi f_{fund}L}} \quad (5.12)$$

$$S = 3V_{ph}I_{ph} \quad (5.13)$$

$$P = S\cos(\phi) \quad (5.14)$$

Four PWM methods that are, SPWM, SVPWM, NTV and carrier based method are tested. In the experiments input voltage is increased to 380V with 50V steps. Until input voltage reaches 360V, power switches were all turned off. After the input voltage exceeded 360V, switching and; thus, power conversion started.

Oscilloscope measurements are used to examine the results. Output line-to-line voltage waveform for AB phase, output phase currents for phase B and phase C, NPP waveform are the measured signals. In the following parts, waveforms of these signals are presented.

Table 5.4: Parameters of the Experiment

Parameters	Values
Input Voltage, V_{DC}	380V
Modulation Index, m_i	0.75
Switching Frequency, f_s	10kHz
Fundamental Frequency, f_{fund}	100Hz
Load Inductance, L	51.53mH
Load Resistance, R	33.26Ω
DC-link Capacitors, C	100μF

5.3.1 Detailed Evaluation of Current and Voltage Waveforms

Experiment is done with parameters provided in Table 5.4. Resulting current waveforms of the experiment for different methods are shown in Fig. 5.8a, Fig. 5.9a, Fig. 5.10a and Fig. 5.11a. Sinusoidal current waveform is achieved for all methods. However, amplitude of current of phase B and phase C are slightly different due to imbalance of loads.

Output line-to-line voltage between phase A and phase B for different methods are shown in Fig. 5.8b, Fig. 5.9b, Fig. 5.10b and Fig. 5.11b. In all waveforms, three level voltage waveform is observed, which means line-to-line voltage waveform has 3 different values. Since the DC-link voltage is not equally divided between two capacitors, line-to-line voltage of the SPWM method has a relatively high harmonic content.

Experimental NPP waveforms for different PWM methods are given in Fig. 5.8c, Fig. 5.9c, Fig. 5.10c and Fig. 5.11c. Waveforms also include a filtered version of the signals. Filter used is a 10th order low pass Butterworth filter with pass band edge frequency of 1000π . Waveforms obtained in SPWM and SVPWM cases are more sinusoidal than other methods. In NTV method, low frequency ripple is lower than SPWM and SVPWM case. In carrier based method, low frequency signal is almost completely eliminated. However, all methods have a dominant high frequency ripple,

which means most of the ripple occurring on the neutral point is due to the high frequency ripple. This can be due to the low capacitance of electrolytic capacitors at high frequencies.

Harmonic Content of Phase Current and Line-to-line Voltage

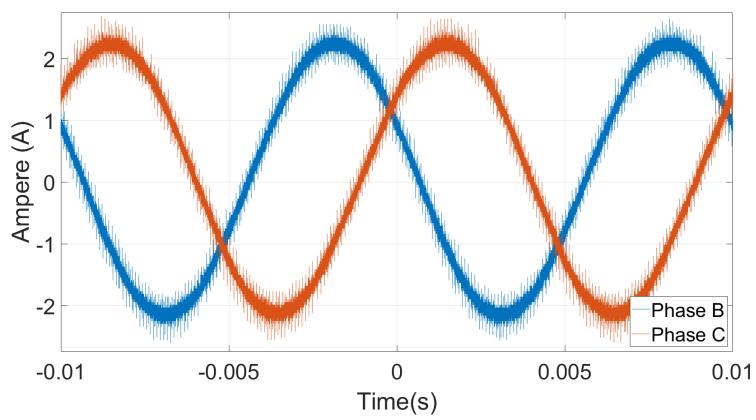
In motor drive applications, high harmonic content creates torque ripple. The torque ripple causes control problems and mechanical component deformation. Moreover, core losses of the motor increase with harmonic content.

Notice that, fundamental frequency is critical for observing harmonic content. Since the switching frequency is constant, changing fundamental frequency changes the proportion of fundamental frequency to switching frequency which is $\frac{f_{fund}}{f_{sw}}$. Increasing this proportion decreases the harmonic content, while increasing the proportion increases the harmonic content.

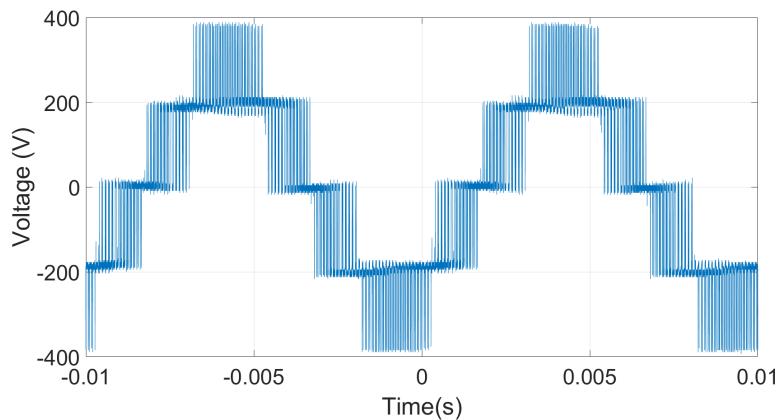
Another parameter effecting harmonic content is dead-time of the semiconductors. In this study dead-time was selected as 2μ seconds. Having a lower dead-time decreases the harmonic content. Specifically, zero crossings of the voltage waveform is affected from the dead-time. This is because duty cycles of the switches are quite small during zero crossings which causes deformation of the waveform on these time intervals.

Harmonic content is measured by using FFT function of Matlab Simulink environment. Both phases current and line-to-line voltage harmonics are observed. Phase currents are observed until frequency of 15kHz. Since the load is an RL type load, high frequency voltage ripples are filtered on the current waveform. Therefore, high frequency components are low. Line-to-line voltages are observed until frequency of 150kHz. This is because of the fact that, voltage waveforms include switching effects. Visual distribution of the harmonics and listing of some harmonic components are presented in the related figures.

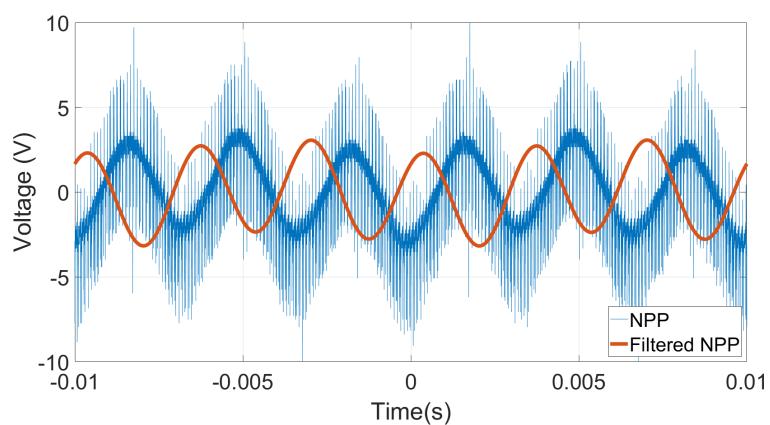
Total harmonic distortion is calculated from the results of the FFTs. Total harmonic distortion is a measure of harmonic content of a signal. Its expression is provided in (5.15). In RL load cases, current THD is lowered according to filtering effect of the RL load. Having a load with lower power factor reduces the current THD.



(a) SPWM Method Phase B and Phase C Current Waveform

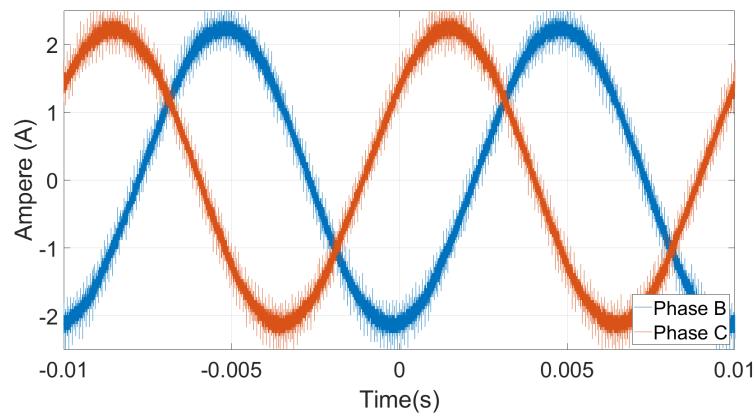


(b) SPWM Method Line-to-Line Voltage Waveform (AB)

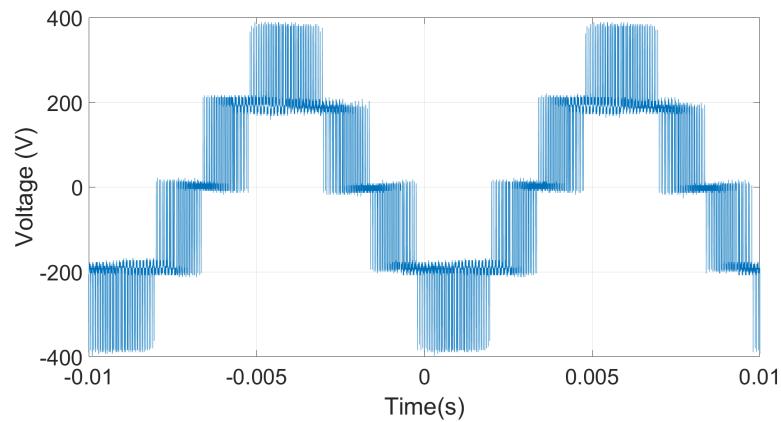


(c) SPWM Method Neutral Point Potential Waveform (AC Coupled)

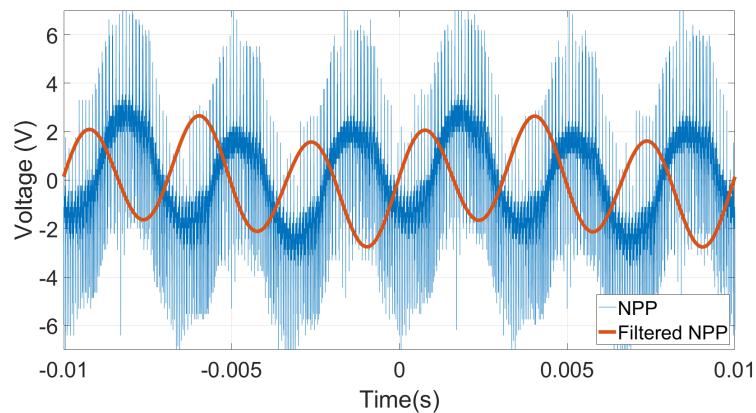
Figure 5.8: SPWM Method Oscilloscope Measurements



(a) SVPWM Method Phase B and Phase C Current Waveform

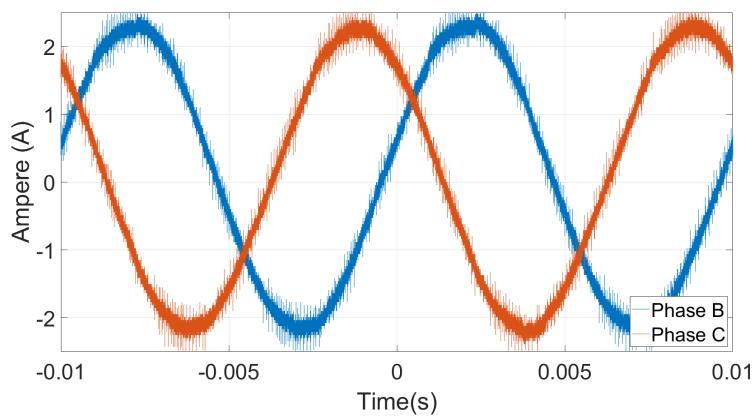


(b) SVPWM Method Line-to-Line Voltage Waveform (AB)

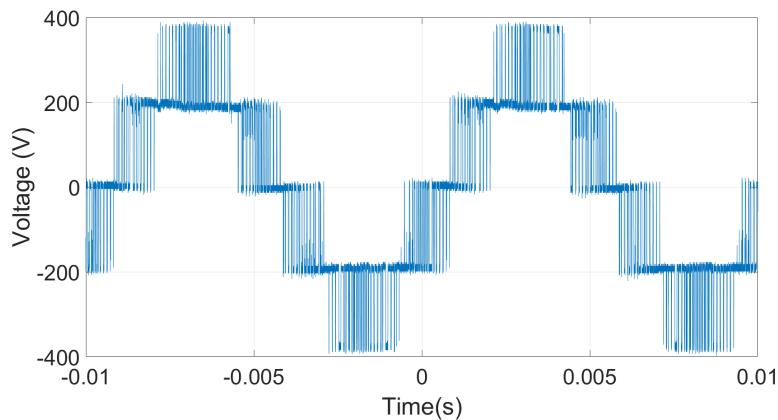


(c) SVPWM Method Neutral Point Potential Waveform (AC Coupled)

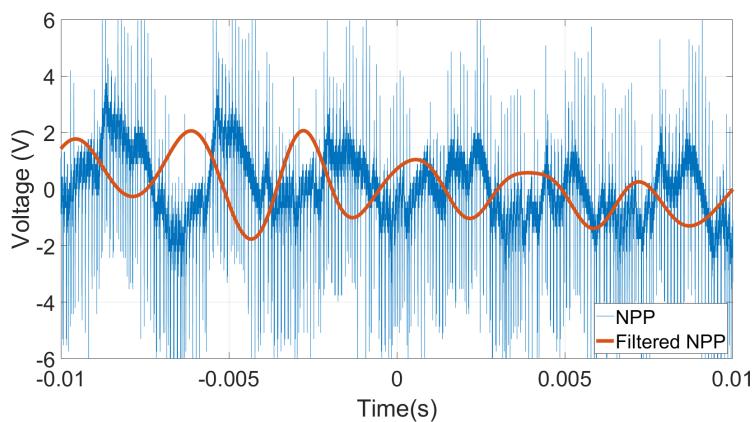
Figure 5.9: SVPWM Method Oscilloscope Measurements



(a) NTV Method Phase B and Phase C Current Waveform

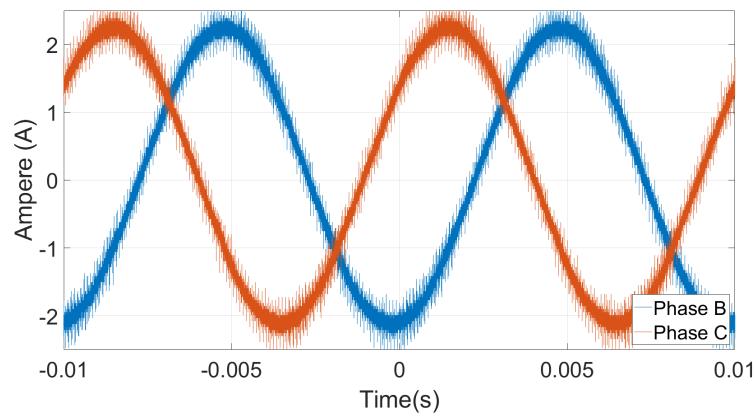


(b) NTV Method Line-to-Line Voltage Waveform (AB)

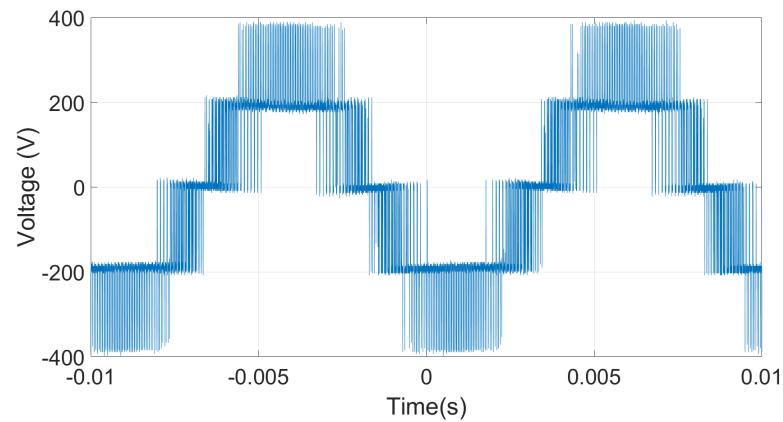


(c) NTV Method Neutral Point Potential Waveform (AC Coupled)

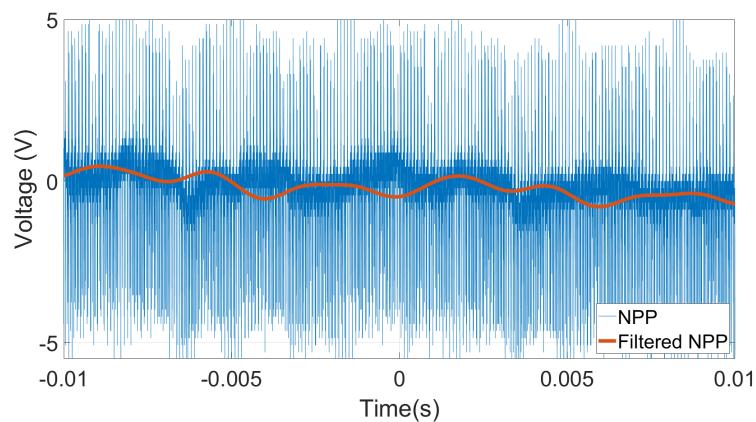
Figure 5.10: NTV Method Oscilloscope Measurements



(a) Carrier Based Method Phase B and Phase C Current Waveform



(b) Carrier Based Method Line-to-Line Voltage Waveform (AB)



(c) Carrier Based Method Neutral Point Potential Waveform (AC Coupled)

Figure 5.11: Carrier Based Method Oscilloscope Measurements

The results of measurements are given on the title of the related figures (Fig. 5.12, Fig. 5.13, Fig. 5.14, Fig. 5.15, Fig. 5.16, Fig. 5.17, Fig. 5.18, Fig. 5.19) and also listed in Table 5.13.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \dots}}{V_1} \quad (5.15)$$

Since voltage imbalance of neutral point causes even number of harmonics at the output, having higher neutral point potential ripple causes higher THD at output voltage.

Figure 5.12 shows harmonic content of Phase B current with SPWM method. Notice that, harmonics are normalized according to fundamental component. Therefore, fundamental component is observed as 100 and other components are expressed as a percentage of fundamental component. Moreover, Table 5.5 shows the list of harmonic components. It is observed that, harmonic content mostly consists of the DC component.

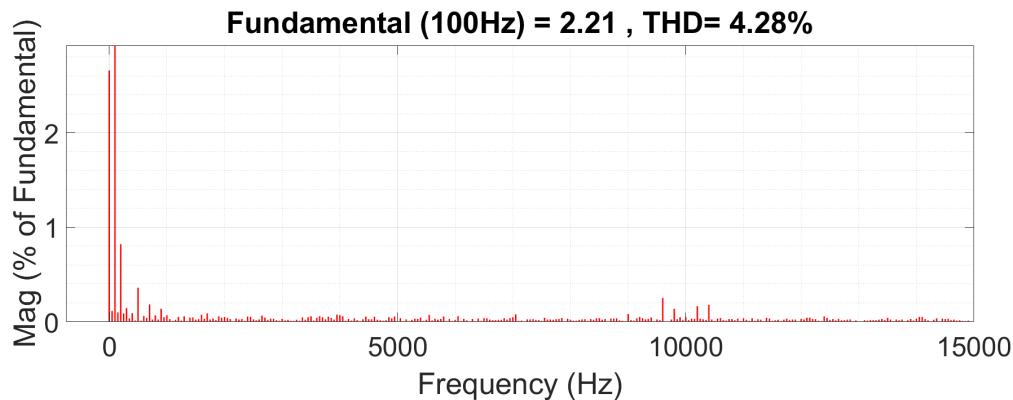


Figure 5.12: SPWM Phase B Current FFT Result

Table 5.5: SPWM Phase Current Harmonics

Harmonic No	Amplitude (%)	Harmonic No	Amplitude (%)
DC	2.52	4th	0.08
2nd	0.24	5th	0.34
3rd	0.19	6th	0.11

Figure 5.13 shows the FFT result for Phase B current with SVPWM method. Total

harmonic distortion of the signal is measured as 4.46%. This value is slightly higher than SPWM case which was 4.28%. This may be because of NPP ripple. Normally, THD of SVPWM is expected to be lower than SPWM method. However, due to negative effect of NPP ripple, second harmonic of current in SVPWM method is higher than SPWM method.

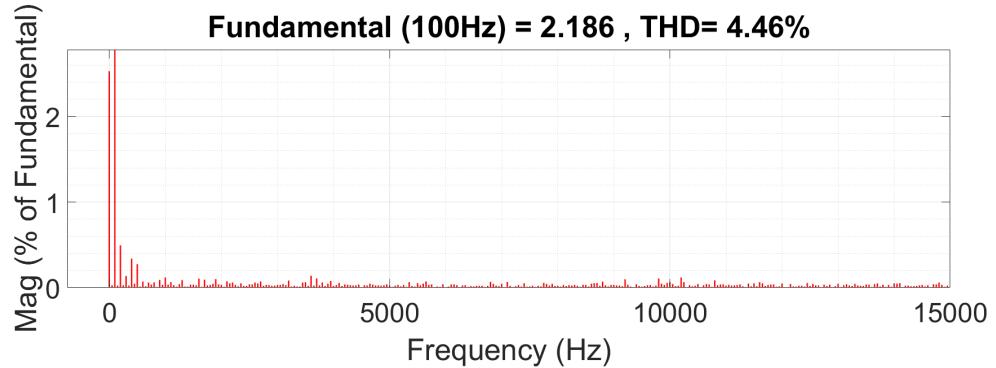


Figure 5.13: SVPWM Phase B Current FFT Result

Table 5.6: SVPWM Phase Current Harmonics

Harmonic No	Amplitude (%)	Harmonic No	Amplitude (%)
DC	2.53	4th	0.34
2nd	0.49	5th	0.27
3rd	0.14	6th	0.07

Figure 5.14 shows the FFT result for Phase B current with NTV method. Total harmonic distortion of the signal is measured as %3.91. This value is lower than SVPWM case. This may be because of lower NPP ripple. Since NPP ripple has a different waveform than SVPWM case, and since it has a lower amplitude, current THD of NTV method is lower than SVPWM method.

Figure 5.15 shows the current FFT result with Phase B current of carrier based method. Total harmonic distortion in this method is higher than other methods. This may be because of the limited switching count of SVPWM and NTV method. However, since carrier based method does not use space vector diagram step change in carrier based method is higher than other two methods.

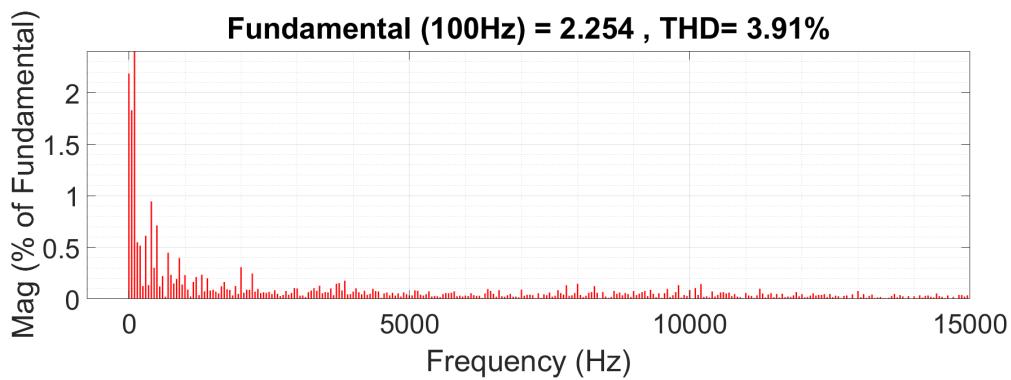


Figure 5.14: NTV Phase B Current FFT Result

Table 5.7: NTV Phase Current Harmonics

Harmonic No	Amplitude (%)	Harmonic No	Amplitude (%)
DC	2.19	4th	0.95
2nd	0.52	5th	0.71
3rd	0.61	6th	0.22

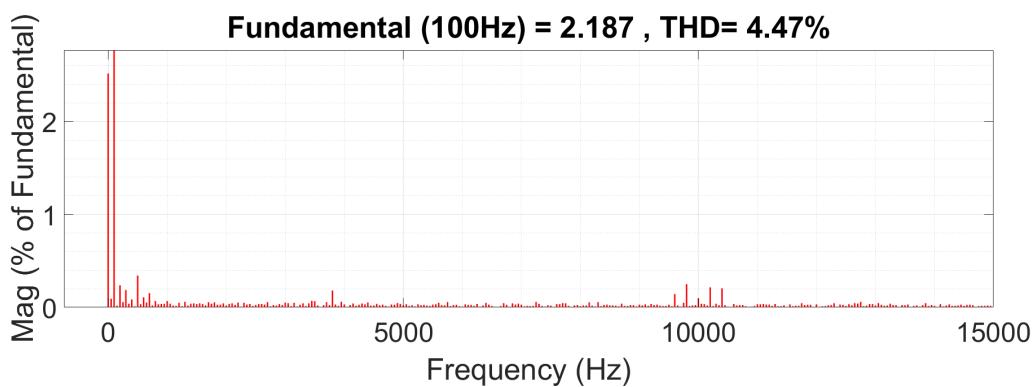


Figure 5.15: Carrier Based Method Phase B Current FFT Result

Table 5.8: Carrier Based Method Phase Current Harmonics

Harmonic No	Amplitude (%)	Harmonic No	Amplitude (%)
DC	2.19	4th	0.95
2nd	0.52	5th	0.71
3rd	0.61	6th	0.22

Figure 5.16 shows the harmonic content of line to line voltage of SPWM method. Voltage harmonics are occurring at the multiples of switching frequency as expected. Total harmonic distortion is measured as %43.02.

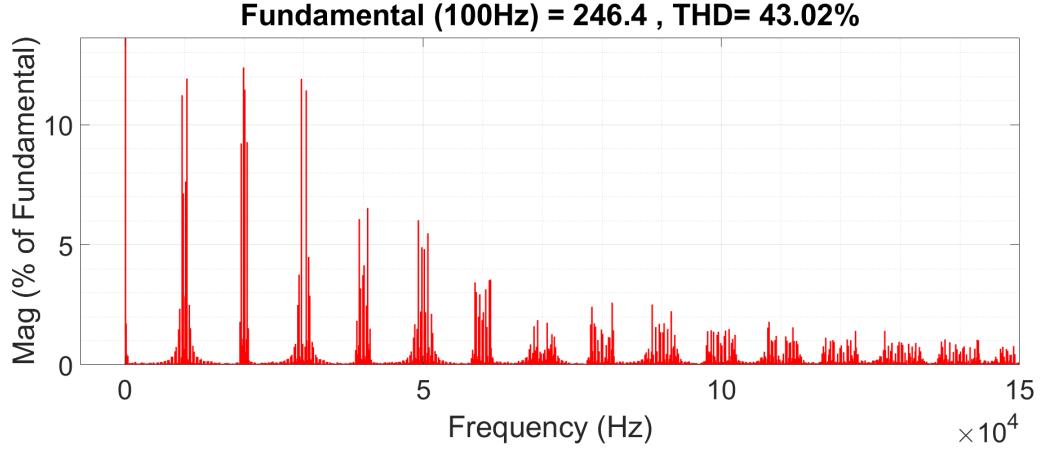


Figure 5.16: SPWM Line-to-Line Voltage FFT Result

Table 5.9: SPWM Line-to-Line Voltage Harmonics

Harmonic No	Amplitude (%)	Harmonic No	Amplitude (%)
DC	0	4th	0.31
2nd	1.72	5th	0.37
3rd	0.45	6th	0.03

Figure 5.17 shows the harmonic content of line-to-line voltage of SVPWM method. Voltage harmonics are occurring at the multiples of switching frequency as expected. Total harmonic distortion is measured as %43.47. The distortion is very similar to SPWM case.

Figure 5.18 shows the harmonic content of line-to-line voltage of NTV method. Voltage harmonics are occurring at the multiples of switching frequency as expected. Total harmonic distortion is measured as %44.23. The distortion is slightly larger than SPWM and SVPWM cases. This may be a result of changing effective switching frequency in NTV method.

Figure 5.19 shows the harmonic content of line-to-line voltage of carrier based method.

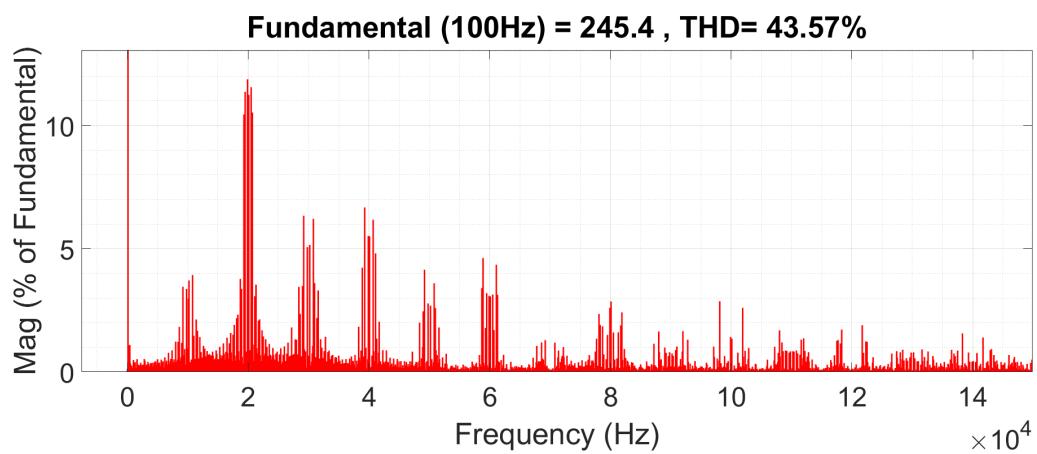


Figure 5.17: SVPWM Line-to-Line Voltage FFT Result

Table 5.10: SVPWM Line-to-Line Voltage Harmonics

Harmonic No	Amplitude (%)	Harmonic No	Amplitude (%)
DC	0.10	4th	1.09
2nd	1.09	5th	0.35
3rd	0.44	6th	0.13

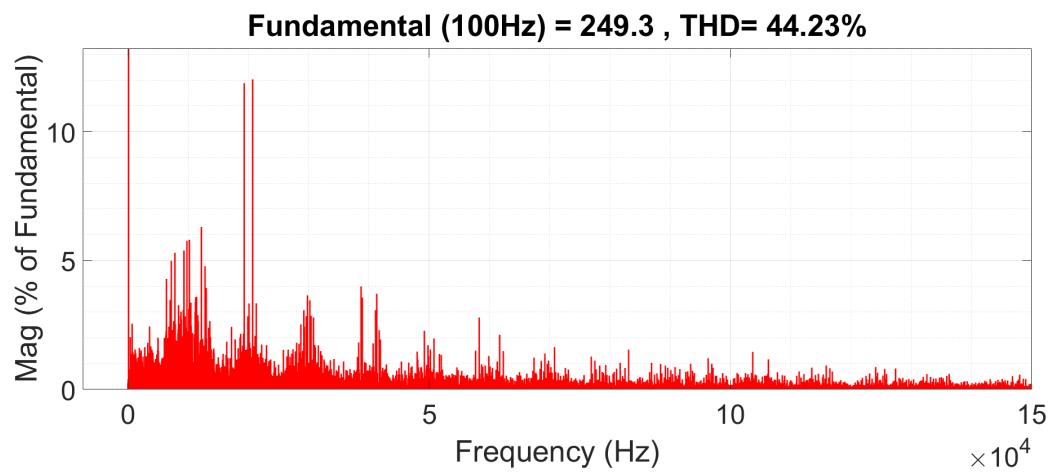


Figure 5.18: NTV Line-to-Line Voltage FFT Result

Table 5.11: NTV Line-to-Line Voltage Harmonics

Harmonic No	Amplitude (%)	Harmonic No	Amplitude (%)
DC	0.25	4th	2.03
2nd	0.57	5th	1.01
3rd	0.44	6th	1.39

Voltage harmonics are occurring at the multiples of switching frequency as expected. Total harmonic distortion is measured as %47.44. The distortion rate is highest among all methods. This is a result of higher step number in one switching period.

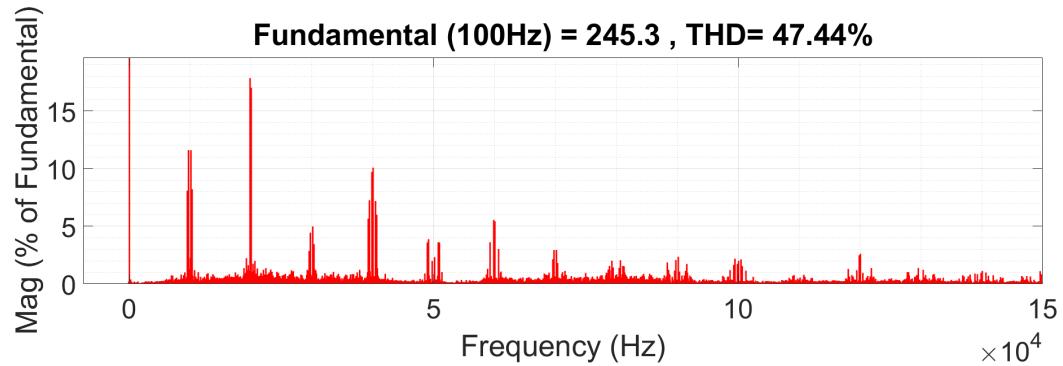


Figure 5.19: Carrier Based Method Line-to-Line Voltage FFT Result

Table 5.12: Carrier Based Method Line-to-Line Voltage Harmonics

Harmonic No	Amplitude (%)	Harmonic No	Amplitude (%)
DC	0.20	4th	0.09
2nd	0.26	5th	0.17
3rd	0.39	6th	0.06

Overall, harmonic contents of the PWM methods are close to each other for case #2 which means similar waveforms in different PWM methods is achieved. THD is in acceptable range for all of the methods.

5.3.2 NPP Ripple at Different Operating Conditions

In this section, NPP ripple measured at 20 operating points are given for each PWM method separately. Numeric simulations are also performed at each operating point by using the full simulation models presented in Chapter 4 and including the dead time. The comparison here aim to verify the correctness of the capacitor sizing results by exploring the effect PWM method on NPP ripple.

Table 5.15, Table 5.16, Table 5.17 and Table 5.18 shows simulation and experimental NPP ripple amplitude results for different PWM methods. NPP ripple amplitude is

Table 5.13: THD Results

Signal Name	THD (%)
SPWM Current	4.28
SPWM Voltage	43.02
SVPWM Current	4.46
SVPWM Voltage	43.57
NTV Current	3.91
NTV Voltage	44.23
Carrier Based Method Current	4.47
Carrier Based Method Voltage	47.44

obtained by measuring peak-to-peak amplitude of the signals. Filtered version of the amplitude is obtained by applying a 10^{th} order low pass filter Butterworth filter with passband limit of $1000\pi rad/sec$. DC-link capacitors selected for the experiment and simulation are $100\mu F$.

Table 5.15 shows results for SPWM method. First column shows the NPP ripple amplitude for full simulation model built on Matlab Simulink. Second column has the filtered version of the signal given in first column. Third column has the experimentally obtained result of NPP signal. Fourth column has the filtered version of the third column. Simulation results and experimental results are far from each other when high frequency part is included. However, when the signals are filtered, low frequency part of the signals are close to each other. This can be due to capacitance variations electrolytic capacitors with frequency. These capacitors have reduced capacitance for high frequency signals which causes higher ripples at high frequencies. Largest low frequency NPP ripple occurred at Cases #2, #3 and #4 due to low frequency, high load current and low power factor. Deviation between simulation and experiment is higher at low NPP ripple cases.

It is verified that having higher load current has an increasing effect on the NPP ripple. Decrease in the NPP ripple between Case #2 and Case #13 is explained with

decrease in the load current.

It is observed that voltage difference between filtered simulation results and experimental simulation results have a maximum difference of 1.40V. Therefore, simulation results and experimental results are consistent for the SPWM case.

Table 5.16 has results for SVPWM method. Again, simulation results and experimental results are far from each other when filter is not applied. Largest low frequency NPP ripple occurred at Cases #1, #3, #4 due to high load current. Deviation between simulation and experiment is higher at low NPP ripple cases, which is due to the resolution limit of the neutral point voltage sensor.

It is verified that having higher load current has an increasing effect on the NPP ripple. Decrease in the NPP ripple between Case #2 and Case #13 is explained with decrease in the load current.

It is observed that voltage difference between filtered simulation results and experimental simulation results is high in Case #3 and Case #4. Except for these two cases, maximum difference between filtered simulation results and experimental results is 1.07V. Therefore, except for the two cases, simulation and experimental results are consistent.

Table 5.17 has results for NTV method. Similar to previous two methods, simulation and experimental results are far from each other when filter is not applied. However, in NTV method, even filtered simulation and experimental results have high deviation. This may be because of the low sensor accuracy. Largest amplitudes are observed at Cases #1 and #5 due to high current and high modulation index.

It is verified that having higher load current has an increasing effect on the NPP ripple. Decrease in the NPP ripple between Case #2 and Case #13 is explained with decrease in the load current.

It is observed that filtered simulation and experimental results have more than 2.5V difference. These differences may be occurring because of sensor errors on the PCB. Except for these cases, other cases show consistent results between simulation and experiment results.

Table 5.18 has results for carrier based method. Similar to previous methods, NPP ripple amplitude difference between simulation and experimental results are high when high frequency part of the signal is included. However, when the signals are filtered, results are closer. However, experimental results are still many times larger than simulation results. This is because of small low frequency ripple is not measured accurately by the voltage sensor.

It is verified that having higher load current has an increasing effect on the NPP ripple. Decrease in the NPP ripple between Case #2 and Case #13 is explained with decrease in the load current.

It is observed that filtered simulation and experimental results have more than 1.5V difference in two cases. These differences may be occurring because of sensor errors on the PCB. Except for these cases, other cases show consistent results between simulation and experiment results.

Measurements are conducted for one value of DC-link capacitor and the results show the effect of the PWM method on the NPP ripple. It is verified that low frequency NPP ripple can be successfully calculated with simulation models. However, further investigations are required to find the reason of higher high frequency ripple in the measurement results compared to simulations.

Figure 5.20 shows low frequency neutral point potential ripple results for different PWM methods. Parallel with the results of the previous chapter, carrier based method provides lowest low frequency neutral point potential ripple compared to the other PWM methods. On the other hand, NTV method resulted in higher low frequency neutral point potential ripple than SPWM and SVPWM methods which was not expected. This may be because of insufficient voltage sensor accuracy. However, maximum low frequency neutral point potential is lower in NTV method compared to SPWM and SVPWM methods.

Table 5.14: NPP Ripple for Selected Operation Points with $C_1 = C_2 = 100\mu F$

No	f (Hz)	Current (A_{Peak})	Voltage (V_{Peak})	MI (%)	PF	L (mH)	R (Ω)	S (VA)	P (W)
1	130	3.15	167.20	0.88	0.75	46.04	39.76	789	592
2	100	3.13	142.50	0.75	0.74	51.53	33.26	669	495
3	70	3.13	100.70	0.53	0.74	50.56	23.61	473	350
4	33	3.13	53.20	0.28	0.76	55.82	13.28	250	190
5	140	3.03	171.00	0.90	0.77	41.22	43.24	778	599
6	100	2.95	140.60	0.74	0.75	50.15	35.79	621	466
7	173	2.79	176.70	0.93	0.80	35.51	50.61	739	591
8	140	2.43	172.90	0.91	0.81	47.13	57.63	629	509
9	107	2.36	142.50	0.75	0.78	56.13	47.42	504	393
10	73	2.36	98.80	0.52	0.79	54.88	33.22	349	276
11	190	2.67	178.60	0.94	0.81	31.63	54.51	716	580
12	133	2.09	169.10	0.89	0.80	57.38	64.65	530	424
13	100	2.09	169.10	0.71	0.77	79.64	62.51	529	407
14	210	2.48	134.90	0.94	0.82	27.78	44.55	501	411
15	240	2.39	178.60	0.94	0.81	29.97	60.59	641	520
16	273	2.15	178.60	0.94	0.82	31.36	67.78	577	473
17	400	1.39	178.60	0.93	0.88	30.93	112.47	373	328
18	337	1.24	176.70	0.93	0.90	31.23	127.67	330	297
19	267	0.97	176.70	0.93	0.91	44.00	165.85	257	234
20	203	0.79	176.70	0.92	0.85	94.60	189.36	210	179

Table 5.15: SPWM NPP Ripple Amplitude Results for Simulation and Experiment

No	SPWM Simulation (V)	SPWM Filtered Simulation (V)	SPWM Experiment (V)	SPWM Filtered Experiment (V)
1	7.18	6.86	19.45	5.47
2	8.05	7.65	20.20	6.25
3	8.04	7.64	20.89	6.55
4	7.56	7.41	21.99	7.48
5	6.67	6.24	18.19	4.89
6	7.47	7.06	19.25	6.28
7	5.25	2.87	17.73	2.49
8	5.38	5.02	18.14	4.08
9	5.66	5.33	17.24	4.39
10	5.52	5.17	19.64	4.84
11	4.53	1.17	16.90	1.13
12	4.75	4.46	16.71	3.93
13	4.07	3.81	17.93	3.27
14	4.90	0.63	17.76	0.90
15	3.27	0.21	16.19	0.54
16	2.62	0.17	16.37	0.53
17	1.14	0.07	13.45	0.19
18	1.20	0.07	15.17	0.39
19	1.20	0.13	12.68	0.40
20	1.22	0.22	15.37	0.43

Table 5.16: SVPWM NPP Ripple Amplitude Results for Simulation and Experiment

No	SVPWM Simulation (V)	SVPWM Filtered Simulation (V)	SVPWM Experiment (V)	SVPWM Filtered Experiment (V)
1	5.72	5.47	17.56	5.48
2	6.89	6.50	19.74	5.43
3	6.04	5.53	21.23	8.49
4	6.14	5.10	23.32	12.99
5	5.48	5.19	17.97	4.65
6	6.45	6.06	18.64	5.02
7	4.20	2.74	17.21	2.35
8	4.18	3.94	17.42	3.86
9	4.96	4.64	17.38	4.68
10	6.46	5.67	18.82	6.39
11	3.87	1.76	16.33	1.66
12	4.55	4.55	18.12	3.91
13	3.50	3.25	16.65	3.73
14	4.43	1.54	16.57	0.72
15	2.24	0.18	15.62	0.54
16	2.22	0.53	16.14	0.82
17	1.66	0.99	13.13	0.33
18	1.05	0.35	15.22	0.39
19	1.30	0.74	15.80	0.90
20	0.93	0.31	16.13	0.81

Table 5.17: NPP Ripple for Selected Operation Points with $C_1 = C_2 = 500\mu F$

No	NTV Simulation (V)	NTV Filtered Simulation (V)	NTV Experiment (V)	NTV Filtered Experiment (V)
1	5.14	3.77	19.27	7.80
2	4.32	1.29	18.85	4.53
3	3.76	1.10	21.26	2.02
4	1.99	0.53	19.61	3.10
5	5.17	3.59	19.64	6.75
6	4.94	1.58	18.27	3.38
7	4.68	3.17	17.84	4.28
8	4.02	2.72	19.03	5.43
9	3.89	1.29	17.17	3.51
10	2.99	0.93	19.90	1.54
11	4.45	1.94	17.46	2.93
12	3.63	2.36	17.65	3.84
13	2.75	0.81	18.63	2.50
14	5.73	1.93	17.66	3.89
15	4.05	0.92	19.85	1.34
16	3.53	0.89	17.23	2.53
17	1.83	0.39	14.81	0.86
18	1.86	0.47	16.59	0.61
19	1.42	0.34	16.35	0.73
20	1.22	0.37	15.05	1.20

Table 5.18: NPP Ripple for Selected Operation Points with $C_1 = C_2 = 500\mu F$

No	CB M. Simulation (V)	CB M. (Filtered) Simulation (V)	CB. M. Experiment (V)	CB M. (Filtered) Experiment (V)
1	0.61	0.10	15.90	0.98
2	0.71	0.12	16.71	2.39
3	0.66	0.17	16.96	1.41
4	0.44	0.13	17.30	3.98
5	0.59	0.13	16.32	1.21
6	0.74	0.13	15.94	1.24
7	0.52	0.09	15.35	0.92
8	0.48	0.10	17.10	1.17
9	0.61	0.11	15.52	1.14
10	0.55	0.14	16.45	1.13
11	0.49	0.07	16.56	1.00
12	0.44	0.10	15.84	1.11
13	0.43	0.08	15.36	1.42
14	0.54	0.06	15.95	0.66
15	0.38	0.04	16.38	0.81
16	0.35	0.04	17.00	0.61
17	0.21	0.01	13.41	0.23
18	0.21	0.03	16.09	0.55
19	0.18	0.02	14.71	0.45
20	0.15	0.02	15.87	0.56

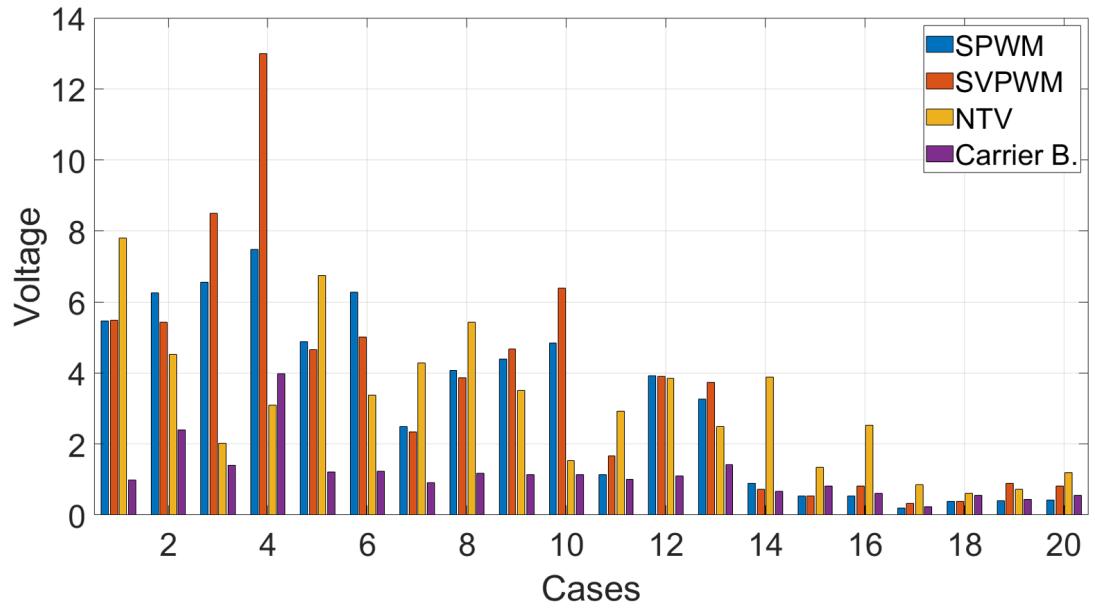


Figure 5.20: Experimental Low Frequency NPP Ripple for Different Methods

Chapter Summary

In this chapter, experimental setup and designed prototype 1kVA three-level neutral point clamped inverter are introduced. Components of the prototype inverter PCB are explained in detail. Then proper operation of the prototype is verified by observing output voltage and current. NPP ripple waveform is presented for four PWM methods. NPP ripple amplitude is observed and analyzed for determined worst operating conditions. Lastly, performance of NPP ripple suppression of different PWM methods is evaluated.

CHAPTER 6

CONCLUSION

In this thesis, capacitor sizing problem of the three-level NPC inverter is examined. Application of the inverter is selected as the variable speed drive for electric vehicles. In order to observe the differences between the most common electric drive topology and the drive with a three-level NPC inverter, two-level VSI inverter topology with its most common PWM methods is presented. Then, the topology and most common PWM methods of the three-level neutral point clamped inverter are explained. NPP ripple problem of three-level neutral point clamped inverter is provided. Relationship between low frequency NPP ripple and the main operating parameters of the inverter are shown. Numeric simulation results are used to verify relationship between low frequency NPP ripple and the main operating parameters. Low frequency NPP ripple model which is used to get numeric simulation results was a faster model than full simulations. The model is extended to be used in all five PWM methods. Information obtained from the numeric results of the low frequency NPP ripple model is used to identify the worst case operating conditions of a reference motor. Additionally, full simulation models were designed to identify worst case NPP ripple operating point of each PWM method and scaling of the capacitors is completed for every PWM method. Moreover, capacitor sizes are compared with a two-level inverter case. It is verified that total capacitor size in three-level inverter is larger than two-level inverter. Furthermore, capacitor size with carrier based method was smallest among the five PWM methods. For experimental validation of the results, a prototype 1kVA inverter is designed and tested. Harmonic content of the output waveform showed similar performance for different PWM methods. Low frequency NPP ripple was lowest in carrier based method.

Relationship between motor characteristics and DC-link capacitor size is verified. The reference machine that is selected to be a PMaSynRM has its worst NPP ripple at base speed and maximum torque region. Therefore, capacitor sizing is done considering this case. However, different motor types are expected to have different worst case operating conditions. Low power factor and high torque regions are expected to display highest NPP ripple.

Carrier based method required the smallest DC-link capacitor between three-level NPC inverter PWM methods. This is because this method is capable of eliminating low frequency NPP ripple completely. However, the method has a higher step number for one switching period compared to other methods. Due to this reason, efficiency of this method is lower than other methods [28]. Therefore, there is a trade-off between efficiency of the PWM method and the ability of suppressing NPP ripple.

In the literature, capacitor sizing was presented for two-level VSIs [33]. Moreover, some papers described the relationship between low frequency NPP ripple and some operating parameters for three-level NPC VSIs [30]. However, capacitor sizing of three-level neutral point clamped inverter for variable speed drive was not studied. This study presents a capacitor sizing for three level neutral point clamped inverter for variable speed drives. The contributions of this study to the field can be summarized as below:

- Relationship between low frequency NPP ripple and main operating parameters affecting NPP ripple is analyzed and presented for five different PWM methods. Analyzed main operating parameters were power factor, fundamental frequency, modulation index and load current.
- For a reference PMaSynRM motor drive application, capacitor sizing procedure is completed. Full simulation models are built to numerically verify the behaviour of three-level neutral point clamped inverter. NPP ripple is observed by using full simulation models. Capacitor selection procedure that is based on low frequency NPP ripple calculations is verified by using full simulations.
- A prototype 1 kVA three-level neutral point clamped inverter was designed. Four PWM methods are tested on the designed inverter. Proper operation of the

prototype is verified. Proof of concept for capacitor sizing is completed.

- It is verified both numerically and experimentally that carrier based method requires the smallest capacitor size between five investigated methods. It is observed that, low frequency NPP ripple is almost completely eliminated in carrier based method.

Future Work

1. In the experiment part, high frequency NPP ripple was higher than expected. It is observed that, this difference may be because of the use of electrolytic capacitors. Since electrolytic capacitors have lower performance at higher frequencies, using film capacitor may reduce the high frequency NPP ripple. In the future, new tests can be carried out with film capacitors to decrease the high frequency NPP ripple.
2. Different motor types can be investigated in terms of capacitor sizing. Since different motor types have different characteristics, capacitor sizing should be modified for these motors.
3. Effect of NPP ripple on thermal design of DC-link capacitor will be evaluated.
4. Carrier based method decreases the NPP ripple. On the other hand, switching losses of the inverter increases with this method. Therefore, there is a trade-off between motor loss and inverter loss. Optimum point between motor loss and inverter loss will be investigated.
5. In this study, capacitor sizing is done for five PWM methods. However, there are many other PWM methods presented in the literature. Capacitor sizing method will be extended into other PWM methods of three-level NPC inverter.
6. In this study, desired maximum NPP ripple is selected as 5% of the DC-link voltage. However, for different applications different NPP ripple limit should be decided. Desired NPP ripple for different applications can be decided, considering lifetime of the capacitor, power semiconductor voltage rating and harmonic content of output current and voltage.

7. A comparison between DC-link capacitor volume and weight between two-level inverter and three-level NPC inverter can be performed. In this study, capacitance of the DC-link capacitor, is found larger in three-level NPC inverter than in two-level inverter. However, capacitor voltage rating in two-level inverter is two times the capacitor voltage rating of three-level NPC inverter.
8. In this study DC-link capacitor sizing is made by considering NPP ripple. However, DC-link capacitor size also determines input current ripples of the inverter. If the DC voltage supply that is providing energy to the three-level NPC inverter is not able to provide rippled current to the inverter, then DC-link capacitor size should be increased to keep the input current ripples low. In the future, input current constraint can be added to capacitor selection method.

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