# Space Vector Modulation for Three-Level NPC Converter With Neutral Point Voltage Balance and Switching Loss Reduction

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***Abstract*—This paper investigates the different control objectives, such as loss reduction, neutral point (NP) balance and noise reduction of the space vector modulation (SVM), for the three-level neutral point clamped (NPC) converter. A detailed loss model and simulation model is built for quantitative loss and NP voltage ripple analysis. An improved SVM method is proposed to reduce NP imbalance and switching loss/noise simultaneously. The coordinately selected small vectors consider both the NP charge and the pulse sequence so that the minimized NP ripple and switching events are guaranteed in one switching cycle. In addition, the switching events between switching cycles are also considered to reduce the total switching loss. This method ensures an evenly distributed device loss in each phase leg and also a constant system efficiency under different power factors. The control result for NP balance and loss reduction is verified by using both a simulation model and an experimental prototype on a 200-kVA three-level NPC converter hardware.**

***Index Terms*—Neutral point (NP) balance, neutral point clamp, pulse sequence, space vector modulation (SVM), switching event.**

## I. Introduction

THE emerging concept of renewable energy microgrid system raises challenges to the power conversion system (PCS) which provides bidirectional interface between the utility grid and the dc bus [1]–[6]. For such a high power application, the three-level neutral point clamped (NPC) converter is most commonly used, especially for the renewable energy and microgrid interface [7]–[9]. A 200-kVA three-level NPC PCS is shown in Fig. 1 and discussed in this paper. The system uses two-stage architecture with bidirectional dc/dc chopper and dc/ac converter. The dc-link voltage is 1200 V and the ac-line voltage can be 480 V/600 V. The switching frequency for this 200-kVA PCS is pushed to 20 kHz to achieve high power density, low harmonics and high control bandwidth. The output side is connected to an LCL filter for current harmonic attenuation. The inductance for inverter and grid-side inductor is 0.27 mH and the filter capacitance is 10 $\mu$F.

Manuscript received September 4, 2013; revised October 30, 2013; accepted December 3, 2013. Date of current version May 30, 2014. This work was supported in part by the Renewable Energy and Nano-grid Consortium, Center for Power Electronics Systems, Virginia Tech. Recommended for publication by Associate Editor F. W. Fuchs.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2013.2294274

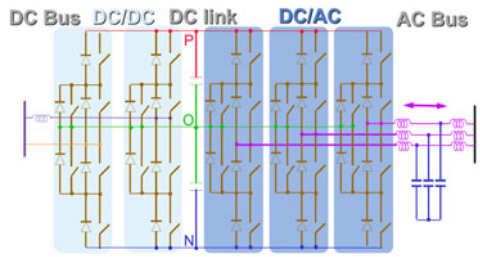


Fig. 1. System structure of the three-level NPC PCS.

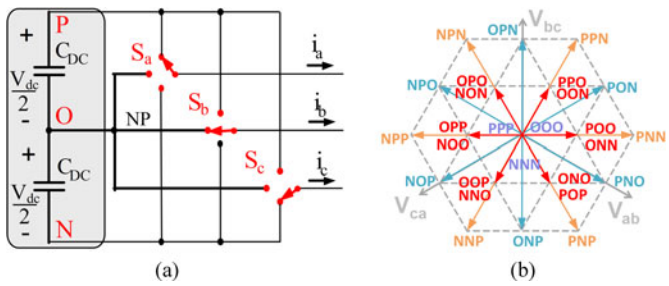


Fig. 2. Circuit and space vector diagram for three-level NPC converter. (a) Circuit diagram. (b) Space vector diagram.

To modulate the dc/ac part of the three-level NPC converter, different modulation schemes are available like the carrier-based SPWM method, the space-vector-based space vector modulation (SVM) (or SVPWM) method and the hybrid modulation [10]–[16]. The SPWM method is easy to implement by simply comparing the reference and carrier wave. On the contrary, the SVM method is complex in its calculation and implementation. But it has more control freedom because the vector selection and pulse generation can be flexibly configured. Considering the extra control flexibility and freedom, SVM is used for the high-frequency converter to enable a better performance.

Each phase of the three-level NPC converter can be equaled to a three-pole one-throw switch that connects to the positive, negative, or neutral rail as shown in Fig. 2(a). There are total 33 switching status, corresponding to 19 space vectors in the line-to-line voltage space as shown in Fig. 2(b). Among them, there are six long vectors, six medium vectors, six small vectors, and one zero vectors. The small and zero vectors come in pairs and have redundant switching status to choose. For the SVM method, the selection of the redundant vector is the key step that enables the modulation scheme to achieve different control objectives such as NP voltage balancing [17]–[21], switching loss reduction [22] or common-mode (CM) noise reduction [23]–[25].

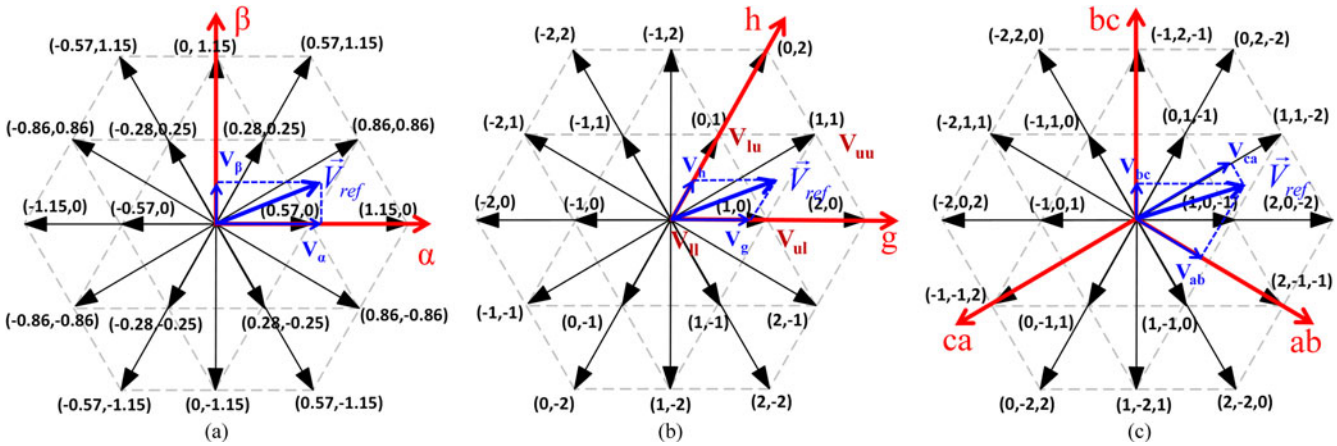


Fig. 3. Three types of coordinate systems for three-level NPC vector space diagram. (a) $\alpha$–$\beta$ coordinate. (b) $g$–$h$ coordinate. (c) $a$-$b$-$c$ coordinate.

The NP voltage balance is the basis to maintain a good output voltage and current waveform and is essential for the proper function of the NPC converter. As a result, it is treated as the control priority by most of the conventional SVM schemes for three-level NPC converter.

Although different NP balancing algorithms are proposed [26]–[30], none of them deals with the switching loss reduction because the redundant vector selection is based on single objective. However, for the high-power high-frequency NPC PCS, loss and noise reduction is another important goal besides the NP balance. This paper gives a thorough survey on the different control objectives of SVM for three-level NPC converter. The control result for NP voltage ripple, switching loss and CM noise spectrum are compared and analyzed. A detailed loss model is built based on both double pulse test on real hardware and simulation. The loss model provides a powerful tool to quantify the system loss for different SVM schemes. Based on the existing control algorithms, this paper proposes a new SVM scheme to achieve multiple objectives at the same time. The NP voltage is balanced together with the switching loss/noise reduced. The small vectors are selected based on both the NP charge and the pulse sequence. Moreover, the switching loss between switching cycles is also reduced by properly placing the pulse sequence order. This measure further reduces the total loss and most importantly makes the phase leg loss distribution symmetrical. The proposed SVM scheme maintains the same total loss and NP balance result under different power factors. The control result is verified on both simulation model and hardware of the three-level NPC converter.

## II. Reference Vector Location and Duty Cycle Calculation

The trajectory of the rotating voltage reference mapped on the space vector diagram is a circle. In steady state, the voltage reference vector $V_{\rm ref}$ rotates inside the inscribed circle of the space vector hexagon. The radius of this circle is the longest voltage reference vector the converter can generate. The first step for SVM is to determine the location of the $V_{\rm ref}$ vector and find three vectors to synthesis it. The duty cycle of these three vectors is also calculated in this step.

There are three different coordinate systems for the vector space as shown in Fig. 3. The calculation for the $V_{\rm ref}$ location and duty cycle can be done in any of the coordinate systems. The commonly used one is the orthogonal $\alpha$–$\beta$ coordinate in Fig. 3(a) [31]. In this coordinate, the location for $V_{\rm ref}$ and the duty cycle for the vectors are calculated with trigonometric functions. A nonorthogonal $g$–$h$ coordinate system shown in Fig. 3(b) is mentioned in [32]. The benefit of this coordinate system is that all the vectors have an integer coordinate in this system. Therefore, trigonometric functions are replaced by algebraic operation. Thus, the calculation process is largely simplified. Another coordinate system in Fig. 3(c) is proposed by [33]. This system has three axes and shares the same benefit of the $g$–$h$ coordinate.

For the three-level space vector hexagon, there are several sector division methods to locate the voltage reference and to calculate the duty cycle. The hexagon division method shown in Fig. 4(a) divides the three-level vector hexagon into six of the two-level hexagons [34]. Using this division, the calculation rules for the three-level SVM follows the rules of two-level SVM. However, this division method results in overlapped areas. Also the origins for the two-level hexagons are different. These problems need to be dealt with by an extra process. The triangle division method in Fig. 4(b) is commonly used [31]. The three-level vector hexagon is divided into six large triangles. Each of them can be further divided into four small triangles. The vertexes of the small triangle are the nearest three vectors (NTVs) to synthesis the $V_{\rm ref}$. Taking the shaded area in Fig. 4(b) as an example and considering the orthogonal $\alpha$–$\beta$ coordinates in Fig. 3(a), the criterion to judge this sector is as follows:

$$\sqrt{3}M\cos\theta - M\sin\theta < 1, \quad \sqrt{3}M\cos\theta + M\sin\theta > 1 \quad (1)$$

where $M$ is the length of the $V_{\rm ref}$ normalized to dc-link voltage $V_{\rm dc}$, and $\theta$ is the rotation angle:

$$\theta = \tan^{-1}\frac{V_{\rm ref}(\beta)}{V_{\rm ref}(\alpha)}, \quad M = \frac{\sqrt{V_{\rm ref}^2(\alpha) + V_{\rm ref}^2(\beta)}}{V_{\rm dc}}. \quad (2)$$

From the aforementioned equation, it is noticed that the calculation involves complex trigonometric functions which increase the computation cost. Also, there are 24 small triangles in total.

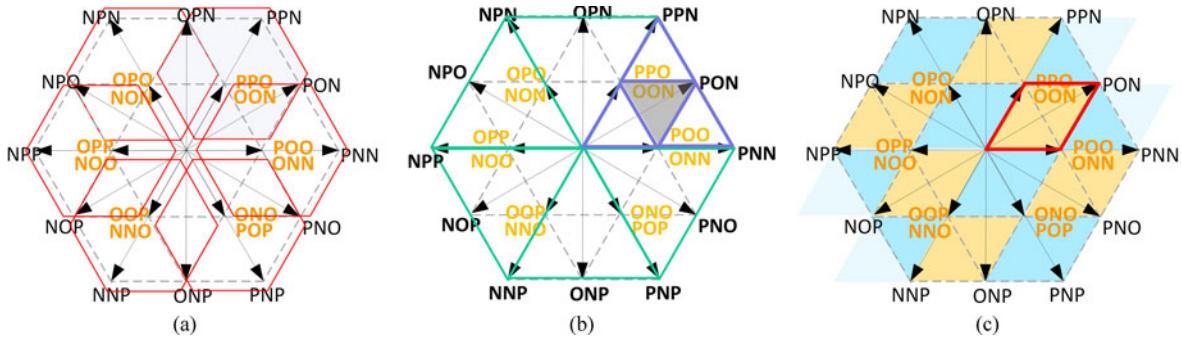


Fig. 4. Three types of sector division methods for three-level NPC vector space diagram. (a) Hexagon division. (b) Triangle division. (c) Parallelogram division.

The boundary conditions for each triangle are not the same. A case by case analysis is needed in calculation.

The parallelogram sector division [32] in Fig. 4(c) comes with the *g*–*h* coordinate. The space vector diagram is divided into 14 parallelograms instead of 24 triangles. The coordinate for $V_{\rm ref}$ in the *g*–*h* system is easily transformed from $\alpha$–$\beta$ system by the following transformation:

$$\begin{bmatrix} V_g \\ V_h \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & -1 \\ 0 & 2 \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}. \tag{3}$$

Because all the vectors in the *g*–*h* system have an integer coordinate, the vertexes of the parallelogram can be easily identified by rounding up or down the $V_g$ and $V_h$. There is one example in Fig. 3(b) to define the variables $V_{ul}, V_{lu}, V_{ll}$, and $V_{uu}$ in (4)[Comp: Please link equation (4).] for the given voltage reference:

$$\begin{aligned} V_{ul} &= \begin{bmatrix} \text{ceil}\,(V_g) \\ \text{floor}\,(V_h) \end{bmatrix}, \quad V_{lu} = \begin{bmatrix} \text{floor}\,(V_g) \\ \text{ceil}\,(V_h) \end{bmatrix} \\ V_{ll} &= \begin{bmatrix} \text{floor}\,(V_g) \\ \text{floor}\,(V_h) \end{bmatrix}, \quad V_{uu} = \begin{bmatrix} \text{ceil}\,(V_g) \\ \text{ceil}\,(V_h) \end{bmatrix}. \end{aligned} \tag{4}$$

The NTVs can then be located with the vector's location determined. Duty cycle calculation for NTVs is also simple with algebraic operation instead of trigonometric functions:

$$\begin{aligned} &d_{lu} = V_{uu}\,(g) - V_{\rm ref}\,(g), \quad d_{ul} = V_{uu}\,(h) - V_{\rm ref}\,(h) \\ &d_{uu} = 1 - d_{lu} - d_{ul}. \end{aligned} \tag{5}$$

The above calculation only involves algebraic operation. Also the whole calculation process can be applied to all the sectors. The case by case analysis is no longer needed. For these reasons, the calculation process is largely simplified. This simplification is important to save computation costs for the neutral point (NP) balance and loss reduction control of the proposed SVM since the switching frequency is high.

## III. Control Objectives With Small Vector Selection

With the reference vector's location determined and the duty cycle for the vectors calculated, the next step is the selection of the redundant vector to achieve different control objectives. It can be noticed in Fig. 2(b) that there are six small vectors in the vector space but 12 switching status corresponding to them. Each small vector has a pair of switching status and the redundancy of the small vector provides extra control freedom.

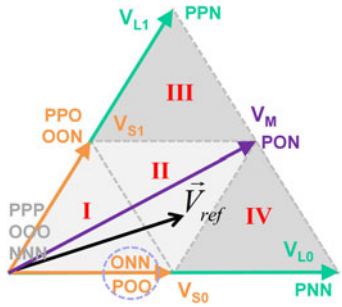


Fig. 5. 60° section of the space vector diagram.

Depending on applications and operating conditions, the redundant small vector can be used to balance the NP voltage, reduce EMI noise or reduce the switching loss. Based on the 200-kVA three-level NPC PCS, the principle for the control objectives is analyzed and the control results for the NP voltage, the CM noise, and the switching loss are compared in this section.

### A. NP Voltage Balance

To reduce the harmonics in the output voltage and current, the NP voltage must be controlled to be half of the dc-link voltage so that the voltage across the top dc-link capacitor equals to that of the bottom dc-link capacitor. Among the four types of vectors for three-level NPC converter, only the medium and small vectors connect the phase current to the NP. These two types of vectors influence the NP voltage balance as they charge or discharge the dc-link capacitors. The medium vector charges or discharges the two dc-link capacitors with different current and causes the imbalance. This imbalance can only be compensated by correctly selecting the small vector. Taking the circled small vector pair $V_{\rm S0}$ shown in the space vector diagram in Fig. 5 as an example, the switching status for them is shown in Fig. 6. This pair of small vectors connects phase A current to the NP and charges or discharges different dc-link capacitors depending on the phase current direction. The voltage difference for the two dc-link capacitors can be defined as $\Delta V = V_{\rm PO} - V_{\rm ON}$. If phase current $i_a > 0$, vector ONN reduces $V_{\rm ON}$ and increases $\Delta V$ while POO reduces $V_{\rm PO}$ and decreases $\Delta V$. Under $i_a < 0$ case, the result is just the opposite. The conclusion is that the two switching status in the small vector pair have an opposite

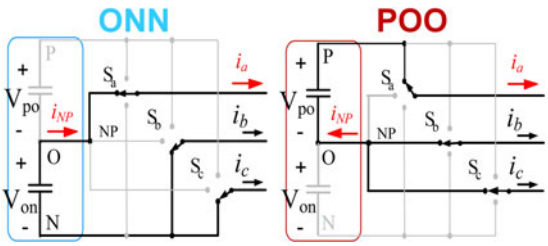


Fig. 6. Circuits for the switching status of small vector pair $V_{S0}$.

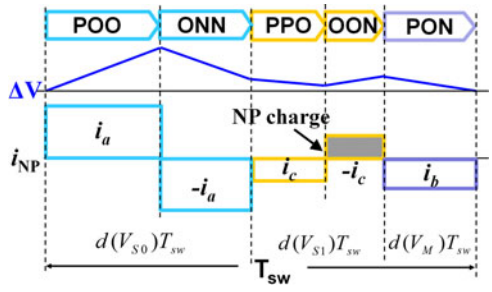


Fig. 7. NP voltage and current for active balance scheme.

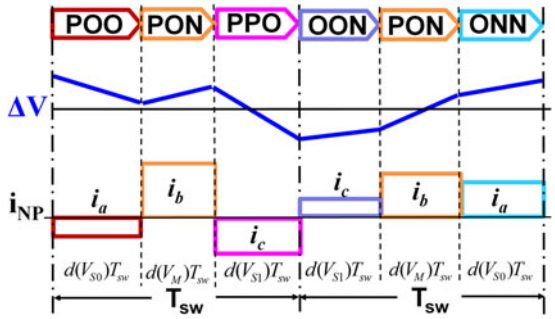


Fig. 8. NP voltage and current for hysteresis balance scheme.

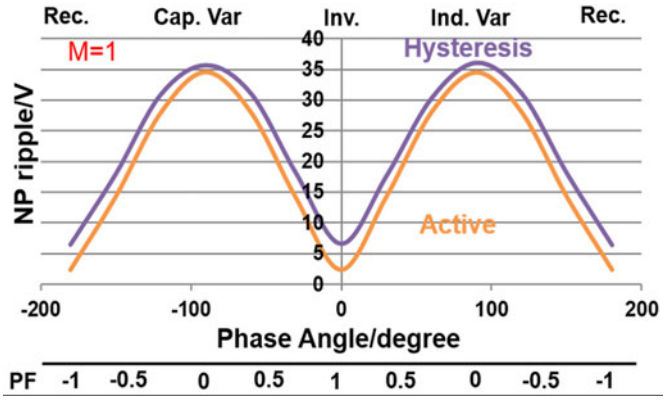


Fig. 9. NP voltage ripple comparison with different power factor.

influence on the NP voltage and this is the basis to balance the NP voltage.

There are three different approaches to select the small vectors for NP balancing. The passive balancing method alternately uses the two switching status in a pair in each new switching cycle. Since the influence of the two statuses is opposite, the NP voltage can be balanced naturally.

This method does not need sensing of the NP voltage and phase current. But it can only work under a perfectly balanced three-phase system and the balancing result is poor under system dynamics.

The active balance scheme uses both two switching status in the small vector pair in every switching cycle. Fig. 7 uses the region II in Fig. 5 to illustrate the concept. The gist of this control scheme is to achieve a net zero NP charge in one switching cycle so that $\Delta V$ returns to the initial value after the switching cycle. The charge can be calculated by sensing the phase current and knowing the duty cycle of each vector. The duty cycle ratio for the two switching statuses in the pair is solved by the following equations:

$$\Delta Q = [i_a d_{\mathrm{POO}} + i_c d_{\mathrm{OON}} - i_a d_{\mathrm{ONN}} - i_c d_{\mathrm{PPO}} - i_b d_{\mathrm{PON}}]T_{sw} = 0 \tag{6}$$

$$d_{\mathrm{POO}} + d_{\mathrm{ONN}} = d(V_{s0}), \quad d_{\mathrm{PPO}} + d_{\mathrm{OON}} = d(V_{s1}). \tag{7}$$

The active scheme has a perfect balancing result within one switching cycle. However, it introduces extra switching actions because it uses both the two switching status in one small vector pair. Also the control scheme is complex with a larger computation cost.

Compared with the active balance, the hysteresis balance scheme uses only one switching status in one switching cycle. Fig. 8 also uses triangle region II in Fig. 5 to show the concept for hysteresis balance. The selected small vector moves the NP voltage to the opposite direction of the imbalance. In each switching cycle, the switching status is selected based on the voltage different $\Delta V$ and the phase current. This method is robust to the system dynamics because it has neutral voltage feedback. The NP balancing result is not as good as that of the active scheme since the NP voltage has a strong harmonic component at half of the switching frequency. But this method has the benefit of having the least switching actions because it only uses one switching status for one small vector in one switching cycle.

Finally, different NP balancing schemes are compared together. The comparison is based on the simulation of the PCS mentioned earlier. The dc-link voltage is 1200 V and dc-link capacitor is 2.5 mF, which is the rated value for the PCS. Fig. 9 shows the NP voltage ripple comparison for the two schemes under different power factors. Fig. 10 shows the same comparison under different power factor and modulation index cases. The power factor is defined at the output of the converter. The figures show that the three-level NPC converter has an intrinsically large NP voltage ripple at a low power factor. When the power factor is zero, the load current is provided only by the dc-link capacitor and consequently results in the largest ripple. The in-depth explanation for this pheromone is that the medium vectors which cause the imbalance have stronger impact on NP charge at low power factor case while the small vectors that balance the NP have weaker impact on NP charge. The good balancing result of the active balance scheme is verified by the lower NP voltage ripple under all power factor and modulation index cases in Figs. 9 and 10. Other features for the three

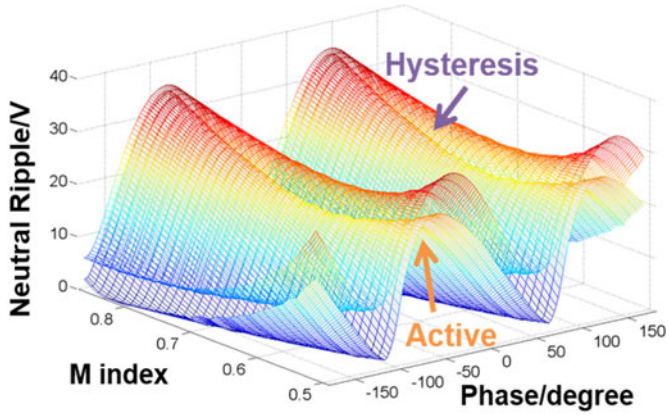


Fig. 10. NP voltage ripple comparison with different PF and M.

TABLE I
COMPARISON FOR THE THREE NP BALANCE SCHEMES

| Scheme | Sensors | $\Delta V_{NP}$ | Complexity | Loss |
|---|---|---|---|---|
| Passive | No | large | low | high |
| Hyst. | $i_{abc}/V_{dc}$ | small | medium | low |
| Active | $i_{abc}$ | small | high | high |

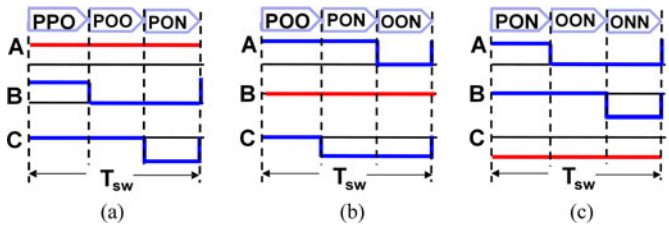


Fig. 11. Vectors and switching sequences for loss reduction. (a) Phase A unchanged. (b) Phase B unchanged. (c) Phase C unchanged.

balancing schemes are also compared in Table I. The active and hysteresis scheme with feedback has a better balancing result under system dynamics and different power factor case. But they are consequently more complicated in the control algorithm. The hysteresis scheme has a good balancing result and the least switching actions in each cycle. Therefore, it is chosen as the basis for the NP balance scheme proposed later in this paper.

### B. Switching Loss Reduction

The redundant vector can also be used for the switching loss reduction. The basic principle for this control objective is to avoid switching the largest phase current by properly selecting the small vectors. The small vector selection is based on the phase current information. Still taking the space vector diagram in Fig. 5 as example. For the triangle regions I and II, which contain two small vectors in its vertexes, each of the three phases can avoid switching in one cycle. Considering region II, if the current in phase A is the largest among the three phases, then the small vectors POO, PPO are selected together with the medium vector PON to keep phase A stay at positive as shown in Fig. 11(a). If phase B has the largest current, then OON and POO are selected with PON so that Phase B can stay at the neutral as shown in Fig. 11(b). It is the same case for phase C with the largest current shown in Fig. 11(c). For regions III and IV, which contain only one small vector, the redundant small vector can only avoid switching for one phase current out of two phases instead of three phases. In these regions, the control rule only switches the relatively smaller current, not necessarily the smallest among the three phases. Considering region III as example, the small vector can only keep phase A or phase C unchanged in the switching cycle. If phase A has a larger current, then the small vector PPO is selected together with the long vector PPN and medium vector PON.

This method avoids the switching of the larger phase current and hence reduces the switching loss incurred. The loss reduction result is analyzed by the detailed loss model built from the hardware double pulse test and simulation model on the three-level NPC converter. Detailed information on the hardware is introduced in Section V. The loss reduction result by simulation is given at the end of this section.

### C. Common Mode Noise Reduction

Besides the NP voltage ripple and switching loss, the common mode voltage can also be reduced or even eliminated by the redundant small vector selection. The CM voltage is defined as one-third of the summation of the three phase output voltage: $V_{\rm CM} = (V_{\rm AO} + V_{\rm BO} + V_{\rm CO})/3$. Different types of vectors result in different CM voltage. The long vectors generate $\pm 1/6 V_{\rm dc}$ CM voltage, where $V_{\rm dc}$ is half of the dc-link voltage. For the medium vectors, they generate 0 CM voltage. For the small vectors, they generate either $\pm 1/6 V_{\rm dc}$ or $\pm 1/3 V_{\rm dc}$ CM voltage. For the zero vectors, they generate either $\pm 1/2 V_{\rm dc}$ or 0 CM voltage. One method to deal with the CM noise only uses the medium vectors and the zero vector OOO since they do not generate any CM voltage. This method can totally eliminate the CM voltage noise. But it reduces the dc-link voltage utilization rate. Also this method does not use the NTVs, thus the switching loss and *dv/dt* is largely increased. Another method for the CM noise uses the NTVs. The small vector with the smaller CM voltage is selected so that the total CM noise is reduced.

### D. Control Result Comparison for Different Objectives

Finally, the different control objectives are compared together. SVM schemes for NP balance, loss reduction, and noise reduction are compared together with SPWM as a benchmark. The comparisons are based on the NP voltage ripple, the total system loss, and the CM noise. For NP balance, hysteresis balance scheme is used.

The NP voltage is first compared since it is the foundation to ensure the proper function of the converter. Fig. 12 compares the inverter output voltage and the neutral voltage difference for different modulation methods. The comparison is based on a 1200-V dc-link voltage and a 2.5-mF dc-link capacitor with unit power factor. That is the rate value for the PCS. The SVM for NP balance has the smallest NP voltage ripple which is below 3 V. On the contrary, the SVM for loss reduction and noise reduction has a very large NP voltage ripple and the output voltage waveform is even distorted. This is because these modulation methods select small vectors only for the loss or noise

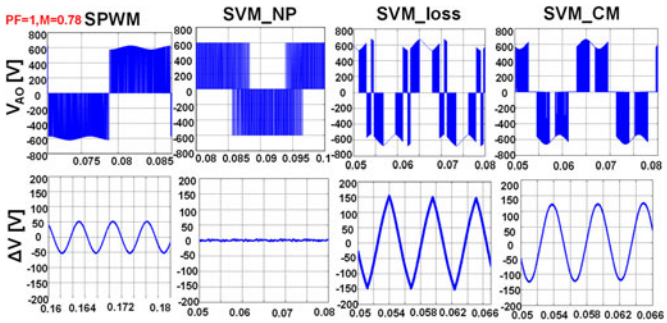


Fig. 12. NP voltage ripple comparison for different modulation methods.

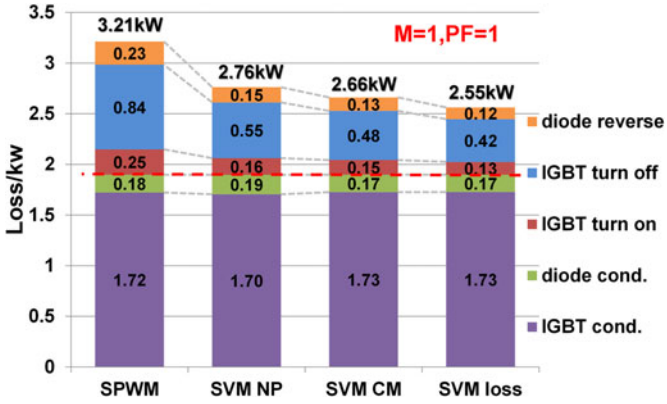


Fig. 13. System loss breakdown at unit power factor for three SVM schemes.

reduction; the NP voltage is unregulated. The figure shows that the voltage ripple for these two modulations is even larger than that of the naturally balanced SPWM. Because the NP balance is critical to the converter performance, the small vector selection for loss or noise reduction is not practical unless the dc-link capacitor is large enough or the two dc-link cells are supported with two separate dc sources so that ripple can be avoided. But the size and cost for such a large capacitor is another issue.

The system total loss under unit power factor and unit modulation index in line cycle is compared in Fig. 13 for different modulation methods. The conduction loss below the red dotted line in the figure for the three methods is the same. However, the switching loss is largely reduced if the small vectors are used for the purpose of loss reduction. For SVM with CM loss reduction, the small vectors are predetermined. But for SVM with NP balance, the small vectors are selected based on the hysteresis scheme. Therefore, the SVM with NP balance has a larger switching loss because of the extra switching events when changing small vectors. Fig. 14 shows the same comparison under all power factors. The SVM with loss reduction still has the lowest loss under all power factors. Unit power factor is the best case for loss reduction.

The CM noise reduction result for all these methods is finally compared. The CM voltage spectrum for the NP balance SVM and the CM noise reduction SVM is compared up to 1 MHz under the unit and zero power factor case. The spectrum is shown in Fig. 15. The SVM with CM reduction has less noise at whole frequency range when compared to the SVM for NP

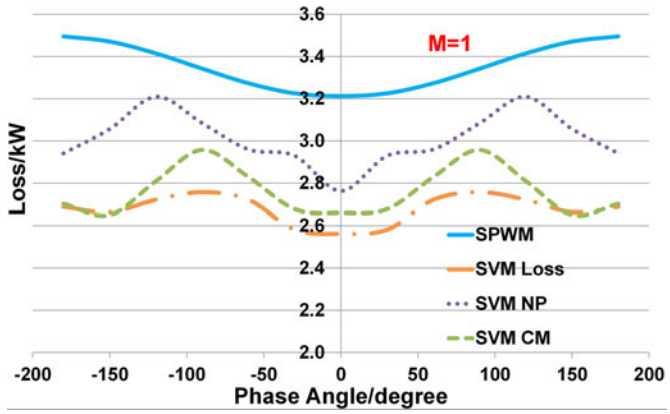


Fig. 14. System total loss at all power factors for three SVM schemes.

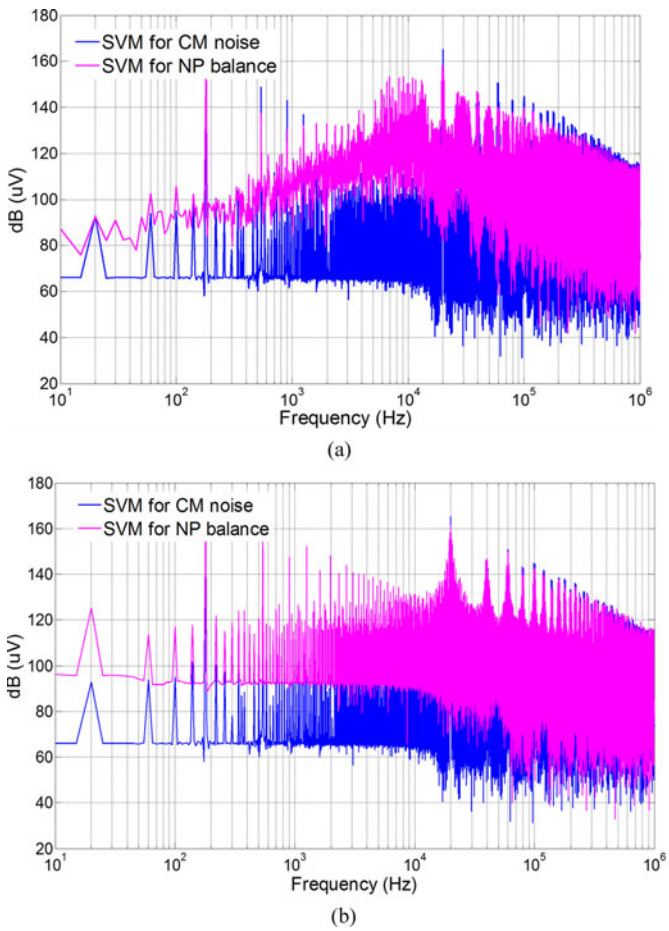


Fig. 15. CM noise spectrum comparison under different power factors. (a) CM voltage spectrum at unity power factor. (b) CM voltage spectrum at zero power factor.

balance. The CM reduction method works for both unit and zero power factor cases but the unbalanced NP voltage is an issue for this method. The voltage ripple is extremely large because the small vectors are used for noise reduction. Therefore, this method is also not practical unless large capacitor is used to support the dc-link voltage balance.

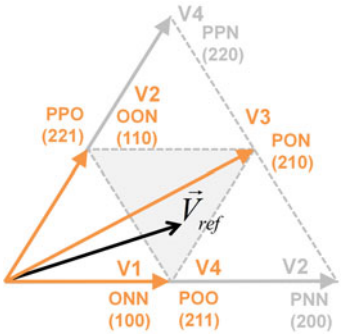


Fig. 16. 60° of the space vector diagram using number code system.

## IV. Improved SVM for Neutral Balance and Loss Reduction

The aforementioned analysis shows different control objectives for the SVM. The key to achieve these objectives is the small vector selection. Since the selection is based on single objective and the NP voltage balance is essential for the proper function of the converter, the small vector is most commonly used for NP balance. But for the 200 kVA, 20-kHz PCS, loss reduction is also important. This is the motivation to improve the SVM to achieve both NP voltage balance and loss reduction at the same time. A number system is first introduced for simplification and expression convenience. The switching status P-O-N are coded with number 2–1–0, respectively. Then the vectors can be labeled with the number code and can also be expressed by the summation of the switching status code for the three phases. For the space vector diagram in Fig. 5, the number expression of the vectors is shown in Fig. 16. Taking small vector OON as an example, the number code for it is 110 and the vector can be labeled as V2.

### A. Loss Reduction Within Switching Cycle

To achieve the NP voltage balance, the hysteresis balancing scheme is used for small vector selection as this method uses only one switching combination in each switching cycle and thus has less switching actions. Although the freedom for the small vector is used for the NP balance, the switching loss can still be minimized by proper pulse sequence alignment, which is another control freedom for SVM. With the NTVs determined by the NP balance, the pulse sequence can be aligned in different manners. It can be symmetrical or asymmetrical in one switching cycle. The pulse can be arranged with or without certain order. The different pulse sequence results in different THD and switching events in one cycle. Taking the shaded area in Fig. 16 as an example, and assuming ONN and OON are selected as small vectors by the NP balancing control, different switching patterns are then shown in Fig. 17. For pattern 1 in Fig. 17(a), there are three segments of switching status in the switching cycle. The NTVs are applied one by one. For patterns 2 and 3 in Fig. 17(b) and (c), they are symmetric in one switching cycle. Two of the NTVs are divided into two parts and are aligned symmetrically to the center. These alignments have

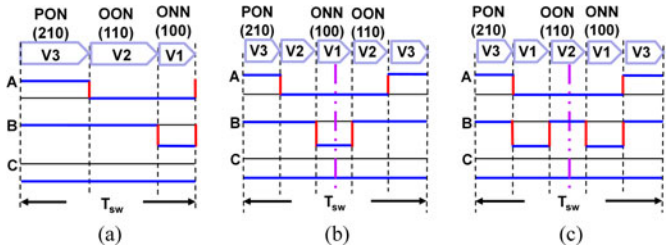


Fig. 17. Three types of pulse sequence alignment patterns in switching cycle. (a) Pattern 1. (b) Pattern 2. (c) Pattern 3.

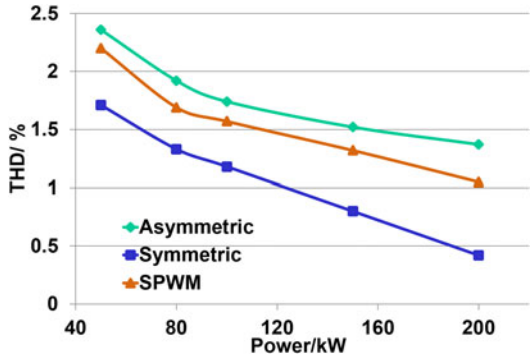


Fig. 18. Grid current THD for different sequence patterns.

five segments in one cycle. The difference between patterns 2 and 3 is the sequence order for the five pieces.

The grid current THD for these two alignments is compared under different power levels together with the SPWM as a benchmark. The converter is connected to the LCL filter with parameters given in the first section. The THD is calculated up to 50 kHz. The result in Fig. 18 shows that the symmetric sequence has a smaller THD compared with the asymmetric sequence at all power level. The SPWM method is also a symmetric sequence but has more switching events in each cycle; therefore, it has a THD in between the symmetric and asymmetric sequence.

Different pulse sequences also cause different switching events in the cycle. In the number system for vectors, it is easily noticed that the transition between vectors with an adjacent number has only one switching event. For example, the transition from V3 (PON) to V2 (OON) causes only switching from P to O in phase A. To minimize the switching events for loss and *dv/dt* reduction in each cycle, the vectors is sequenced in an order of consecutive vector number and only the vectors with adjacent number are involved. The pulse sequence patterns in Fig. 17(a) and (b) are arranged with the above order and the sequence in Fig. 17(c) does not follow the above order. It is clearly shown that the sequence with order only has four switching events in one cycle, which is the least that can ever be achieved for the three-level NPC modulation. In contrast, the sequence without order has two more switching events every cycle. This introduces an enormous switching loss and *dv/dt* for the high-frequency high-power NPC converter. The system total loss can be minimized by arranging the pulse sequence in the manner with the least switching events. A system loss

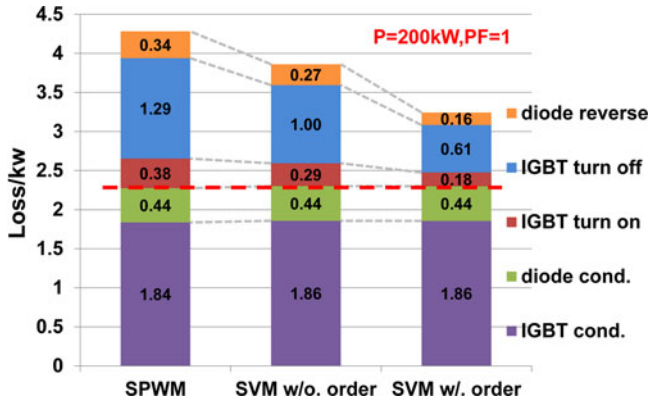


Fig. 19. System loss breakdown for three pulse sequence patterns.

TABLE II
LOSS REDUCTION RESULT COMPARISON FOR PULSE SEQUENCE PATTERNS

| | $P_{sw}$ | $P_{cond}$ | $P_{total}$ | $\eta$ |
|---|---|---|---|---|
| SPWM | 2.01kW | 2.27kW | 4.28kW | 97.8% |
| Pattern2 | 1.56kW | 2.30kW | 3.76kW | 98.0% |
| Pattern3 | 0.94kW | 2.30kW | 3.24kW | 98.3% |

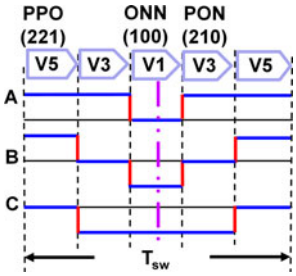


Fig. 20. Pulse sequence pattern 4.

breakdown for the converter at rated power is shown in Fig. 19 to compare the loss reduction result for the different pulse sequence patterns. The loss reduction result is also summarized in Table II. The result shows a 53% switching loss reduction and 0.5% efficiency improvement for the proposed pulse sequence with order compared to the SPWM method.

The above pulse sequence example is based on an arbitrary small vector selection given by the hysteresis NP balance. As mentioned earlier, this NP balance scheme relies on the phase current and NP voltage information for small vector selection. For the bidirectional PCS, various small vector combinations are possible with different power factors. In the shaded triangle area in Fig. 16, if the small vector PPO (V5) and ONN (V1) are selected together with the medium vector PON (V3), the pulse sequence for this pattern is shown in Fig. 20. Even if the pulse sequence alignment considers the vector number order, the order is not consecutive and therefore, the switching events in one cycle are doubled. With this small vector selection, the minimum switching events are eight instead of four. This is because the small vectors are selected only based on the NP voltage balancing without considering the pulse sequence order. To explore the operating condition under which the undesired scenario can happen, small vectors combinations are considered

TABLE III
SMALL VECTORS COMBINATION FOR HYSTERESIS NP BALANCE SCHEME

| | $i_a>0,i_c>0$ | $i_a<0,i_c<0$ | $i_a>0,i_c<0$ | $i_a<0,i_c>0$ |
|---|---|---|---|---|
| $\Delta V>0$ | V4(211)<br>V2(110) | V5(221)<br>V1(100) | V5(221)<br>V4(211) | V2(110)<br>V1(100) |
| $\Delta V<0$ | V5(221)<br>V1(100) | V4(211)<br>V2(110) | V2(110)<br>V1(100) | V5(221)<br>V4(211) |

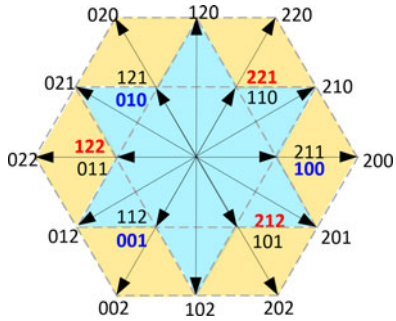


Fig. 21. Area division of space vector diagram for patterns 2 and 4.

under different phase current as noted in the shaded area in Fig. 16. In that region, phases A and C are connected to the NP. Therefore, $i_a$ and $i_c$ together with the NP voltage difference $\Delta V$ influence the small vector selection. All the possible small vector selections are listed in Table III. The undesired pattern 4 with more switching events happens when V1 and V5 are selected. Considering the switching status for the NTVs, it can be determined that phase A switches between P and O while phase C switches between O and N. For the three-level NPC converter, this means the reference voltage for phase A is in the positive half-line cycle and the phase C reference voltage is in the negative half-line cycle. In the meantime, the phase current for these two phases is in opposite polarity. This is to say the phase voltage and the phase current are not in phase with each other. With the earlier analysis, it is concluded that the undesired pattern 4 only happens under a nonunit power factor case. The simulation result reveals that the smaller the power factor is, the more frequently the pattern 4 case happens. When the power factor is 1, there is no pattern 4 in the whole line cycle. It can also be concluded that the pattern 4 happens when the NTVs contain two small vectors. In the space vector diagram in Fig. 21, the star shaped area has possibility of having pattern 4 while the rest of the areas are free for extra switching events. The figure shows that the modulation index is irrelevant to the undesired case. The only influential factor is the power factor. Fig. 22 shows the frequency of the undesired case happened in one line cycle under different power factors. The green areas have only desired switching pattern with the least switching events while the red area has the undesired pattern 4. The figure clearly shows that the lower the power factor is, the more frequently the undesired pattern 4 happens.

To avoid the undesired pattern 4, an improved SVM for NP balance and loss reduction is proposed to minimize the switching events in each switching cycle while maintaining the NP voltage balance. This method is based on the hysteresis control

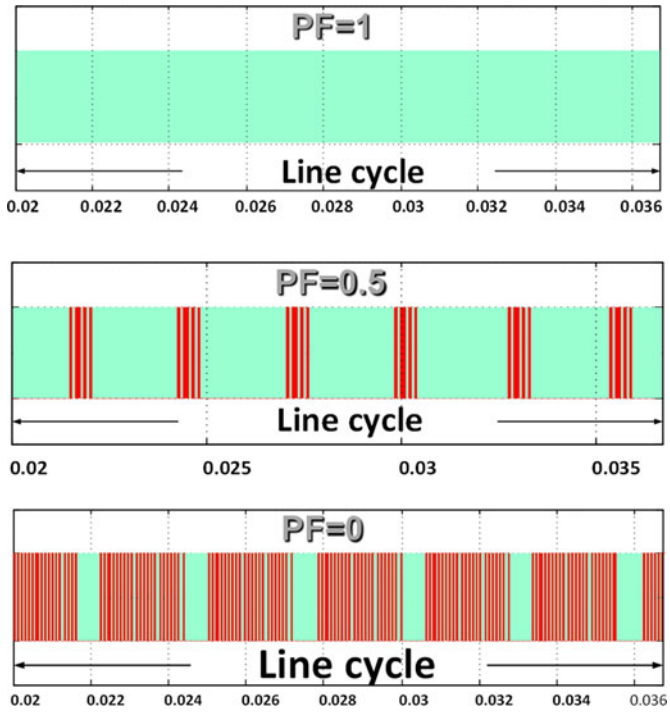


Fig. 22. Frequency for undesired pattern 4 to happen in one line cycle.

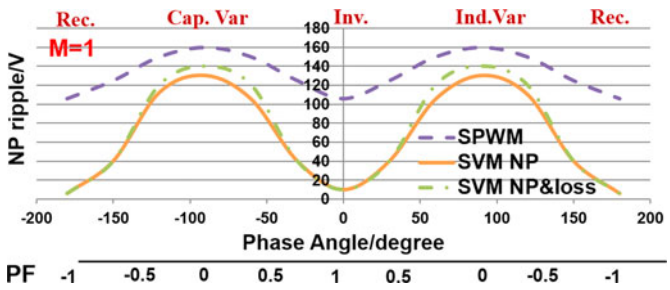


Fig. 23. NP voltage ripple comparison under different power factors.

for NP voltage balance. But it coordinately selects the small vector so that the NP voltage can be balanced and the pulse sequence can be properly aligned. Compared with the hysteresis control which selects a small vector solely for NP voltage balance, the improved method can achieve multiple objectives simultaneously. The details of this method are then introduced.

For the yellow colored region in Fig. 21, there is only one small vector and the consecutive vector number can always be guaranteed. The small vector selection only focuses on the NP balance. For the star shaped area, under the nonunit power factor case when a consecutive vector number is impossible, one of the small vectors in the NTVs is selected for NP balance and the other one is selected for loss reduction. Considering the previous region, the NP charge caused by the small vectors V1 and V5 is

$$Q_{V5} = i_c d(V_5) T_{sw}, \quad Q_{V1} = i_a d(V_1) T_{sw}. \tag{8}$$

The small vector with the larger NP charge is kept for NP balance and the other small vector is replaced by its counterpart in the small vector pair to ensure the consecutive vector number. In this particular case when V1 and V5 are selected by the

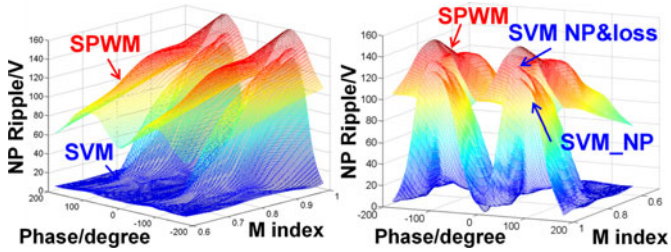


Fig. 24. NP voltage ripple comparison under different PF and M.

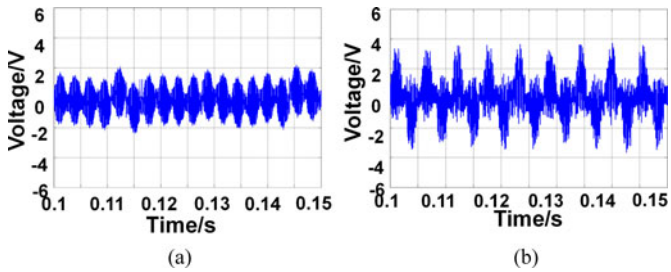


Fig. 25. NP voltage ripple comparison with full capacitive Var. (a) SVM only for NP balance. (b) SVM for NP balance and loss.

hysteresis control, if $Q_{V5}$ is larger than $Q_{V1}$, then it has a stronger influence on the NP voltage and is, therefore, kept for the NP balance. V1 is replace by V4 so that the vector number order is V3-V4-V5 instead of V1-V3-V5. By coordinately selecting the small vector, the consecutive vector number and the minimum switching events in one cycle can always be guaranteed. In principle, this method sacrifices a little NP voltage balancing result to gain loss reduction under a low-power factor case.

The NP balancing results for the SVM with hysteresis NP balance and the proposed SVM with NP balance and loss reduction are first compared. Fig. 23 gives the NP voltage ripple comparison at different power factor cases. It shows that the proposed balance scheme has the same NP voltage ripple at high-power factor. The ripple for the proposed scheme is larger at very low PF than that of the hysteresis balance. Fig. 24 gives the NP ripple comparison under all power factor and modulation index cases for the two balance scheme together with SPWM as benchmark. The proposed scheme has smaller ripple than SPWM and basically the same ripple as hysteresis control. The result shows this method sacrifices very little NP balance result to gain loss reduction. Fig. 25 gives a detailed time-domain NP voltage ripple waveform comparison for the conventional SVM and the proposed SVM under zero power factor. The proposed method sacrifices very little NP balancing result. The NP voltage ripple is still within 5 V.

The loss reduction result is also compared. Since the lower the power factor is, the higher frequency for the undesired case to happen, the total system loss breakdown is compared in Fig. 26 for the two schemes under zero power factor. The conduction loss stays the same while the switching loss is largely reduced since the switching events in certain switching cycles are reduced from 8 to 4 by the proposed method. For other power factors smaller than 1, the switching loss is also reduced by the

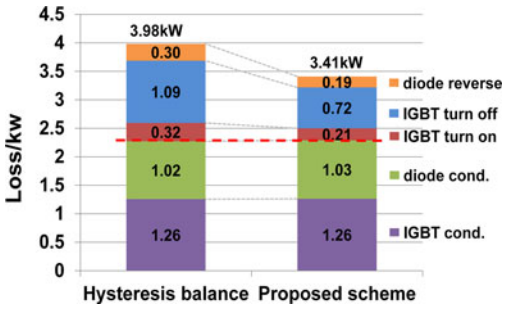


Fig. 26. System loss breakdown comparison at PF = 0.

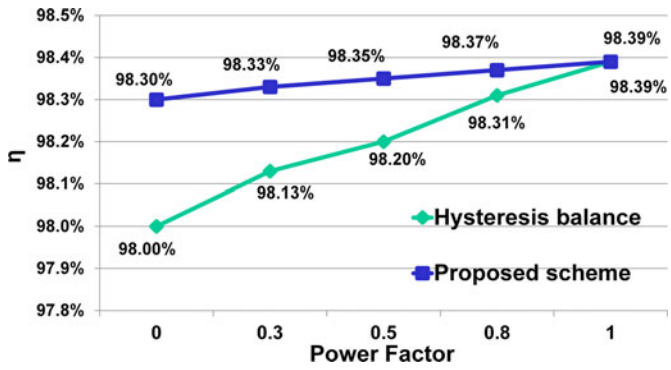


Fig. 27. System efficiency comparison at all power factor cases.

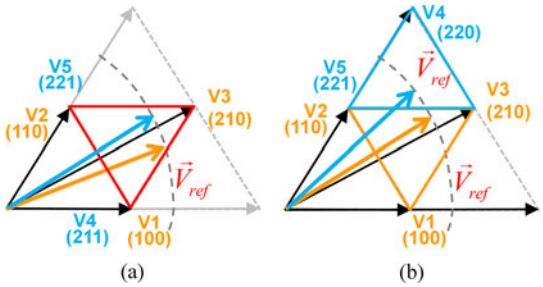


Fig. 28. Two scenarios for NTV change. (a) Switching status changed. (b) NTV sector changed.

proposed method. Fig. 27 gives the system efficiency comparison under different power factors to illustrate the loss reduction result. The proposed SVM has constant efficiency under all PF cases, while the SVM with hysteresis balance has larger loss at low PF case because of the extra switching events. The above comparison for the balancing result and loss reduction result shows that the proposed SVM method sacrifices little NP ripple but gains large efficiency improvement under small power factor case. This feature is important for the high-power high-frequency PCS with bidirectional power flow.

### *B. Loss Reduction Between Switching Cycles*

Besides minimizing the switching events in one switching cycle, the switching events between two switching cycles are also considered and eliminated for loss reduction. If the NTVs for two switching cycles are the same, the pulse sequence starts and ends with the same vector and no switching event occurs between the two cycles. But the NTVs for two switching

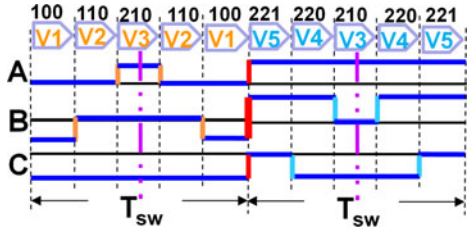


Fig. 29. Pulse sequence with extra switching events between cycles.

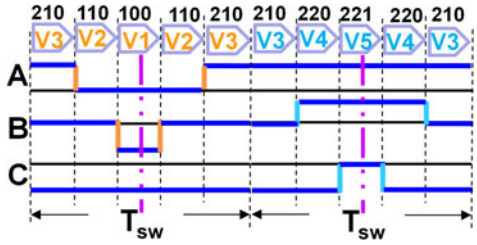


Fig. 30. Pulse sequence without extra switching events between cycles.

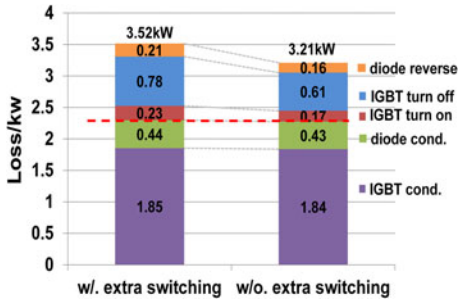


Fig. 31. Loss reduction result by eliminating switching between cycles.

cycles are not always the same. There are two scenarios that cause different NTV in two cycles. One scenario, shown in Fig. 28(a), happens when the small vectors are changed by the SVM control scheme like NP balance. Another scenario, shown in Fig. 28(b), happens when the voltage reference rotates from one triangle sector to another. The different NTVs may result in extra switching events if the last vector of one cycle is different from the first vector of the next cycle as shown in Fig. 29. Although the switching events in these two cycles are minimum, there is extra switching on each phase between the two cycles. Phase B even switched between P and N, which is not the nearest level and should be forbidden because of the possibility of phase leg shoot through. The above pulse sequence alignment rule only requests the consecutive vector number; it does not decide which vector starts first. If the pulse sequence ends and starts with the same vector within two cycles, the extra switching events between two cycles can be eliminated as shown in Fig. 30. This pulse sequence can be achieved by coordinately considering the two sets of NTVs of the adjacent two switching cycles.

The loss reduction result by eliminating the extra switching events between two switching cycles is given in Fig. 31. By eliminating the switching events between the two cycles, a 300-W switching loss is reduced. Besides the loss reduction benefit, further investigation on the phase leg loss distribution also reveals that by eliminating the extra switching events between

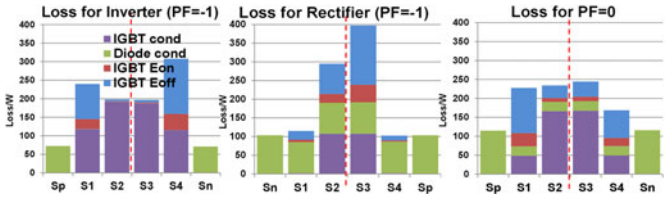


Fig. 32. Phase leg loss distribution w/. extra switching between cycles.

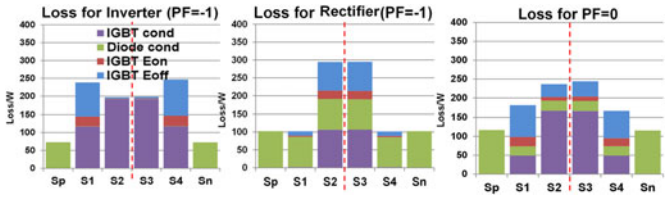


Fig. 33. Phase leg loss distribution w/o. extra switching between cycles.

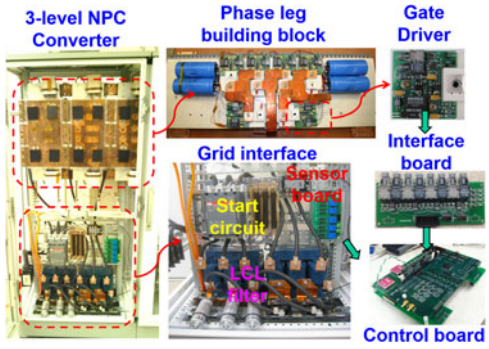


Fig. 34. Hardware structure of the three-level NPC converter.

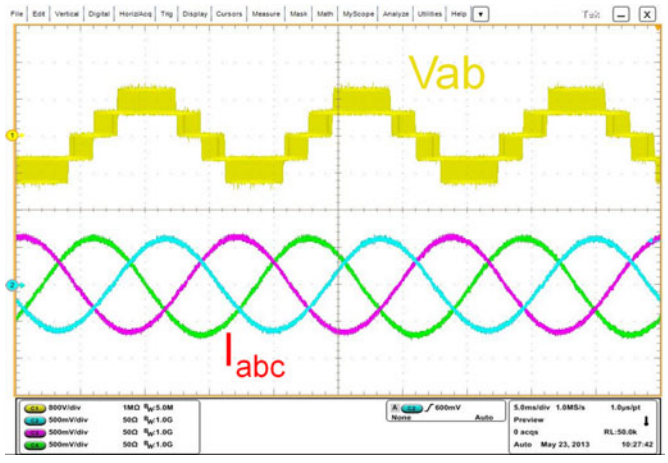


Fig. 35. Line–line voltage and three-phase current for SVM.

cycles, the loss distribution on the phase leg can be evenly distrusted on each device. For the NPC phase leg, the operation of the top cell and the bottom cell is symmetric in one line cycle. For the SPWM modulation, the loss distribution pattern for the top cell devices is the same as that of the bottom cell devices. But for the SVM method, if extra switching events exist between two cycles, the loss distribution pattern is uneven for the two cells because the extra switching events are not symmetrically applied to the top and bottom cells. Fig. 32 shows the phase leg

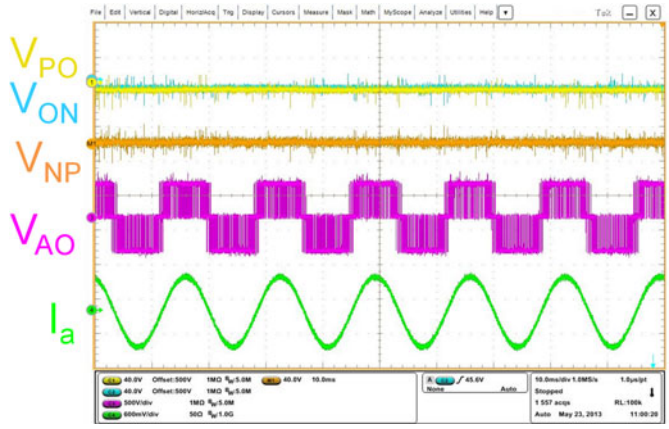


Fig. 36. NP voltage ripple and dc-link voltage for the proposed SVM.

loss distribution for a DNPC phase leg under different power factors case. With different PF, different devices undertake the extra switching loss. By eliminating the extra switching events between switching cycles, the phase leg loss distribution is symmetric for top and bottom cell devices as shown in Fig. 33. The symmetric loss distribution patterns facilitate the thermal design and give the devices even loss and thermal stress.

## V. Experimental Result Verification

The proposed SVM method with both NP balance and loss reduction is verified by both simulation models built in MATLAB/SIMULINK and an experimental prototype of the 200-kVA three-level NPC PCS. The hardware structure is shown in Fig. 34. The converter system contains several parts. The power stage is composed by the modularized three-level NPC phase leg building block. The building block is carefully designed in the device selection, layout structure, gate driver design, and turn ON/OFF optimization. The whole process ensures the minimum parasitic and switching loss of the phase leg. The gate drivers of the devices are interfaced with the control board by an interface board to provide gate signal and fault signal. The grid interface part includes the contactor, fuse, LCL filter, and a sensor board, which is also connected to the control board as feedback for the SVM control. The selected device for the IGBT and diode is the SKM400GA12 V from Semikron. The converter is connected to 480-V ac grid via the LCL filter. With the given dc-link voltage and the ac-side voltage, the modulation index is 0.8.

The NP balancing result for the proposed SVM method is tested under unit power factor. Limited by the test environment, the whole system is run at 65-kW power. But the phase leg building block is tested under full power. The loss model in simulation matches the experimental result well. Therefore, all the loss breakdown results in this paper are verified by experiment. For the NP balance result, the line-to-line output voltage and three-phase grid current for the proposed SVM is shown in Fig. 35. The voltage scale is 500 V/div, the current scale is 50 A/div, and the time scale is 10 ms/div in the figure. The NP balancing result for the proposed SVM is shown in Fig. 36 with the voltage for top and bottom dc-link capacitors displayed

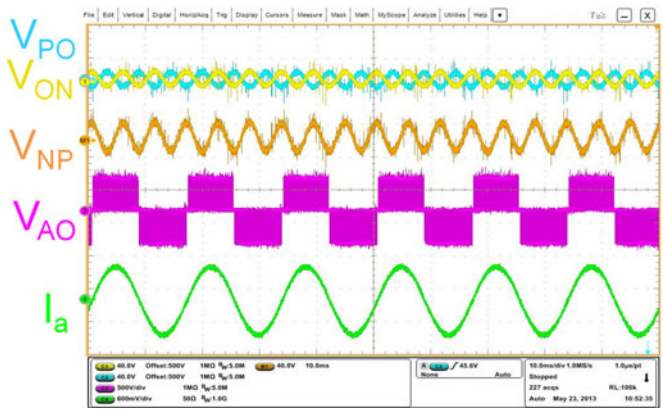


Fig. 37. NP voltage ripple and dc-link voltage for the SPWM.

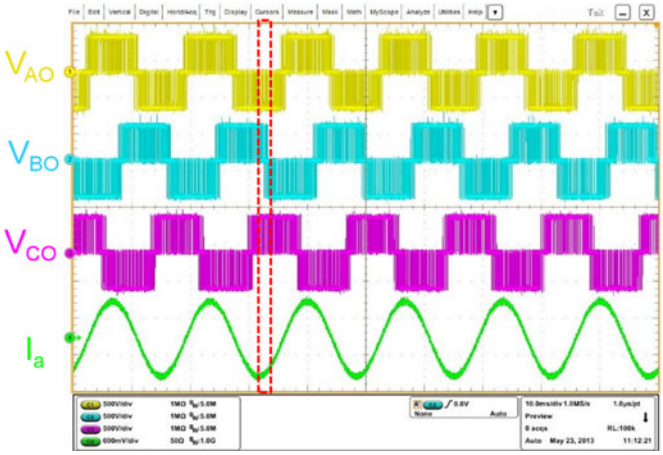


Fig. 38. Three-phase output voltage for the proposed SVM.

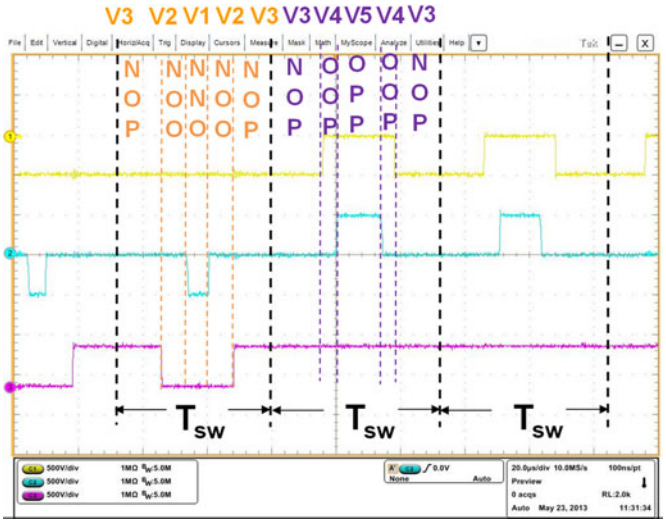


Fig. 39. Switching combinations within switching cycles.

together with the output voltage and NP voltage ripple. Fig. 37 shows the same result for the SPWM method. The experimental result shows that SPWM has a large NP voltage ripple. The proposed SVM method on the contrary has very little NP voltage variation, which verifies the NP balancing result.

To verify the proposed pulse sequence alignment, the three-phase output voltage is displayed in Fig. 38. The phase to neutral voltage is then zoomed in to observe the switching status of the three phases within the time interval of several switching cycles as shown in Fig. 39. The time scale shown in Fig. 39 is 20 $\mu$s/div. The result in the figure shows that the pulse sequence in each switching cycle only has four switching events. One phase stays constant in the cycle. Fig. 39 also shows the scenario for vectors change. The two switching cycles have different NTVs, but because of the proper sequence order, there are no extra switching events between the two cycles. This result verifies the proposed pulse sequence alignment for switching loss reduction.

## VI. Conclusion

This paper proposes a new SVM scheme for the three-level NPC converter with bidirectional power flow and high switching frequency. The different calculation methods are first compared and a simplified calculation method is adopted to save the computation cost for the control scheme. Different control objectives using the redundant small vectors are discussed. The principles for the NP voltage balance, switching loss reduction, and common mode noise reduction by SVM are introduced. Different control schemes are compared by simulation result. Based the conventional SVM for NP balance, an improved SVM method is proposed. This method balances the NP voltage while maintaining the minimum switching events in every switching cycle. The multiple control objectives are achieved simultaneously by properly selecting the small vector that considers both the NP charge and pulse sequence. Also the pulse sequence order is carefully treated so that the extra switching events between two switching cycles are eliminated. By doing so, the switching loss is further reduced and the phase leg loss is distributed more evenly on each device. With this modulation method, the NP voltage can be perfectly balanced and the switching loss/noise is largely reduced. The system efficiency stays the same under all power factor cases. The control result is verified by both simulation model and experimental prototype on a 200-kVA, 20-kHz three-level NPC converter.

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