Evaluation of the Low-Frequency Neutral-Point Voltage Oscillations in the Three-Level Inverter

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***Abstract*—The nearest vectors to the reference vector are commonly used in space-vector modulation (SVM) strategies. The main advantages of these modulation strategies are the low switching frequencies of the devices, the good output voltage spectra, and the low electromagnetic interference. However, when these techniques are applied to the three-level neutral-point (NP)-clamped inverter, low-frequency oscillations appear in the NP voltage for some operating conditions. As a result, the value of the dc-link capacitors must be increased in order to attenuate such oscillations. In this paper, these amplitudes are quantified for two modulation strategies that use nearest vectors to the reference vector. Owing to the nondimensional variables used in the analysis, the information provided will help for the calculation of the dc-link capacitors in a given specific application. Simulated and experimental examples are presented.**

***Index Terms*—DC-link capacitors, low-frequency oscillation, nearest vectors, neutral-point balance, three-level inverter.**

I. Introduction

SINCE ITS introduction in 1981 [1], the neutral-point-clamped (NPC) voltage-source inverter (Fig. 1) has demonstrated some advantages over the conventional two-level inverter for high-power applications. To maximize the performance of this converter, the voltages of the two series-connected dc-link capacitors must be confined to one half the level of the dc-link voltage. In some applications, the neutral-point (NP) voltage is imposed by a solid neutral terminal at the dc side provided by two independent rectifiers [2]. This solution requires a transformer with two isolated secondary windings that increases the overall cost of the system. This special transformer can be avoided with a back-to-back connection of NPC converters [3], [4]; nevertheless, the cost of this connection is also high, because it requires an active NPC rectifier with the same topology than the inverter. This solution is especially interesting for regenerative motor drives applications.

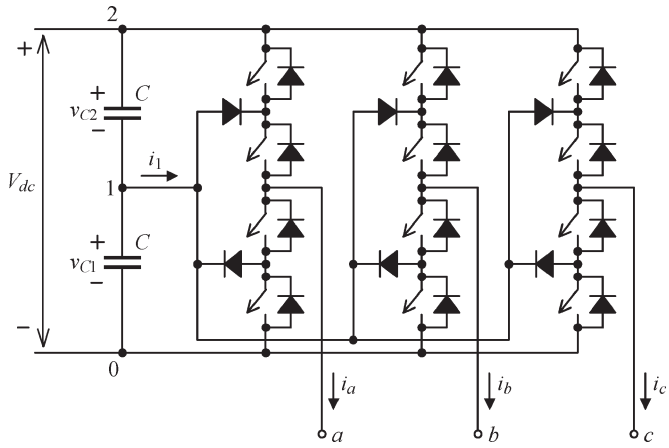

Fig. 1. NPC inverter.

This paper is focused on those cases in which the NP of the three-level converter is floating, and voltage balancing between the capacitors should be controlled by the converter itself. Several publications discuss ways to solve this balance problem [5]–[8]; however, this objective may be unattainable when operating with high modulation indices [8]. In such conditions, a low-frequency ripple appears in the NP potential. Because of this oscillation, the output line-to-line voltages will also contain low-frequency harmonics [9], and additionally, the devices of the bridge and the capacitors themselves must withstand higher voltages than when balance is achieved.

The switching frequency of the devices produces NP voltage ripple with higher frequency than this oscillation. Thus, the dc-link capacitors must be sized for the attenuation of such low-frequency oscillation. Some useful graphics are presented in this work to help for the calculation of the value of the dc-link capacitors. As the variables presented in the figures are nondimensional variables, the results of this analysis can be used for any specific application.

II. Space-Vector Modulation (SVM)

Assuming balanced voltages in the dc-link capacitors, the vector diagram in Fig. 2 is obtained. Each sextant of the diagram is divided into four regions in order to show the vectors nearest to the reference vector ($\vec{V}_{\mathrm{REF}}$), which must be

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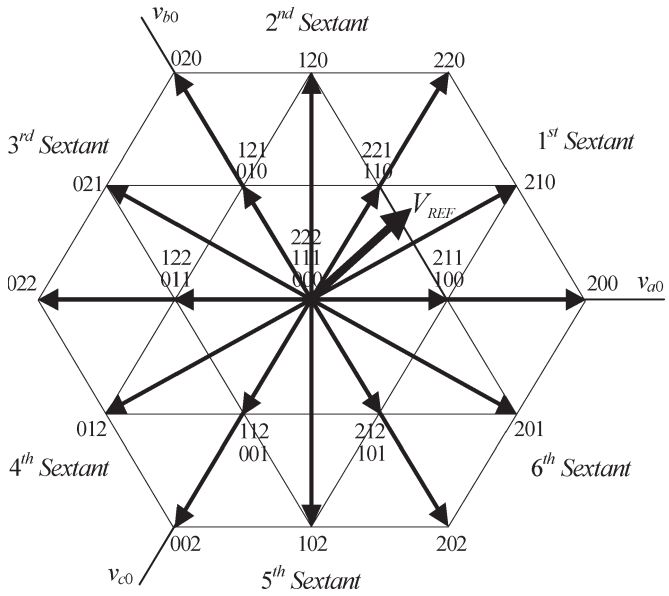

Fig. 2. Space-vector diagram of the NPC converter.

generated for each modulation period. The large vectors (200, 220, 020, 022, 002, and 202) and the zero vectors (000, 111, and 222) of the diagram do not affect the voltage balance of the capacitors, because they do not produce NP current (i_1).

The medium vectors (210, 120, 021, 012, 102, and 201) of the diagram cause voltage imbalances due to the connection of one output phase to the NP. The short vectors (100–211, 110–221, 010–121, 011–122, 001–112, and 101–212) are produced by different states of the converter; nevertheless, they generate the same output line-to-line voltages. Any modulation strategy must base voltage balance on careful utilization of these redundant vectors, since the current produced in the NP has opposite direction depending on which vector is applied. Preserving the NP voltage balance requires the average NP current to be zero.

The use of the nearest vectors to the reference vector [10] is the preferred modulation strategy from the standpoint of the switching frequencies of the power devices, output voltage spectra, and electromagnetic interference (EMI). In this work, the optimal nearest redundant vectors for the balance are chosen for each modulation cycle [8], [9]. Therefore, optimal balancing results are achieved.

Two modulation techniques are analyzed in this approach, namely: 1) three-nearest-vector (NTV) modulation and 2) symmetric modulation.

III. Modulation Techniques

A. NTV Modulation

The NTV modulation technique uses only three of the closest vectors to the reference vector per modulation cycle. Thus, a single short vector is selected from each pair of redundant vectors. The choice is made according to the objective of maintaining balanced voltages in the dc-link capacitors; therefore, the present voltage imbalance and the direction of the instantaneous output currents must be known. The NP

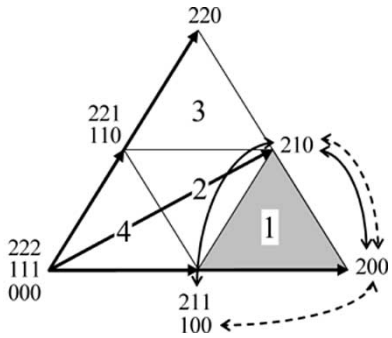

Fig. 3. Example of NTV modulation. Vectors and sequences used for the modulation when the reference vector is located in region 1.

TABLE I
Sequences of Vectors in the First Sextant by NTV Modulation

Region	Short Vectors	Sequences	Steps
1	100	100-200-210 // 210-200-100	2 // 2
	211	200-210-211 // 211-210-200	2 // 2
2	100-110	100-110-210 // 210-110-100	2 // 2
	100-221	100-210-221 // 221-210-100	4 // 4
	211-110	110-210-211 // 211-210-110	2 // 2
	211-221	210-211-221 // 221-211-210	2 // 2
3	110	110-210-220 // 220-210-110	2 // 2
	221	210-220-221 // 221-220-210	2 // 2
4	100-110	100-110-111 // 111-110-100	2 // 2
	100-221	100-111-221 // 221-111-100	4 // 4
	211-110	110-111-211 // 211-111-110	2 // 2
	211-221	111-211-221 // 221-211-111	2 // 2

current (i_1) must be positive in order to discharge the lower capacitor, and must be negative to charge it. For example, if i_a is positive, vector 100 will discharge the lower capacitor $(i_1 = i_a > 0)$, and vector 211 will charge it $(i_1 = i_b + i_c = -i_a < 0)$.

Assuming that the reference vector is located in region 1 (Fig. 3), if the short vector 100 were selected for the NP balance, the vectors used for that modulation period would be 100–200–210. On the other hand, if vector 211 were instead selected, the set of vectors used for the modulation would be 200–210–211.

Table I shows all the sequences of the vectors in the first sextant that are more capable of minimizing the switching frequencies of the devices. These sequences depend on the short vectors that are selected according to voltage-balance requirements. The number of changes or steps between consecutive vectors associated with each sequence is also indicated in this table. The worst cases are region 2 (vectors 100–221) and region 4 (vectors 100–221), both of which require four switching steps, which is twice the number required by any other sequence. When a sequence is repeated in a subsequent modulation period, the sequence is flipped in order to minimize the number of steps from one cycle to the next.

Despite the simplicity of using only three vectors per modulation cycle, two drawbacks exist.

1) There are significant switching-frequency ripples in the voltages of the capacitors.
2) When changing sequences due to a new region or different selection of short vectors, two switching steps can be produced (two legs must switch one level). Due to this, and the fact that there are some sequences that require

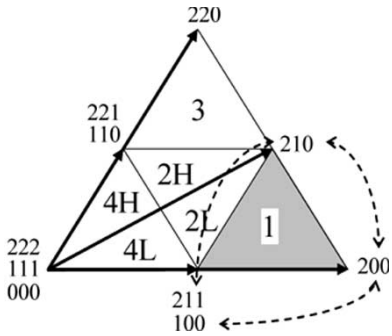

Fig. 4. New regions for symmetric modulation. Example of vector sequence for region 1.

four steps (Table I), the switching frequencies will not be constant.

The symmetric modulation approach can overcome these disadvantages and practically keep the switching frequencies constant.

B. Symmetric Modulation

Symmetric modulation is characterized by using four vectors per modulation sequence. This modulation is very similar to NTV in some respects. The new vector added to the sequence is one of the short vectors that was not selected using NTV. Thanks to this, the duty cycles are basically calculated by the same process, with the only difference being that the duty cycle applied in NTV to only one of the double vectors is now shared between both of them. For instance, if the reference vector lies in region 1, the sequence will be 100–200–210–211. To satisfy the zero-NP-current condition, the duty cycle calculated for the couple 100/211 ($d_{100/211}$) should now be properly shared between them. This duty cycle can be distributed according to a variable x

$$d_{100} = d_{100/211}\frac{1-x}{2} \text{ and } d_{211} = d_{100/211}\frac{1+x}{2}. \quad (1)$$

Since the duty cycles must always be positive, this distribution variable considers values in the interval $x \in [-1, 1]$. The precise value for this variable can be calculated for each modulation period in accordance to the objective of achieving balanced voltages in the dc-link capacitors at the end of any modulation period.

In order to reduce the switching frequencies of the devices, regions 2 and 4 are now split into 2L, 2H, 4L, and 4H (Fig. 4). The line that divides such regions, which coincides with vector 210, has been drawn according to a geometric-symmetry criterion. The best vector sequences in the first sextant are given in Table II. All of these sequences require the same number of switching steps.

Although symmetric modulation generates better output voltage spectra than NTV, it usually produces larger amplitudes of low-frequency oscillations in the voltages of the capacitors. This fact is a consequence of the lesser degree of freedom in the utilization of redundant vectors, since one of the double vectors cannot be chosen in regions 2L, 2H, 4L, and 4H. A simulation example that sustains this statement is presented in Fig. 5.

TABLE II
SEQUENCES OF VECTORS IN THE FIRST SEXTANT BY SYMMETRIC MODULATION

Regions	Sequences	Steps
1	100-200-210-211 // 211-210-200-100	3 // 3
2L	100-110-210-211 // 211-210-110-100	3 // 3
2H	110-210-211-221 // 221-211-210-110	3 // 3
3	110-210-220-221 // 221-220-210-110	3 // 3
4L	100-110-111-211 // 211-111-110-100	3 // 3
4H	110-111-211-221 // 221-211-111-110	3 // 3

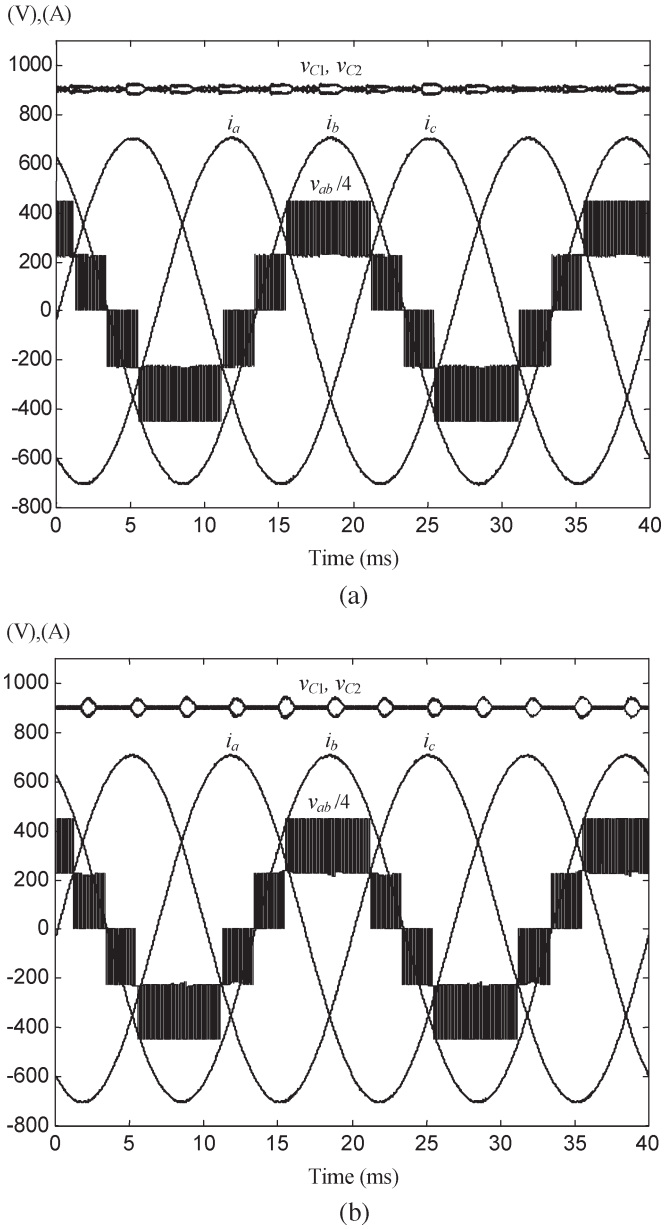

Fig. 5. Simulation results for: (a) NTV modulation and (b) symmetric modulation.

In this example, the converter is supplied by a dc voltage source $V_{\rm dc} = 1800$ V and operates with an $R-L$ wye-connected load with parameters $R = 1\ \Omega$ and $L = 2$ mH. The dc-link capacitors are $C = 1000\ \mu$F and the fundamental frequency of the output voltages is $f = 50$ Hz. This figure shows the voltages of the dc-link capacitors (v_{C1} and v_{C2}),

a line-to-line voltage (v_{ab}), and the output currents (i_a, i_b, and i_c) when the converter operates with a switching or sample period $T_s = 50$ μs (or sample frequency $f_s = 20$ kHz).

IV. NP Current Model

In this section, the limits of the ability to control the NP balance for both modulation techniques are shown.

When the reference vector is located in the first sextant, the local averaged NP current $\bar{i}_1$ can be expressed as

$$\bar{i}_1 = \mathbf{D}\mathbf{i}_{abc}$$

with

$$\mathbf{D} = [(d_{100} - d_{211}) \quad d_{210} \quad (d_{221} - d_{110})]$$

and

$$\mathbf{i}_{abc} = [i_a \quad i_b \quad i_c]^{\mathrm{T}}. \tag{2}$$

To validate this expression for the entire vector diagram, the equivalent alternating current (ac) for each sextant must be taken into account. A new transformation matrix $\mathbf{S}$ is introduced for interchanging the currents, depending on which sextant the reference vector occupies

$$\bar{i}_1 = \mathbf{D}\mathbf{S}\mathbf{i}_{abc} \text{ with } \mathbf{S} = \begin{bmatrix} s_1 + s_6 & s_2 + s_3 & s_4 + s_5 \\ s_2 + s_5 & s_1 + s_4 & s_3 + s_6 \\ s_3 + s_4 & s_5 + s_6 & s_1 + s_2 \end{bmatrix} \tag{3}$$

where s_i defines the sextant in which the reference vector lies, such that

$$s_i = \begin{cases} 1, & \text{if } \vec{V}_{\mathrm{REF}} \text{ lies in the sextant } i \\ 0, & \text{otherwise} \end{cases}, \quad i = \{1, 2, 3, 4, 5, 6\}. \tag{4}$$

As in steady-state conditions, the term $\mathbf{i}_{abc}$ in (2) will be time dependent; thus, a rotating coordinate transformation can be included to handle the constant values for those variables, given as

$$\bar{i}_1 = \mathbf{D}\mathbf{S}_T\mathbf{i}_{dq} \tag{5}$$

where $\mathbf{S}_T = \mathbf{S}\mathbf{T}_{dq}^{-1} = \mathbf{S}\mathbf{T}_{dq}^{\mathrm{T}} = \mathbf{T}_{dq}\mathbf{S}^{\mathrm{T}}$ and $\mathbf{i}_{dq} = \mathbf{T}_{dq}\mathbf{i}_{abc}$.

Equation (5) is general for the three-level diode-clamped converter, since it allows the local averaged NP current to be analyzed for any SVM technique.

V. Low-Frequency NP Voltage Amplitude

The equivalent dynamic circuit of the NP connection is shown in Fig. 6. In this model, the dc-link voltage is assumed constant, which can be achieved either by a dc power supply or by controlling this voltage by a proper control loop.

It can be noticed that the values of each of the capacitors are not important from the standpoint of NP voltage balance since they are virtually connected in parallel. Thus, the equivalent value is

$$C_{\mathrm{NP\ equiv}} = C + C = 2C. \tag{6}$$

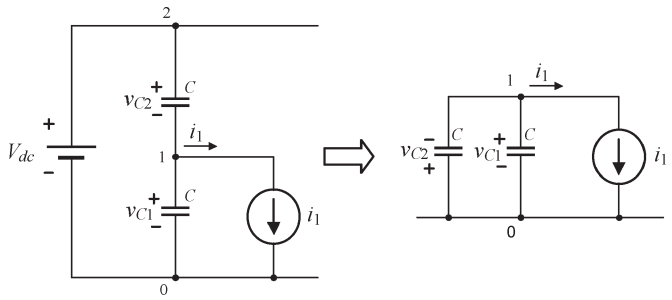

Fig. 6. Dynamic model of the NP in the three-level converter.

On the other hand, the capacitors are connected in series from the dc-link standpoint, therefore

$$C_{\mathrm{dc\ equiv}} = \frac{C \cdot C}{C + C} = \frac{C}{2}. \tag{7}$$

In conclusion, slightly different values of the capacitors hardly affect the dynamics of the NP voltage. Nevertheless, they should not be much different; otherwise, their filtering effect on the dc-link voltage will be diminished due to the series connection.

The scheme presented in Fig. 7 is used to determine the amplitude of the NP voltage oscillations. This diagram is based on the mathematical NP current model (5), and the precise modulation strategy under analysis is defined in the space-vector modulator block.

Fig. 8(a) shows the maximum NP voltage ripple that could occur because of the NP current when the converter operates by NTV modulation. The normalized amplitude of the ripple ($\Delta V_{\mathrm{NPn}}/2$) is defined as

$$\frac{\Delta V_{\mathrm{NPn}}}{2} = \frac{\frac{\Delta V_{\mathrm{NP}}}{2}}{\frac{I_{\mathrm{rms}}}{fC}} \tag{8}$$

where ΔV_{NP} is the peak-to-peak low-frequency NP voltage oscillation, f is the fundamental output frequency, I_{rms} is the root mean square (rms) output currents, and C is the value of the dc-link capacitors.

Fig. 8(b) provides helpful information for determining the value of the capacitors for a practical application. For example, assuming the worst operating conditions of unity modulation index ($m = 1$) and current angle $\varphi = -84^\circ$ or $\varphi = +96^\circ$, the maximum normalized ripple is

$$\frac{\Delta V_{\mathrm{NPn}}}{2} = \frac{\frac{\Delta V_{\mathrm{NP}}}{2}}{\frac{I_{\mathrm{rms}}}{fC}} = 0.0297. \tag{9}$$

If the values were $I_{\mathrm{rms}} = 220$ A, $f = 50$ Hz, and $C = 1000$ μF, the amplitude of the NP voltage ripple would be

$$\begin{aligned} \frac{\Delta V_{\mathrm{NP}}}{2} &= \frac{\Delta V_{\mathrm{NPn}}}{2}\frac{I_{\mathrm{rms}}}{fC} \\ &= 0.0297\frac{220}{50 \cdot 1000 \cdot 10^{-6}} \\ &= 130.7 \text{ V}. \end{aligned} \tag{10}$$

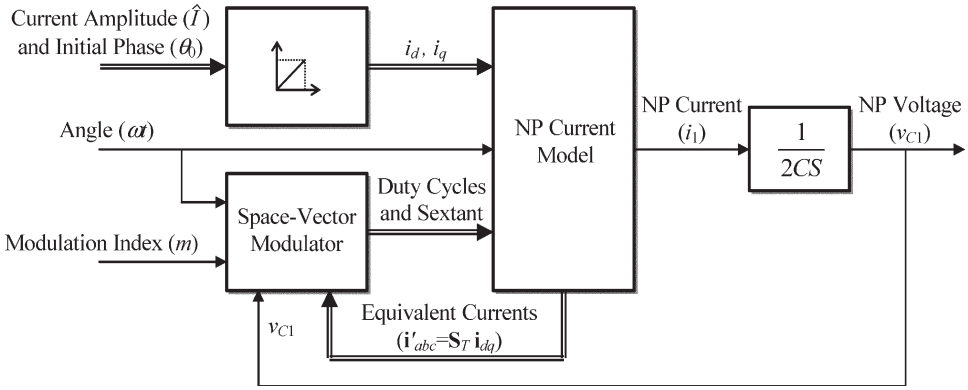

Fig. 7. Diagram used to determine the amplitude of the low-frequency NP voltage oscillations.

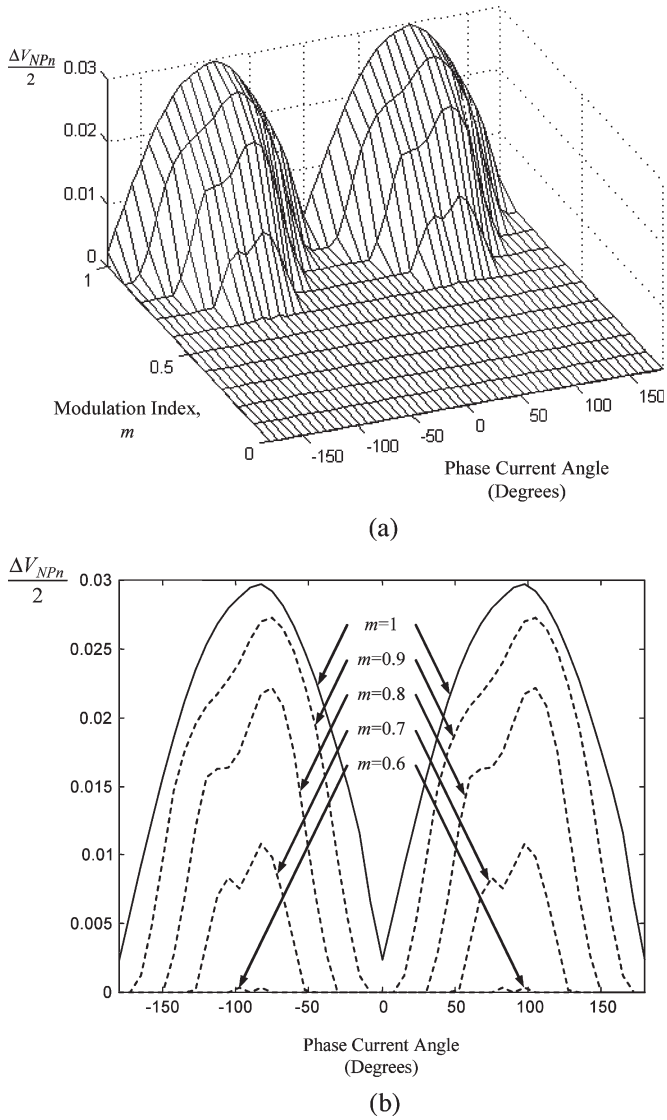

Fig. 8. Normalized NP voltage ripple for NTV.

It can be observed that the value of the total dc-link voltage $V_{\rm dc}$ does not affect the NP voltage oscillation. This statement is true under the assumption that the output currents are sinusoidal, and they are not affected by this oscillation, which can be acceptable in the case of relatively small NP voltage amplitudes. Significant inductive loads contribute to make output currents less sensitive to NP voltage imbalances.

If in this example, the maximum amplitude allowed to the NP voltage oscillation were 100 V, the value of the dc-link capacitors could be calculated from (10). Hence, the minimum value for those capacitors would be 1307 μF.

The normalized amplitude of the low-frequency NP voltage ripple for symmetric modulation is presented in Fig. 9. This figure shows the existence of this oscillation for a more extensive operating area compared to NTV modulation. Nevertheless, the maximum value of the ripple is the same than with NTV ($\Delta V_{\rm NPn}/2 = 0.02973$), and it is produced under the same operating conditions ($m = 1$ and current angle $\varphi = -84^\circ$ or $\varphi = +96^\circ$).

In fact, the amplitude of the NP voltage oscillation when $m = 1$ is practically the same for both modulation techniques, independently of the phase current angle. This is because the duty cycles of the short vectors are very small or even zero for the maximum modulation index, and therefore, there is very little NP current control. Furthermore, since the NP voltage cannot be maintained at its reference under such conditions, when dealing with symmetric modulation, any duty cycle calculated for a couple of short vectors is entirely applied to a single short vector. Hence, symmetric modulation becomes NTV, because it makes use of only three vectors per modulation cycle.

VI. Experimental Results

The amplitude of the low-frequency NP voltage oscillation has been verified by simulation and experimentally. For the experimental results, the modulation algorithm is programmed in a 32-bit floating-point digital processor (Sharc ADSP 21062) with 25-ns instruction processing time. The value of the dc-link capacitors is $C = 1650$ μF and the total dc-link voltage is maintained to $V_{\rm dc} = 50$ V by a dc power source. An asynchronous motor is connected as a load. The switching or sample period is 50 μs (20-kHz sample frequency) and the fundamental output frequency is $f = 60$ Hz. The modulation index is maximum $m = 1$, so that both modulation strategies, NTV and symmetric modulation, generate the same voltage amplitude in the NP.

Fig. 10 shows two output currents (i_a and i_c) and the voltages of the capacitors (v_{C1} and v_{C2}). The rms output phase

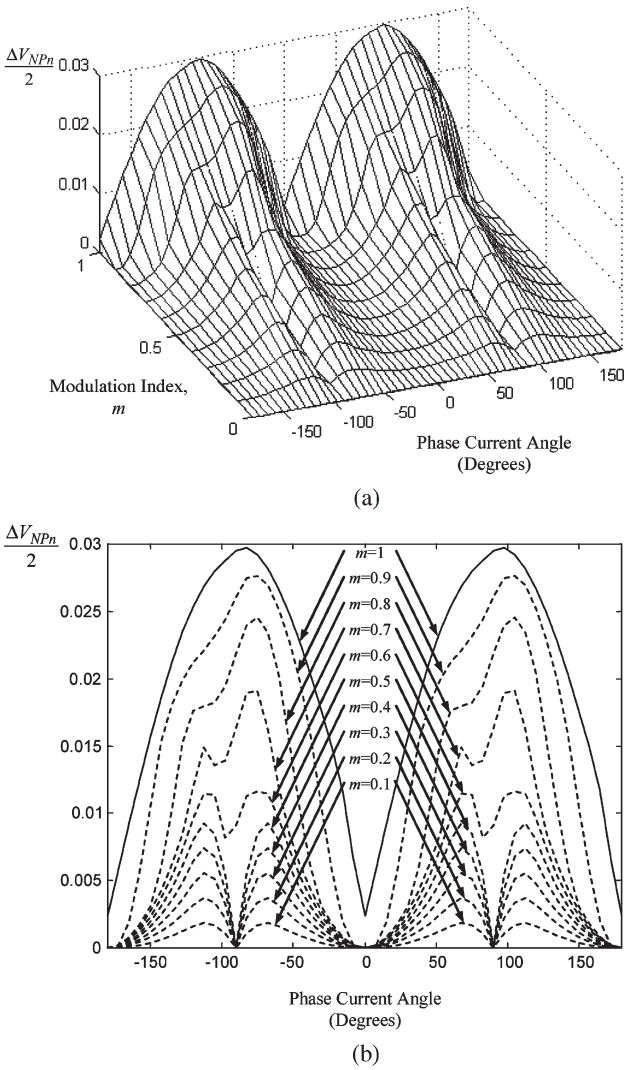

Fig. 9. Normalized NP voltage ripple for symmetric modulation.

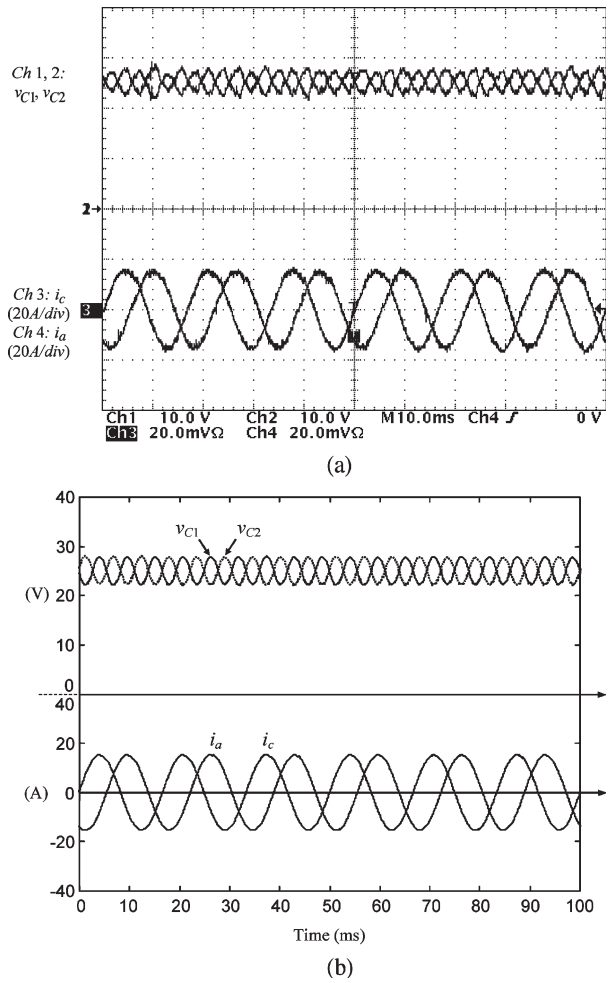

Fig. 10. Low-frequency NP voltage oscillations in the voltages of the capacitors. (a) Experimental results. (b) Simulation results.

current in the operating point is $I_{\rm rms} = 11.3$ A, with angle $\varphi = -45^\circ$. In such conditions, the amplitude of the NP voltage ripple should be

$$\begin{aligned}\frac{\Delta V_{\rm NP}}{2} &= \frac{\Delta V_{\rm NPn}}{2}\frac{I_{\rm rms}}{fC}\\ &= 0.0227\frac{11.3}{60\cdot 1650\cdot 10^{-6}}\\ &= 2.6\ \text{V}\end{aligned} \tag{11}$$

which clearly coincides with the amplitude obtained in the experiment. Because of this oscillation, the capacitors and the devices of the bridge must support higher voltage. The maximum voltage applied to the devices and components in this operating condition can be calculated as

$$V_{\rm Max} = \frac{V_{\rm dc}}{2} + \frac{\Delta V_{\rm NP}}{2} = 27.6\ \text{V}. \tag{12}$$

In this case, the amplitude of the switching-frequency ripple in the NP is very small. Therefore, the maximum voltage can be calculated by this method, which considers averaged variables. On the other hand, if the switching-frequency ripples were more significant, they should be taken into consideration and must be added to the calculated value of the maximum voltage.

The amplitude of the low-frequency NP voltage oscillation has been experimentally verified for some other operating points of the converter.

VII. Conclusion

The NP balancing effectiveness of two SVM techniques has been analyzed in this paper. Both techniques utilize the nearest vectors to the reference vector at any modulation cycle. The short vectors are properly selected for achieving the best balancing results, besides minimizing the switching frequencies of the devices. NTV uses three vectors per modulation cycle, while symmetric modulation uses four vectors. Although these modulation techniques can achieve low switching frequencies of the devices, good output voltage spectra, and low EMI, low-frequency oscillations appear in the NP voltage for some operating conditions. Some practical graphics are presented in this paper to obtain the amplitude of the low-frequency NP voltage ripple for both modulation strategies. Since nondimensional variables are presented, this information is very useful for the calculation of the values of the dc-link capacitors for any practical application.

The symmetric modulation technique has less NP current control than NTV modulation. Symmetric modulation normally uses four vectors per modulation cycle, but only three vectors are used when the NP voltage imbalance is at the edge of or beyond the control limits. The problem is that, in contrast to NTV modulation, when the reference vector lies in the inner regions, one short vector is imposed, and therefore, there is one fewer variable for the NP current control.

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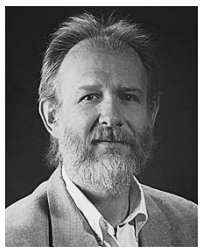

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