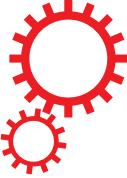


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Fault-Tolerant Control of ANPC Three-Level Inverter Based on Order-Reduction Optimal Control Strategy under Multi-Device Open-Circuit Fault

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Shi-Zhou Xu , Chun-Jie Wang, Fang-Li Lin & Shi-Xiang Li

The multi-device open-circuit fault is a common fault of ANPC (Active Neutral-Point Clamped) three-level inverter and effect the operation stability of the whole system. To improve the operation stability, this paper summarized the main solutions currently firstly and analyzed all the possible states of multi-device open-circuit fault. Secondly, an order-reduction optimal control strategy was proposed under multi-device open-circuit fault to realize fault-tolerant control based on the topology and control requirement of ANPC three-level inverter and operation stability. This control strategy can solve the faults with different operation states, and can works in order-reduction state under specific open-circuit faults with specific combined devices, which sacrifices the control quality to obtain the stability priority control. Finally, the simulation and experiment proved the effectiveness of the proposed strategy.

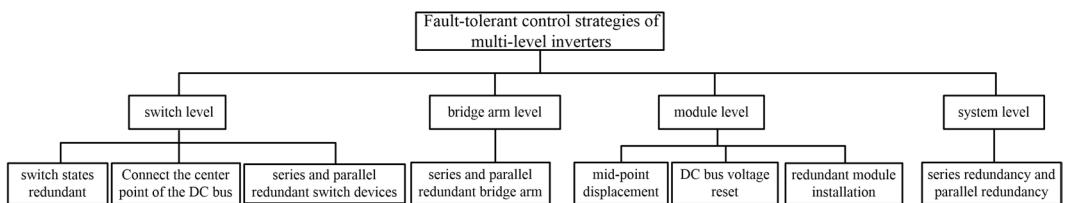
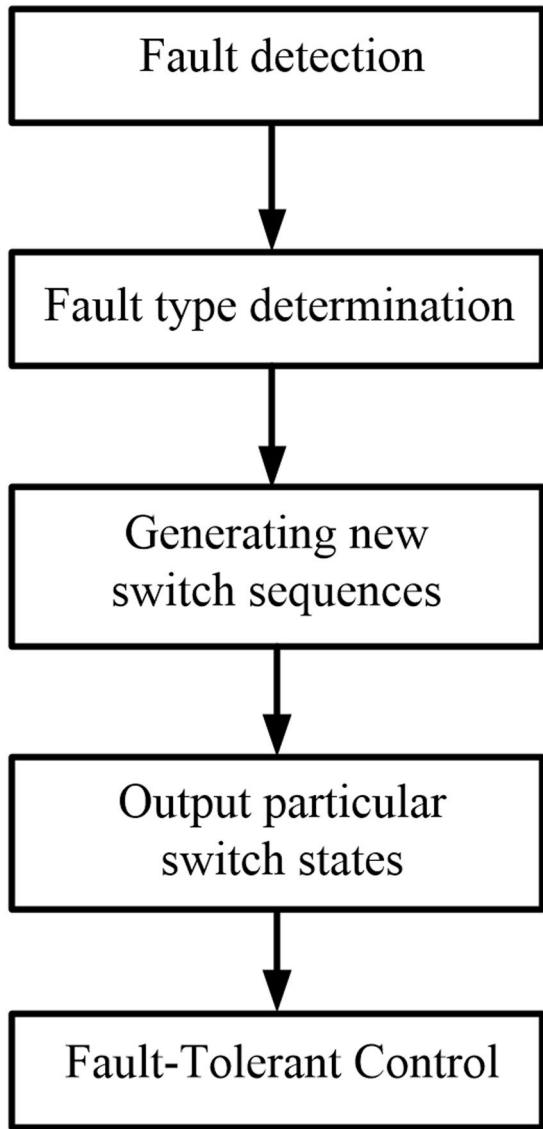
The ANPC three-level topology has the advantages of NPC three-level topology. What's more, it can overcome the unbalanced power-loss generation of power devices caused by different switching frequency using selecting different zero switching states. It has a much higher system freedom and much flexible control strategies, which can use different PWM control strategies to control the system to realize the corresponding performances. Therefore, the ANPC inverter has been paid much attention by researchers all over the world, and becomes mature as a system, but at present, the multi-device open-circuit fault is one of the urgent faults that need to be solved.

Right now, the fault-tolerant control strategy research on two-level inverter has been relatively mature and had many corresponding results. The most widespread topological structures of two-level fault-tolerant control are double winding redundant topology, bridge-arm redundant topology, switch-redundancy topology, three-phase four-bridge-arm fault tolerant topology, four-switch two-phase fault tolerant topology, three-phase H bridge topology, modular redundant topology, etc. The most frequently used control methods of two-level inverter fault-tolerant control are vector control, direct torque control, weak magnetic speed-up control and so on.

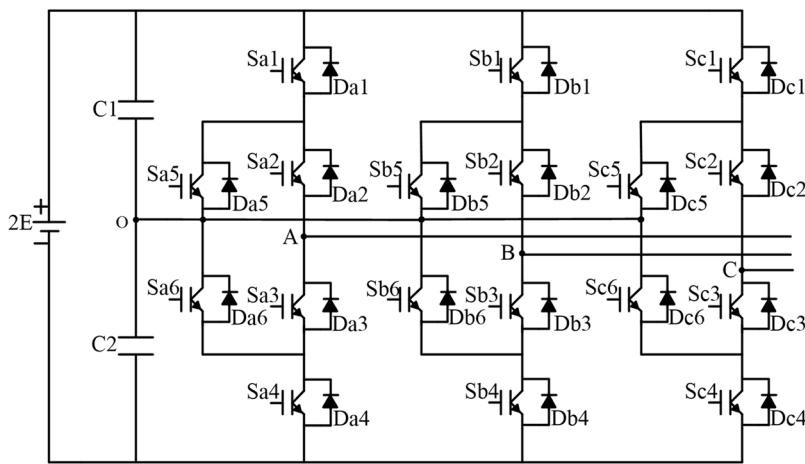
The multi-level inverter topologies are much more novel and complicated, so the fault-tolerant control research on them are much later. While, in recent years, multi-level inverters have been used widely in industrial field because of their inherent advantages, more output levels, less harmonic content, lower bus voltage acting on power devices, and so on, compared with two-level inverters. Therefore, the researchers in this field all over the world have paid much attention to multi-level inverters, and some achievements on fault-tolerant control of NPC(Neutral-Point-Clamped) three-level inverter have been made. The fault-tolerant control methods can be divided into four types, namely, switch level fault-tolerant control, bridge arm level fault-tolerant control, module level fault-tolerant control and system level fault-tolerant control, which are shown in Fig. 1.

The fault-tolerant control strategies of switch level can be divided into several kinds, and the most important three kinds are using the inherent redundant switch states^{1–4}, connecting the center point of DC bus^{5–12}, series and parallel redundant switch devices^{13–16}. The strategies proposed in^{17–21} are the ones belong to bridge-arm level, which have a redundant bridge arm in parallel. When the bridge arm is open or short circuit during operating, the redundant bridge arm will replace it and keep the system working as normal. This redundant bridge-arm

College of Electronic and Electrical Engineering, Henan Normal University, Xinxiang, 453007, China. Chun-Jie Wang, Fang-Li Lin and Shi-Xiang Li contributed equally to this work. Correspondence and requests for materials should be addressed to S.-Z.X. (email: xushizhousee@163.com)

**Figure 1.** Categories of fault-tolerant control methods for multi-level inverters.**Figure 2.** Flow chart of order-reduction optimal control strategy.

fault tolerant control costs too much and has a much less application. The topologies of the cascaded multilevel converter (CMC) and modular multi-level converter (MMC) have the feature of modularity, which can use the module-level fault-tolerant control methods. The module-level fault-tolerant control methods can be divided into three types, mid-point displacement, DC bus voltage reset, and redundant module installation. The system-level fault-tolerant control is the one install a redundant inverter to replace the fault one during the malfunction occurring, ensuring the performance of the whole system unchanged. The common system redundancy includes series redundancy and parallel redundancy. A comparison of fault-tolerant control strategies were shown in ref.²². A SBPM-based SOH monitor was proposed in ref.²³, which provides a practical method for the realization of fault-tolerant control. An *in-situ* voltage fault diagnosis method based on the modified Shannon entropy was

**Figure 3.** Topology of ANPC three-level inverter.

| Sa1/Da1 Sa4/Da4 | Sa2 | Da2 | Sa3 | Da3 | Sa5 | Da5 | Sa6 | Da6 | Phase state |
|--------------------|------|------|------|------|------|------|------|------|-------------|
| Ok | Ok | Ok | Ok | Ok | Fail | Ok | Fail | Ok | NRF |
| Ok | Ok | Ok | Ok | Ok | Ok | Fail | Ok | Fail | NRF |
| Ok | Ok | Ok | Ok | Ok | Ok | Ok | Fail | Fail | NRF |
| Ok | Ok | Ok | Ok | Ok | Fail | Fail | Ok | Ok | NRF |
| Ok | Ok | Ok | Ok | Ok | Fail | Fail | Fail | Fail | NRF-2L |
| Fail | Ok | Fail | Ok | Fail | Fail | Ok | Fail | Ok | RF |
| Fail | Fail | Ok | Fail | Ok | Ok | Fail | Ok | Fail | RF |
| Fail | Ok | Ok | Fail | Fail | Ok | Ok | Fail | Fail | RF |
| Fail | Fail | Fail | Ok | Ok | Fail | Fail | Ok | Ok | RF |

Table 1. Output states of fail phases under multiple devices open-circuit failure in single phase.

proposed in ref.²⁴, which is capable of predicting the voltage fault in time through monitoring battery voltage during vehicular operations. Another practical method of design, control and analysis of fault tolerant soft-switching DC-DC converter was proposed in ref.²⁵. Similarly, a variable slope trapezoidal reference signal based control for DC fault tolerant hybrid modular multilevel converter was studied in ref.²⁶, which offers a very useful method for reference. In ref.²⁷, the state-of-art equivalent circuit models for ultracapacitors are studied and the hybrid pulse power characterization test is conducted to collect the data for parameter identification, on which base the genetic algorithm is employed to extract the optimal model parameters to evaluate the model accuracy, complexity and robustness. In ref.²⁸, a novel fractional-order model composed of a series resistor, a constant-phase-element (CPE), and a Walburg-like element, were proposed to emulate the UC dynamics. All these methods provided useful references for fault-tolerant control strategies.

The topology of active neutral-point clamped three-level inverter became a research hot spot on the moment it was proposed. It can balance the power losses of inverter power devices by choosing four zero switching states to reduce the failure possibility of those devices with high switching frequency. So, the ANPC inverter has a much higher operation stability compared with NPC inverters. However, it is not enough and it is necessary to realize the fault-tolerant control for ANPC inverters to meet the high stability requirement of inverters used in some import special occasions. The design of hardware fault tolerant control architecture for wind energy conversion system with DFIG based on reliability analysis was presented in ref.²⁹. The power loss and the single device failure of ANPC three-level inverter were analyzed in ref.³⁰. The stabilities of NPC three-level inverter and ANPC three-level inverter were analyzed and compared in ref.³¹, which pointed out that the ANPC inverter has a much higher stability than NPC inverter when some power devices break down. The possible open-circuit and short-circuit faults of single device in ANPC inverter were analyzed in theory in ref.³², and the corresponding fault-tolerant control method was proposed. The simulation and experiment results proved the effectiveness of the proposed method. Meanwhile, The open-circuit and short-circuit faults of multiple devices in ANPC inverter were analyzed in theory, too, but without simulation and experiment. In this paper, on the basis of the existing researches, the fault-tolerant control strategy of ANPC three-level inverter will be studied further to improve the stability.

Principle of Order-Reduction Optimal Control Strategy

The flow chart of the order-reduction optimal control strategy is shown in Fig. 2.

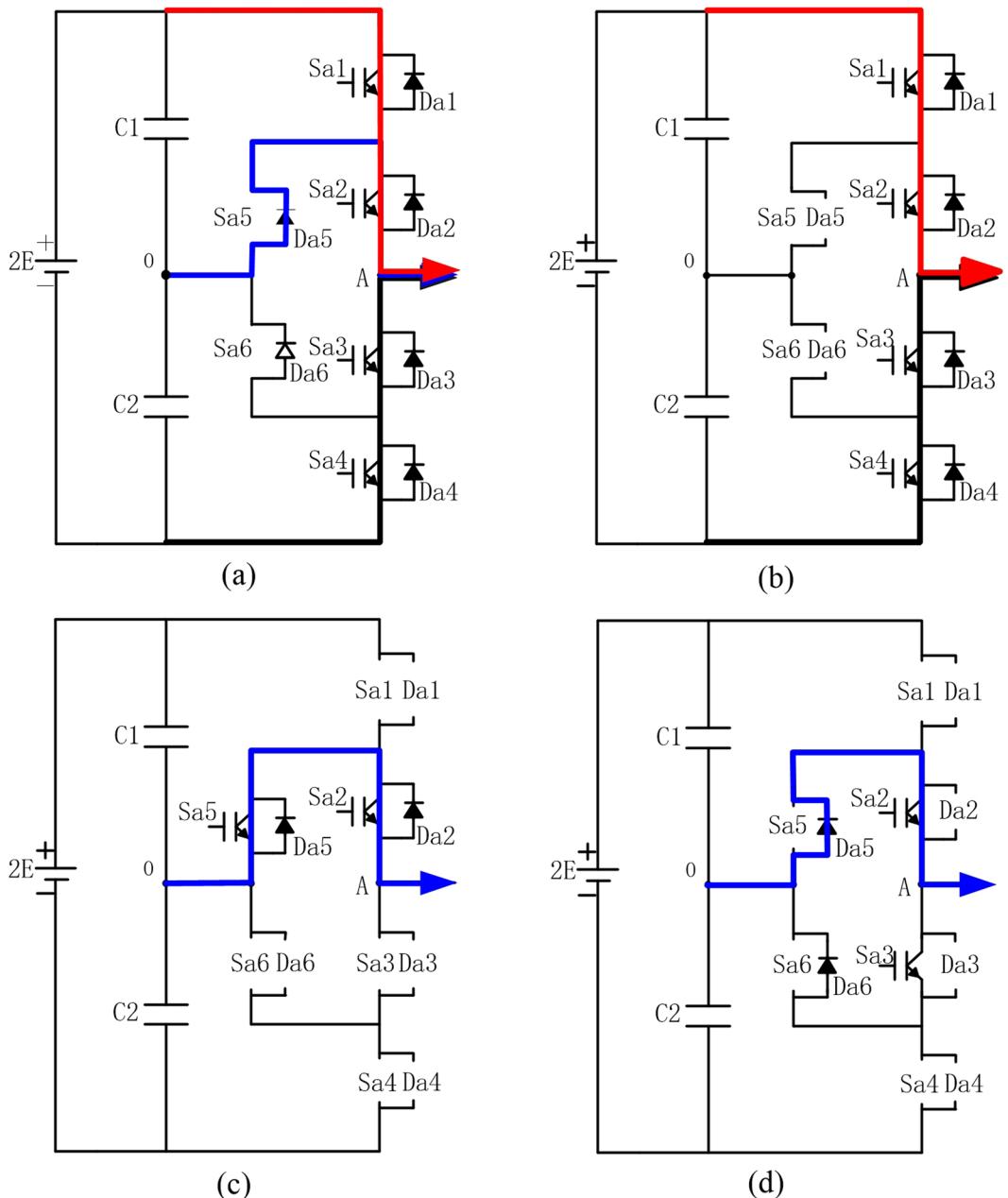
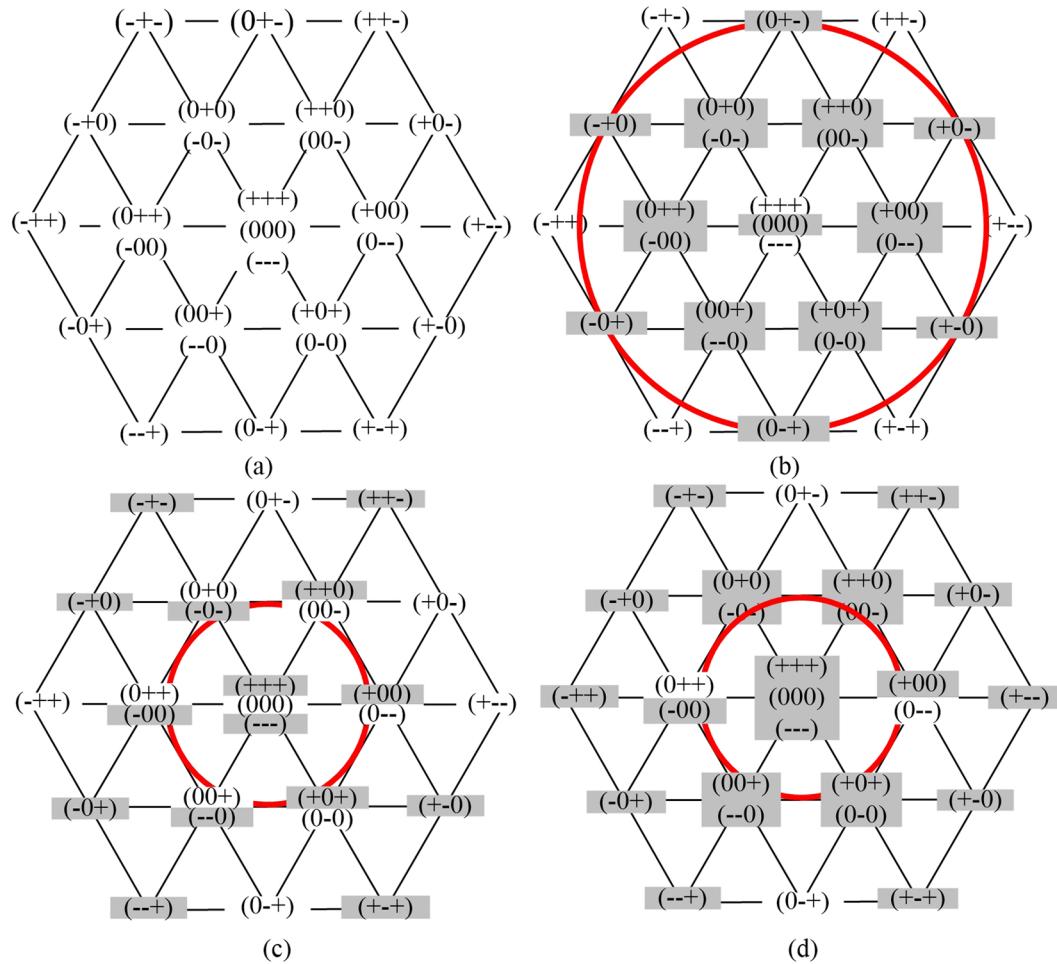
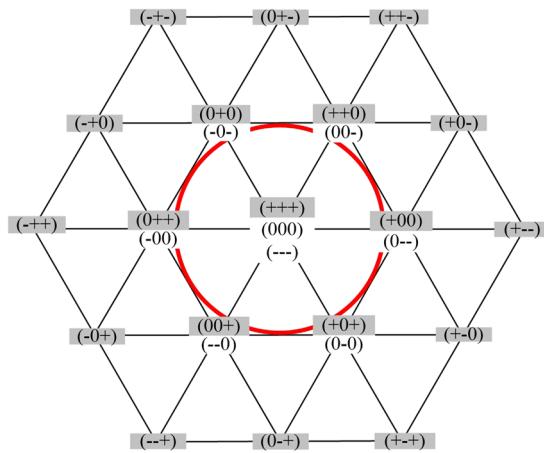


Figure 4. Current flow paths under multi-device open-circuit faults in 3-L ANPC inverter. **(a)** S_{a5} and S_{a6} in open-circuit state; **(b)** S_{a5}/D_{a5} and S_{a6}/D_{a6} in open-circuit state; **(c)** S_{a1}/D_{a1} , S_{a3}/D_{a3} , S_{a4}/D_{a4} and S_{a6}/D_{a6} in open circuit state; **(d)** S_{a1}/D_{a1} , D_{a2} , D_{a3} , S_{a4}/D_{a4} , S_{a5} and S_{a6} in open-circuit state.

| | Phase A state | Phase B state | Phase C state |
|--------|---------------|--------------------|--------------------|
| Mode 1 | Healthy/NRF | Healthy/NRF | Healthy/NRF |
| Mode 2 | NRF-2L | Healthy/NRF/NRF-2L | Healthy/NRF/NRF-2L |
| Mode 3 | RF | Healthy/NRF/NRF-2L | Healthy/NRF/NRF-2L |

Table 2. Operation states under fault-tolerant control with multi-device open-circuit fault.

The topology of ANPC three-level inverter was shown in Fig. 3. It can be seen from the topology that the ANPC three-level inverter turn the two clamped diodes of each bridge arm from NPC three-level inverter into IGBT modules to add the flowing paths of the zero state.

**Figure 5.** Voltage vector diagram of 3L-ANPC inverter under multi-device open-circuit fault.**Figure 6.** Voltage vector diagram of 3L-ANPC inverter using lower dc-link capacitor for fault tolerant operation.

The impacts caused by multiple devices open circuit of ANPC three-level inverter on the fault phases were summarized in Table 1. In Table 1, “healthy” means this phase works normally without fault device; “NRF” (No Reduction Fault) means this phase has faults, but this fault phase still can output three kinds of levels, “+”, “0”, and “-”; “NRF-2L” means has faults, but this fault phase only outputs two kinds of levels, “+” and “-”; “RF” (Reduction fault) means has faults, and this fault phase only outputs “0” level. For example, if Sa1/Da1, Sa2/Da2, Sa3/Da3 and

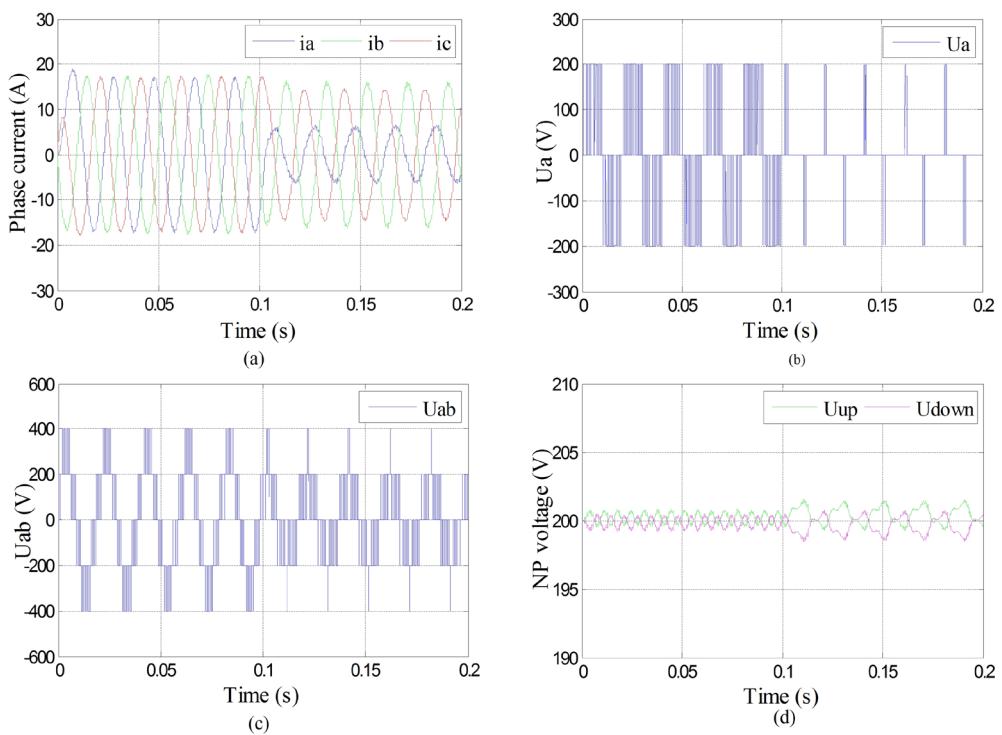


Figure 7. Phase current, phase voltage, line voltage and neutral-point voltage under Sa1 and Sa4 open-circuit fault. (a) Three-phase currents under Sa1 and Sa4 open-circuit fault; (b) Phase voltage of phase A under Sa1 and Sa4 open-circuit fault; (c) Line voltage between phase A and B under Sa1 and Sa4 open-circuit fault; (d) Neutral-point voltage under Sa1 and Sa4 open-circuit fault.

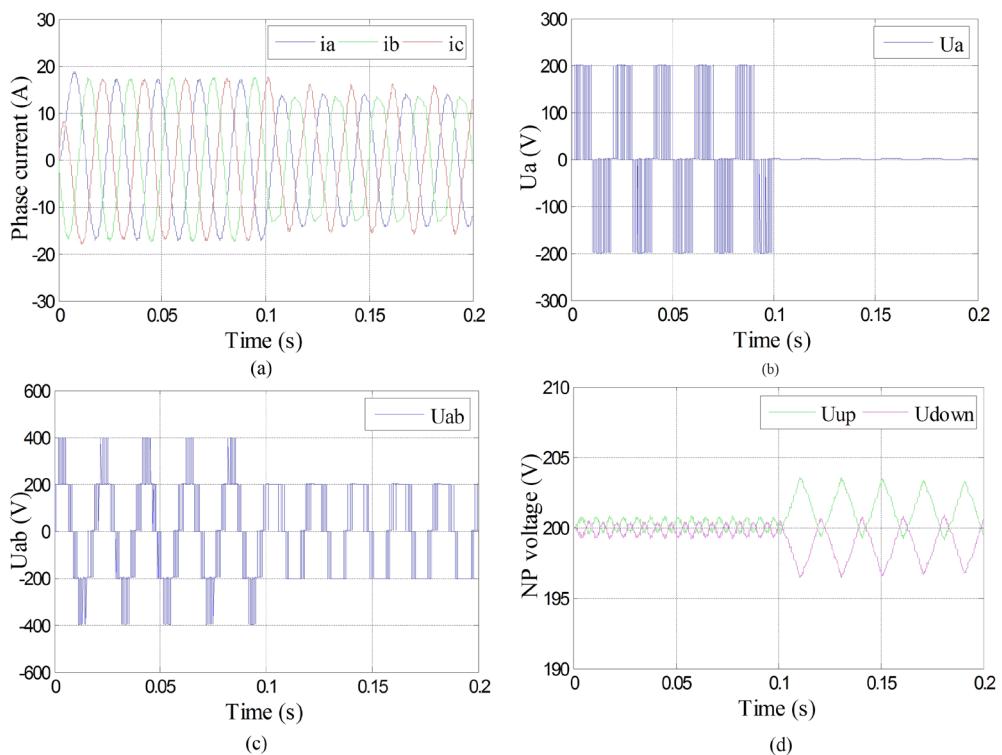


Figure 8. Phase current, phase voltage, line voltage and neutral-point voltage under Sa1 and Sa4 open-circuit fault with fault-tolerant control. (a) Three-phase currents under Sa1 and Sa4 open-circuit fault with fault-tolerant control; (b) Phase voltage of phase A under Sa1 and Sa4 open-circuit fault with fault-tolerant control; (c) Line voltage between phase A and B under Sa1 and Sa4 open-circuit fault with fault-tolerant control; (d) Neutral-point voltage under Sa1 and Sa4 open-circuit fault with fault-tolerant control.

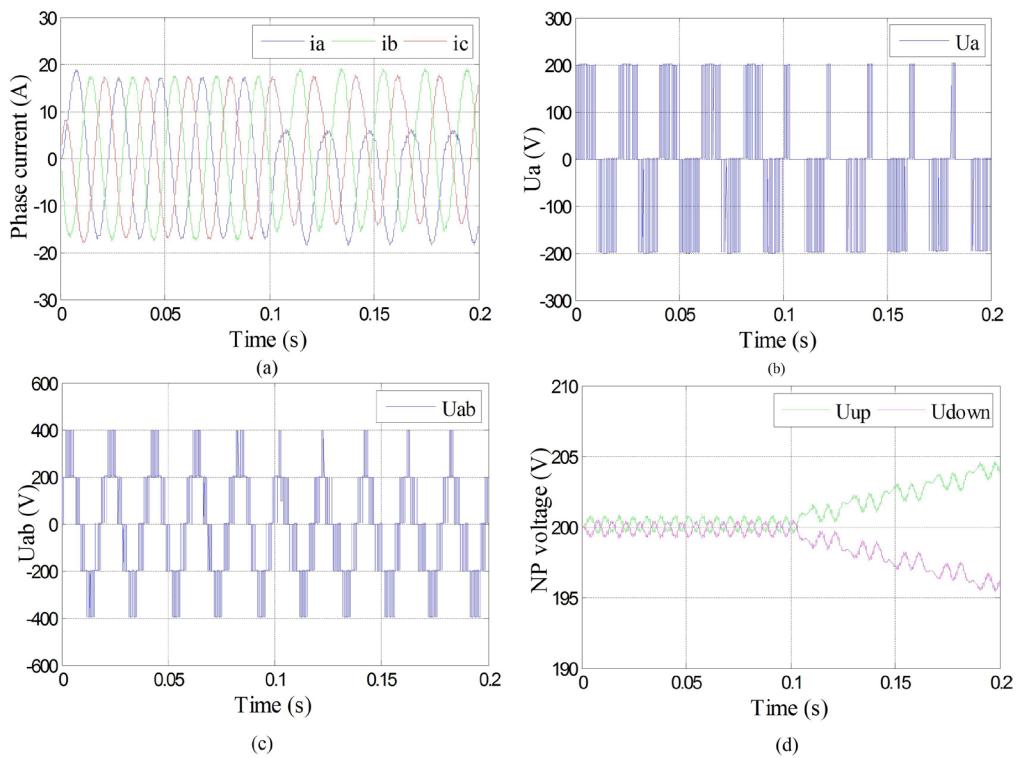


Figure 9. Phase current, phase voltage, line voltage and neutral-point voltage under Sa1 and Sa5 open-circuit fault. (a) Three-phase currents under Sa1 and Sa5 open-circuit fault; (b) Phase voltage of phase A under Sa1 and Sa5 open-circuit fault; (c) Line voltage between phase A and B under Sa1 and Sa5 open-circuit fault; (d) Neutral-point voltage under Sa1 and Sa5 open-circuit fault.

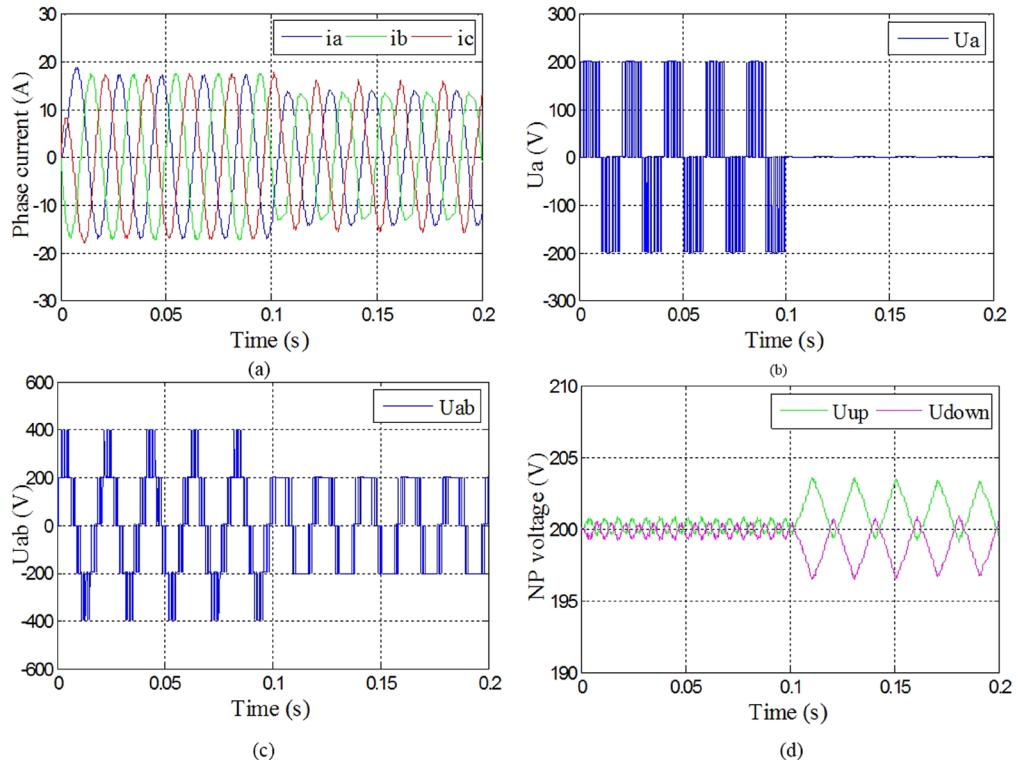


Figure 10. Phase current, phase voltage, line voltage and neutral-point voltage under Sa1 and Sa5 open-circuit fault with fault-tolerant control. (a) Three-phase currents under Sa1 and Sa5 open-circuit fault with fault-tolerant control; (b) Phase voltage of phase A under Sa1 and Sa5 open-circuit fault with fault-tolerant control; (c) Line voltage between phase A and B under Sa1 and Sa5 open-circuit fault with fault-tolerant control; (d) Neutral-point voltage under Sa1 and Sa5 open-circuit fault with fault-tolerant control.

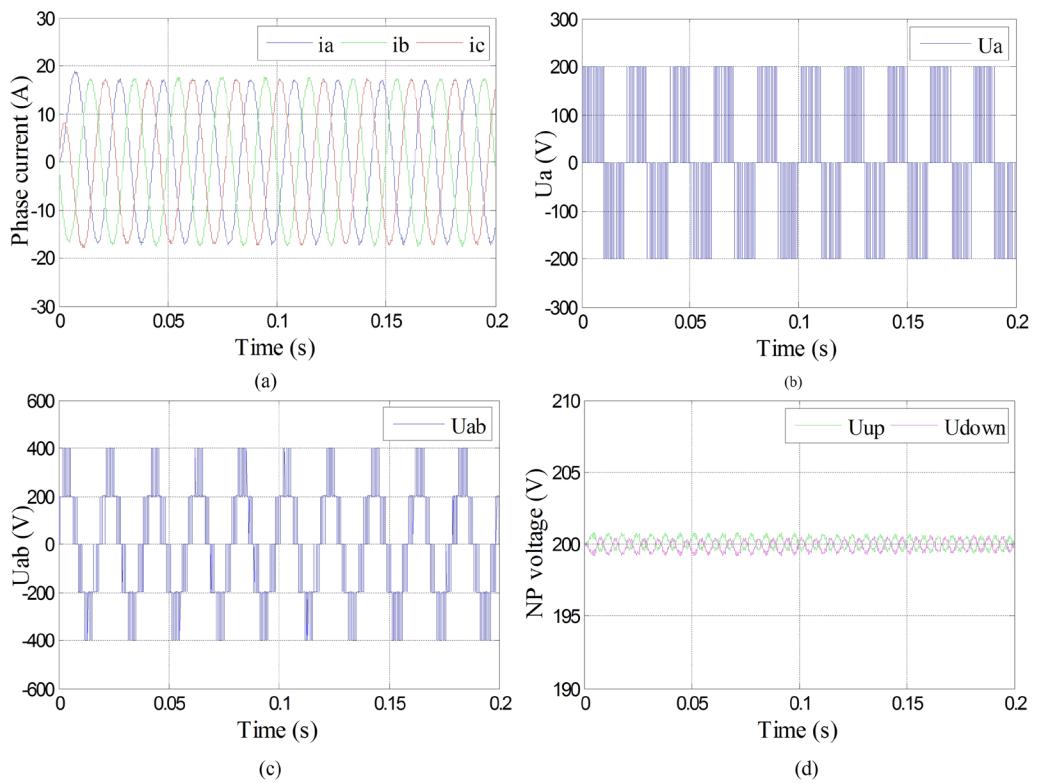


Figure 11. Phase current, phase voltage, line voltage and neutral-point voltage under Sa5 and Sa6 open-circuit fault with fault-tolerant control. **(a)** Three-phase currents under Sa5 and Sa6 open-circuit fault with fault-tolerant control; **(b)** Phase voltage of phase A under Sa5 and Sa6 open-circuit fault with fault-tolerant control; **(c)** Line voltage between phase A and B under Sa5 and Sa6 open-circuit fault with fault-tolerant control; **(d)** Neutral-point voltage under Sa5 and Sa6 open-circuit fault with fault-tolerant control.

Sa4/Da4 are healthy, even though both Sa5 and Sa6 fail at the same, this fault phase will still work in “NRF” state, and output “+”, “0”, and “-”; if Sa2/Da2 and Sa5/Da5 works normally, even though all the power devices of this fault phase are in open-circuit state, this fault phase still works under “RF” state, and output “0” level.

It can be seen from Table 1 that when Sa1/Da1, Sa2/Da2, Sa3/Da3 and Sa4/Da4 are all work in normal state, even if Sa5 and Sa6 work in open-circuit fault state, this fault phase are still under “NRF” state, and output “+”, “0” and “-” levels, as shown in Fig. 4(a); when Sa1/Da1, Sa2/Da2, Sa3/Da3 and Sa4/Da4 are all work in normal state, and Sa5/Da5 and Sa6/Da6 work in open-circuit fault state, this fault phase works in “NRF-2L” state, outputs “+” and “-” levels, as shown in Fig. 4(b); when Sa2/Da2 and Sa5/Da5 work in normal state, even if all the power devices in this fault phase are in open-circuit fault state, it still stays in “RF” state, and outputs “0” level, as shown in Fig. 4(c); when Sa2, Sa3, Da5 and Da6 work in normal state, even if all the other devices in this fault phase are in open-circuit fault, this fault phase still works under “RF” state, and only outputs “0” level, as shown in Fig. 4(d).

According to the output states of each phase in Table 1, the fault-tolerant control method under multi-device open-circuit fault of three-phase ANPC inverter can be summarized, and is shown in Table 2.

When one phase of three-phase ANPC three-level inverter breaks down, the operation under fault-tolerant control can be divided into three modes according to the output states of fault phase. In mode 1 and 2, the maximum modulation is the same as normal operation, while in mode 3, its maximum modulation decreases to 0.577. What's more, only under mode 1, the inverter outputs the same waveform quality as the normal one. The voltage vector diagram was introduced to illustrate the fault-tolerant control operation modes, and it is shown in Fig. 5. In Fig. 5, gray indicates the states that cannot output normally, and white indicates the states that can output normally.

When ANPC three-level inverter works under “healthy” or “NRF” state, each phase can still output “+”, “0” and “-”. The voltage vector diagram is shown in Fig. 5(a), and under this state, all the voltage vectors can still be used as normal to maintain the inverter work as normal. If one of the three phases works under NRF-2L state, the working condition of the inverter can be supposed to be much worse. All the three phases were supposed to be under NRF-2L state, and the voltage vector diagram is shown in Fig. 5(b), where the external hexagon still has six correct voltage vectors to be used. Therefore, the ANPC three-level inverter works under the same condition as the two-level inverter's. Although the waveform quality is reduced, its maximum modulation is the same as the one in normal state.

When one phase of the ANPC three-level inverter is under RF state and the other two phases are under healthy or NRF states, the voltage vector is shown in Fig. 5(c). It can be seen from Fig. 5(c) that the six voltage vectors of the inner hexagon is still valid as normal, which means the fault tolerant control is useful under this condition, but the maximum modulation is reduced to 0.577. Compared with the proposed fault states former,

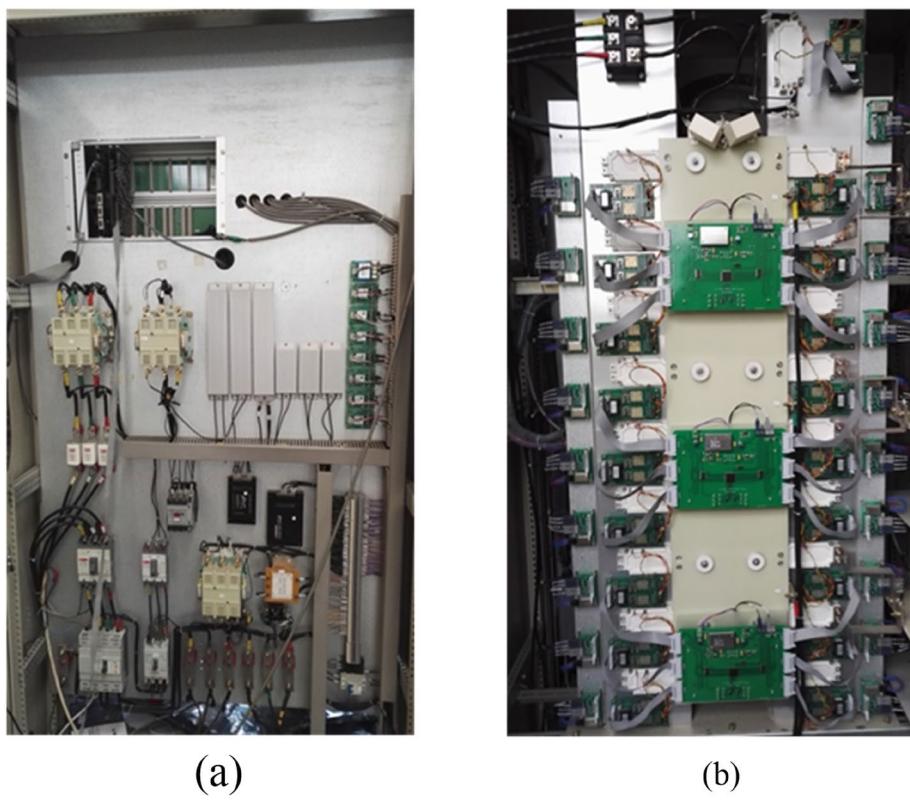


Figure 12. The experiment platform. **(a)** The front of the experiment platform; **(b)** The front of the experiment platform.

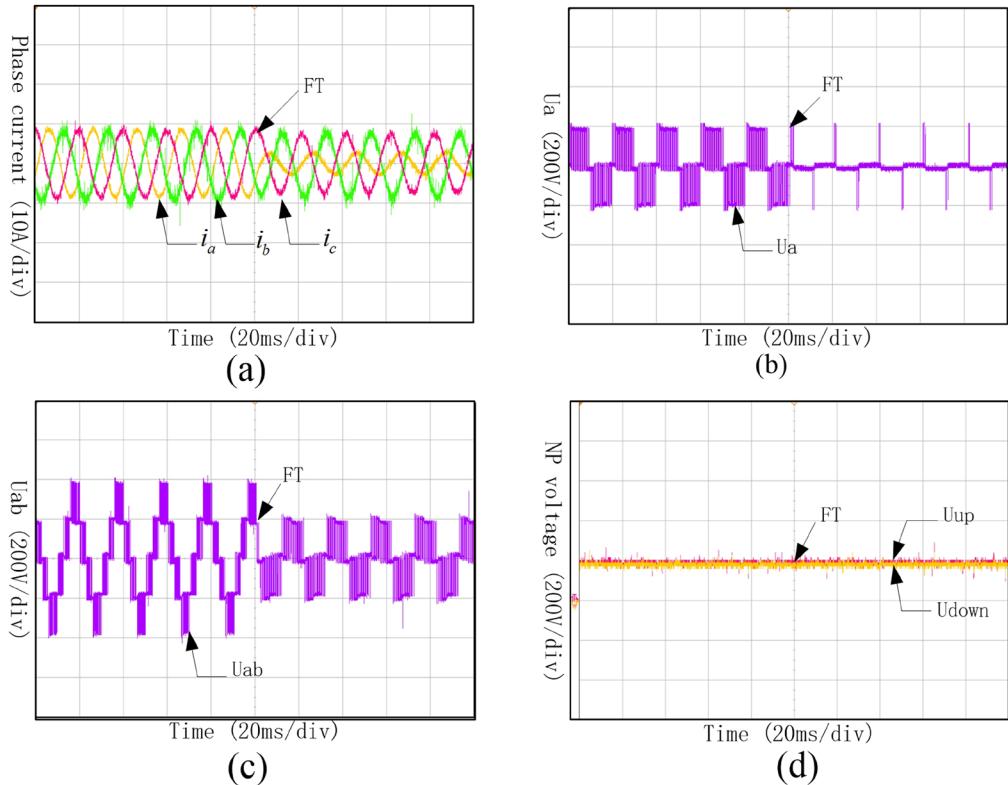


Figure 13. Waveforms of phase current, phase voltage, line voltage and neutral-point voltage under Sa1 and Sa4 open-circuit fault. **(a)** Three-phase currents under Sa1 and Sa4 open-circuit fault; **(b)** Phase voltage of phase A under Sa1 and Sa4 open-circuit fault; **(c)** Line voltage between phase A and B under Sa1 and Sa4 open-circuit fault; **(d)** Neutral-point voltage under Sa1 and Sa4 open-circuit fault.

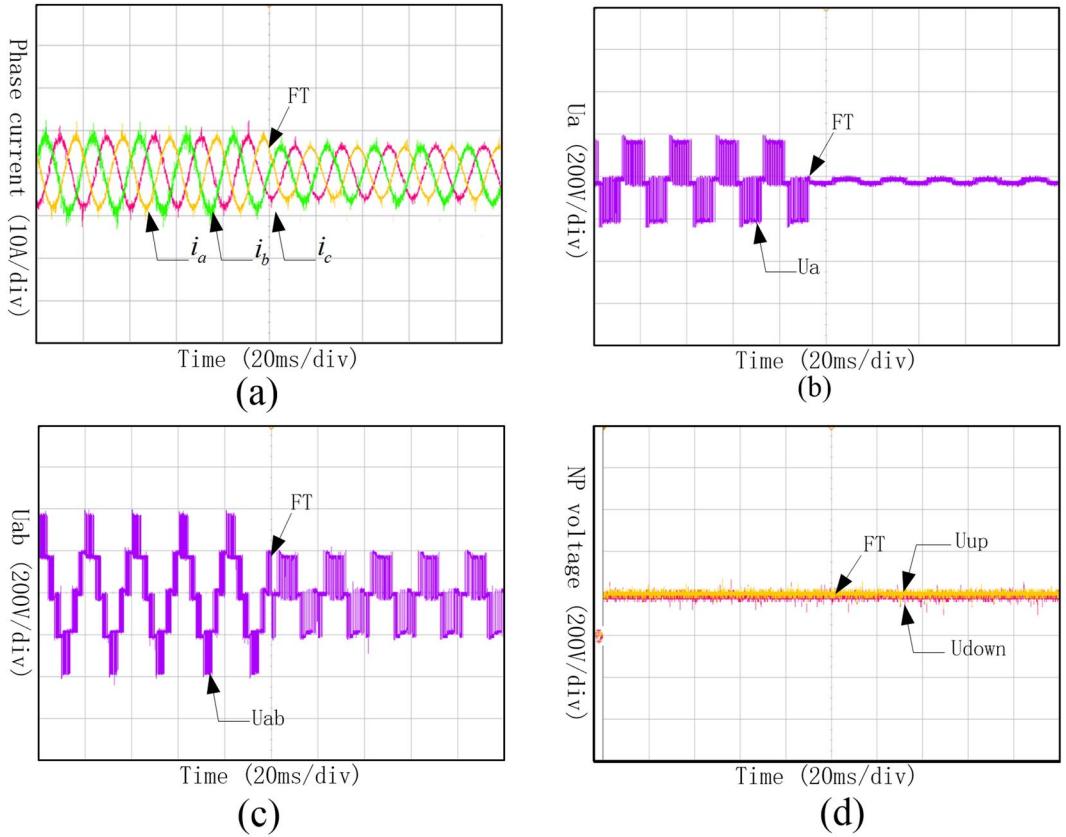


Figure 14. Waveforms of phase current, phase voltage, line voltage and neutral-point voltage under Sa1 and Sa4 open-circuit fault with fault-tolerant control. (a) Three-phase currents under Sa1 and Sa4 open-circuit fault with fault-tolerant control; (b) Phase voltage of phase A under Sa1 and Sa4 open-circuit fault with fault-tolerant control; (c) Line voltage between phase A and B under Sa1 and Sa4 open-circuit fault with fault-tolerant control; (d) Neutral-point voltage under Sa1 and Sa4 open-circuit fault with fault-tolerant control.

there is a much worse operation state, one phase of the ANPC three-level inverter is under FR state and the other two phases both work under NRF-2L state. Under this state, the four valid voltage vectors are shown in Fig. 5(d). When the three-phase ANPC three-level inverter operates under this mode, its equivalent circuit is the same as four-switched three-phase inverter, and can realize the fault-tolerant control operation with the maximum modulation reduced to 0.577.

When phase A and B both work under RF state, even though phase C works under healthy state, only (00−), (000) and (00+) are can be valid. Under this condition, the ANPC three-level inverter can not work with fault-tolerant control according to what has been analyzed before. However, when the topology of the inverter is recomposed and only one capacitor of the DC-bus side is used to generate a two-level voltage waveform, the fault-tolerant control can be realized. For example, if Sa1/Da1, Sb1/Db1 and Sc1/Dc1 goes into open-circuit state at the same time, the fault phases can only output “0” and “−” level, and the voltage vector diagram is shown in Fig. 6.

Under this condition, the fault-tolerant control mode of ANPC three-level inverter can be equalled to a two-level inverter, whose maximum modulation decreased to 0.577. In the same way, if Sa4/Da4, Sb4/Db4, and Sc4/Dc4 come into open-circuit fault at the same time, the fault phase can only output “+” and “0” and the whole system will still work with fault-tolerant control.

Simulation and Experiment

Simulation. The experiment parameters are: DC busbar voltage \$U_{dc} = 400V\$, the upper and lower capacitance of DC side \$C_1 = C_2 = 10mF\$, the sampling frequency \$f_{sw} = 2KHz\$, the modulation \$M = 0.8\$, frequency \$f = 50Hz\$, the resistance load \$R_1 = 8\Omega\$, \$L = 23mH\$.

The waveforms of the output current of phase A, B and C, the phase voltage of phase A, the A-B line voltage, and the neutral-point voltage under open-circuit fault were shown in Fig. 7. It can be seen from the Fig. 7(a) that the three-phase currents are no longer symmetrical, and the current of phase A has been changed. The phase voltage of phase A and the line voltage of A-B, as shown in Fig. 7(b) and (c) respectively, have also been distorted when Sa1 and Sa4 come into open circuit. Meanwhile, the neutral-point voltage, as shown in Fig. 7(d), has been shifted, but it still can keep balance.

The three-phase currents, phase voltage of phase A, line voltage between phase A and B, and the neutral-point voltage were shown in Fig. 7 under Sa1 and Sa4 open-circuit fault in phase A with fault-tolerant control. It can be seen from Fig. 8(a) that even though the amplitudes of three-phase currents decreased, they were maintained symmetry. It

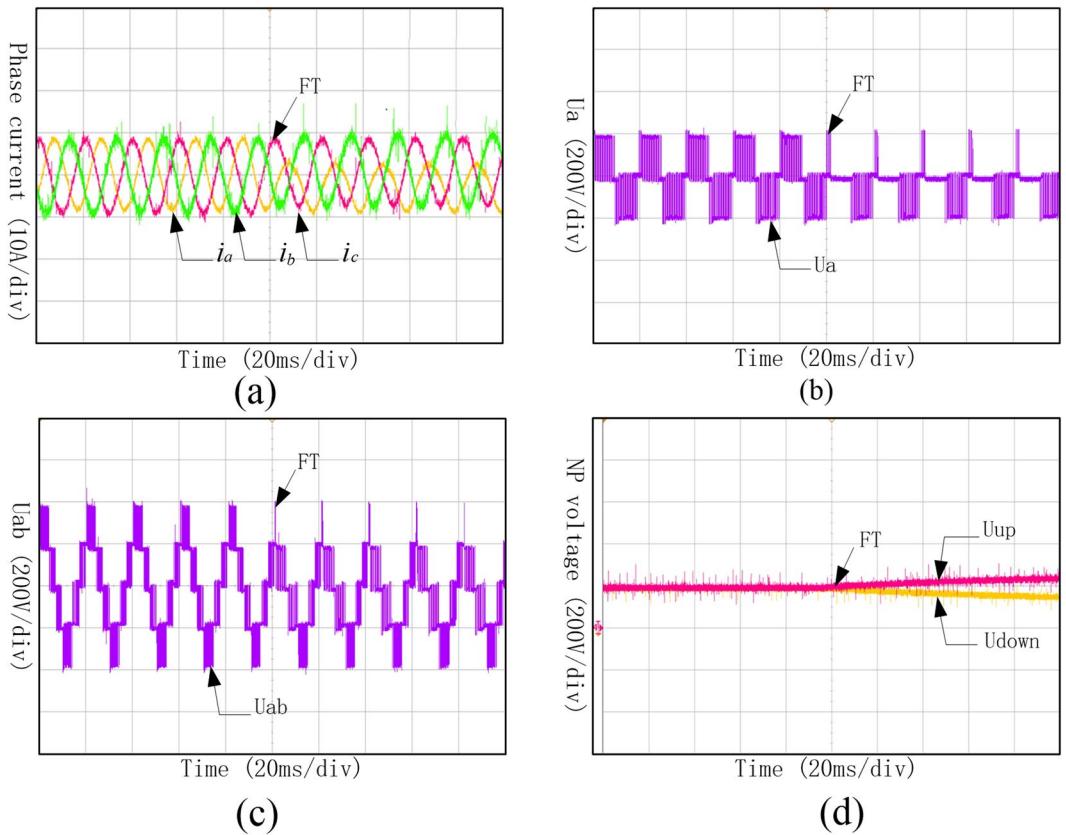


Figure 15. Waveforms of phase current, phase voltage, line voltage and neutral-point voltage under Sa1 and Sa5 open-circuit fault. (a) Three-phase currents under Sa1 and Sa5 open-circuit fault; (b) Phase voltage of phase A under Sa1 and Sa5 open-circuit fault; (c) Line voltage between phase A and B under Sa1 and Sa5 open-circuit fault; (d) Neutral-point voltage under Sa1 and Sa5 open-circuit fault.

can be seen from Fig. 8(b) that the phase voltage of phase A changed into 0 with fault-tolerant control after the fault occurrence of phase A. It can be seen from Fig. 8(c) that even though the amplitude of line voltage between phase A and B decreased, they were maintained symmetry. It can be seen from Fig. 8(d) that the neutral-point voltage shifted a little under fault-tolerant control compared with normal condition, but it can still keep balance.

The three-phase currents, phase voltage of phase A, line voltage between phase A and B, and the neutral-point voltage were shown in Fig. 9 under Sa1 and Sa5 open-circuit fault in phase A. It can be seen from Fig. 9(a) that the phase current of phase A changed most significantly. It can be seen from Fig. 9(b-d) respectively that the phase voltage of phase A, line voltage between phase A and B, and the neutral-point voltage had also changed or shifted. Meanwhile, the balance of neutral-point voltage was lost.

The three-phase currents, phase voltage of phase A, line voltage between phase A and B, and the neutral-point voltage were shown in Fig. 10 under Sa1 and Sa5 open-circuit fault in phase A with fault-tolerant control. It can be seen from Fig. 10(a) that even though the amplitudes of three-phase currents decreased, they were maintained symmetry. It can be seen from Fig. 10(b) that the phase voltage of phase A changed into 0 with fault-tolerant control after the fault occurrence of phase A. It can be seen from Fig. 10(c) that even though the amplitude of line voltage between phase A and B decreased, they were maintained symmetry. It can be seen from Fig. 10(d) that the neutral-point voltage shifted a little under fault-tolerant control compared with normal condition, but it can still keep balance.

The three-phase currents, phase voltage of phase A, line voltage between phase A and B, and the neutral-point voltage were shown in Fig. 11 under Sa5 and Sa6 open-circuit fault in phase A with fault-tolerant control. It can be seen from Fig. 11(a-d) respectively that the three-phase currents, phase voltage of phase A, line voltage between phase A and B decreased, neutral-point voltage were still kept as the same as the ones before fault occurrence. Therefore, when Sa5 goes into open-circuit fault, it can be maintained operation as normal without fault-tolerant control.

Since the symmetry of the ANPC topology, it is valid only to analyze the upper bridge arm of the fault phase during the multi-device open-circuit fault. What's more, the open-circuit fault of diodes is the same as IGBT's, so it will not be analyzed in detail repeatedly.

Experiment. The experiment parameters are: DC busbar voltage $U_{dc} = 400$ V, the upper and lower capacitance of DC side $C_1 = C_2 = 10$ mF, the sampling frequency $f_{sw} = 2$ KHz, the modulation M = 0.8, frequency $f = 50$ Hz, the resistance load $R_1 = 8 \Omega$, $L = 23$ mH. The experiment platform is shown in Fig. 12.

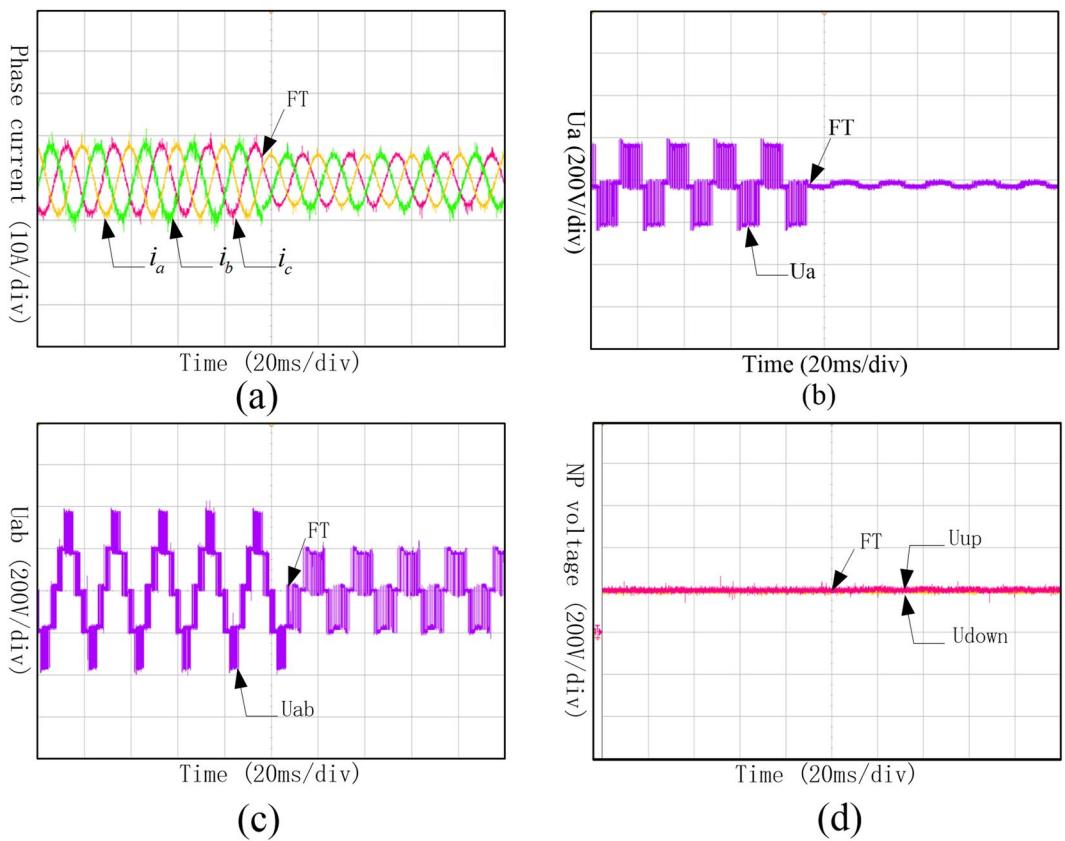


Figure 16. Waveforms of phase current, phase voltage, line voltage and neutral-point voltage under Sa1 and Sa5 open-circuit fault with fault-tolerant control. (a) Three-phase currents under Sa1 and Sa5 open-circuit fault with fault-tolerant control; (b) Phase voltage of phase A under Sa1 and Sa5 open-circuit fault with fault-tolerant control; (c) Line voltage between phase A and B under Sa1 and Sa5 open-circuit fault with fault-tolerant control; (d) Neutral-point voltage under Sa1 and Sa5 open-circuit fault with fault-tolerant control.

It can be found from Fig. 13(a) that, when Sa1 and Sa4 come into open-circuit fault at the same time, the three-phase current was no longer symmetric, and the current of phase A changed most obviously. It can be found from Fig. 13(b) and (c) that phase voltage of phase A and line voltage between phase A and B distorted because of the open circuit of Sa2. As shown in Fig. 13(d), the neutral-point voltage shifted a little, but it still could keep balance.

It can be found from Fig. 14(a) that, when Sa1 and Sa4 came into open-circuit fault at the same time and operated with fault-tolerant control, the amplitude of the three-phase current would decrease a little, but they are still symmetry. It can be found from Fig. 14(b) that phase voltage of phase A changed into 0 during the fault-tolerant control operation after the fault occurrence. As shown in Fig. 14(c), even though the line voltage between phase A and B decreased, it still can keep symmetry. Meanwhile, the neutral-point voltage which is shown in Fig. 14(d) can still keep balance.

It can be seen from Fig. 15 that the Three-phase currents under Sa1 and Sa5 open-circuit fault are no longer symmetry, and the current of phase A changed most significantly. Phase voltage of phase A and the line voltage between phase A and phase B distorted because of the open-circuit fault of Sa2. Meanwhile, the neutral-point voltage shifted under this condition, and lost the ability of keeping balance.

It can be seen from Fig. 16(a) that even though the amplitudes of the three-phase currents have been decreased, they are still in symmetry. Under the fault-tolerant control, the phase voltage of phase A, shown in Fig. 16(b), changed into 0 after the fault occurrence. The amplitude of line voltage between phase A and B also decreased, which is shown in Fig. 16(c), and still can keep symmetry as three-phase currents did. Meanwhile, the neutral-point voltage which is shown in Fig. 16(d) can still keep balance.

The experiment results shown in Fig. 17 proved that the three-phase currents, phase voltage, line voltage and neutral-point voltage did not change after the Sa5 and Sa6 open-circuit fault and can still output the same waveforms as the ones before fault occurrence. Therefore, it is unnecessary to apply the fault-tolerant control when Sa5 and Sa6 come into open-circuit fault, and the whole can maintain operating as normal.

These experiment results above are consistent with the simulation results. This order-reduction optimal control strategy can realize the fault-tolerant control to keep the system working in slowing down or output capacity reducing state to improve the reliability of the whole system.

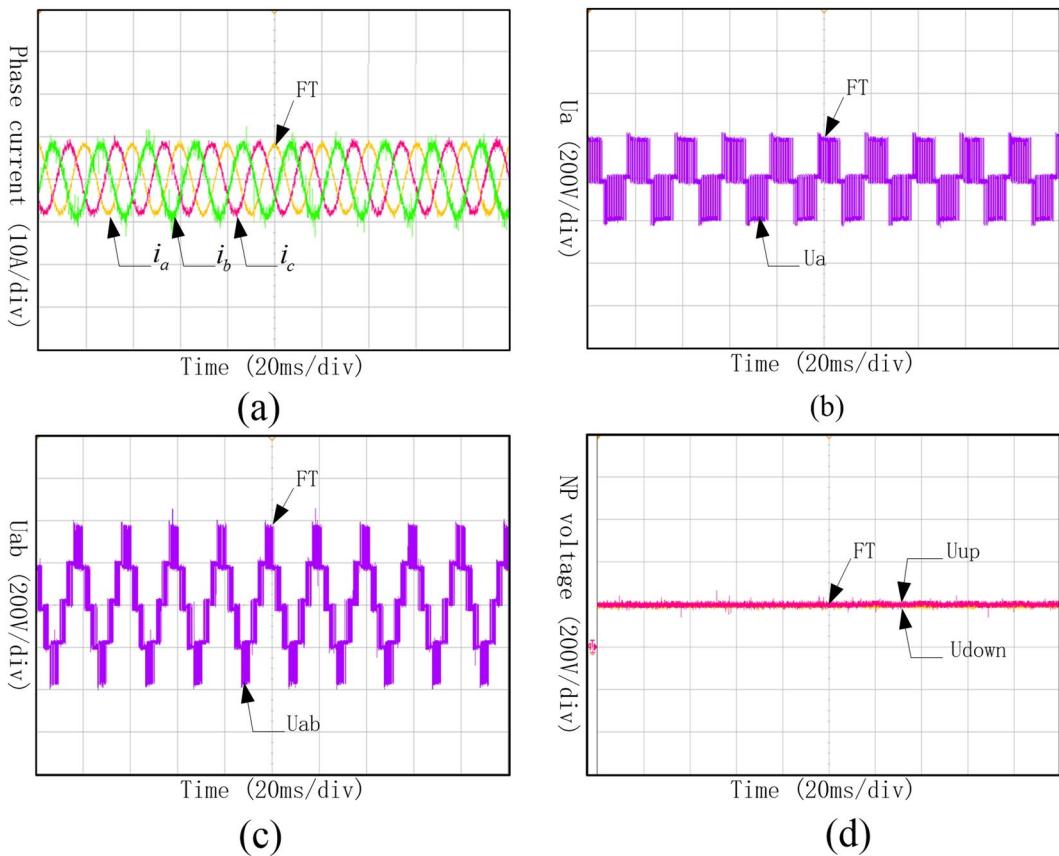


Figure 17. Waveforms of phase current, phase voltage, line voltage and neutral-point voltage under Sa5 and Sa6 open-circuit fault. **(a)** Three-phase currents under Sa5 and Sa6 open-circuit fault; **(b)** Phase voltage of phase A under Sa5 and Sa6 open-circuit fault; **(c)** Line voltage between phase A and B under Sa5 and Sa6 open-circuit fault; **(d)** Neutral-point voltage under Sa5 and Sa6 open-circuit fault.

Conclusions

To improve the operation stability, this paper summarized all the possible states of multi-device open-circuit fault and proposed an order-reduction optimal control strategy to realize fault-tolerant control based on the topology and control requirement of ANPC three-level inverter and operation stability. This control strategy can solve the faults with different operation states, and can work in order-reduction state under specific open-circuit faults with specific combined devices, which sacrifices the control quality to obtain the stability priority control. Finally, the simulation and experiment proved the effectiveness of the proposed strategy. This paper may offer a practical method potentially to solve the multi-device open-circuit problem in ANPC three-level inverters.

Data availability statement. The authors are responsible for ensuring that data will be available from the data owner post-publication, in the same manner as the authors obtained the data.

References

- Park, J. J., Kim, T. J. & Hyun, D. S. Study of neutral point potential variation for three-level NPC inverter under fault condition. *Industrial Electronics, 2008. IECON 2008. Conference of IEEE*, 983–988 (2008).
- Choi, U. M., Lee, K. B. & Blaabjerg, F. Diagnosis and tolerant strategy of an open-switch fault for t-type three-level inverter systems. *IEEE Transactions on Industry Applications* **50**(1), 495–508 (2014).
- Lezana, P., Pou, J. & Meynard, T. A. *et al.* Survey on fault operation on multilevel inverters[J]. *IEEE Transactions on Industrial Electronics* **57**(7), 2207–2218 (2010).
- Li, S. & Xu, L. Strategies of fault tolerant operation for three-level pwm inverters. *IEEE Transactions on Power Electronics* **21**(4), 933–940 (2006).
- Mohammadpour, A., Sadeghi, S. & Parsa, L. A generalized fault-tolerant control strategy for five-phase pm motor drives considering star, pentagon, and pentacle connections of stator windings. *IEEE Transactions on Industrial Electronics* **61**(1), 63–75 (2013).
- Kwak, S. Four-leg-based fault-tolerant matrix converter schemes based on switching function and space vector methods. *IEEE Transactions on Industrial Electronics* **59**(1), 235–243 (2012).
- Nguyen-Duy, K., Liu, T. H., Chen, D. F. & Hung, J. Y. Improvement of matrix converter drive reliability by online fault detection and a fault-tolerant switching strategy. *IEEE Transactions on Industrial Electronics* **59**(1), 244–256 (2011).
- Khwan-On, S., Lillo, L. D., Empringham, L. & Wheeler, P. Fault-tolerant matrix converter motor drives with fault detection of open switch faults. *IEEE Transactions on Industrial Electronics* **59**(1), 257–268 (2011).
- Farnesi, S., Fazio, P. & Marchesoni, M. A new fault tolerant NPC converter system for high power induction motor drives. *IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics & Drives*, 337–343 (2011).

10. Hoang, K. D., Zhu, Z. Q., Foster, M. P. *et al.* Comparative study of current vector control performance of alternate fault tolerant inverter topologies for three-phase PM brushless ac machine with one phase open-circuit fault[C], Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on. IET, 1–6 (2010).
11. Shahbazi, M., Poure, P., Saadate, S. & Zolghadri, M. R. Fault-tolerant five-leg converter topology with FPGA-based reconfigurable control. *IEEE Transactions on Industrial Electronics* **60**(6), 2284–2294 (2013).
12. Najmi, E. S. *et al.* Fault tolerant Nine Switch Inverter. Power Electronics, Drive Systems and Technologies Conference, IEEE, 534–539 (2011).
13. Ceballos, S., Pou, J., Robles, E., Zaragoza, J. & Martin, J. L. Performance evaluation of fault-tolerant neutral-point-clamped converters. *IEEE Transactions on Industrial Electronics* **57**(8), 2709–2718 (2010).
14. Liu, J., Yao, J., Yang, S. & Wang, K. Loss analysis of two kinds of flexible HVDC converters. *Power Electronics and Motion Control Conference, IEEE* **3**, 1669–1674 (2012).
15. Cordeiro, A., Palma, J., Maia, J. & Resende, M. Combining mechanical commutators and semiconductors in fast changing redundant inverter topologies. Eurocon-International Conference on Computer As A Tool, IEEE, 1–4 (2011).
16. Chen, A., Zhang, C., He, X. *et al.* Fault-tolerant design for flying capacitor multilevel inverters[C]//Power Electronics and Motion Control Conference, 2009. IPEMC'09. IEEE 6th International, 1460–1464 (2009).
17. Andreu, J., Kortabarria, I., Ibarra, E. *et al.* A new hardware solution for a fault tolerant matrix converter, Industrial Electronics, 2009. IECON'09. 35th Annual Conference of IEEE. IEEE, 4469–4474 (2009).
18. Song, Y., Wang, B. A hybrid electric vehicle powertrain with fault-tolerant capability, Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE, 951–956 (2012).
19. Naidu, M., Gopalakrishnan, S. & Nehl, T. Fault Tolerant Permanent Magnet Motor Drive Topologies for Automotive X-By-Wire Systems. Industry Applications Society Meeting, 2008. Ias '08, IEEE, 1–8 (2008).
20. Rodriguez, M. A., Claudio, A., Theilliol, D., Vela, L. G. & Hernandez, L. A strategy to replace the damaged element for fault-tolerant induction motor drive. International Conference on Electrical Engineering, Computing Science and Automatic Control, IEEE 51–55 (2008).
21. Ceballos, S. Efficient modulation technique for a four-leg fault-tolerant neutral-point-clamped inverter. *IEEE Transactions on Industrial Electronics* **55**(3), 1067–1074 (2008).
22. Toumi, S. *et al.* A comparison of fault-tolerant control strategies for a pmsg-based marine current turbine system under generator-side converter faulty conditions. *Journal of Electrical Systems* **13**(3), 1–16 (2017).
23. Hu, X., Jiang, J., Cao, D. & Bo, E. Battery health prognosis for electric vehicles using sample entropy and sparse bayesian predictive modeling. *IEEE Transactions on Industrial Electronics* **63**(4), 2645–2656 (2017).
24. Wang, Z., Hong, J., Liu, P. & Zhang, L. Voltage fault diagnosis and prognosis of battery systems based on entropy and z -score for electric vehicles. *Applied Energy* **196** (2017).
25. Li, T. & Parsa, L. Design, control and analysis of a fault tolerant soft-switching dc-dc converter for high power high voltage applications. *IEEE Transactions on Power Electronics* **99** (2017).
26. Ghat, M. B., Shukla, A. & Mishra, R. Variable slope trapezoidal reference signal based control for a dc fault tolerant hybrid modular multilevel converter with cascaded full bridges. *IEEE Transactions on Industry Applications* **99** (2107).
27. Zhang, L., Wang, Z., Hu, X., Sun, F. & Dorrell, D. G. A comparative study of equivalent circuit models of ultracapacitors for electric vehicles. *Journal of Power Sources* **274**(8), 899–906 (2015).
28. Zhang, L., Hu, X., Wang, Z., Sun, F. & Dorrell, D. G. Fractional-order modeling and state-of-charge estimation for ultracapacitors. *Journal of Power Sources* **314**, 28–34 (2016).
29. Weber, P., Poure, P., Theilliol, D. & Saadate, S. Design of hardware fault tolerant control architecture for Wind Energy Conversion System with DFIG based on reliability analysis. *IEEE International Symposium on Industrial Electronics*, 2323–2328 (2008).
30. Jing, W. Study on Power Device Losses of High-Power Three-Level Converter [D]. China University of Mining and Technology (2011).
31. Jun, L., Alex, Q. H Reliability Comparison for 3L-NPC and 3L-ANPC Converters for Drives Application[J]. *IEEE International Electric Machines & Drives Conference (IEMDC)*, IEEE 271–276 (2011).
32. Jun Li, A. Q. & Huang, Z. L. *et al.* Analysis and Design of Active NPC(ANPC) Inverters for Fault-Tolerant Operation of High-Power Electrical Drives[J]. *IEEE Transactions on Power Electronics* **27**(2), 519–533 (2012).

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Author Contributions

Shi-Zhou Xu proposed the idea, built the experiment platform, and wrote the main manuscript text; Chun-Jie Wang Carried out the experiment; Fang-Li Lin dealt with the experiment waveforms; Shi-Xiang Li made the article typesetting.

Additional Information

Competing Interests: The authors declare that they have no competing interests.

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