Studies About Fault Tolerance in 3-Level NPC Inverters

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Contents

1 Aim of the Study

In industry and daily life AC machines have lots of application areas. Such as in today's one of the most famous trends, electrical vehicles. Or for renewable energy systems like wind turbines. These machines need a source to work. However, for different demands of these machines, magnitude and frequency of the AC source must be controlled. For some applications, the source is DC. For example, Energy is stored in the batteries as DC for the motor of the car. And this DC source must be converted to AC and controlled to manage demands of the motor. The best way to control these parameters is to use power electronic circuits. These are the inverter.

3-phase inverters are designed according to requirements of AC motors. However, there might be unexpected fails in the system. Some motors have to operate under this condition. In this research, I'm mainly focus on the 3-level NPC Inverter's fault status and control methods under this fault conditions Also, I will investigate the behaviour of DC link capacitor voltage and how to moderate unbalance situations of the capacitor voltage.

2 Literature Review

2.1 3-Phase Inverters

The AC machines are one of the most commonly used machines in industrial applications. However, the source of these devices is mostly DC supply. Moreover, the level of input voltage and current must be controlled for the torque and speed demand of the motor. For this reason, there must be an interface between the supply and the motor. This must be a power electronics circuit to control the level of the voltage and current according to the demand. This circuit is called a DC/AC converter or inverter.

The industrial motors are commonly 3-phase motors. Therefore, inverters must be the 3-phase inverters. The 3-phase inverters can be classified according to output voltage levels. In figure 1, 2-level voltage source inverter topology can be seen. Switches (Q1 to Q6) can be opened and closed according to PWM signal of their gate drivers. The opening time of switches determines the output voltage and current level. The controller can manipulate that to achieve demanding torque for the motor. This manipulation ratio is called the modulation index (m_i). This index can be calculated as in equation 1.

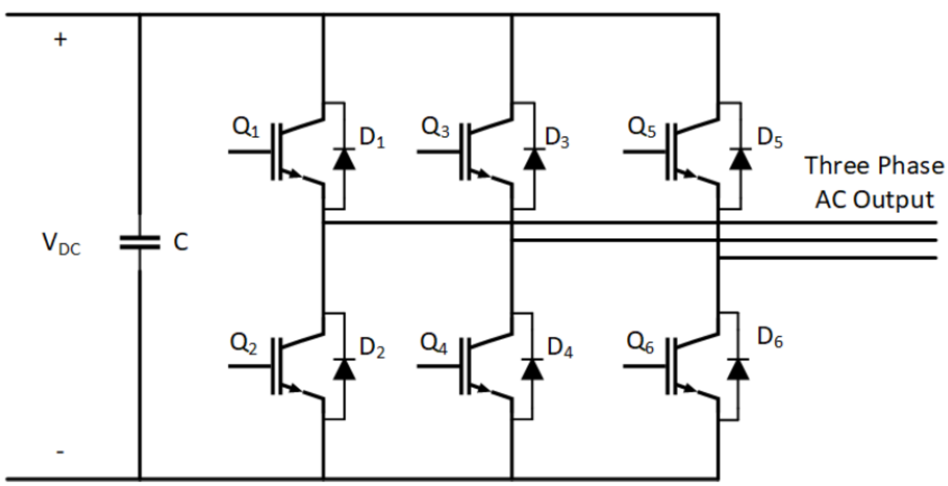

Figure 1: 2-Level Inverter Topology.

$$m_i = \frac{2V_{ph}}{V_{DC}} \tag{1}$$

2.2 2-Level Inverters and Control Methods

The voltage source inverters can be classified by the output voltage level. In 2-level inverters, phase voltage changes between $-V_{DC}/2$ to $+V_{DC}/2$. For example, the peak voltage level can be expressed as in equation 2. The equation 3 can be used for the line-to-line voltage.

$$V_{AN} = m_i \frac{V_{DC}}{2} \tag{2}$$

$$V_{l-l} = m_i \frac{\sqrt{3}V_{DC}}{2\sqrt{2}} \tag{3}$$

The voltage level can be manipulated by adjusting the opening and closing time of the switches. This can be done by applying turn-on and turn-off voltage to the switches. In figure 1, the switches are IGBTs. This can be Si or SiC MOSFETs according to applications. However, the IGBT is enough for this research topic, as well as most motor drive applications like this. Detailed information will be given in the component selection part of the report.

Each switch's opening and closing time must be adjusted with a reasonable time interval. The control of these time intervals can be defined using pulse width modulation (PWM) signals. There are different PWM techniques based on their applications and complexity. In this research, Sinusoidal PWM (SPWM) and Space Vector PWM techniques will be observed. These two techniques for 2-level inverters are explained in the following sections.

2.2.1 Sinusoidal PWM Technique

In sinusoidal PWM, to determine opening and closing time of the switch, there are carrier signal and reference signal in control part. For each phase there is a one carrier signal with 120-degree phase shift. The reference signal for legs is common, with only one triangular signal. The carrier signal and reference signal is compared for each phase separately. The top switch will be opened if the carrier is larger than the reference. Otherwise, the bottom switch will be opened in this leg. Therefore, the output voltage of the each phase will be change between $-V_{DC}/2$ and $+V_{DC}/2$. The carrier signals for each phase and opening and closing behaviour of switches with respect to this comparison can be seen in Figure 2. The maximum voltage level for the output is $V_{DC}/2$. However, when the SVPWM is used, maximum voltage can be $V_{DC}/\sqrt{3}$. The comparison of both methods can be seen in Figure

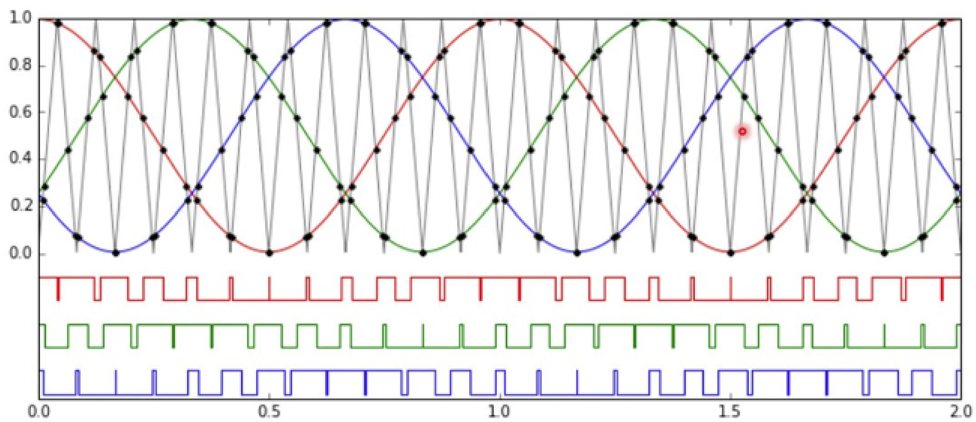

Figure 2: 2-Level Inverter Sinusoidal PWM Signals.

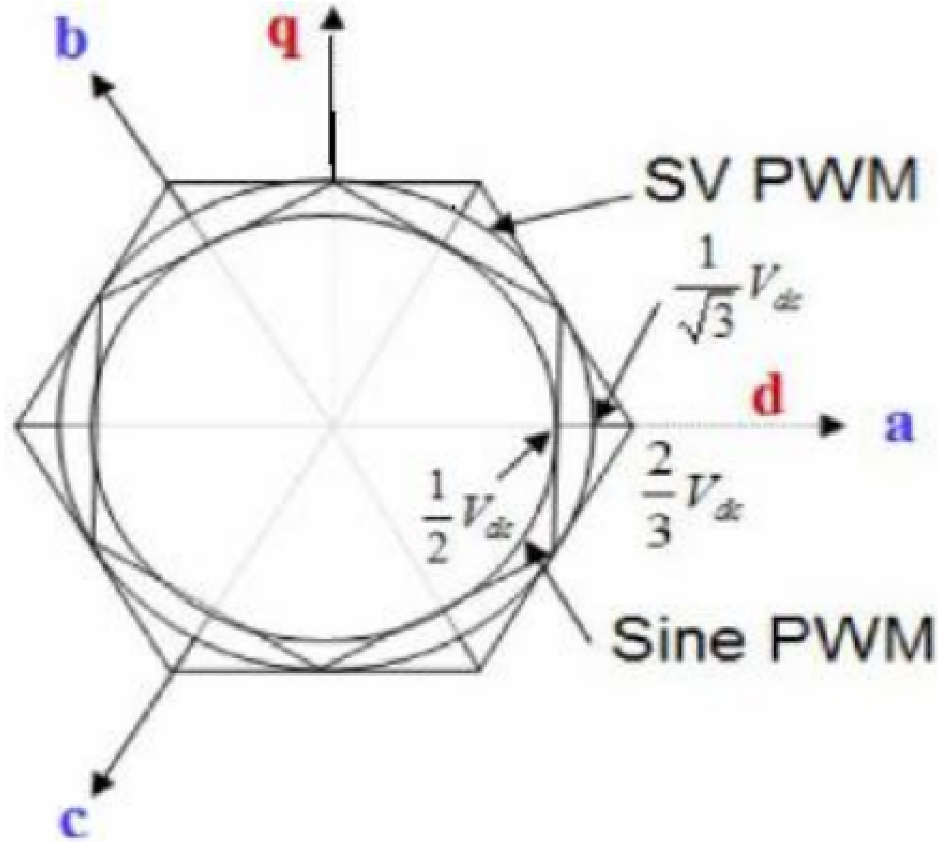

Figure 3: Sinusoidal PWM and SVPWM Comparison.

2.2.2 Space Vector PWM (SVPWM) Technique

In Space Vector PWM, the aim is that we want to control a stationary frame instead of a rotationary frame. The sinusoidal signals are converted to d and q frames, and according to the reference vector, the time and magnitude of the applied vectors are determined. In each leg, we can obtain positive (1) or negative (0) voltage at the output. Since there are three legs, we can obtain 8 different vectors. When the voltage is positive, we open the top of the leg. Otherwise, we open the bottom switch to obtain negative voltage. Opening the entire top (111) or bottom (000) vectors gives the zero vector. These are the same vectors according to the reference vector. The vector diagram can be seen in Figure 4.

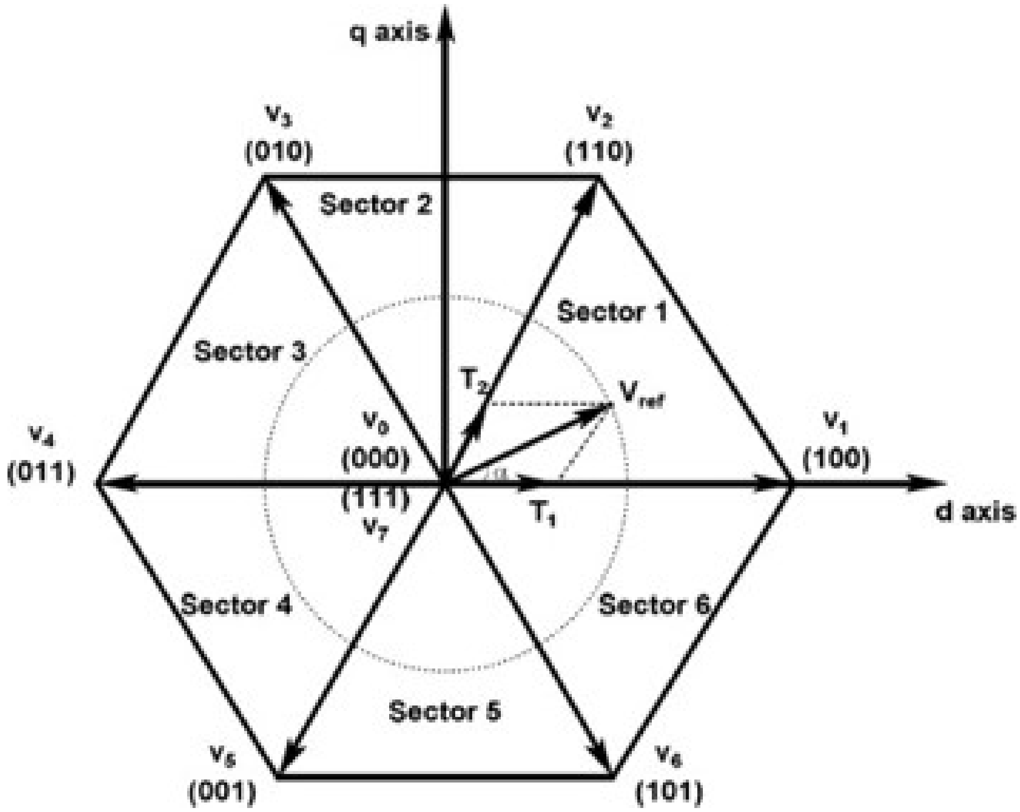

Figure 4: 2-Level Inverter SVPWM Vector Diagram.

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The opening and closing sequences of the switches affect the inverter's efficiency. Therefore, in each time, only changing one switch position increases the inverter's efficiency. The zero vectors are used to ensure this transition.

2.3 3-Level Inverters and Control Methods

In the 3-level inverters, there are three different voltage levels. They are $+V_{DC}/2$, 0 and $-V_{DC}/2$. These voltage levels can be named P-state, O-state, and N-state, respectively. Two more switches are at the middle of each leg to obtain these levels. Therefore, there are 12 switches in a 3-level inverter topology. The NPC and T-Type inverters can be seen in figure 5a and figure 5b respectively.

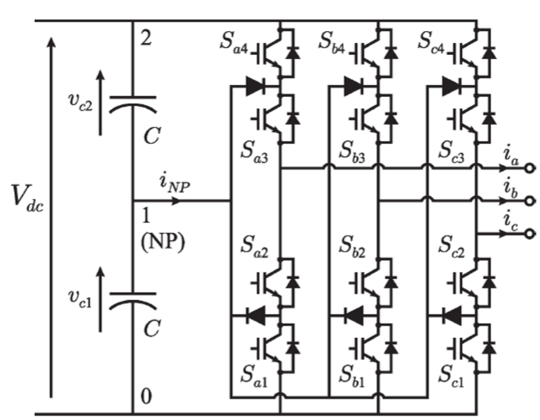


Figure 5a: 3-Level NPC Inverter

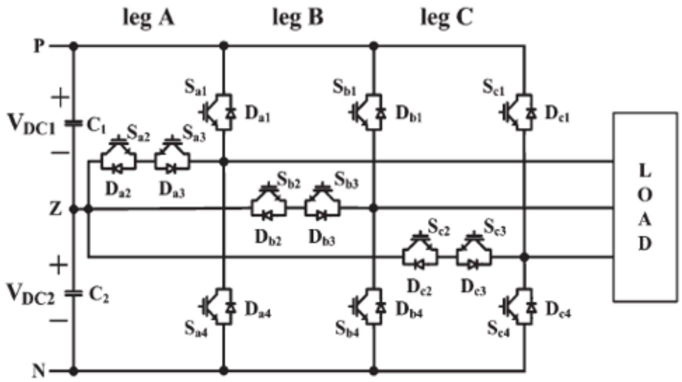


Figure 5b: 3-Level T-Type Inverter

In T-type inverters, P,O, and N states can be obtained by opening different switches in each leg. For example, to obtain P-state at leg-A, Sa1 and Sa2 switches must become open at the same time. The O-state can be obtained by opening Sa2 and Sa3 switches. The Sa3 and Sa4 must be opened to obtain N-state in this topology. All these possibilities are shown in Table 1.

State	Vout	Sa1	Sa2	Sa3	Sa4
P-state	$+V_{DC}/2$	ON	ON	OFF	OFF
O-state	0	OFF	ON	ON	OFF
N-state	$-V_{DC}/2$	OFF	OFF	ON	ON

Table 1: 3-Level T-Type Inverter Voltage States.

These states can be obtained like 2-level inverters by using the sinusoidal PWM technique. In 3-level inverters, there is one more carrier signal. One carrier signal is between 0 and 1 and the other is between 0 and -1. These signals can be seen in figure 6.

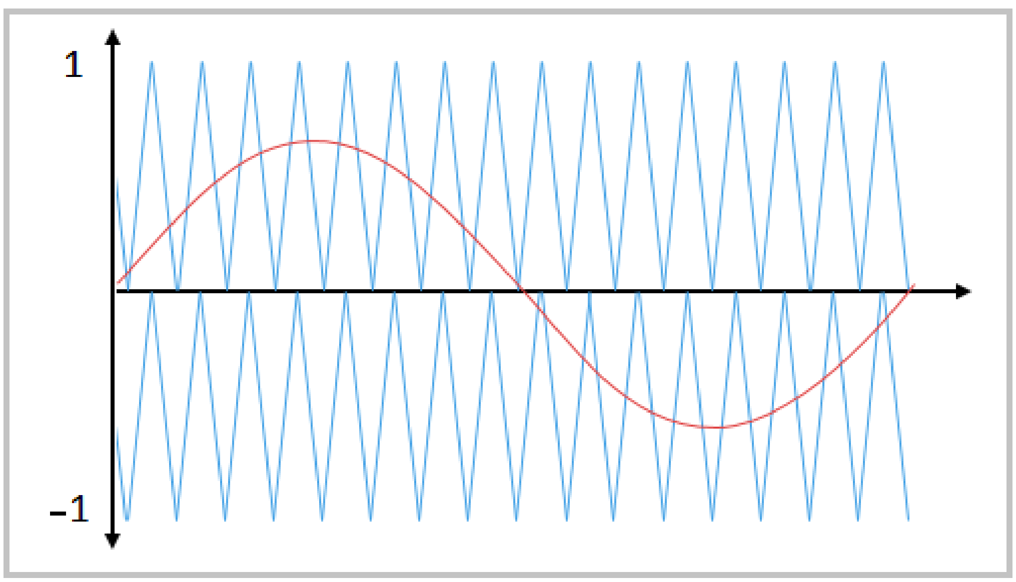


Figure 6: 3-Level Inverter Sinusoidal PWM Method, carrier and reference signals.

Concerning the magnitude of these signals, the states of each leg will be determined. For example, if the first signal (between 0 and 1) and the second carrier signal (between 0 and -1) are larger than the reference signal, the state of the leg is "P." The whole possibilities can be seen in Table 2. For 3 phases, there must be three reference signals with a 120-degree phase shift.

As was mentioned in the 2-level inverter section of this report, another PWM technique is Space Vector PWM. This technique is investigated in the following section.

State	Comparison	Sa1	Sa2	Sa3	Sa4
P-state	Carrier1 < reference carrier2 < reference	ON	ON	OFF	OFF
O-state	Carrier1 > reference carrier2 < reference	OFF	ON	ON	OFF
O-state	Carrier1 < reference carrier2 > reference	OFF	ON	ON	OFF
N-state	Carrier1 > reference carrier2 > reference	OFF	OFF	ON	ON

Table 2: 3-Level Inverter Sinusoidal PWM Voltage States.

2.3.1 SVPWM for 3-Level Inverters

In 3-level inverters, there are 3 different states for each leg. Therefore, 27 different vectors are possible for the 3-level inverter. PPP, OOO, NNN are the same and the zero vector as in 2-level inverters. The vector diagram of SVPWM can be seen in Figure 7. The inner vectors have alternative vectors. Therefore, there is a redundancy for these vectors.

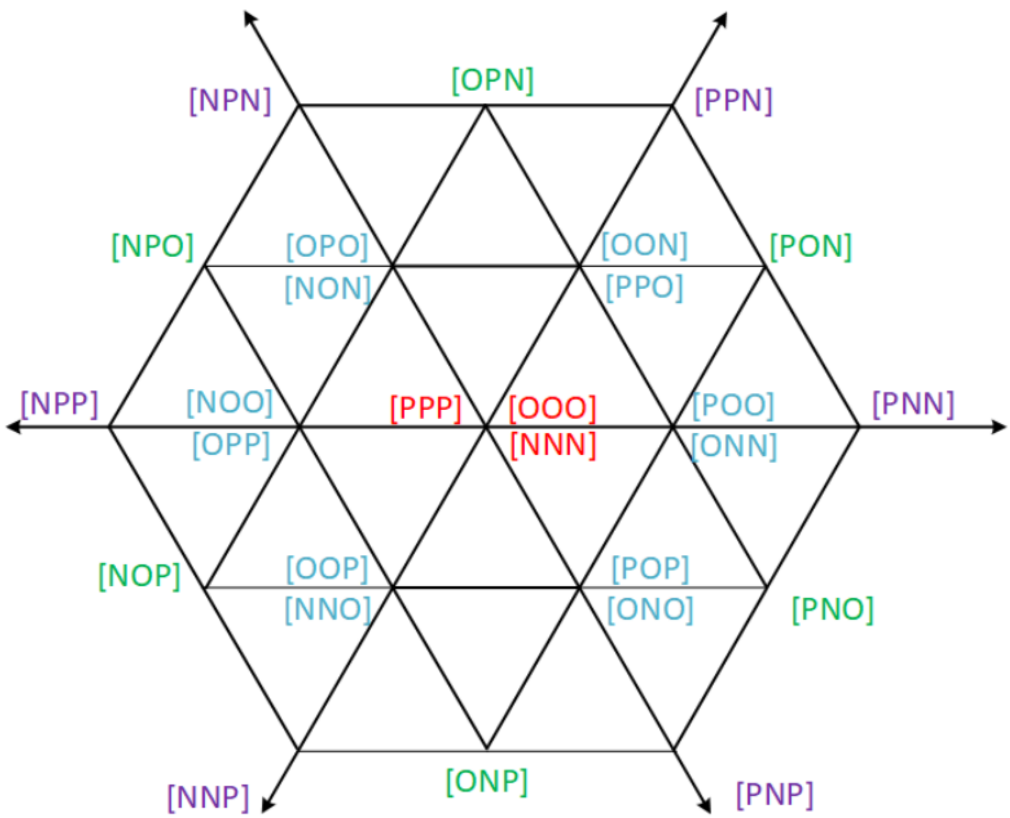


Figure 7: 3-Level Inverter SVPWM Vector Diagram.

As in 2-level inverters, detecting the region of the reference vector is critical to applying correct vectors in the regarding period. There are 6 different regions for the vector. Then, center-aligned SVPWM methods can be applied to the control algorithm. The vector is shifted to the center of each region, and each region can be considered as a 2-level vector diagram.

The regions can be seen in Figure 8. To determine the sectors, situations of the phase voltage can be used. The decision of main sectors is shown in Table 3. Afte the main sector is specified, the origin is moved to the center of the region. The reference vector is also moved to the center according to shifted ratio. The ratios can be seen in Figure 9

Va	Vb	Vc	Main Sector	Center Vectors
>0	<0	<0	1	POO/ONN
>0	>0	<0	2	OON/PPO
<0	>0	<0	3	OPO/NON
<0	>0	>0	4	OPP/NOO
<0	<0	>0	5	OOP/NNO
>0	<0	>0	6	POP/ONO

Table 3: 3-Level Inverter SVPWM Region Decision.

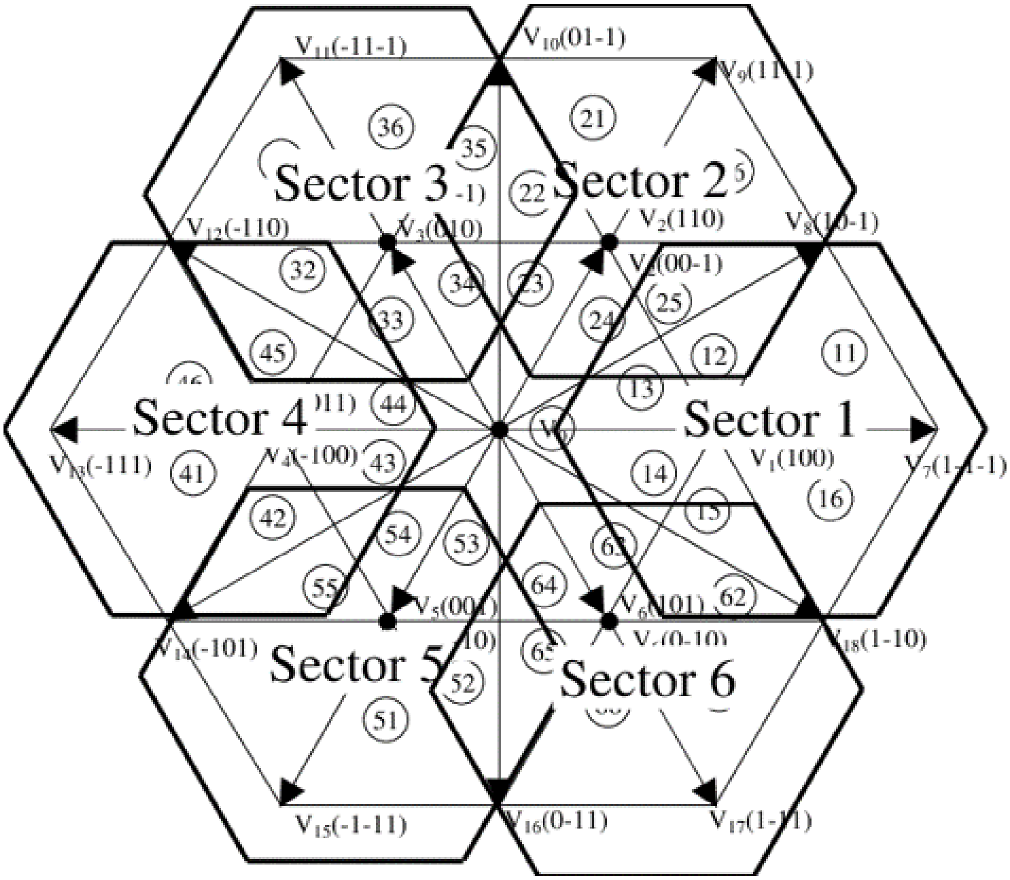


Figure 8: 3-Level Inverter SVPWM Vector Diagram Regions for Center Aligned Method.

Major Region Number	Required Computation
1	$\alpha' = \alpha - \frac{V_{DC}}{3}$ $\beta' = \beta$
2	$\alpha' = \alpha - \frac{V_{DC}}{6}$ $\beta' = \beta - \frac{V_{DC}}{\sqrt{3}}$
3	$\alpha' = \alpha + \frac{V_{DC}}{6}$ $\beta' = \beta - \frac{V_{DC}}{\sqrt{3}}$
4	$\alpha' = \alpha + \frac{V_{DC}}{3}$ $\beta' = \beta$
5	$\alpha' = \alpha + \frac{V_{DC}}{6}$ $\beta' = \beta + \frac{V_{DC}}{\sqrt{3}}$
6	$\alpha' = \alpha - \frac{V_{DC}}{3}$ $\beta' = \beta + \frac{V_{DC}}{\sqrt{3}}$

Figure 9: 3-Level Inverter SVPWM New Center Shift Ratio for Center Aligned Method.

2.4 3-Level Inverters Fault Status

So far, inverters have been investigated under normal operations. However, due to the nature of the components or some possible faults caused by external factors, some parts of the inverter might be failing. In some applications, the motor must continue with failure. Before examining the operation behavior of the inverter, it is necessary to classify the error conditions.

In this research, the failure of the switches will be investigated. The fault in the switch may appear as an open circuit or short circuit fault.

2.4.1 Short Circuit Fault State

In the short circuit failure, over current is observed between two switch terminals. The switch can not resist this current thermally, which affects other switches. Under short circuit conditions, the inverter can not keep driving the motor. Therefore, observing the short circuit condition is not suitable for this research.

2.4.2 Open Circuit Fault State

In open circuit conditions, the inverter can continue driving the motor. This is because the open circuit failure keeps is local. The current of the other switches does not increase as a short circuit failure. On the other hand, the voltage stress over the switch in the same leg becomes V_{DC} as in a 2-level inverter. If the designer wants to drive the motor under fault conditions, the voltage and current ratings of the switch must be chosen concerning this condition.

2.4.3 Space Vectors Under Fault Conditions

The SVPWM method can still work with some restrictions in open circuit failure. As mentioned in the SVPWM section of the report, some space vectors have redundancy and can be obtained by using different states of the vector diagram. However, which switch is open circuit is important for the circuit's operating behavior. These conditions will be investigated in this section.

The failure conditions and available vectors are similar for each leg. For this reason, only the fault states of phase A were considered in the following examples. The one leg ofthe 3-level NPC inverter can be seen in figure 10.

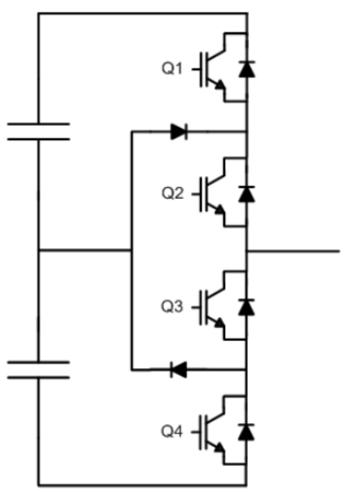


Figure 10: 3-Level NPC Inverter Leg-A Swithces.

Q1 Open Circuit When the switch named Q1 is an open circuit, the only state that we can not obtain is the P-state when the current is positive. In P-state, when the current is negative, it follows the path over the diode of Q1. The path of positive current can be seen in figure 11a. Therefore, for the Q1 fault, we can not obtain the vector beginning with P in the diagram. On the other hand, there are alternatives for PPO, POO POP vectors. Therefore we can obtain the yellow region in figure 11b.

As can be seen in the SV diagram, the inner hexagonal area is still available for the motor drive. Therefore, with lower performance (due to the smaller vector we can use), we can still drive the AC motor properly.

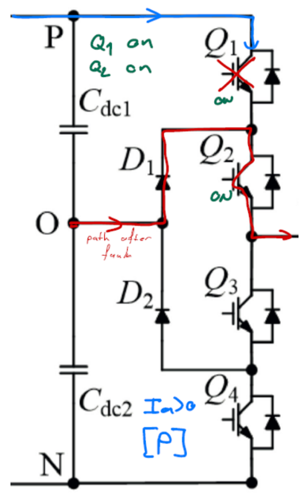


Figure 11a: Current Path for Ia positive, P state, Q1:ON Q2:ON.

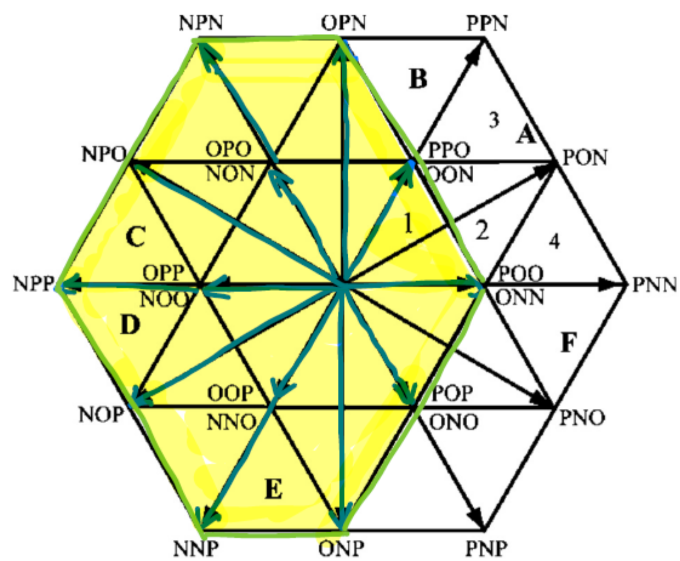
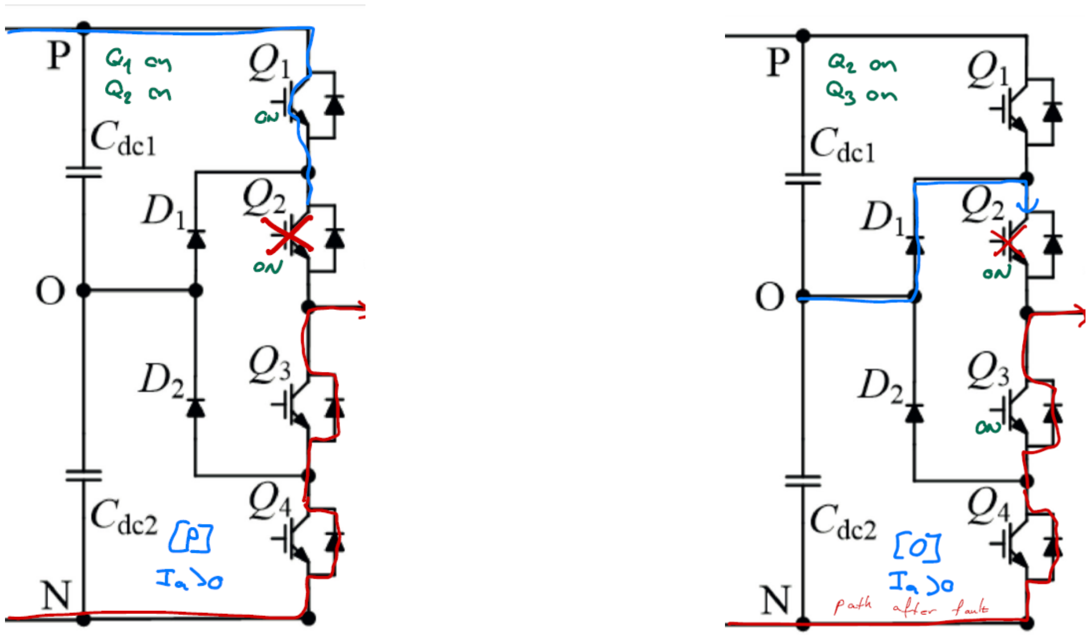


Figure 11b: SVPWM Diagram after Q1 open circuit.

Q2 and Q3 Open Circuit The failure conditions of Q2 and Q1 are more dramatic than those of Q1. When Q2 becomes an open circuit, the P and O states can not be obtained for positive current. The current path of phase-a current can be seen in figure 12a and 12b for P-state and O-state respectively.

When this failure happens, the vectors, including the P or O state, can no longer be obtained. Therefore, only the vectors in the small yellow area in figure 13 are available. So, the inner hexagonal area isn't actually used for this kind of failures.



(a) P State Error

(b) O-State Error

Figure 12: Current Path for Ia positive, P state and O State.

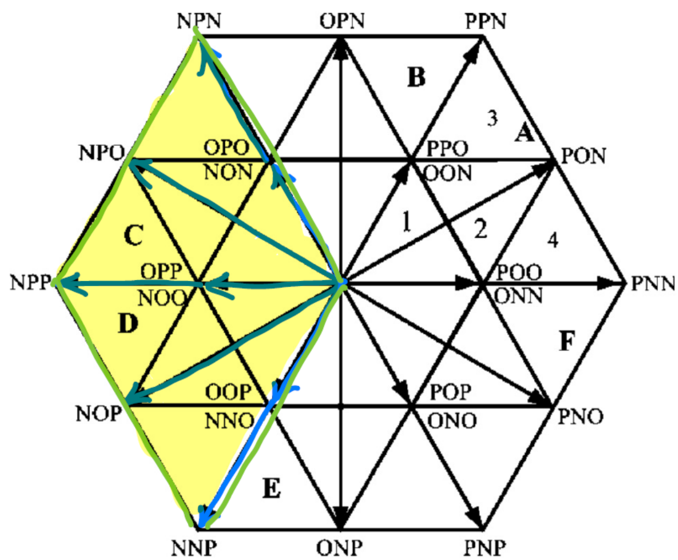
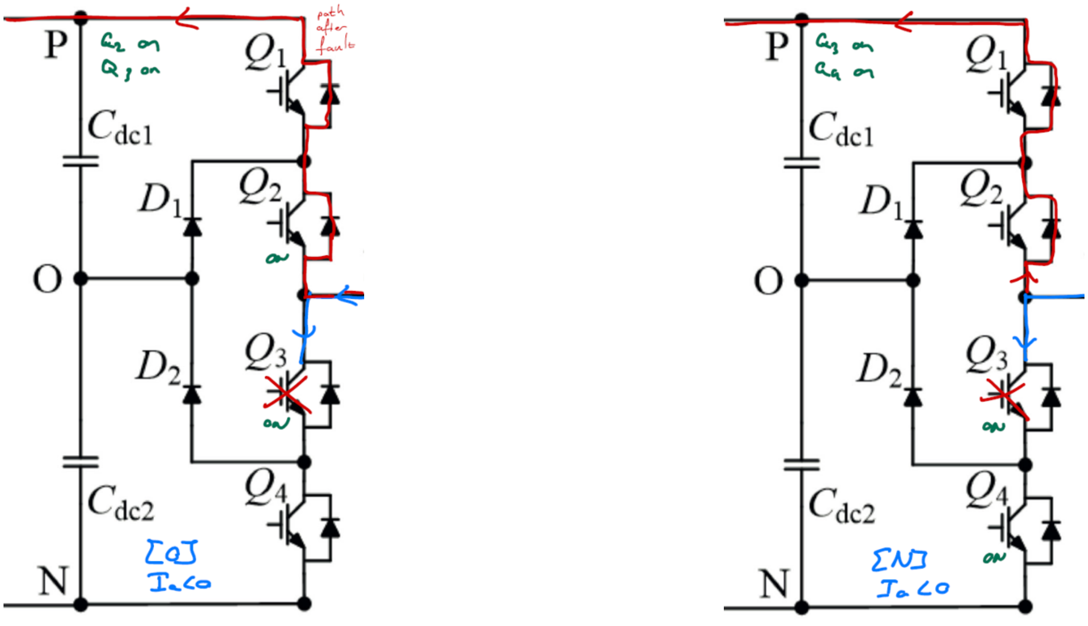


Figure 13: SVPWM Diagram after Q2 open circuit.

There is a similar behavior for the open circuit condition of Q3. This time, O and N states can not be obtained for the negative phase current. The current path for the O and N states can be seen in Figure 14a and 14b, respectively. This time, only the small right area is available for the motor drive. The available vectors can be seen in Figure 15.



(a) O-State Error

(b) N-State Error

Figure 14: Current Path for Ia negative, N state and O State.

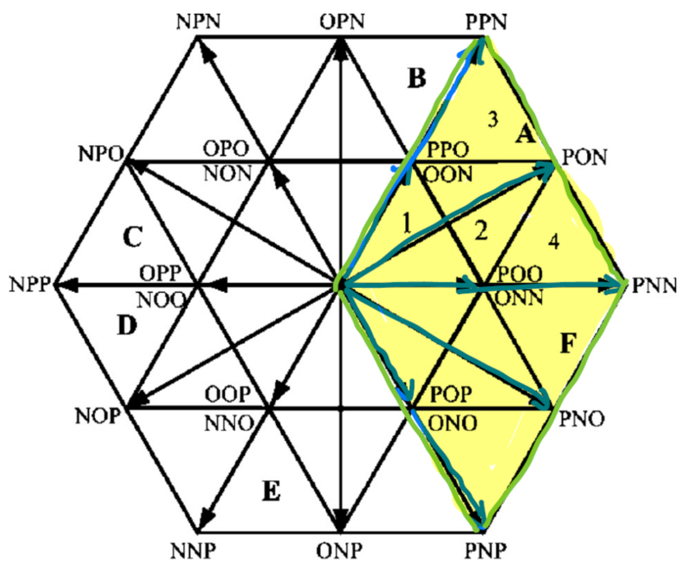


Figure 15: SVPWM Diagram after Q3 open circuit.

Q4 Open Circuit The fault behavior of Q4 is also similar to Q1. The only impossible state for the inverter is the N-state for the negative phase current. The current path for the negative current at state N can be seen in Figure 16a. Therefore, the only vectors that we can not use are NPN, NPO, NPP, NOP, and NNP. The available diagram can be seen in Figure 16b. Like the Q1 fault, we can use the inner hexagonal area to drive the motor.

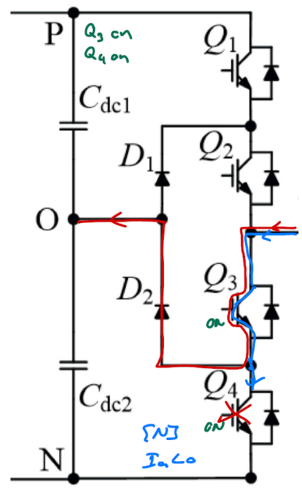


Figure 16a: Current Path for Ia negative, N state

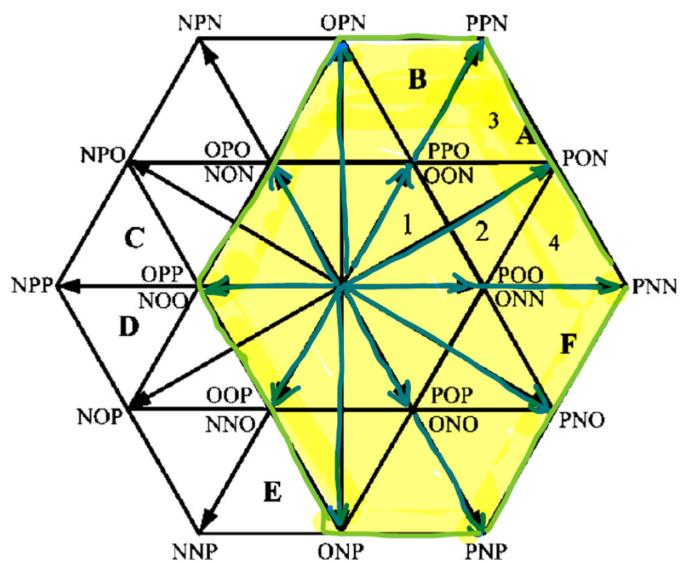


Figure 16b: SVPWM Diagram after Q4 open circuit.

3 2-Level and 3-Level NPC Inverter PCB Boards

The 3D borads of 2-level inverter and 3-level inverter can be seen in Figure 17a and Figure 17b respectively.

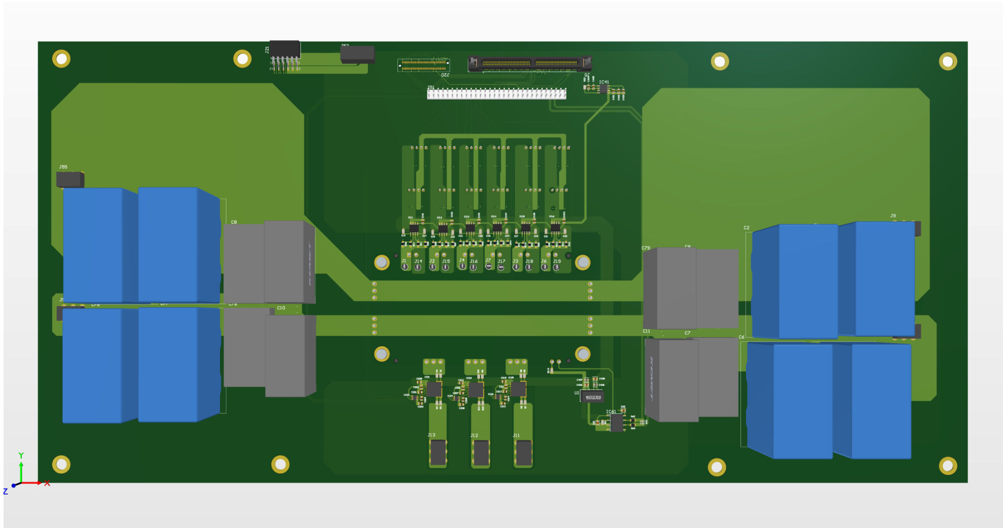


Figure 17a: 2-Level Inverter PCB Board

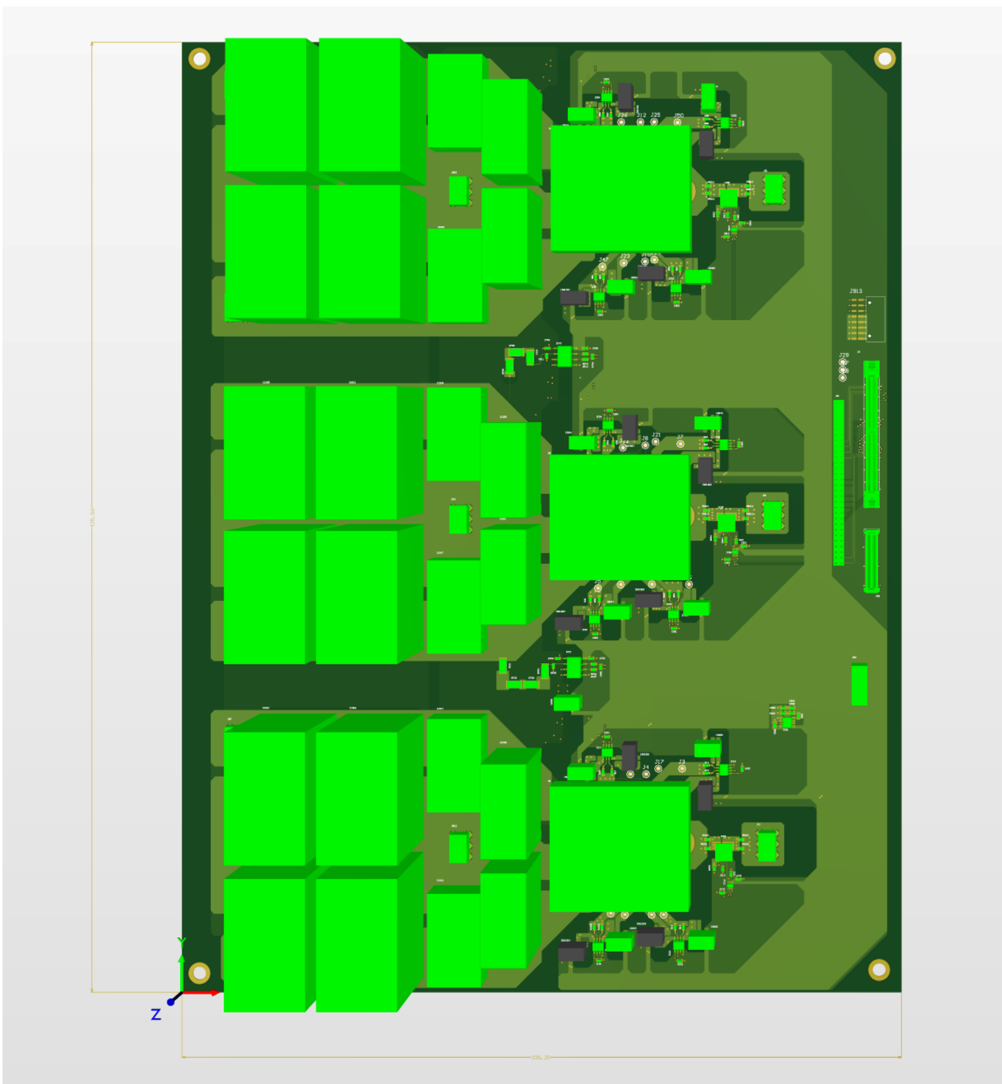


Figure 17b: 3-Level Inverter PCB Board

4 Conclusions and Future Works

In this report, mainly literature review was explained briefly. The 2-level and 3-level inverters are designed according to 15kW IPMSM motor driving. The schematic of the inverters can be found at the attachment with this report. The components of 3-level inverter and 2-level inverter were placed to boards. However, there are problems for the cards. Also, there is a simulation in Matlab. The control of the inverter is working properly. However, the control of neutral point needs to be fixed. This will be improved. All future work are explained in the next section.

4.1 Future Works

The planned progress for the thesis is as follows.

- The components of 3-level inverter is placed on board. While low voltage part of the card is testing a short circuit was observed. This problem will be solved and short circuit test will be completed.
- There is a Matlab simulation for 3-level NPC inverter. However, control of neutral point of the inverter is not working properly. The contol circuit will be improved.
- The NPP control methods are studied but not in details. Methods are searched to improve control method of the circuit.
- Under fault conditions, there is no control methods for unbalanced DC link capacitor problem. It will be investigated whether this topic will be suitable for the article.
- High voltage tests of the inverter will be completed and performance measuremnts will be taken.
- Fault conditions will be observed on board by using C2000. The fault situations are planned to be created by interrupting the PWM output from the controller.