Strategies of Fault Tolerant Operation for Three-Level PWM Inverters

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***Abstract*—This paper proposes fault tolerant operation strategies for three-level neutral point clamped pulsewidth modulation inverters in high power, safety-critical applications. Likely faults are identified and fault tolerant schemes based on the inherent redundancy of voltage vectors are presented. Simulation verification is performed to show fault handling capabilities. Prototyping and principle investigation are performed on a 150-KW inverter and testing results are presented.**

***Index Terms*—Fault tolerant, neutral-point-clamped (NPC) inverter, pulsewidth modulation (PWM), three-level inverter.**

I. Introduction

In HIGH performance safety-critical applications, such as flywheel energy storage systems, any failure of a power electronics inverter has very serious consequences towards the overall system. Fault tolerant requirements are of extreme importance and have been extensively discussed in the literature. It is established that deploying a power electronics inverter capable of continuing operation in the presence of any single point failure is essential for the system.

Past research works described in the literature have concentrated on improving reliability by means of multiple independent phase units [1], [2] for two-level inverters. Based on the general concept of parallel redundancy, the redundant-phase approach heavily depends on the capability of a general n-phase motor to continue operation with $(n-1)$ or less stator phases excited. The principle of phase redundancy is also extended to the electric machine design by Mecrow [2] and Nabae [3], where fault tolerant permanent magnet machine drive schemes, including phase redundancy in PM motor design and interaction of solid state converter failure with motors, are examined.

With more and more use of three-level neutral point clamped (NPC) pulsewidth modulation (PWM) inverters in high power, high performance, safety-critical drive applications, it is a very significant task to analyze the fault tolerant operation capability of three-level NPC-PWM inverters. This constitutes the research topic of this paper.

Compared to a conventional two-level dc–ac inverter, a three-level inverter has a very distinguished power circuit. The ac outputs of a three-level inverter are inherently of more than two levels of dc voltages and often have more than one choice of modulation to achieve the same wanted ac voltages. In effect, three-level inverters have challenged many researchers to invent so-called optimal switching strategies to address various special issues. Up until recently, there exist a large number of recorded activities in developing new and effective switching schemes for three-level inverters. Nabae [3] proposed the concept of (NPC) three-level inverters for the purpose of developing high efficiency motor drive systems. The fifth and seventh harmonic elimination modulation scheme was proposed for the inverter operation. Liu [4] conducted a comparative study between harmonic elimination and optimal PWM strategies for high power three-level induction motor applications. Liu [5] also proposed a space vector modulation scheme to avoid the narrow pulse problem in the low index modulation region. An analogy to controlling the two level inverters, sine-triangle (PWM) schemes are proposed in Carrara [6] and Sinha [7]. It has been suggested that $N-1$ triangle carrier signals should be used for an N-level inverter and only one sinusoidal modulation signal for each phase. Zhang [8] proposed a genuine use of three-level inverter to eliminate motor common mode voltage. However, as seen in the above mentioned literature, there rarely are recorded activities in enhancing the inverter reliability in three-level inverter through PWM modulation scheme development.

In this paper, we propose several fault tolerant inverter modulation strategies. The strategies target continuing operation of a three-level inverter at any single power device failure. In particular, all the proposed strategies do not rely on adding redundancy by constructing an additional phase leg, as is usually done in a two-level inverter to achieve fault tolerant capability. Instead, the proposed strategies make use of the inherent redundancy of a three-level inverter to achieve fault-tolerant capabilities.

We will focus on dealing with short-circuit faults in the paper. The issue of device open circuit fault is addressed only slightly and deserves a separate paper. Likely faults are identified and fault tolerant schemes are presented. Simulation verification is provided to show fault handling capability. Prototyping and principle investigation are performed in the laboratory on a 150-kW three-level (NPC) inverter and testing results are presented.

II. Three-Level Inverters and Fault Tolerant Strategy

A. Power Electronics Circuit and the Associated Voltage Vector Diagram

A typical three-level (NPC) inverter circuit is shown in Fig. 1. There are 12 active power devices (transistors anti-parallel with diodes) and six voltage clamping diodes in the circuit.

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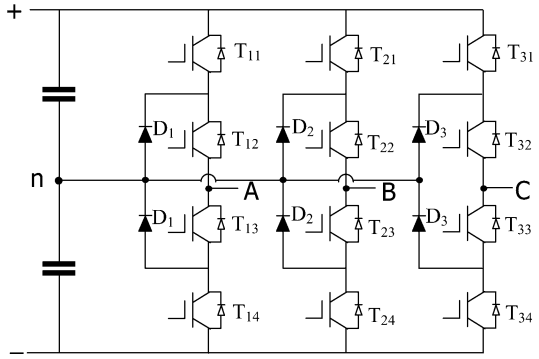

Fig. 1. Three-level (NPC) inverter circuit.

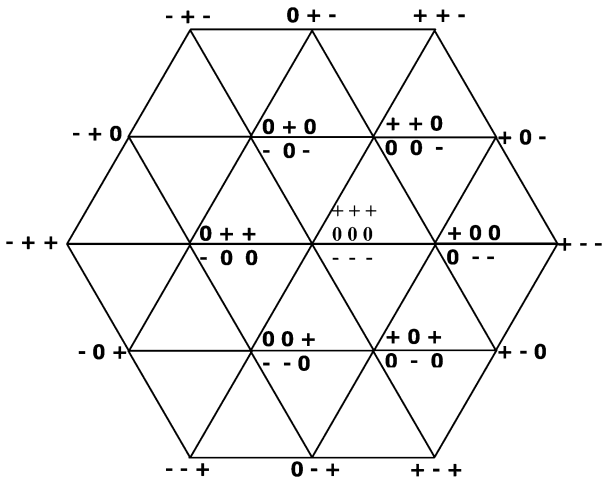

Fig. 2. Vector diagram of three-level inverters.

The associated voltage vector diagram is shown in Fig. 2. The convention used in the figure is described as follows. At each jointing point of lines is indicated one set of three-phase ac output voltage in terms of dc bus voltage levels. Notice that the three-phase ac output voltages are specified as a combination of $-$, 0, and $+$, representing if the ac terminals are connected to the negative, mid-point, and positive dc bus. For example, $0\pm$ implies that Phase A is connected to the mid-point, Phase B the positive point, and Phase C the negative point of the dc bus. According to the vector diagram, there are 19 different voltage vectors. However, there are 27 connection possibilities to the dc bus points for the 19 ac vectors.

As evidenced by the voltage vector diagram, inherent redundancy exists in the process of ac voltage vector synthesizing. This feature can be utilized to produce a fault tolerant PWM inverter modulation scheme to enhance the system reliability.

In the following, we first focus on the case of power device short circuit fault, and assume that there is only one power device short circuit in one of the inverter legs in each fault mode. The fault tolerant objective is to continue the inverter operation while waiting for the next service opportunity in a safety-critical situation although in some cases we have to derate the system.

B. Fault Conditions Detection and Mode Transition

Assuming Phase A failure, possible single-device short circuit conditions are categorized as follows (see Fig. 1).

- Case I: $\boldsymbol{T}_{11}$ or $\boldsymbol{T}_{14}$ short circuit.
- Case II: $\boldsymbol{T}_{12}$ or $\boldsymbol{T}_{13}$ short circuit.
- Case III: Clamping diode $\boldsymbol{D}_{11}$ or $\boldsymbol{D}_{12}$ short circuit.

If fault conditions occur in the other two phases, we can categorize the faults accordingly. To detect the fault occurrence of short circuits, we can accomplish that by monitoring the gating signals and the corresponding voltage across the switches. In the event of a short circuit, the voltage across the faulted power device is deadly zero regardless of "turn-on" or "turn-off" gating signals being applied. Likewise, in the event of an open circuit, the voltage across the faulted power device is always none-zero value. Detecting these abnormal symptoms, the DSP controller will be able to make a decision regarding fault conditions. Note that the fault detection does not have to depend on additional hardware sensors but those peripherals already built into the gating circuitry and power modules.

For certain fault conditions, system derating is necessary (which will be made clear in later sections) and transitions into various fault tolerant operation modes can be designed in either a controlled fashion or by an uncontrolled system recovery fashion. In the latter case, we simply turn off the entire power module temporarily and the system will derate by itself. Our field testing indicates that a typical DSP is fast enough to accommodate the protection process. For the TI TMS320x2000 DSP, the interrupt latency is 10 clock cycles and with the 20-MHz DSP, the latency is only 0.5 μs, sufficiently fast for mode transition and power module protection.

C. Fault Tolerant Modulation Strategies

In the following analysis of the power inverter circuit with different fault conditions, we want to produce the modified voltage vector diagrams that give us the available vectors for fault tolerant operation. Modulation schemes under these fault conditions constitute a set of fault tolerant operation modes. As soon as a short circuit fault is detected and categorized, the related hardware triggers mode transition and the system is brought into one of these fault tolerant operation modes.

Fig. 3 represents the voltage vector diagram of the three-level inverter with the active device T_{11} short circuited. Due to the failure of T_{11}, all voltage vectors requiring T_{11} in the status "open" are disabled. The affected unavailble voltage vectors are shaded in red ink in the voltage diagram.

In a similar approach, Figs. 4 and 5 show the available and unavailable voltage vectors under the conditions of devices $\boldsymbol{T}_{12}$ and $\boldsymbol{D}_{11}$ short circuit, respectively.

As these voltage vector diagrams indicate, in the fault Case II or III, because the available maximum voltage amplitude is substantially reduced, the system has to be derated. While for fault condition in Case I, the system is not required to reduce its rating because most of the large voltage vectors are still available. However, for all cases of fault, the normal PWM modulation schemes have to be modified to avoid using the unavailable voltage vectors; otherwise, further damages and a total failure of the entire system may occur. As will be clarified later, one major impact of the PWM modulation modifications is on the capacitor middle-point potential control. The following section discusses this issue and the middle-point voltage control scheme is presented and analyzed.

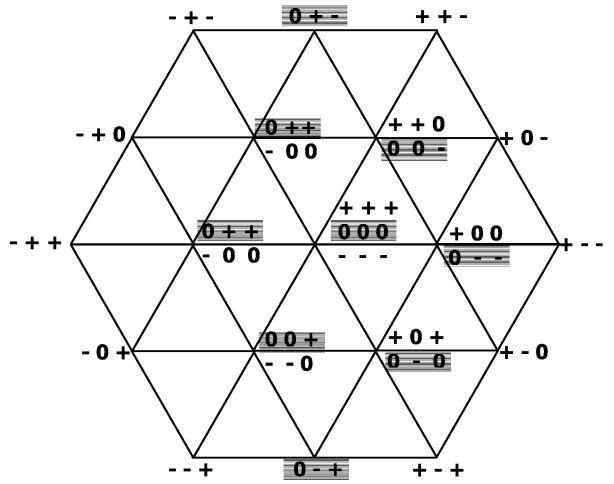

Fig. 3. Case of T_{11} short-circuited.

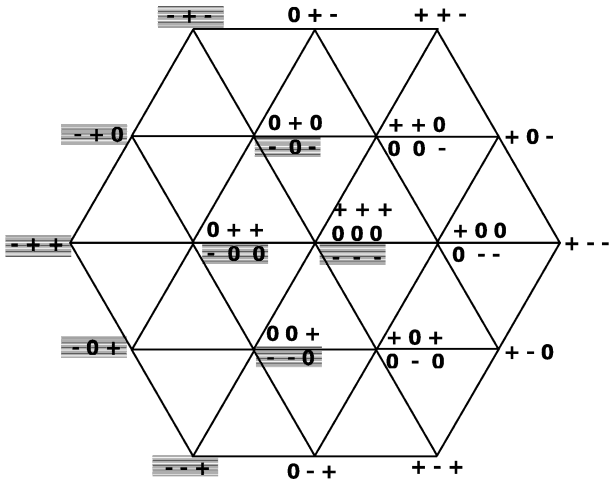

Fig. 4. Case of T_{12} short-circuited.

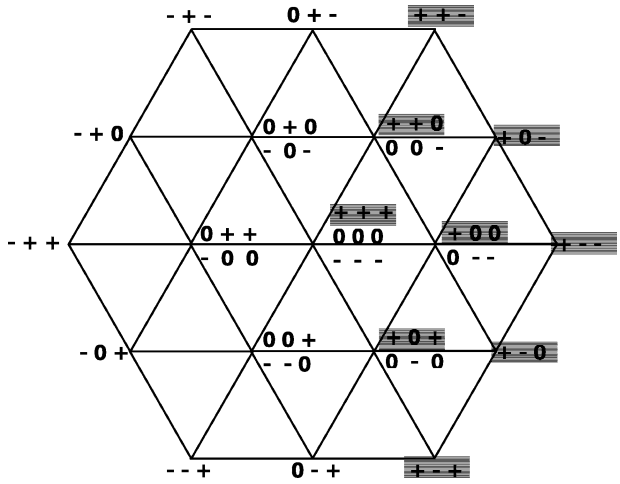

Fig. 5. Case of D_{11} short-circuited.

D. Capacitor Middle-Point Potential Control

Capacitor middle-point potential control is of essential importance for the fault tolerant modulation application and in one of our previous papers [9], we proposed a feedback control method based on detailed discussion. We will explain the controller principle through sliding mode control theory.

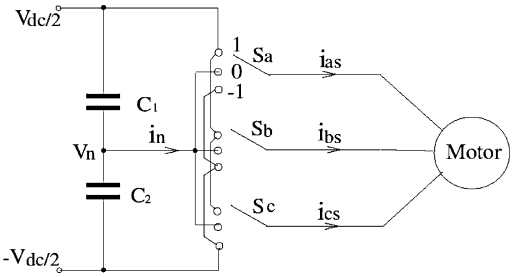

Fig. 6. Circuit model for calculating the capacitor middle-point voltage.

Fig. 6 shows the circuit configuration related to the dc bus capacitor middle-point voltage. The voltage reference is chosen at the ideal middle-point potential. The change rate of the capacitor middle-point voltage $\boldsymbol{V}_n$ is related to the current $\boldsymbol{i}_n$ through the equation

$$\dot{V}_{\boldsymbol{n}} = -\frac{\boldsymbol{i_n}}{\boldsymbol{C_1 + C_2}}. \tag{1}$$

Further, $\boldsymbol{i_n}$, the center tap current is related to the power switch status and all the ac phase currents on the load side. To clarify how all the switching action will affect the mid-pint voltages, we can first define the switching status as $\boldsymbol{S} = (\boldsymbol{S_a}, \boldsymbol{S_b}, \boldsymbol{S_c})$ with $\boldsymbol{S}_a, \boldsymbol{S}_b, \boldsymbol{S}_c \in \{1, 0, -1\}$ corresponding to the respective switching positions as labeled in Fig. 6. Then

$$\boldsymbol{i_n} = (1 - |\boldsymbol{S_a}|)\boldsymbol{i_{as}} + (1 - |\boldsymbol{S_b}|)\boldsymbol{i_{b_s}} + (1 - |\boldsymbol{S}_c|)\boldsymbol{i}_{cs}. \tag{2}$$

To actively control the capacitor mid-point voltage, by sliding mode control theory, let the sliding "surface" be $\sigma = \boldsymbol{V_n}$, then

$$\boldsymbol{\sigma\dot{\sigma}} = \boldsymbol{V_n}\dot{\boldsymbol{V}}_{\boldsymbol{n}} = -\frac{\boldsymbol{V_n i_n}}{\boldsymbol{C_1 + C_2}} = -\frac{\boldsymbol{V_n}|i_{\boldsymbol{n}}|}{\boldsymbol{C_1 + C_2}}\text{sign}(\boldsymbol{i_n}). \tag{3}$$

The sliding surface $\{\boldsymbol{\sigma} = \boldsymbol{V_n} = 0\}$ is stable if we can select the control such that $\boldsymbol{\sigma\dot{\sigma}} \leq 0$, i.e., $\boldsymbol{sign(i_n)V_n} \geq 0$.

As noted in [9], this can always be satisfied as long as the inner nonzero voltage vectors are not completely destroyed by the faulted power devices. In the fault tolerant modulation modes, we may lose some of these inner vectors but not most of them. A simulation is performed to investigate the capacitor middle-point potential behavior under the sliding mode control scheme. In the simulation, we assume that the system has been in the normal operation for a while and suddenly $\boldsymbol{T}_{12}$ is shorted at $t = 0.6$ s. Results are presented in Fig. 7, where the capacitor middle-point potential is seen as stable.

E. Simulation on Controlled Transition Into the Derated Fault Tolerant Mode

In this simulation, the system of a three-level inverter driving an interior permanent magnet (IPM) motor with a constant load torque is simulated. It is assumed that short circuit of $\boldsymbol{T}_{12}$ has

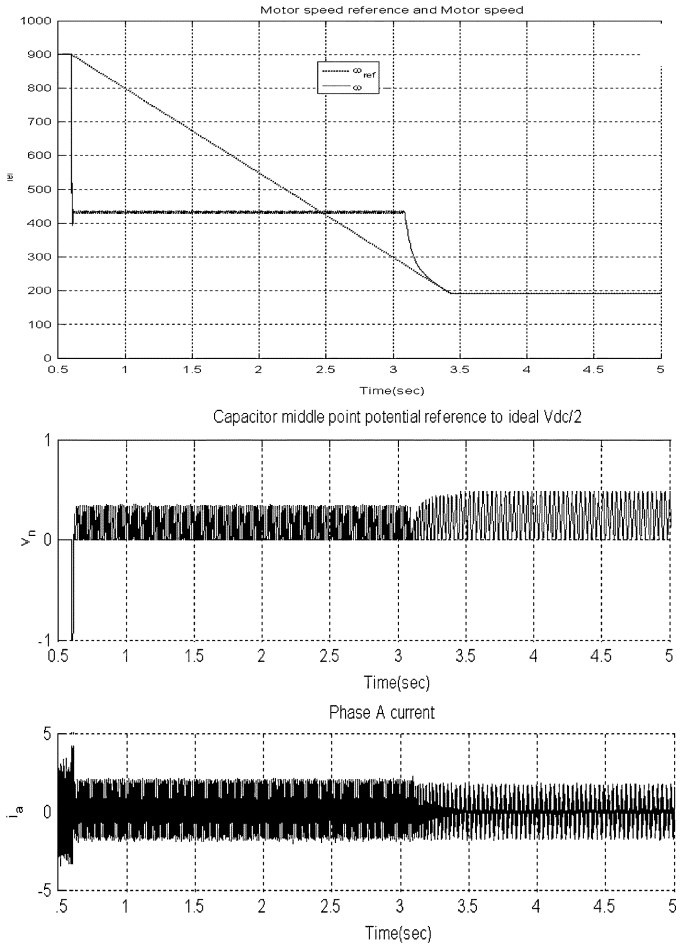

Fig. 7. Controlled transition into a deated fault tolerant modulation mode (T_{11} is shorted).

occurred at the instant $t = 0.6$ s. At the moment of fault, the shorted T_{12} is detected and fault categorized. Note that this fault condition immediately imposes two constraints on the subsequent fault tolerant operation: a) the three-level inverter lost some of the inner vectors and b) more importantly, because the available voltage amplitude is reduced under the fault condition (see Fig. 4), the system power rating has to be reduced. In the simulation, the fault tolerant strategy with derating is implemented. Fig. 7 depicts the system behavior with the motor decelerated to a lower speed to fit the available inverter voltage. The results also show the changes of the capacitor middle-point voltage and phase current from health to the fault tolerant operation. Transient process exists because of the current regulator saturation in the transition process, where the command voltage vector is scaled down to within the synthesizable area. As seen in the figure, capacitor middle-point potential is under control by using the feedback scheme discussed above.

III. Prototyping and Experimental Investigation

Selected fault tolerant strategy is implemented and built into the controller for a prototype system to verify the principle discussions. The prototype system is ultimately targeted for a fault tolerant three-level inverter to a flywheel energy storage system supplying power to critical loads. A 150-kW three-level inverter

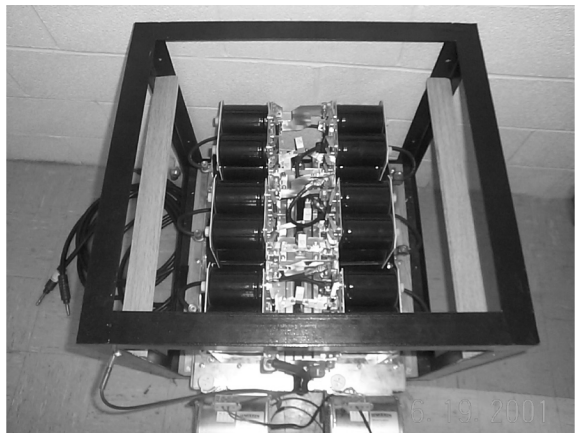

Fig. 8. Picture of the constructed three-level inverter.

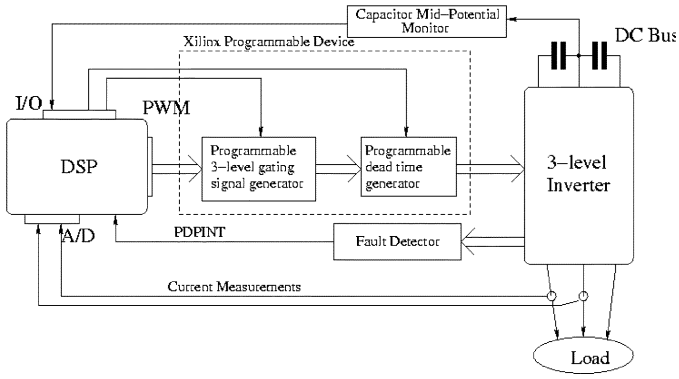

Fig. 9. System configuration and DSP–three-level inverter interfacing.

is first constructed through the modular approach. Fig. 8 shows the picture of the three-level inverter and Fig. 9 the block diagram of the overall system, including power inverter and DSP controller.

A. DSP Controller and Implementation of PWM Modulation Schemes

The central issue of DSP controller design is to implement the PWM schemes for both normal and fault tolerant situations. In prototyping, the fault tolerant modulation scheme is implemented with the normal nearest three vectors (NTV) modulation technique and the DSP can switch between these two schemes in real time upon receiving fault signals.

By NTV, any voltage vector is synthesized by the three base vectors, which form the surrounding triangle to the desired vector. Switching to the fault tolerant strategy, the normally available base vectors in NTV have to be changed to whatever available according to the faulting conditions as described in Figs. 3–5.

In terms of hardware, Fig. 10 shows a detailed description of block diagram for the dash-line framed part in Fig. 9. This part of the circuit is used to interface the DSP controller and the gating circuitry of the power module.

Upon NTV or fault-tolerant algorithm execution in real time, the DSP generates a set of (PWM) signals relevant to Phases A, B, and C. However, the set of gating signals need further interpretation and deployment to the specific gating circuits of the

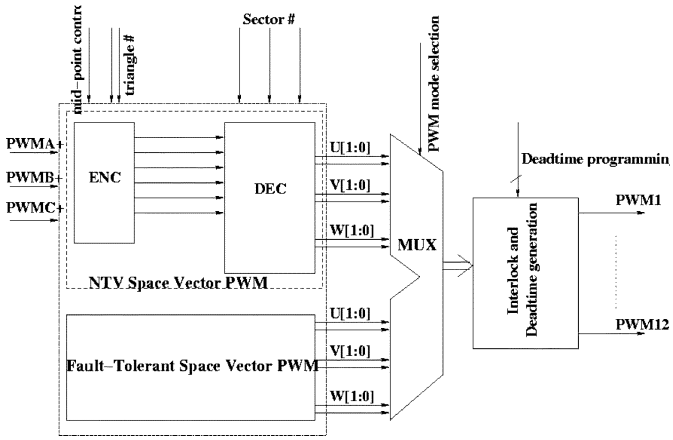

Fig. 10. Interface structural description.

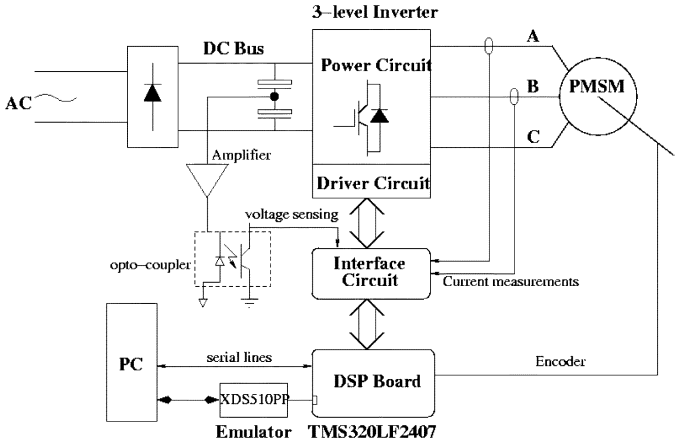

Fig. 11. Laboratory setup for the three-level inverter testing.

three-level inverter; that is how the interfacing circuit of Fig. 10 comes to play. As indicated in the figure, multiple modulation schemes (including the fault tolerant ones) coexist in the design and can be selected by using multiplexing structures. As an example, in the Fig. 2 space vector modulation schemes (NTV space vector and fault-tolerant space vector PWM) are stored in the memory. The DSP can use I/O pins to control the MUX in real time operation for scheme selection and activation.

As to the fault tolerant modulation scheme implementation, we have basically followed the NTV design with a modification in such a way that the unavailable vectors are eliminated and new base vectors are formed depending on fault categories. In the fault tolerant scheme, the controller will first turn off all active power devices in the power converter to let the load of the system—the electric machine be coasted down to a proper speed. Then, the controller switch to a new PWM algorithm where the lost vectors due to fault are not used. At the same time, the dc bus mid-point voltage is monitored and controlled. Fig. 4 is an example that shows the availability of the basis voltage vectors when power device $\boldsymbol{T}_{12}$ is shorted. For hardware design, a Xilinx CPLD is used to map the general PWM signals into the specific 12 gating signal deployment.

B. Control of the Capacitor Middle-Point Potential

In order to implement the capacitor middle-point potential control algorithm presented in Section III, the DSP controller needs to evaluate the current $\boldsymbol{i_n}$ coming in or flowing out of the capacitor middle point. Whenever there is an ac terminal among the three phases connected to the dc bus mid-point through switches, there may be a current flowing in or out of the capacitor middle point, causing mid-point voltage to drift. For the mid-point voltage control, $\boldsymbol{i_n}$ calculations are listed in the following, where $\boldsymbol{T}_1$ and $\boldsymbol{T}_2$ are the duty ratio of the first and the second voltage vectors respectively in a single space vector PWM period.

Note that in $\boldsymbol{i_n}$ evaluation, we have neglected the current contributed by the six outer vectors involving both upper and lower half dc bus: $(+0-), (0+-), (-+0), (-0+), (0-+)$, and $(+-0)$. In the case of using the only upper half dc bus, $\boldsymbol{i_n}$ experiences exactly the opposite of the corresponding current flow when using the lower half dc bus. In order to implement the software programming, the following matrix representation is needed. For example, in Sector 0 and Triangle 0 (see Fig. 2), using the upper half dc bus, we have

$$\boldsymbol{i_n} = [\boldsymbol{T}_1 \ \boldsymbol{T}_2 \ 1-\boldsymbol{T}_1 \ -\boldsymbol{T}_2] \begin{bmatrix} 1 & 0 & 0 \\ 1 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \boldsymbol{i_a} \\ \boldsymbol{i_b} \\ \boldsymbol{i_c} \end{bmatrix}.$$

Since the matrices are all of sparse type, typical techniques for sparse matrix and the associated data structure algorithm can be used in the software programming, which is very CPU time-saving.

C. Laboratory Test Setup and Test Results

1) Laboratory Setup: Due to the limitations, the prototyped 150-kw three-level inverter can not be tested to its full power rating in our university laboratory. Additionally, for contract and confidentiality reasons, the tested data in the full power level are not allowed to release in the paper. Instead, a low voltage eight-pole PM machine is used as the load to the three-level inverter and much reduced voltage is used. The testing is essentially at the level of proof-of-concept to verify implementation method of fault-tolerant control scheme for the three-level inverter. All of the tests presented below are run under the condition of 50-V dc bus supply and with the eight-pole PM machine. The machine parameters are as follows and consistent to the case simulated:

$$\boldsymbol{L_d} = 80\,\mu\boldsymbol{H}, \quad \boldsymbol{L_q} = 108\,\mu\boldsymbol{H}, \quad \text{and} \quad \chi = \frac{\boldsymbol{L_d}}{\boldsymbol{L_q}} = 0.74.$$

System connection and hardware interfacing are described in Fig. 11, including the three-level inverter, PM machine, electrical (ac current and mid-point dc bus voltage) and mechanical (rotor positions) feedback signals, DSP controller and peripherals, and a host PC.

2) Test Results of Fault Tolerant Operation: In the testing, the DSP controller first detects a fault after a period of time in normal operation—for example, shorting circuit of device $\boldsymbol{T}_{12}$, and then the controller activates the fault tolerant control

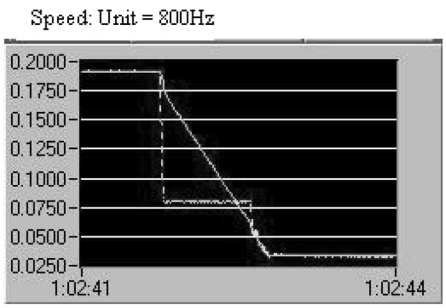

Fig. 12. Speed control during the transition into fault tolerant mode.

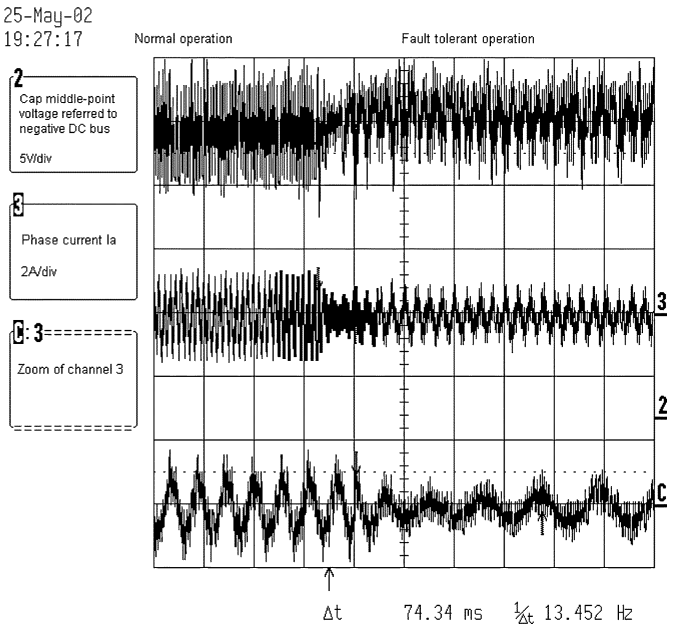

Fig. 13. Controlled transition into fault tolerant operation mode.

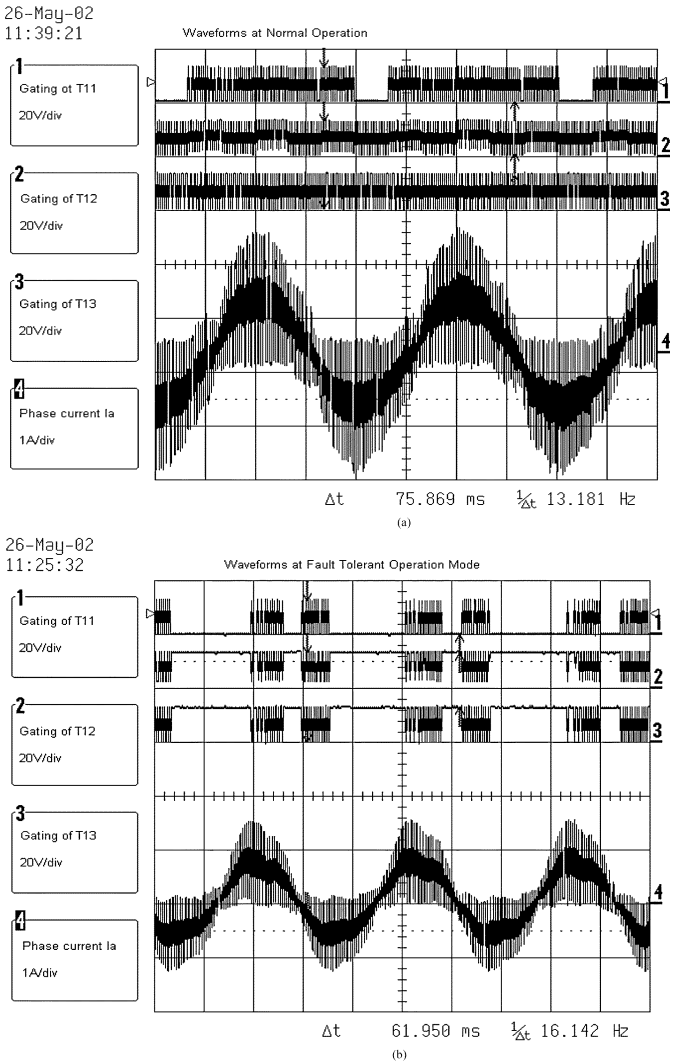

Fig. 14. (a) Gating signals and current waveforms at normal operation mode. (b) Gating signals and current waveforms at fault tolerant mode.

strategy. All the necessary steps in the algorithm intend to ensure that the system continues to operate instead of a total shutting down until the next service opportunity comes.

As we predicted by the computer simulation in last section and the testing results in Fig. 12, the motor speed is reduced as soon as the fault occurs and subsequently the DSP controller starts to reconstruct the voltage vectors within the available region in the voltage vector diagram. Since the motor is very small in inertia, the motor speed reduces very fast and as soon as the motor speed falls into the controllable range, the current regulator restores its function and the speed regulator recaptures the rotor to follow the commanded speed reference.

The mid-point dc bus voltage, and the ac current in Phase A are shown in Fig. 13 as the first and second traces recorded by a digital scope. The third trace is the amplified phase current showing the current transition from the normal to the faulted conditions.

In controlling the midpoint voltage, the algorithms decribed in Section II-D are applied; that is, the average current $\boldsymbol{i_n}$ over an allowable time interval (deciated by the size of dc capacitors) needs to be zero. Otherwise, an unstable mid-point voltage results. In the tested case, the short device is $\boldsymbol{T}_{12}$. As indicated by the vector diagram in Fig. 4, most vectors on the left side are no longer available but for those available, the controller still has a choice of vectors associated with upper or lower half dc buses. The fault tolerant control scheme ensures that whenever the voltage vectors in the smaller hexgon are used, the control algorithm rotates the selection of voltage vectors involving the upper and lower half dc bus. Note that in the tested fault case, the selectable vectors are much less than the ones in a none-faulted mode. Therefore, the system will not have tight control over the mid-point voltage. As predicted, the testing results still show a controlled midpoint voltage with a larger ripple. The dc bus mid-point potential during the mode transition shows its normal behavior and is in good conformity with the simulation predictions presented in the last section.

The testing results are generally in a good agreement with those obtained by computer simulations as shown in Fig. 7. As we stated before, the ac output voltage is reduced after the transition from normal to the fault tolerant modes. Upon the mode transition, the base voltage vectors and the synthesis method have to be updated in real time. Fig.14 (a) and (b) compare the gating signals to T_{11}, T_{12}, and T_{13}, and the current $\boldsymbol{I}_{\mathrm{a}}$ before and after the fault occurs. It is evident that the inverter-motor

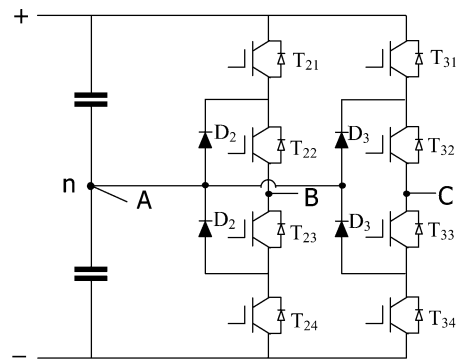

Fig. 15. Circuit configuration for fault tolerant operation at device open circuit.

system did not stop its operation but simply changes its operation modes.

IV. Brief Treatment of Device Open Circuit Fault

To fully deal with fault conditions, the three-level inverter should also have its capability to handle conditions caused by a device open circuit fault. In such a case, we have to abandon one inverter leg and connect the corresponding motor terminal to the capacitor middle point. For convenience of discussion, we assume that the Phase A inverter leg is lost due to a power device fault of open circuit. Fig. 15 shows the circuit configuration when the faulted terminal is reconnected to the mid-point of the dc bus through a preinstalled thyristor. We can examine the voltage vector availability by inspecting the space vector diagram in Fig. 16 where the lost voltage space vectors are crossed out.

A. Voltage Vector Diagram Under the Inverter Reconfiguration

Denote $\boldsymbol{d_2}$ and $\boldsymbol{d_3}$ the switching functions for Phases B and C, respectively, with $d_2, d_3 \in 1,0,-1$. Assume also that the load is a three-phase Y-connected balanced load. Then it can be proven that the available voltage vectors are

$$\begin{aligned} \boldsymbol{V_{dq}^s} &= \boldsymbol{V_q^s} - j\boldsymbol{V_d^s} \\ &= \left\{ -\frac{\boldsymbol{d_2}+\boldsymbol{d_3}}{2} + \boldsymbol{j}\frac{\sqrt{3}}{2}(\boldsymbol{d_2}-\boldsymbol{d_3}) \right\} \frac{\boldsymbol{V}_{\rm dc}}{3}. \end{aligned} \tag{4}$$

In the expression, the possible values of $\boldsymbol{d_2}$ and $\boldsymbol{d_3}$, $(1, 0, -1)$ refer to the ac output voltage terminals connected to positive, mid-point, or negative of the dc bus. The above space vector expression shows that there are only nine voltage vectors under this connection. Fig. 16 shows these vectors in the stationary d–q plane and the associated switching status.

As can be seen from the expression for the stationary reference frame, the maximum d-axis voltage vector magnitude is $1/\sqrt{3}\boldsymbol{V}_{\rm dc}$, and the q-axis $1/3\boldsymbol{V}_{\rm dc}$. The necessity of derating from the regular dc–ac inverter is very clear in terms of the voltage magnitude. It is helpful to recall that the regular inverter is capable of producing voltage vector with maximum magnitude of $2/3\boldsymbol{V}_{\rm dc}$.

If the dc bus capacitors are large enough, the current rating does not have to change. However, if the capacitor is relatively small or the balanced load is at a very low frequency, the dc bus mid-point potential may drift significantly during the positive or negative current half cycles. So it is possible that the current capability of the new configuration may also have to be derated.

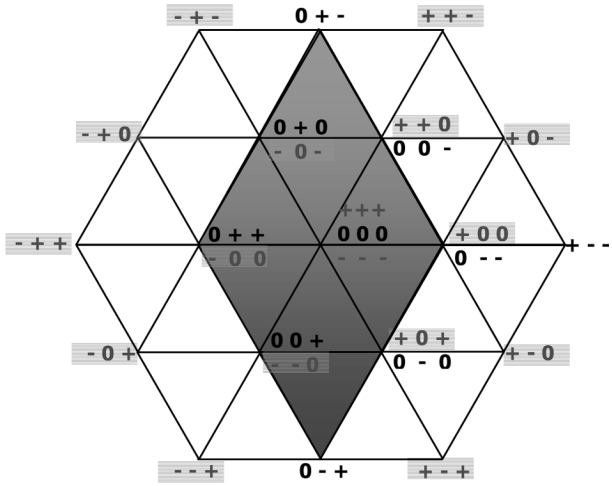

Fig. 16. Vector diagram at the open circuit fault tolerant operation.

B. Space Vector PWM Scheme in Open Circuit Fault

Fig. 16 indicates that as the convex hull of all the available voltage vectors all contain the zero vector. Then, the space vector PWM scheme can be implemented to drive a three-phase balanced load. It is very interesting to make a comparison of the space vector diagram of a three-level inverter with that of a two-level inverter under the similar device open circuit fault. In the three-level inverters, because the ac output can be clamped to capacitor bank middle point, we have five more vectors available. There is some redundancy in the voltage vector diagram as well. This redundancy may be utilized to accommodate PWM modulation schemes to actively control the capacitor middle-point potential, especially under unbalanced situations or at very low fundamental frequencies. This constitutes a future research topic. Another point that is worth noticing is that in the three-level inverter, we have a zero vector available under the device open circuit fault tolerant control configuration. This makes the PWM modulation much easier for the three-level inverters. To appreciate the point, note that in the two-level configuration, because none of the available voltage vectors are the native zero vectors, if needed, we have to synthesize the zero vectors using other none-zero native voltage vectors. While in three-level inverters, three zero vectors are available and we don't need any extra zero vector synthesizing at all, eliminating switching noise and associated losses.

V. Conclusion

In this paper, we proposed several fault tolerant modulation strategies for three-level (NPC) PWM inverters under single device short circuit fault conditions. A simulation is performed to verify the feasibility of the strategies. Laboratory prototyping and an experimental investigation are performed to verify the theoretical analysis and discussion. Applications of the fault-tolerant three-level power inverter and its control algorithms in high power, high performance, and safety-critical

situations such as flywheel energy storage systems is still underway. More detailed analysis on fault conditions, including open-circuit fault and laboratory results will be reported in a future paper if permission is given.

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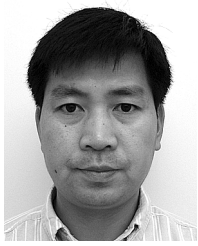

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