# A Survey on Neutral-Point-Clamped Inverters

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***Abstract*—Neutral-point-clamped (NPC) inverters are the most widely used topology of multilevel inverters in high-power applications (several megawatts). This paper presents in a very simple way the basic operation and the most used modulation and control techniques developed to date. Special attention is paid to the loss distribution in semiconductors, and an active NPC inverter is presented to overcome this problem. This paper discusses the main fields of application and presents some technological problems such as capacitor balance and losses.**

***Index Terms*—Neutral-point-clamped (NPC) inverters.**

## I. Introduction

MOST industrial processes need to increase efficiency and reduce production costs. This is achieved by increasing the size of installations and increasing the power of all electrical machines and equipment. This increase in power is reached in two ways: 1) by developing high-voltage semiconductors with voltage blocking capabilities of 3300, 4500, and 6500 V and 2) by developing a multilevel inverter. Now, it is possible to directly connect the power converter to the medium-voltage (MV) network.

At low voltage, there is a single topology that dominates the market: the voltage-source two-level inverter. However, at medium and high voltages, the situation is completely different. A wide variety of topologies share the market and the applications of industrial MV drives [1, Fig. 1]. In effect, for high-power applications, it is possible to use direct converters (cycloconverters) or indirect converters (with current or voltage dc link).

The continuous development of high-voltage insulated-gate bipolar transistors (IGBTs) and integrated-gate commutated thyristors (IGCTs) and the application of these power semiconductors in several multilevel voltage-source converter (VSC) topologies have led to a drastic increase of the nominal voltage and power ratings of self-commutated converters in recent years. Pulsewidth modulation (PWM) VSCs have replaced thyristor-based converters in a wide range of applications. This is largely due to substantial system advantages, such as increased availability due to ride through capability and/or a redundant converter design, drastically improved dynamic performance, extended operating range, reduced line harmonics, and an adjustable power factor at the point of common coupling.

Highly popular are the voltage-source multilevel inverters, which can be divided into three categories, according to their topology: neutral point clamped (NPC), flying capacitor (FLC), and cascade H-bridge [1], [2].

Among the high-power converters shown in Fig. 1, the NPC inverter introduced 25 years ago is the most widely used in all types of industrial applications [3], [4], in the range of 2.3 to 4.16 kV, with some applications up to 6 kV.

This paper presents a survey of the most relevant developments of this topology: concerning the modulation strategies and control methods, as well as the efficiency and use of power semiconductors. New topologies like the active NPC (ANPC) inverter are also discussed. Special attention is paid to the use of these inverters in nonregenerative and regenerative applications. Finally, the future of development in operation, control, and applications is highlighted.

## II. Diode-Clamped Three-Level Inverter

### A. Basic Operation of the Three-Level NPC Inverter

Fig. 2 shows the power circuit of the three-level diode-clamped inverter. The clamping diode dc is used to connect the neutral point $N$ to the midpoint of the transistor. This neutral $N$, generating an additional voltage level, yields the name "three-level inverter."

Fig. 3 shows the switching state that generates a positive voltage, at a load terminal. In this case, transitions $S_{a1}$ and $S_{a2}$ are switched ON, giving the value $V_{aN} = V_{\rm dc}/2$, where $\overline{S_{yx}}$ is the inverted signal of $S_{yx}$ ($x = 1, 2$ and $y = a, b, c$), in order to avoid forbidden states, like short circuits. Table I shows the conduction state to be generated.

### B. Modulation and Control Strategies for Three-Level NPC Inverters

As shown in Fig. 4, today, there are three main methods established to control the behavior of the fundamental voltage generated by the three-level inverter to the load. These methods are as follows: 1) carrier-based PWM; 2) space vector modulation (SVM); and 3) selective harmonic elimination (SHE).

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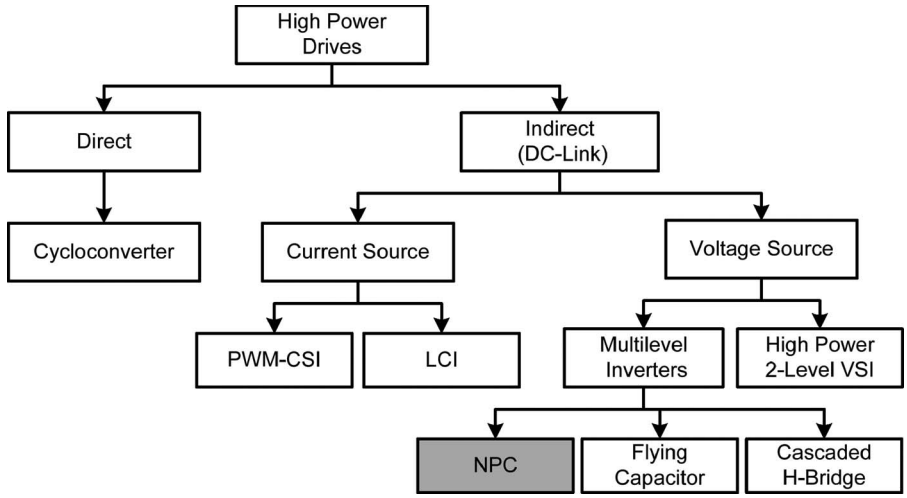


Fig. 1. Families of high-power converters.

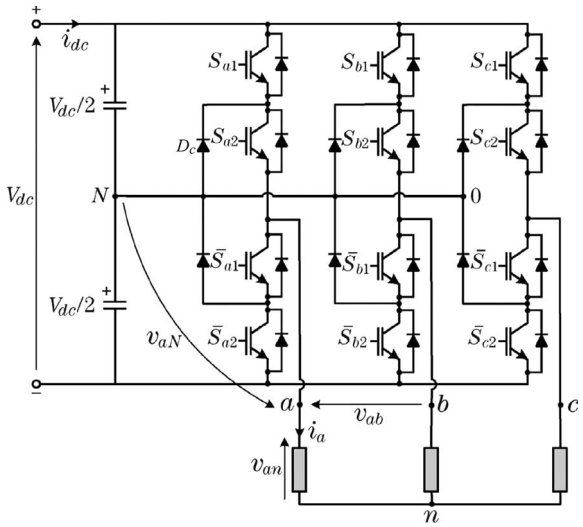


Fig. 2. Power circuit of the three-level diode-clamped inverter.

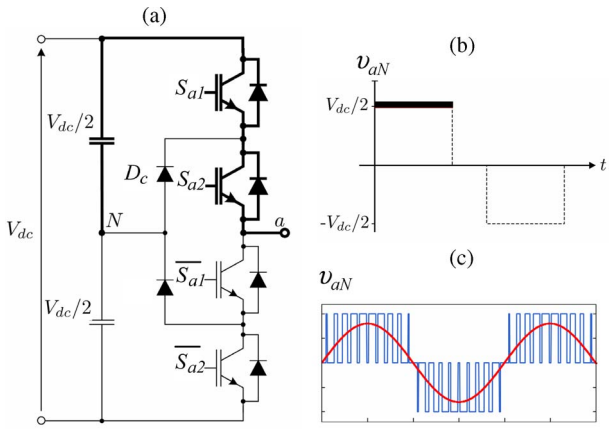


Fig. 3. Working principle of the three-level NPC inverter. (a) Conduction state to generate a positive load voltage. (b) Positive load voltage. (c) Complete load voltage showing three levels.

All modulation and control methods can be applied to the motor side inverter or the side active front end (AFE) inputs.

*1) Carrier-Based Three-Level PWM Modulation [5]–[9], [61]:* This highly popular method is based on the comparison

TABLE I
THREE-LEVEL SWITCHING STATE

| Output Voltage | Gate Signal | | Switching State |
|---|---|---|---|
| $v_{aN}$ | $S_{a1}$ | $S_{a2}$ | $S_a$ |
| $V_{dc}/2$ | 1 | 1 | (+) |
| 0 | 0 | 1 | (0) |
| $-V_{dc}/2$ | 1 | 0 | (-) |

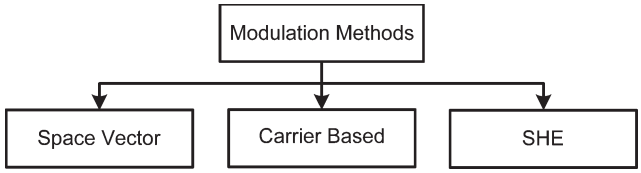


Fig. 4. Modulation methods for three-level diode-clamped inverter.

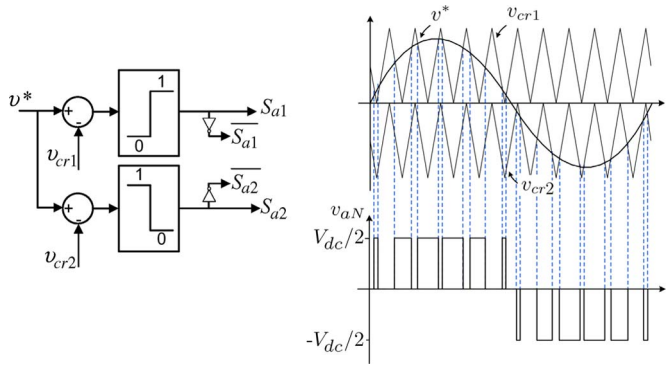


Fig. 5. Carrier-based PWM modulator.

of a sinusoidal reference $v^*$ with two carriers $v_{cr1}$ and $v_{cr2}$. As shown in Fig. 5, the logic is very simple

$$\text{if } v^* > v_{cr1} \Rightarrow S_{a1} = \text{ON} \qquad S_{a2} = \text{ON} \qquad v_{aN} = \frac{V_{\text{dc}}}{2}$$

$$\text{if } v_{cr2} < v^* < v_{cr1} \Rightarrow \overline{S_{a1}} = \text{ON} \qquad S_{a2} = \text{ON} \qquad v_{aN} = 0$$

$$\text{if } v^* < v_{cr2} \Rightarrow \overline{S_{a1}} = \text{ON} \qquad \overline{S_{a2}} = \text{ON} \qquad v_{aN} = -\frac{V_{\text{dc}}}{2}.$$

Today, the research on this modulation method is focused on the search for optimal switching sequences [5], operation at low

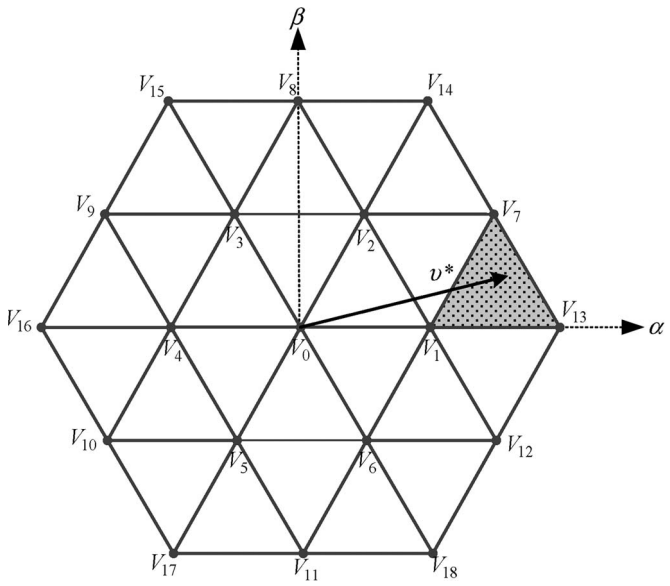


Fig. 6. Space vector modulator in three-level inverter.

modulation index [6], adaption to new topologies [7], [8], and reduction of common mode voltage [9].

*2) Space Vector Modulator [10]–[15], [33], [60]:* The three-level phase inverter has $3^3 = 27$ different switching states which generate different voltage vectors defined by

$$\overrightarrow{V_s} = \frac{2}{3}[V_{aN} + aV_{bN} + a^2V_{cN}] \tag{1}$$

where $a = e^{j(2\pi/3)}$. Fig. 6 shows the different voltages.

Vectors generate the three-level inverter. Some vectors have redundant switching states, meaning that they can be generated by more than one switching state. This is a very attractive feature that is used for the balance of capacitor voltages. In SVM, the reference vector $\upsilon^*$ (see Fig. 6) is generated from the closet vectors using the following:

$$\upsilon^* = \overline{\upsilon} = \frac{1}{T_s}[V_1 \cdot t_1 + V_7 \cdot t_7 + V_{13} \cdot t_{13}] \tag{2}$$

where $\overline{\upsilon}$ is the mean value of the load voltage, $T_s$ is the modulation period, and $t_1$, $t_7$, and $t_{13}$ are the times for the application of vectors $V_1$, $V_7$, and $V_{13}$, respectively. The problem to be solved is the calculation of these times with the following restriction:

$$T_s = t_1 + t_7 + t_{13}. \tag{3}$$

The modulator must also detect the position of the reference vector to identify the closest vectors [33].

Some recent research works are dedicated to the simplification of the modulation method [10], [11], implementation with field-programmable gate array [12], [14], and the reduction of dc-link capacitor [15]. Special care is taken to maintain a high-quality load voltage, operating at a very low switching sequence [13]. This is very important to reduce the losses of high-voltage semiconductors.

*3) SHE [16], [34]–[36]:* SHE is a very attractive option for the application in three-level inverters, because the equipment needs to operate at a very low switching frequency to reduce the semiconductors losses. Fig. 7 shows the load voltage generated by a three-level NPC inverter. Using three switching angles $\alpha_1$, $\alpha_2$, and $\alpha_3$ and 90° symmetry, three harmonics can be controlled [34]. The strategy is to control the fundamental frequency and to eliminate harmonics five and seven using

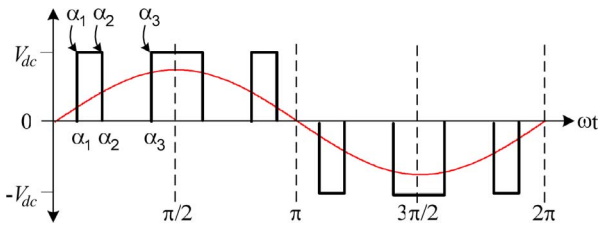


Fig. 7. Three-level SHE.

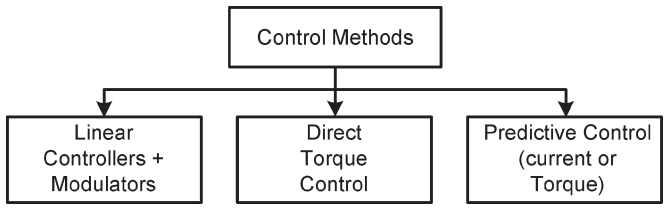


Fig. 8. Control methods for three-level NPC inverters.

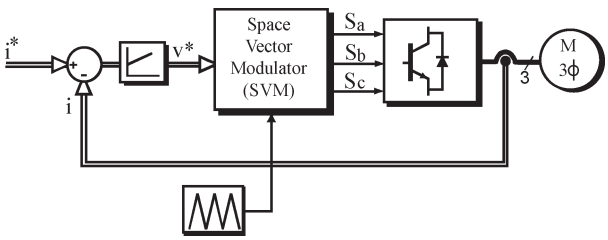


Fig. 9. Linear current control.

$$M = \frac{4}{\pi}\sum_{i=1}^{3}(-1)^{i-1}\cos(\alpha_i) \tag{4}$$

$$0 = \frac{4V_{\rm dc}}{5\pi}\sum_{i=1}^{3}(-1)^{i-1}\cos(5\alpha_i) \tag{5}$$

$$0 = \frac{4V_{\rm dc}}{7\pi}\sum_{i=1}^{3}(-1)^{i-1}\cos(7\alpha_i) \tag{6}$$

where $M$ is the modulation index.

Recent studies of SHE in multilevel inverters are designed to meet harmonic standards [34], [35] and to operate with a high number of levels and a reduced modulation index [36].

*4) Linear Control [33]:* Fig. 8 shows a short overview of control methods used in three-level NPC inverters:

1) linear controller with pulsewidth modulators;
2) direct torque control (DTC);
3) predictive torque control.

The classical linear current control method is shown in Fig. 9. This standard and widely used solution needs to control the fundamental value of the load voltage. For this reason, it needs a carrier-based or SVM modulator [33].

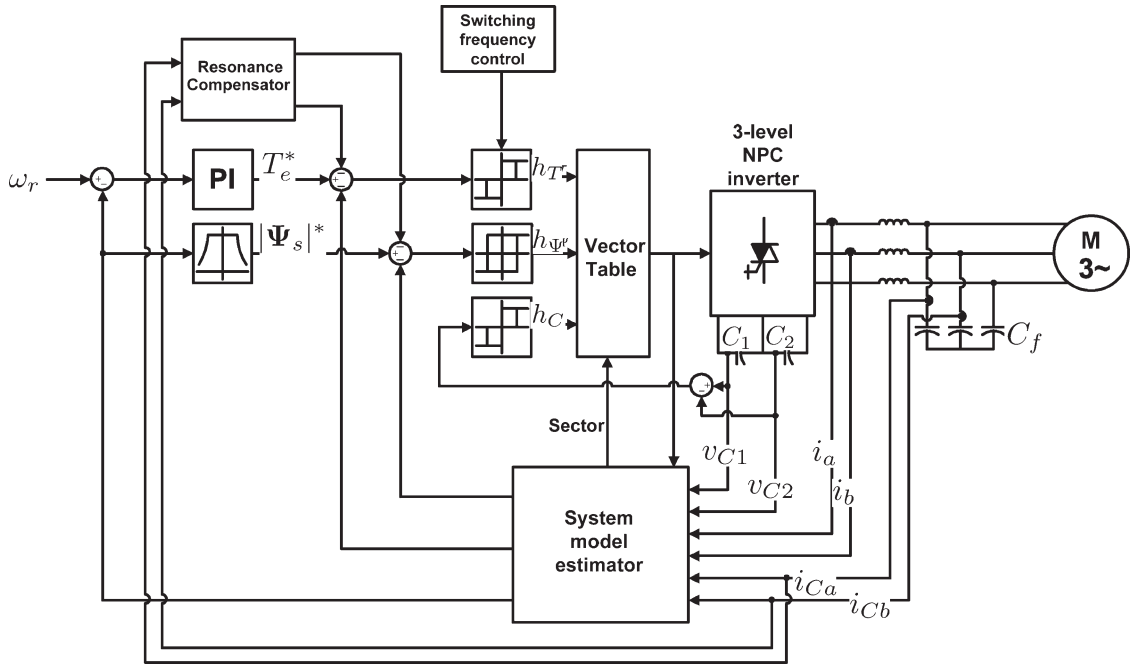


Fig. 10. DTC in a three-level NPC inverter.

*5) DTC [17], [18], [37]:* For high-power drives using three-level NPC inverters, DTC is a well-established technology. This method is based directly on the torque equation of the machine

$$T_e = \frac{3}{2} p \frac{L_m}{L_s L_r - L_m^2} |\psi_s| \cdot |\psi_r| \sin(\theta_{sr}). \tag{7}$$

This method uses a hysteresis controller for the torque and another for the flux, as shown in Fig. 10 [37]. A lookup table directly delivers the gate drive signal for the power semiconductors. A critical issue in high power is the control of the switching frequency. This is important when using DTC because hysteresis controllers operate with variable switching frequency. A constant and reduced switching frequency of no more then 500 Hz is achieved by controlling the width of the hysteresis [37]. A filter is used at the output of the inverter to improve the quality of the voltage.

One recent study compares the reduction of torque ripple when using a three-level NPC inverter instead of a two-level alternative [17]. Another recent work uses the sliding-mode technique to control the torque and flux with three-level NPC inverters [18].

*6) Predictive Control [19], [20], [59], [63]:* In recent years, increasing attention is being paid to the application of predictive control in the field of power electronics and electrical drives [38], [39].

Fig. 11 shows the block diagram of predictive current control in a three-level NPC inverter.

In this method, the inverter is modeled as a system with 27 different switching states, which generates 18 different voltage vectors of the load. Predictive control works according to the following steps.

1) A model of the load is used to predict the behavior of the variable to be controlled for each possible switching state.
2) A cost function is defined, which represents the desired behavior of the system.

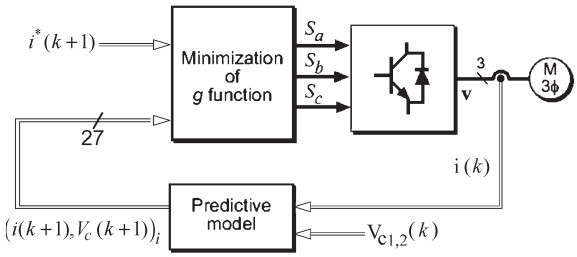


Fig. 11. Predictive current control of a three-level NPC inverter.

3) The switching state that minimizes the cost function is selected and applied to the load in the next sampling interval.

For current control, the cost function to be selected is [20]

$$g = |i_\alpha^* - i_\alpha^p| + \left| i_\beta^* - i_\beta^p \right| \tag{8}$$

where $i_\alpha^*$ and $i_\beta^*$ are the reference currents, and $i_\alpha^p$ and $i_\beta^p$ are the predicted values of the currents.

By changing the cost function to

$$g = |T^* - T^p| + A \cdot |\psi^* - \psi^p| \tag{9}$$

a torque and flux control can be easily achieved. Here, $T^*$ and $\psi^*$ are the reference variables, and $T^p$ and $\psi^p$ are the predicted variables.

A recent work uses predictive control in an NPC AFE with direct power control [19].

Predictive control is a very promising alternative due to the following attractive features.

1) Concepts are very intuitive and easy to understand.
2) It can be applied to a wide variety of systems.
3) The multivariable case can be easily considered.
4) Dead times can be compensated.
5) Easy inclusion of nonlinearities in the model.
6) Simple treatment of constraints.

7) The resulting controller is easy to implement.
8) The methodology is open to include modifications and extensions depending on specific applications.

### C. Balance of Capacitor Voltages [21]–[25], [62]

At the beginning of the NPC topology, there was a very strong critique of the balance in the dc-link capacitor voltages. This subject, the balance of the capacitor voltages, has been one of the most active research topics in high-power electronics. This problem has been solved using the redundancy capability of the NPC inverter.

For example, when using DTC (see Fig. 10), the difference of the capacitor voltages is measured and used to address a different lookup table in order to connect the voltage imbalance [37].

In predictive control, the balance of the capacitor voltages is achieved simply by adding an additional term to the cost function, as shown in the following:

$$g = |i_\alpha^* - i_\alpha^p| + \left|i_\beta^* - i_\beta^p\right| + A \cdot |V_{c1}^p - V_{c2}^p| \tag{10}$$

where $V_{c1}^p$ and $V_{c2}^p$ are the predictive values for the capacitor voltages, and $A$ is a weighting factor that influences the importance of this term [20].

Still today, important research is being done to balance the capacitor voltages using different strategies [21]–[25].

### D. NPC Topologies With Four and Five Levels [26]–[32]

In the last few years, four- and five-level NPC inverters have been studied to increase the power delivered to the load and to improve the quality of the voltage.

So far, these topologies have not found an industrial application; thus, they will be not discussed with more detail.

### E. Advantages of Three-Level NPC Inverters

The three-level NPC VSC (3L-NPC-VSC) has several attractive features which explain its remarkable success on the market. Power electronic building blocks (PEBBs) on the basis of IGCTs and IGBTs and the low part count of power parts enable a modular design with excellent reliability and availability. Common dc bus configurations are available for multidrive and high-power applications. The converter can operate grid-friendly by means of the application of an additional sine filter or higher pulse transformers (12p and higher) for the AFE solution or by 12p, 18p, or 24p diode rectifiers. The simple inclusion of specific options like brake choppers or $dv/dt$—on the machine or transformer side—causes extraordinarily high flexibility. Finally, an excellent dynamic behavior can be achieved through advanced control schemes like vector control or DTC for applications with very high dynamic requirements, i.e., rolling mills.

### F. Disadvantages of Three-Level NPC Inverters

Disadvantages include relatively high switching losses which limit the switching frequency to a couple hundred hertz [41], unsymmetrical semiconductor loss distribution (e.g., [38]–[41]), the necessity of a sine filter for standard machines (e.g., [44]), and the difficult extension of the voltage converter range for use by semiconductors with a higher blocking capability or a series connection of semiconductors (e.g., [42]).

## III. 3L-ANPC-VSC

The main structural drawback of the 3L-NPC-VSC is the unequal loss distribution and the resulting unsymmetrical temperature distribution of the semiconductor junction [38]–[40], [53]–[55]. The most critical operating points which determine the maximum achievable output current of a 3L-NPC-VSC occur at the maximum $(m = 1.155)$ and minimum modulation depths $(m \approx 0)$ at power factors of $pf = 1$ and $pf = -1$. Assuming a conventional three-level SVM, the outer switches $(m = 1.155)$ and the NPC diodes $(m \approx 0)$ experience maximum losses at the inverter operation $(pf = 1)$, whereas the inverse diodes of the outer switches $(m = 1.155)$ and the inner switches $(m \approx 0)$ generate maximum losses at the rectifier operation $(pf = -1)$. At low fundamental frequencies (typically lower than 5 Hz) and modulation indices, a two-level SVM can be applied to achieve an improved junction temperature distribution of the semiconductors of one phase leg. The example in Fig. 12 shows the corresponding junction temperature distribution of one phase leg of a (4.16 kV and 2.1 MVA) 3L-NPC VSC using the state-of-the-art 6.5-kV IGBT modules.

If active switches are placed in both NPC branches, the unequal loss distribution can be substantially improved, and the circuit is called three-level ANPC VSC (3L-ANPC-VSC). Fig. 13 shows the circuit configuration of an IGBT 3L-ANPC-VSC. The topology was first introduced in 2001 [38]. Recent publications investigate the influence of different PWM schemes on the power semiconductor loss distribution [53], [55], [56], the fault tolerance ability of the converter [54], and the application of the three-level ANPC structure in multilevel ANPC VSCs (e.g., four-, five-, and seven-level ANPC VSCs) [57], [58]. Meanwhile, the first high-power MV drives on the basis of the 3L-ANPC-VSC are available in the market (Figs. 20 and 21). The structure and function of the 3L-ANPC-VSC are briefly summarized as follows.

### A. Switching States

Consider a single phase leg of the ANPC VSC. In contrast to the conventional NPC converter, there is more than one switching state to connect the ac terminal to the midpoint (neutral point) of the dc link. By turning on $T_{x5}$ and $T_{x2}$, the phase current can be conducted through the upper path of the neutral tap in both directions. In the same manner, by turning on $T_{x6}$ and $T_{x3}$, the phase current can be conducted through the lower path of the neutral tap in both directions. While the upper NPC path is being used ($T_{x6}$ and $T_{x3}$ are in the OFF state), $T_{x4}$ may be in the ON or OFF state. The same applies to $T_{x1}$ during the conduction of the lower NPC path. The resulting four zero states are designated as "0L2," "0L1," "0U1," and "0U2" (Table II). In the "+" state, the switch $T_{x6}$ is turned on to guarantee equal voltage sharing between $T_{x3}$ and $T_{x4}$. In turn,

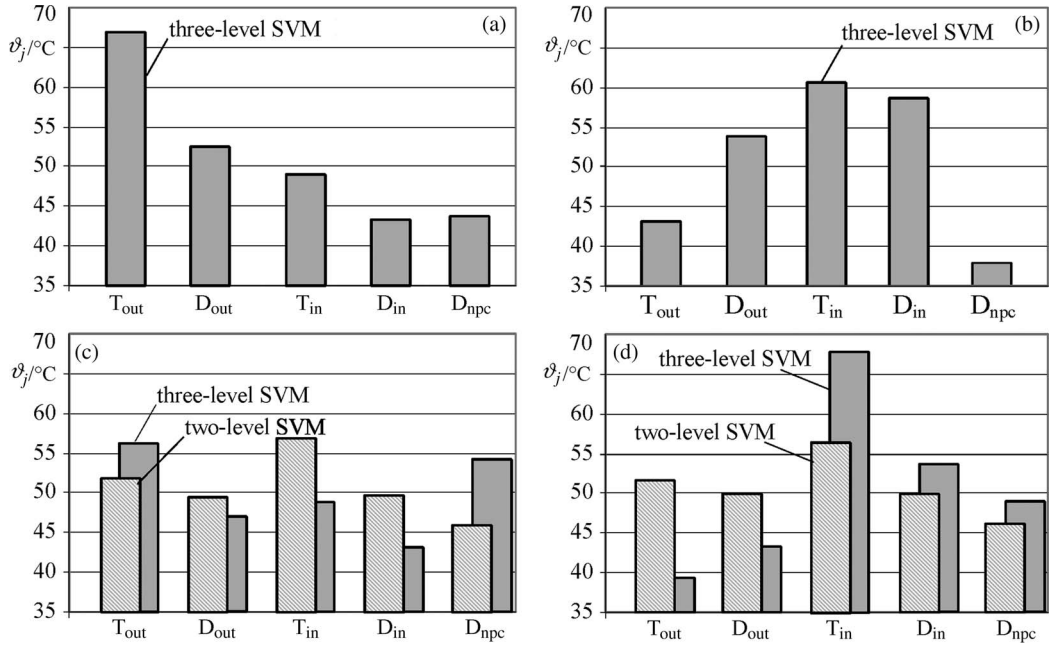


Fig. 12. Simulated average junction temperatures of a (4.16-kV and 2.1-MVA) 3L-NPC-VSC ($V_{\mathrm{DC},n} = 6.118$ kV, $i_{\mathrm{ph,rms}} = 290$ A, $f_c = 450$ Hz, $f_1 = 50$ Hz, $\vartheta_a = 37$ °C, SVM, and IGBT modules: Eupec FZ600R65KF1). (a) $m = 1.15$; $pf = 1$. (b) $m = 1.15$; $pf = -1$. (c) $m = 0.05$, $pf = 1$. (d) $m = 0.05$; $pf = -1$.

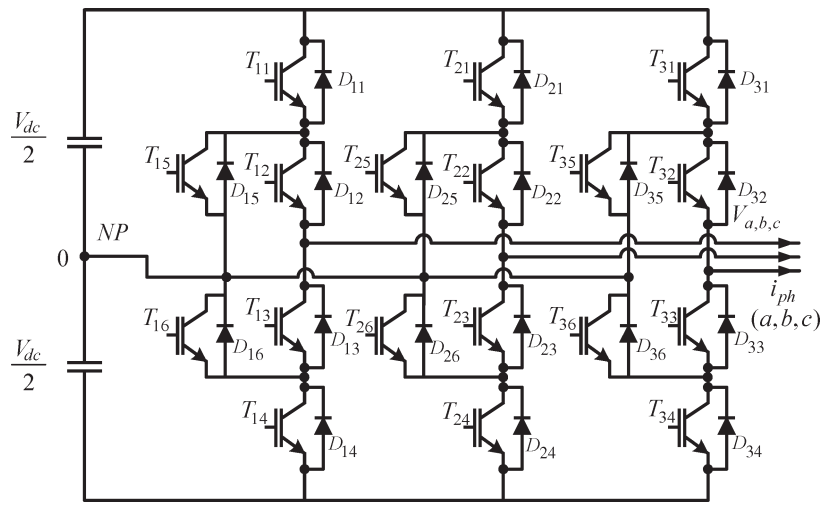


Fig. 13. 3L-NPC-VSC with ANPC switches—ANPC VSC.

TABLE II
SWITCHING STATES OF THE 3L-ANPC-VSC

| | $T_{x1}$ | $T_{x2}$ | $T_{x3}$ | $T_{x4}$ | $T_{x5}$ | $T_{x6}$ |
|---|---|---|---|---|---|---|
| State "+" | 1 | 1 | 0 | 0 | 0 | 1 |
| State "0U2" | 0 | 1 | 0 | 0 | 1 | 0 |
| State "0U1" | 0 | 1 | 0 | 1 | 1 | 0 |
| State "0L1" | 1 | 0 | 1 | 0 | 0 | 1 |
| State "0L2" | 0 | 0 | 1 | 0 | 0 | 1 |
| State "–" | 0 | 0 | 1 | 1 | 1 | 0 |

$T_{x5}$ is turned on in the "−" state to assure equal voltage sharing between $T_{x1}$ and $T_{x2}$. Thus, the static balancing resistors across the switches can be saved [38].

Obviously, the distribution of conduction losses during the zero states can be controlled by the selection of the upper or lower NPC path. The conduction losses in the states "+" and "−" cannot be influenced.

### B. Commutations

The commutations to or from the zero states determine the distribution of the switching losses. All commutations take place between one active switch and one diode. Even if more than two devices turn on or off, only one active switch and one diode experience essential switching losses.

For the following discussion, an operating condition with a positive phase current and a positive output voltage is assumed as an example. For a better comparison, the **conventional commutation $+ \rightarrow 0$** without the use of the ANPC switches is recapitulated first [Fig. 14(a)]. The converter phase leg is switched from the positive dc rail "+" to the neutral tap "0." $T_{x1}$ is turned off, and $T_{x3}$ is turned on after a dead time. The current commutates from $T_{x1}$ to $D_{x5}$. The switches $T_{x2}$ and $T_{x4}$ stay on and off, respectively. Essential turnoff losses occur in $T_{x1}$. During the opposite commutation $0 \rightarrow +$, all switching

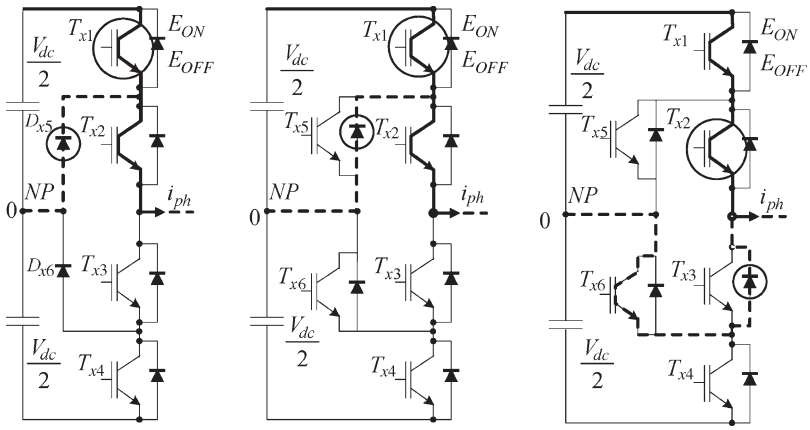


Fig. 14. Commutations in the 3L-NPC-VSC and ANPC VSC for $i_{\rm ph} > 0$ and $v_{\rm ph} > 0$. (a) Conventional NPC commutation $(+ \leftrightarrow 0)$. (b) Type-1 commutation in ANPC VSC $(+ \leftrightarrow 0\text{U}2)$. (c) Type-3 commutation in ANPC VSC $(+ \leftrightarrow 0\text{L}1)$.

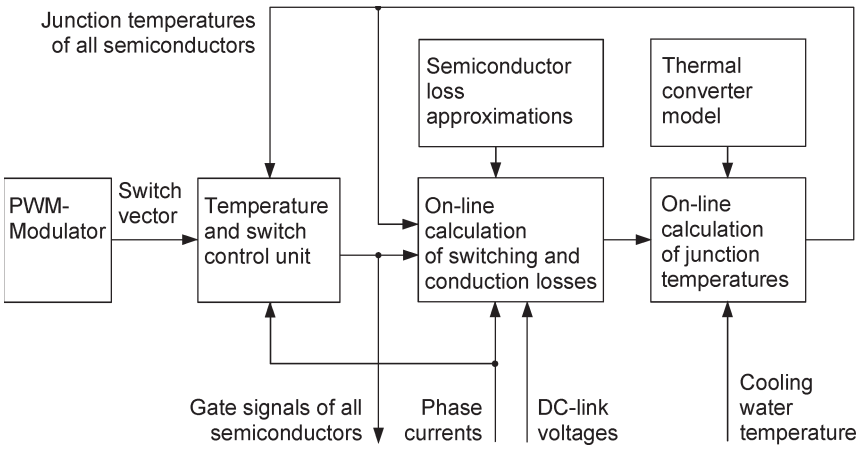


Fig. 15. Block diagram of the loss-balancing system.

transitions take place in the reverse order. The outer switch $T_{x1}$ and the NPC diode $D_{x5}$ experience turn-on and recovery losses, respectively.

The two major commutations from "+" to the zero states in the ANPC VSC are described subsequently. During the $\mathbf{commutation + \rightarrow 0U2}$, the phase current commutates to the upper path of the neutral tap [Fig. 14(b)]. First, $T_{x6}$ has to be turned off. Then, $T_{x1}$ is turned off, and finally, $T_{x5}$ is turned on after a dead time. For the chosen condition $i_{\rm ph} > 0$, this commutation behaves like the conventional commutation in the NPC VSC. $T_{x1}$ experiences turnoff losses, and during the reverse commutation, $0\text{U}2 \rightarrow +T_{x1}$ and $D_{x5}$ experience the corresponding turn-on and recovery losses. By the $\mathbf{commutation + \rightarrow 0L1}$, the phase current is forced to the lower path of the neutral tap [Fig. 14(c)]. In contrast to the previous case, $T_{x1}$ remains in the ON state. $T_{x2}$ is turned off, and $T_{x3}$ is turned on after a dead time. Thus, the inner switch $T_{x2}$ experiences turnoff losses. The turn-on and recovery losses during the reverse commutation $0\text{L}1 \rightarrow +$ occur in the inner switch $T_{x2}$ and the inner diode $D_{x3}$, respectively.

According to [39], the two commutations $+ \leftrightarrow 0\text{U}2$ and $+ \leftrightarrow 0\text{L}1$ are designated as types 1 and 3, respectively. Type-1 commutations always take place between one outer switch or diode and one NPC switch or diode, e.g., between $T_{x1}$ and $D_{x5}$ for $i_{\rm ph} > 0$ and $\nu_{\rm ph} > 0$. Their switching losses can be shifted to the inner devices applying the type-3 commutation. In the example, the losses of $T_{x1}$ and $D_{x5}$ are shifted to $T_{x2}$ and $D_{x3}$. Analogously, this mechanism applies to all operating conditions. It can be used to distribute the switching losses among the semiconductors. Another commutation introduced in [2] as type 2 takes place between one outer and one inner device. With respect to the loss shifting, it can be seen as an intermediate stage between the type-1 and type-3 commutations. Therefore, it is not absolutely necessary and skipped here for the sake of simplicity.

## IV. Loss-Balancing Control

A feedback-controlled loss-balancing system was introduced to balance the switching losses within the 3L-ANPC-VSC (Fig. 15).

The loss-balancing system is inserted after the conventional PWM modulator for the 3L-NPC-VSC. It consists of two functional units: the online calculation of losses and junction temperatures, and the generation of gate signals for the 18 switches. Based on the estimated instantaneous junction temperatures and sampled phase currents, the "temperature and switch control unit" selects the most suitable commutations and zero states for the coming sampling period. The algorithm ensures that the semiconductor with the highest estimated junction temperature

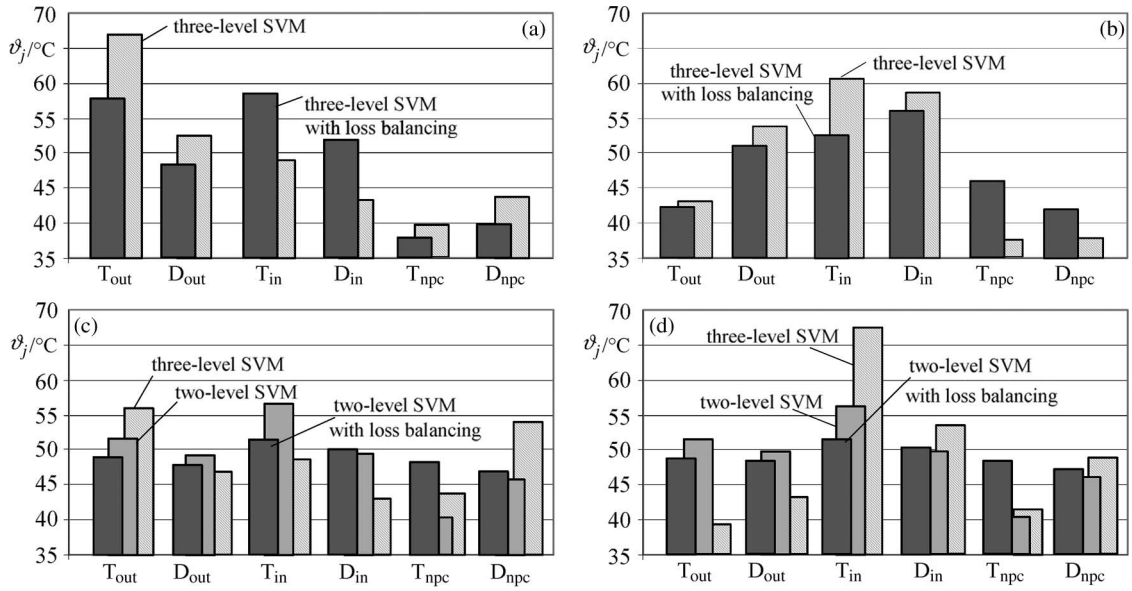


Fig. 16. Simulated average junction temperatures of a (4.16-kV and 2.1-MVA) 3L-ANPC VSC with and without loss balancing ($V_{\mathrm{DC},n} = 6.118$ kV, $i_{\mathrm{ph,rms}} = 290$ A, $f_c = 450$ Hz, $f_1 = 50$ Hz, $\vartheta_a = 37$ °C, SVM, and IGBT modules: Eupec FZ600R65KF1). (a) $m = 1.15; pf = 1$. (b) $m = 1.15; pf = -1$. (c) $m = 0.05; pf = 1$. (d) $m = 0.05; pf = -1$.

is not stressed with significant switching losses during the next commutation. Therefore, a distinctly improved loss and junction temperature distribution is achieved.

Assuming the aforementioned (4.16 kV and 2.1 MVA) 3L-(A)NPC-VSC, Fig. 16 shows that a proper selection of the commutations by a closed-loop junction temperature balancing scheme enables a distinctly more uniform junction temperature distribution. The more equal semiconductor junction temperature distribution enables an increase of the converter output current and power or, alternatively, an increase of the switching frequency. The possible increase of converter power and/or the switching frequency strongly depends on the applied power semiconductor, the loss distribution, and the cooling conditions. It is important to note that the loss-balancing scheme becomes more effective at increasing switching frequencies. As an example, the converter power can be increased by 15% (from $S_C = 2.8$ MVA to $S_C = 3.22$ MVA) for a device switching frequency of $f_s = 150$ Hz and by 52% (from $S_C = 1.2$ MVA to $S_C = 1.82$ MVA) at a device switching frequency of $f_s = 525$ Hz for the 4.16-kV 3L-NPC-VSC being considered [41].

Alternative to the feedback-controlled system reference, Brückner *et al.* [40] propose a lookup-table-based loss-balancing method which allows for a substantially simplified implementation of the loss-balancing system.

## V. Applications

An overview of the available pulsewidth-modulated industrial MV drives in the market is shown in Table III.

The majority of manufacturers offer VSCs with a different number of output voltage levels. Aside from the well-known two-level VSC, there are 3L-NPC-VSCs [46], [47], four-level FLC VSCs [48], [49], multilevel series-connected H-bridge (SCHB) VSCs (e.g., five-level SCHB VSCs, seven-level SCHB VSCs, and nine-level SCHB VSCs) [50], [51], and five-level NPC H-Bridge VSCs. Even if one manufacturer (Allen Bradley) offers PWM current source inverters on the basis of symmetrical IGCTs, the VSC is the preferred topology in the market.

Fig. 17 shows the power circuit of a nonregenerative inverter for general purpose drives, based on IGCT semiconductor, which covers the range 0.3 to 5 MVA. A 12-pulse diode rectifier is used at the input to reduce input current harmonics. Versions with 18 and 24 pulse rectifiers are also used in the market. This solution is used in general applications like ventilators and pumps.

Fig. 18 shows the power circuit of a regenerative NPC inverter, which allows for power regeneration from the machine. This is achieved by including an NPC active front rectifier. This topology is used in a range of 3 to 27 MVA. Typical applications are roll mills, laminators, and downhill conveyors. With the development of very high power windmills of up to 5 MW, NPC inverters can also be used in this application, as shown in Fig. 19 [58].

## VI. PCS8000 Converter for Pump Storage Applications

Based on the ANPC converter technology, a new ANPC PEBB has been developed (see Fig. 20). It comprises two phase legs and is suitable for use in an H-bridge configuration. This new PEBB also features new IGCT semiconductor devices with increased turnoff capability and a $du/dt$ snubber network for further increase of turnoff capability and reduction of switching losses. The ANPC PEBB is integrated into the PCS8000 Power Module with ratings as follows.

1) Output voltage: $Un = 3600$ VACrms.
2) Output current: $In = 2600$ AACrms.
3) DC current capability: $Idc = 2750$ A dc.

TABLE III
MARKET OVERVIEW OF INDUSTRIAL MV PWM DRIVES

| Manufacturer | Type | Power | Voltage(kV) | Topology | Semiconductor | Control |
|---|---|---|---|---|---|---|
| ABB | ACS 1000 | 0.3 – 5 MVA | 2.3; 3.3; 4.0; 4.16 | 3L-NPC-VSC | IGCT | Direct Torque Control |
| | ACS 5000 | 1.7 – 24 MVA | (4.16); 6.0; 6.6; 6.9 | 5L-NPC-HB-VSC | IGCT | Direct Torque Control |
| | ACS 6000 | 3 – 27 MVA | (2.3); 3; 3.3 | 3L-NPC-VSC | IGCT | Direct Torque Control |
| Allen Bradley | Power Flex 7000 | 0.15 – 6.7 (22.5) MVA | 2.4; 3.3; 4.16; 6.6 | PWM-CSI | SGCT | Vector Control |
| Converteam | VDM5000 | 1.4 – 7.2 MVA | 2.3; 3.3; 4.2 | 2L-VSC | MV IGBT | Vector Control |
| | VDM6000 | 0.3 – 8 MVA | 2.3; 3.3; 4.2 | 4L-FLC-VSC | MV IGBT | Vector Control |
| | VDM7000 | 7 – 9.5 MVA 6/8 MVA | 3.3 | 3L-NPC-VSC | GTO PP-MV IGBT | Vector Control |
| Siemens | Perfect Harmony | 0.3 - 30 MVA | 2.3 - 13.8 | ML-SCHB-VSC | LV (MV) IGBT | Vector Control |
| | Sinamics GM150 | 0.6 - 10.1 MVA | 2.3; 3.3; 4.16; 6; 6.6 | 3L-NPC-VSC | MV IGBT | Vector Control |
| | Sinamics SM150 | 5 - 28 MVA | 3.3 | 3L-NPC-VSC | IGCT | Vector Control |

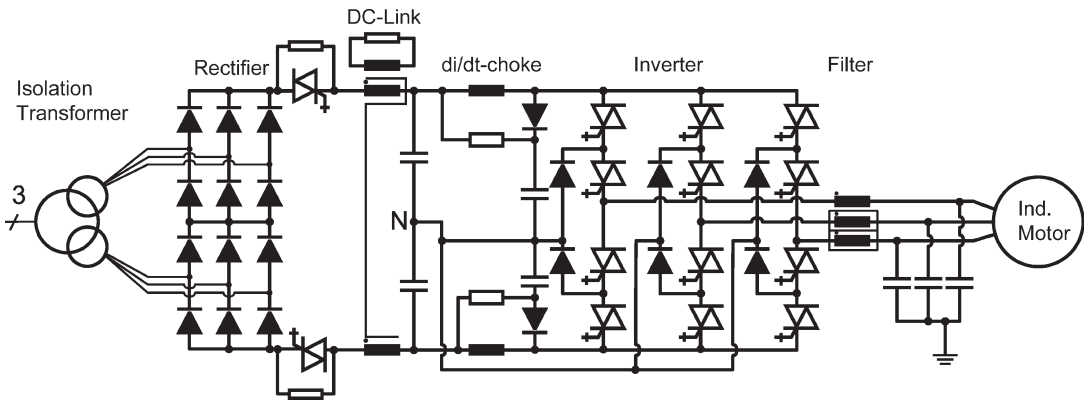


Fig. 17. Nonregenerative NPC inverter.

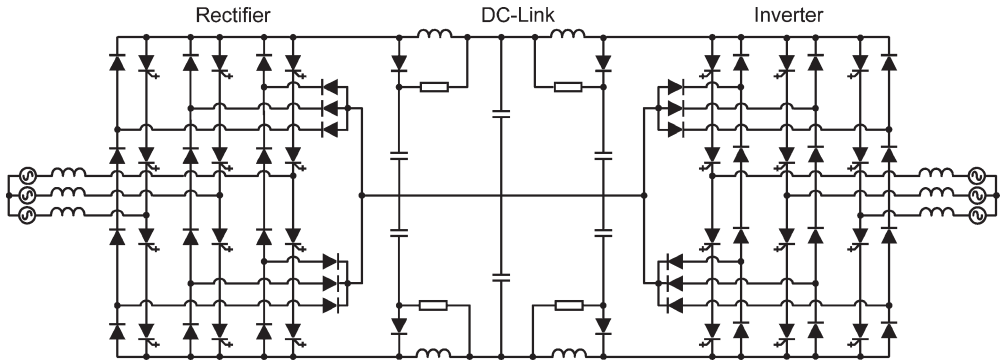


Fig. 18. Regenerative NPC inverter.

A key application of the new ANPC IGCT PEBB is in pump storage power plants. In systems with Francis turbines, Varspeed systems are increasingly being used to achieve the maximum efficiency throughout the operating range. Induction machines with wound rotors (doubly fed induction generator) are used instead of synchronous machines. To control the speed,

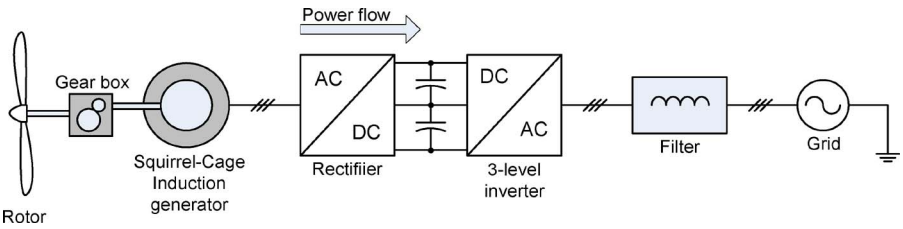


Fig. 19. Three-level inverter in wind generation.

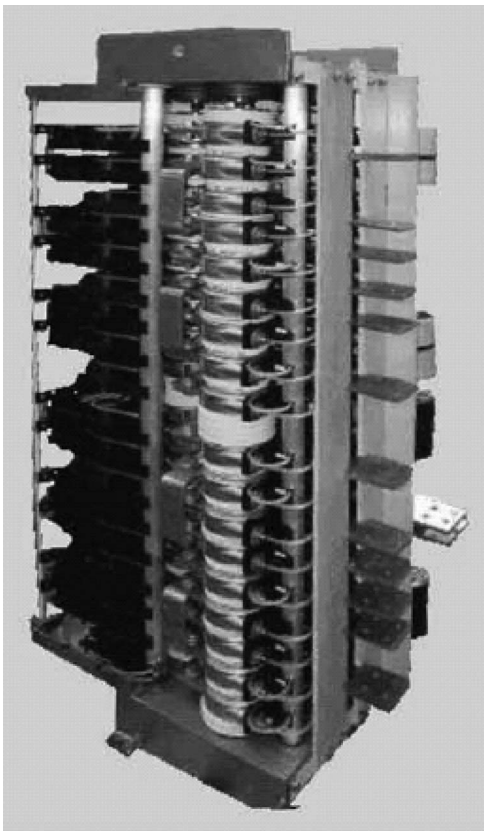

Fig. 20. (Two phase legs in one mechanical assembly) 16-MVA ANPC IGCT PEBB.

large power converters operating at very low fundamental frequencies (5 Hz down to 0 Hz) are needed. Fig. 21 shows an example of a PCS8000 static frequency converter for such an application, comprising two ANPC IGCT PEBBs in the rectifier section (on the left) and three similar PEBBs in the inverter section (on the right). A very low inductance laminated dc bus bar connects the power modules in the back. This connects the power modules to the intermediate dc-link capacitor bank at the rear bottom of the converter frame. Due to its loss-balancing scheme for low-speed operation, the ANPC topology is clearly superior to the conventional NPC topology, as derating for the low-frequency operation can be avoided.

## VII. Comments and Conclusion

It can be considered that the NPC inverter is a completely mature topology today, very well established in high-power applications.

The problem of balance in the capacitor voltages, originally considered as a drawback of this topology, is definitely solved using redundant states.

Fig. 21. PCS8000 converter module based on the ANPC IGCT PEBB.

Classical pulsewidth modulation, SVM, and SHE have been the preferred modulation techniques for operation with low switching frequency, as demanded by this topology. Hysteresis control (with limited switching frequency) is also highly used.

Passive NPC has unequal loss distribution among the semiconductors; this problem is solved using the ANPC.

For the control, DTC and field-oriented control are the standard solutions for speed control. For future development, predictive control appears as a very promising alternative due to its simplicity and very high performance.

The field of application of NPC inverters is permanently growing due to their compactness, efficiency, and good performance.

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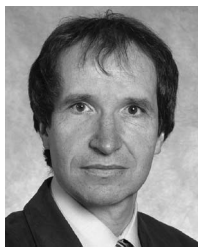

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