Comparison of Two-Level and Three-Level NPC Inverter Topologies for a PMSM Drive for Electric Vehicle Applications

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***Abstract*— Multidimensional comparison of two-level and three-level DC/AC converters for a 120 kW permanent magnet synchronous machine (PMSM) drive is carried out in this study. Comparison of two topologies with Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) by means of output current THD, conduction and switching losses, thermal stresses on semiconductors and switching frequency limitation are investigated at various operating points. Electro-thermal simulation of both topologies are achieved using PLECS tool with Silicon IGBT and diode pairs from SEMIKRON. Results of these analysis show the limitations of two-level inverter topology in terms of the switching frequency and point out the advantage of three-level inverter in high speed PMSM drives.**

Keywords—electric vehicle, motor drive, PMSM, three-level inverter, two-level inverter

I. INTRODUCTION

Permanent Magnet Synchronous Machines (PMSMs) are commonly used in vehicle traction applications and there are numerous studies focusing on increasing the performance and reliability of their drive systems. It is evident that the trend in electric machine design is to increase the rotational speed aiming a higher torque and power density of the drive system. As fundamental frequency of the drive system increases, operation at higher switching frequencies and if possible at higher DC bus voltage levels are required to assure a low output voltage and current THD as well as a good dynamic control performance.

Two-level voltage source inverter (VSI) is the commercial converter type used in PMSM drives. As semiconductor switches, conventional Si IGBT and diode pairs are used for driving PMSMs in traction applications. However, in recent years, SiC MOSFETs and SiC diodes have been involved in the motor drive market to account for the need in higher switching frequency modulation [1]. As stated in [2], switching frequency should be at least 9-12 times of the maximum fundamental frequency. However, conventional Si IGBT diode pairs suffer from high switching losses in two-level VSI topology. SiC MOSFET and Si based IGBT diode pair comparison is done for an 80 kW electric motor PMSM drive in [1]. Usage of SiC MOSFETs instead of Si IGBT results in 5% range extension for the electric car. SiC Mosfets are now preferable with two-level topology due to low switching losses of semiconductors and high switching frequency requirement of PMSM in maximum speed operation.

Three-level topology is expected to be advantageous at higher switching frequency operations with conventional Si IGBT diode pairs due to lower switching losses. The reasons are as follows: First, blocking voltage requirement of the main switch is halved in three-level topology. Second, switching losses do not linearly change with blocking voltage, for example an exponent of 1.3-1.4 is used to account for the effects of the blocking voltage in [3]. That means switching losses per switch are expected to drop below 50% in a 3-level topology, giving us the opportunity to increase the switching frequency.

In the literature, advantages of three-level inverters over two-level inverters are discussed for PMSM drive applications. Three-level and two-level topologies are compared in terms of output voltage THD, efficiency, and fault tolerance in [4]. In all aspects, three-level topology has a superior performance. Similarly, three-level NPC topology is shown to be more compatible with PMSM drives for traction applications in terms of current THD, torque ripple, and switching losses aspects in [5]. Besides, according to the comparative cost analysis of two-level and three-level topologies presented in [2], three-level NPC type topology has a slightly higher initial cost but a lower operational cost due to its higher efficiency. Although superior performance stated in the literature, higher number of switches and floating capacitor voltage are main design challenges of the three-level NPC topology. To address the floating capacitor voltage issue, various balancing techniques are presented in [6-8].

Considering the increase in DC bus voltage levels, topology selection is also getting as important as switch selection. Commercially available semiconductor switches have discrete steps of blocking voltage levels. In DC bus voltage levels around 700-900 V, switches with 1200 V voltage blocking capability are required in 2-level VSIs. At this point, semiconductor technologies with lower switching losses are the choice of developers. On the other hand, a multi-level VSI may provide a solution with conventional semiconductor switches thanks to the lower turn-on and turn-off energies compared to 2-level topologies. This study aims to explore the operating limits of a 3-level NPC VSI by investigating its output characteristics and thermal limits at various switching frequencies.

A multidimensional comparison of two-level and three-level inverter topologies for a 120 kW PMSM drive is made in this paper. Comparison of these topologies with two major switching techniques namely Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are conducted using SEMIKRON conventional Si IGBT diode pairs. DC Bus voltage of the motor drive is selected as 850 V. Therefore; 650 V IGBT diode pair is used in three-level topology while1200 V IGBT is selected for two-level topology. In order to make a

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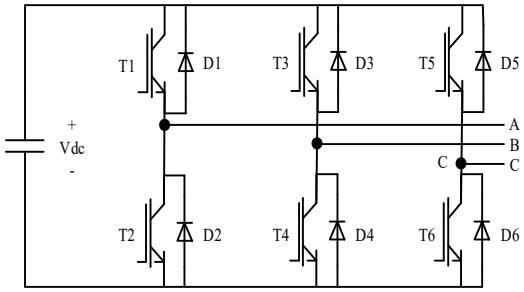

Fig. 1. Two-level topology

reasonable comparison, same heatsinks are assumed in both topologies.

The following four cases are analyzed; two-level topology with SPWM, two-level topology with SVPWM, three-level NPC topology with SPWM, and three-level topology with SVPWM. Comparisons are done in terms of output voltage and current quality, junction temperatures, and switching frequency limitation aspects. First of all, quality of the output voltage and current waveforms are compared at 30% of rated torque and at various rotational speeds. These operation points are selected to account for a daily drive cycle. This is followed by thermal analysis in Plexim/PLECS simulation platform performed at rated torque and rated speed to investigate thermal behavior of the inverter at full load. Junction temperatures of each semiconductor device are calculated and switching frequency limits of each case are explored by limiting the maximum thermal junction temperature of semiconductors to 130°C.

II. TOPOLOGIES AND SWITCHING TECHNIQUES

Two-level three phase topology consists of six switches as shown in Fig. 1. T1 and T2, T3 and T4, T5 and T6 work complementarily in order to avoid cross-conduction. Three-level NPC topology has four main switches and two clamping diodes in each leg as shown in Fig. 2. T1 and T3, T2 and T4 work complementarily. In the other inverter legs, corresponding main switches work complementarily as well. Bi-directional main switches should be used in both topologies. MOSFET, SiC MOSFET, GaNFET, IGBT-Diode pairs could be used as the main switch depending on the current, blocking voltage and switching frequency requirements. For the selected power level, conventional IGBT-Diode pairs are widely used in industry. Therefore; IGBT-Diode pairs from SEMIKRON are selected for the analysis in this paper and the two IGBT-Diode modules used in each topology are given in Table I.

A. Two-Level Inverter with SPWM

In SPWM applied for two-level three phase inverter, three reference sine waves with 120°deg phase shifts wrt. each other are used as reference signals for each leg. By comparing reference sine waves with carrier triangle waveforms, gate signals are obtained for upper and lower switches. Exemplary carrier signal, three reference signals and node voltages with respect to DC bus ground of each leg are shown in Fig. 3.

B. Two-Level Inverter with SVPWM

SVPWM technique is widely used in many inverter applications. The main advantage of SVPWM is the degree of freedom of selecting voltage vectors in a switching period compared with SPWM method. SVPWM also provides a better DC bus voltage utilization than SPWM. For a two-level

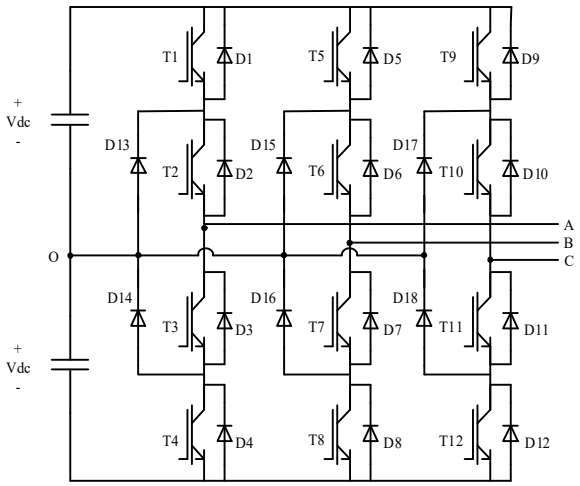

Fig. 2. Three-level NPC topology

TABLE I. SELECTED MODULES

Topology	IGBT and Diode Module	VCE(max)(V)	Ic(A)
Two-level	SKiiP39GB12E4V1 HPTP	1200	388
Three-level NPC	SkiM401MLI07E4	650	317

inverter topology, 61.2% DC bus utilization can be achieved with SPWM and 70.7% with SVPWM. However; SVPWM technique needs higher computational power due to its nature. In recent years, microcontrollers and DSPs allow designers to implement SVPWM algorithms easily.

SVPWM technique is based on the selection of optimum voltage vectors in each switching period. In order to achieve this, three phase reference vectors are transformed to α-β axis (Clarke's transformation) and a rotating reference vector is formed as a combination of $2^3 = 8$ voltage vectors, from which two are zero vectors that are 000 and 111 vectors. In each switching cycle, components of the reference vector and dwell times are calculated by software.

Switch logic signals for corresponding space vectors are given in Table II. Space vectors of two-level topology and defined sectors are shown in Fig. 4 and Table III, respectively. Each region corresponds to a 60°deg rotation of reference vector V_r as shown in Fig. 4.

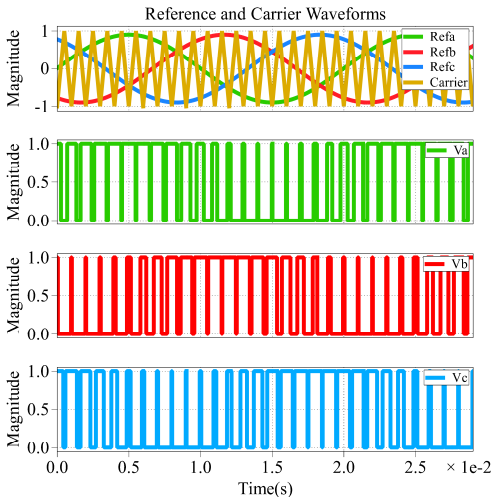

Fig.3. Reference and carrier waveforms of two-level SPWM.

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TABLE II. SWITCH LOGIC FOR CORRESPONDING SPACE VECTORS

		UPPER SWITCHES			LOWER SWITCHES		
Vectors		T1	T3	T5	T2	T4	T6
U0	000	1	1	1	0	0	0
U1	100	0	1	1	1	0	0
U2	110	0	0	1	1	1	0
U3	010	1	0	1	0	1	0
U4	011	1	0	0	0	1	1
U5	001	1	1	0	0	0	1
U6	101	0	1	0	1	0	1
U7	111	0	0	0	1	1	1

Clark's transformation is done as follows:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

Then reference vector V_r is defined as:

$$\overrightarrow{V_r} = V_\alpha + jV_\beta \quad (2)$$

In SVPWM algorithm, amplitude and phase of the reference vector V_r are required. These quantities are determined as follows:

$$\alpha = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \text{ and } |\overrightarrow{V_r}| = \sqrt{V_\alpha^2 + V_\beta^2} \quad (3)$$

After determining the magnitude and the phase of V_r, the space vectors and their on-times must be calculated. In order to calculate on-times for each main vector, volt-seconds law is applied. On-time calculation of vectors in sector 1 can be done as follows:

$$\int_0^{T_s} \overrightarrow{V_r} = \int_0^{T_1} \overrightarrow{V_1} dt + \int_0^{T_2} \overrightarrow{V_2}\, dt + \int_0^{T_0} \overrightarrow{V_0} dt \quad (4)$$

$$\overrightarrow{V_r} = |V_r|\, e^{j\alpha},\ \overrightarrow{V_0} = 0,\ \overrightarrow{V_1} = \frac{2}{3}V_{dc},\ \overrightarrow{V_2} = \frac{2}{3}V_{dc}e^{\frac{j\pi}{3}},\ \overrightarrow{V_7} = 0 \quad (5)$$

$$m_a = \frac{3V_r}{2V_{dc}} \quad (6)$$

TABLE III. SECTOR AND POSITION OF REFERENCE VECTOR

Sector	Position of $\overrightarrow{V_r}$
1	$0^o<\omega t<60^o$
2	$60^o<\omega t<120^o$
3	$120^o<\omega t<180^o$
4	$180^o<\omega t<240^o$
5	$240^o<\omega t<300^o$
6	$300^o<\omega t<360^o$

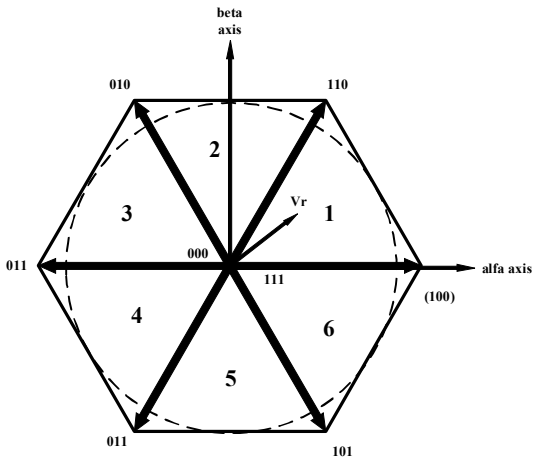

Fig. 4. Two-level space vectors

TABLE IV. ON-TIME OF SEMICONDUCTORS IN EACH REGION

R	T_1	T_2	T_0
1	$T_s m_a(\sin(\frac{\pi}{3}-\alpha)$	$T_s m_a \sin(\alpha)$	$T_0 = T_s - T_1 - T_2$
2	$T_s m_a \sin(\frac{2\pi}{3}-\alpha)$	$T_s m_a(\alpha-\frac{\pi}{3})$	$T_0 = T_s - T_1 - T_2$
3	$T_s m_a \sin(\pi-\alpha)$	$T_s m_a \sin(\alpha-\frac{2\pi}{3})$	$T_0 = T_s - T_1 - T_2$
4	$T_s m_a \sin(\frac{4\pi}{3}-\alpha)$	$T_s m_a \sin(\alpha-\pi)$	$T_0 = T_s - T_1 - T_2$
5	$T_s m_a \sin(\frac{5\pi}{3}-\alpha)$	$T_s m_a \sin(\alpha-\frac{4\pi}{3})$	$T_0 = T_s - T_1 - T_2$
6	$T_s m_a \sin(2\pi-\alpha)$	$T_s m_a \sin(\alpha-\frac{5\pi}{3})$	$T_0 = T_s - T_1 - T_2$

From (5) and (6), on-time calculations of space vectors in each sector are derived as in Table IV. T_1 is the on-time of the first main space vector $\overrightarrow{V_1}$ in the active state, T_2 is the on-time of the second main space vector $\overrightarrow{V_2}$. T_0 time is shared equally among two zero vectors $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$.

C. Three-Level NPC Topology with SPWM

In three-level NPC type three phase inverter topology, SPWM is applied with two different carrier waveforms separated with a DC offset from each other. Carrier waveforms and reference waveforms are shown in Fig. 5. carrier1 is used for the top switches of the upper side of each leg that are T_1, T_5, and T_9 and carrier2 is for bottom switches of the upper side that are T_2, T_6, and T_{10}. Similar to a two level topology, Phase B and Phase C legs have shifted reference sine waves by 120°deg wrt. each other. The lower side switches in each leg works complementarily with top side corresponding switch. Switch logic signals, reference and carrier waveforms are shown in Fig. 6.

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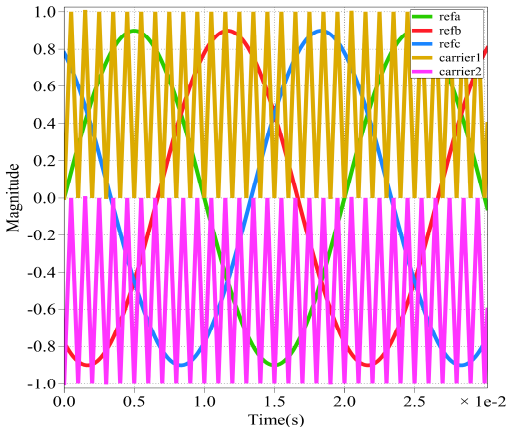

Fig. 5. Three-level SPWM three-phase references and carriers

D. *Three-Level NPC Topology with SVPWM*

In three level topology, there are in total of 3^3=27 voltage vectors. 24 of them are active vectors, from which 12 are short vectors, 6 are medium vectors and 6 are long vectors. Other 3 vectors are zero vectors located in the center. In three level inverter, six main sectors are the same as in two-level case and each sector consists of four sub-sectors. Fig. 7 and 8 show space vectors and four sub-sectors in the first main sector, respectively. Due to the additional degree of freedom, there are various modulation strategies to manage space vectors to generate PWM signals. In this study, symmetrical SVPWM method that is commonly used to achieve low current THD at the output is used [9].

$V_{dc\text{-}cap}$ is defined as the voltage of one of the floating capacitors as can be seen in Fig. 2. The capacitor voltages are assumed to be equal in this study that is $V_{dc\text{-}cap}= V_{dc}/2$. Each connection point can attain three different voltage levels in a 3-level VSI; P represents $V_{dc\text{-}cap}$, O represents zero potential and N represents $-V_{dc\text{-}cap}$ at the switching node of a phase leg as listed in Table V. Small vectors (POO, ONN, etc.) have magnitude of $2V_{dc\text{-}cap}/3$. Medium vectors (PON, OPN, etc.) have magnitude of $2\sqrt{3}\ V_{dc\text{-}cap}/3$. Large vectors (PNN, PPN, etc..) have magnitude of $4V_{dc\text{-}cap}/3$.

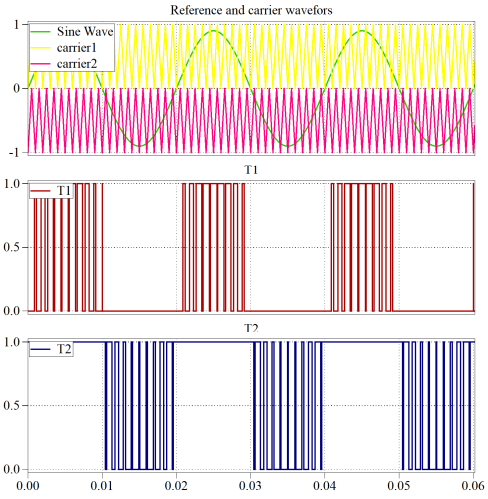

Fig. 6. Three-level SPWM phase A switching signals

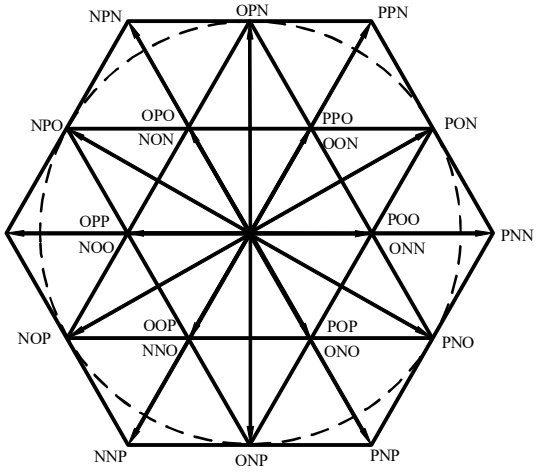

Fig. 7. Three-level space vectors

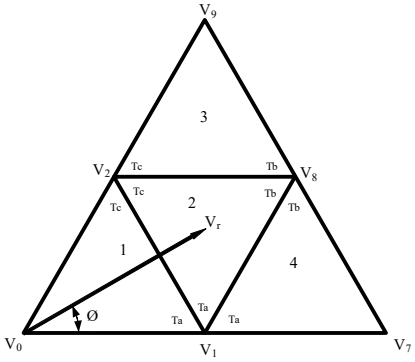

Fig. 8. Sub-sectors in three-level SVPWM

TABLE V. SYMBOLS AND CORRESPONDING SWITCH STATES & PHASE VOLTAGES

Symbol	T1	T2	T3	T4	Voltage
P	1	1	0	0	V_{dc}
O	0	1	1	0	0
N	0	0	1	1	$-V_{dcs}$

Main sector detection is done the same way as in two-level inverter. Sub–sector detection is done with the angle and magnitude of V_r vector. One example of on-time calculation in main sector 1 and sub-sector 1 is as follows:

$$\vec{V_1}T_a + \vec{V_2}T_c = \vec{V_r}T_s \tag{7}$$

$$\frac{2V_{dc}}{3}e^{j0}T_a + \frac{2V_{dc}}{3}e^{\frac{j\pi}{3}}T_c = |\vec{V_r}|T_s \tag{8}$$

k is defined as follows:

$$k = \frac{\sqrt{3}}{2}\left(\frac{|\vec{V_r}|}{V_{dc-cap}}\right) \tag{9}$$

Where,

$$V_\alpha = V_{aref} - 0.5V_{bref} - 0.5V_{cref} \tag{10}$$

$$V_\beta = (V_{bref} - V_{cref})\left(\frac{\sqrt{3}}{2}\right) \tag{11}$$

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TABLE VI. CALCULATED TIMES AND SUB-SECTORS

T / S	T_a	T_b	T_c
1	$2k\sin(\frac{\pi}{3}-Ø)$	$T_s-2k\sin(\frac{\pi}{3}+Ø)$	$2k\sin(Ø)$
2	$T_s-2k\sin(Ø)$	$2k\sin\left(\frac{\pi}{3}+Ø\right)-T_s$	$T_s-2k\sin(\frac{\pi}{3}-Ø)$
3	$2k\sin(Ø)-T_s$	$2k\sin(\frac{\pi}{3}-Ø)$	$2T_s-2k\sin(\frac{\pi}{3}+Ø)$
4	$2T_s-2k\sin(\frac{\pi}{3}+Ø)$	$2k\sin(Ø)$	$2k\sin\left(\frac{\pi}{3}-Ø\right)-T_s$

$$Ø=\tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \quad (12)$$

Then T_a, T_b, and T_c is calculated for each sub-sector as in Table VI, where T_s is switching period, T_a, T_b and T_c are on-time of each vector as shown in Fig. 8.

III. SIMULATION RESULTS AND DISCUSSIONS

A. Electrical Simulations

In this part, a 120 kW PMSM drive is modelled in PLECS software with the motor and driver parameters given in Table VII. Two-level VSI and three-level NPC VSI topologies are simulated with both SPWM and SVPWM, so in total four cases are analyzed. In order to conduct a fair comparison procedure, controller performances of the motor drives are kept same for all cases. Moreover, the same heatsinks are chosen for both topologies to avoid influence of the size of the cooling system. Analyses are done with different switching frequencies (carrier frequencies) varying between 8-12 kHz. Dead time is not included into simulations. Minimum switching frequency is selected as 8 kHz by considering maximum speed of the electric machine, that is 12000 rpm resulting in 600 Hz fundamental stator frequency. Maximum switching frequency is selected

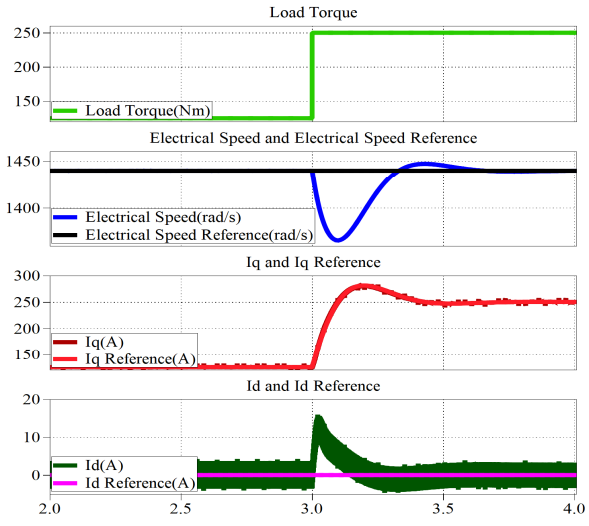

Fig. 9. Dynamic control performance from half load to full load

TABLE VII. MOTOR PARAMETERS AND INVERTER SPECIFICATIONS

Parameter	Value
V_{dc}(V)	850
R_{stator}(mΩ)	6.6
L_d,L_q(uH)	600
Flux induced (V.s)	0.222
Nominal speed (rpm)	4583
Maximum speed (rpm)	12000
Pole pair number	3
$I_{phase,rms}$(A)	177
F_{sw} (kHz)	8-12
T_{max} (Nm)	250

by considering the thermal limitation of the two-level topology by setting the maximum junction temperature to 130 °C.

As a controller structure, field oriented control (FOC) technique is implemented using outer speed and inner current loops. In order to compare controller performances, speed is kept constant at rated speed and step load torque change is applied to all four cases. An exemplary controller performance of motor drive is shown in Fig. 9. Same controller performances, which are speed regulation and dynamic response with a step load change, are achieved for each topology and each switching technique. I_d and I_q currents that are Park's transformation outputs are regulated by the inner current control loop. In FOC technique, I_q current supplies electrical torque to sustain load torque in a surface mount PMSM, whereas I_d current reference is zero until rated speed is exceeded. In the field weakening region, I_d current reference is adjusted to be able to reach higher speed with a limited DC bus voltage.

Current THD analyses are done with constant torque at 75 Nm (30% of the rated torque). At different operating speeds, current THDs are observed with different switching frequencies. The most distinct operation between analyzed cases is observed at rated speed. Therefore, current THD values with rated and half of the rated speed are given in Fig. 10 and Fig. 11, respectively. Difference between current THDs gets more distinct as speed gets close to rated speed since average on time of semiconductors increase with the motor speed. Therefore; current ripple increases for higher speeds.

Three-level NPC topology with SVPWM has superior performance for all motor speeds and switching frequency cases. Three-level topology generates voltage pulses of half of the amplitude of the two-level topology at the output. Therefore; current THD of the three-level topology is

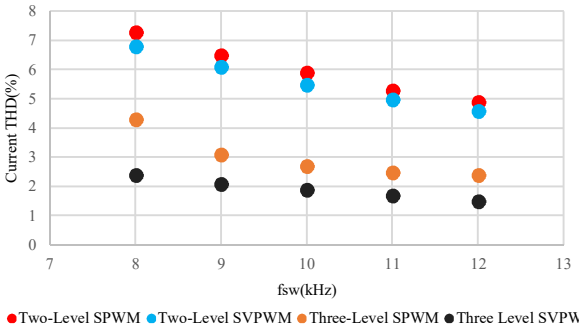

Fig. 10. Current THD (%) vs. switching frequency at 4583 rpm

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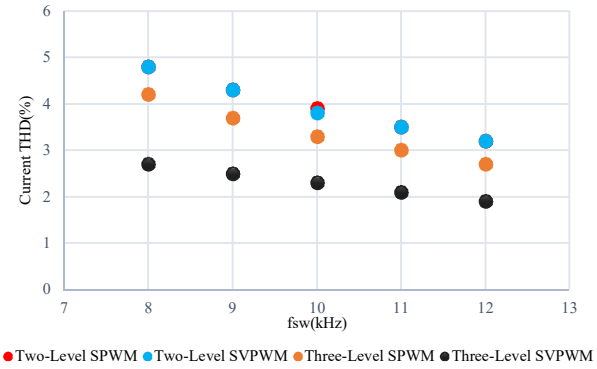

Fig. 11. Current THD (%) vs. switching frequency at 2291 rpm

expected to be lower than the two level topology. Moreover, SVPWM has better performance than SPWM in terms of current THD in both topologies. Whereas, the performance difference is more noticeable in the three-level topology. Current THD in all cases decreases as switching frequency increases and decrease in output current THD is expected to result in lower iron losses in the machine [10].

B. *Electro-thermal Simulations*

Electro-thermal simulations are done at rated speed and rated torque. Both semiconductor modules are assumed to be directly connected to the heatsink without any thermal interface material. PLECS thermal models calculate loss of a semiconductor by summing up the energy losses of semiconductors within a switching period. Then, averaging these in a fundamental cycle of output voltage and current, average loss values of each module are calculated. Loss calculation of the IGBTs and the diode of the selected modules are carried out regarding to the given information in [3].

Electro-thermal simulation models can be seen in Fig. 12 and Fig. 13. Same heatsink thermal parameters are used for both topologies having $R_{s\text{-}a}$=0.023 °C/W as sink-ambient thermal resistance. Since both modules are connected to the heatsink directly, $R_{c\text{-}s}$ case-sink thermal resistances are assumed to be zero. Case-heatsink and heatsink-ambient thermal resistances are implemented in the electro-thermal simulation model as depicted in the circuit schematics given Fig. 12 and Fig. 13. IGBT and diode junction-case thermal resistances are derived from datasheet and SEMISEL design tool values. SEMIKRON's WP16_280 heatsink module is used in both designs. Following assumptions are made for the thermal calculations:

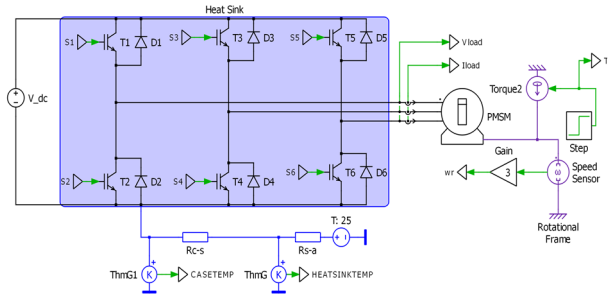

Fig. 12. Two-level topology electro-thermal model

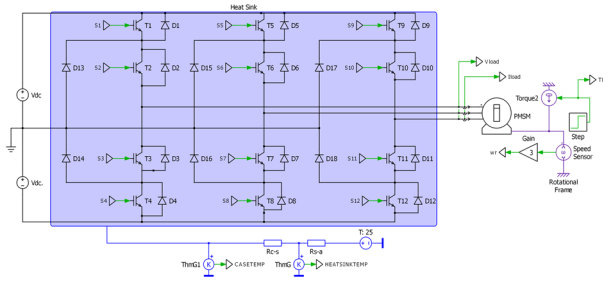

Fig. 13. Three-level topology electro-thermal model

- Water cooling is assumed with a flow rate of 6 l/min.
- Liquid inside the heatsink is assumed to be composed of 50% water and 50% glycol.
- Ambient temperature is set to 25 °C.

1) *IGBT Conduction Losses*

Collector-emitter voltage V_{CE} vs. collector current I_C curve is embedded into PLECS IGBT thermal model. Temperature dependency of conduction losses are not integrated into software due to its negligible effect on losses. Conduction losses is calculated as follows:

$$P_{con,IGBT} = \frac{1}{T_1}\int_0^{T_1} I_{C(t)} V_{CE(t)}\, D_{IGBT}(t)dt \qquad (13)$$

$$V_{CE(t)} = V_{CE0} + I_o(t) r_{ce} \qquad (14)$$

V_{CE0}: Zero crossing of linearized I_{CE} vs. V_{CE} curve

r_{ce}: Inverse slope of I_{CE} vs. V_{CE} curve

By implementing collector-emitter voltage by curve fitting, PLECS software calculates the average conduction loss via (13) and (14).

2) *IGBT Switching Losses*

Switching losses are calculated via given turn-on energy E_{on} and turn-off energy E_{off} graphs in the datasheet of each semiconductor. Turn-on and turn-off energies are calculated for the given collector emitter current and the blocking voltage of the semiconductor switch. Mathematical equations that are (15), (16) and (17) are implemented into the software. By summing up the turn-on and turn-off energies in each switching cycle, total switching loss energy of a IGBT is calculated. By averaging this in one fundamental frequency, switching loss of a IGBT is determined.

K_v in (16) and (17) is a manufacturer dependent coefficient that is selected as 1.3 or 1.4 for IGBTs of SEMIKRON [3].

$$P_{sw,IGBT} = \frac{1}{T_1}\sum_{i=1}^{T_1 f_{sw}} E_{on}(t_i) + E_{off}(t_i) \qquad (15)$$

$$E_{on} = E_{on}(I_c)\left(\frac{V_{in}}{V_{ref}}\right)^{K_v}\left(1 + TC_{Esw}\left(T_j - T_{ref}\right)\right) \qquad (16)$$

$$E_{off} = E_{off}(I_c)\left(\frac{V_{in}}{V_{ref}}\right)^{K_v}\left(1 + TC_{Esw}\left(T_j - T_{ref}\right)\right) \qquad (17)$$

V_{in} : V_{CE} blocking voltage of IGBT

$E_{on,off}(I_c)$: E_{on} and E_{off} value for corresponding current

K_v : Exponents for voltage dependency of switching losses

TC_{Esw} : Temperature coefficient of IGBT switching losses

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3) Diode Conduction Losses

$$P_{con,diode} = \frac{1}{T_1}\int_0^{T_1} I_{F(t)} V_{F(t)}\, D_{diode}(t)dt \qquad (18)$$

$$V_F(t) = V_{F0} + I_o(t) r_d \qquad (19)$$

V_{F0}: Zero crossing of linearized I_F vs. V_F curve of diode

r_d: Inverse slope of I_F vs. V_F curve of diode

4) Diode Switching Losses

Switching loss calculation of diode is done with the same procedure as for the IGBT using (20) and (21).

$$P_{sw,IGBT} = \frac{1}{T_1}\sum_{i=1}^{T_1 f_{sw}} E_{rr}(t_i) \qquad (20)$$

$$E_{rr} = E_{rr}\left(\frac{I_{out}(t)}{I_{ref}}\right)^{K_i}\left(\frac{V_{in}}{V_{ref}}\right)^{K_v}\left(1 + TC_{Err}\left(T_j - T_{ref}\right)\right) \qquad (21)$$

E_{rr}: Reverse recovery energy of diode

TC_{ERR}: Temperature coefficient of diode switching loss

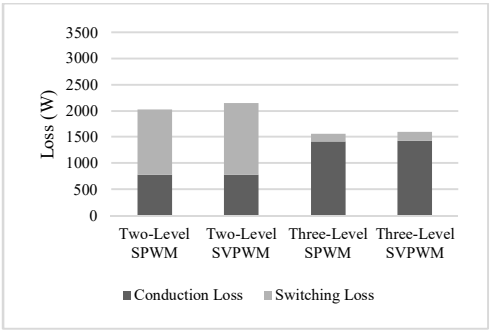
Loss distribution results for analyzed cases are shown in Fig. 14 for switching frequencies of 8-12 kHz. SVPWM and SPWM does not have significant effect on thermal performance in both topologies that is conduction losses and switching losses are almost the same in two switching techniques. Switching loss decrease is significant from two-level to three-level topology. Since three-level topology has more switches than two-level topology, conduction losses are dominant in the three-level topology. Conduction losses are almost doubled in three-level topology.

Due to high fundamental frequency requirement in the field weakening region, high frequency switching is required in PMSM drives. However; in two-level topology, main switches are operating against double V_{CE} voltage stress compared with three-level topology. Therefore; switching losses are dominant in two-level topology. Another reason of high switching losses in two-level topology is as follows: Relation between switching losses and blocking voltage is not linear. Dominance of switching losses can be seen in Fig. 14.

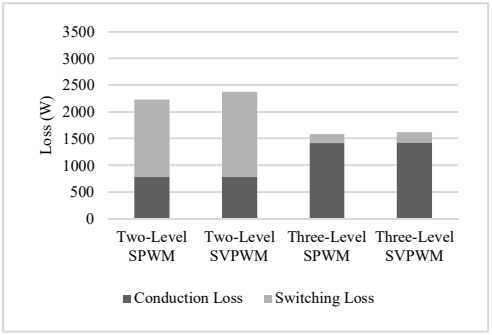
At 12 kHz switching frequency, maximum junction temperature constraint is reached for two-level topology as can be seen in Fig. 15. On the other hand, three-level topology reaches a maximum junction temperature of 130 ºC at 22 kHz switching frequency. That is with the given semiconductors, three-level topology could be used even at 22 kHz although two-level topology is limited to 12 kHz switching frequency. As expected, 22 kHz switching frequency will result in a better output current THD and less torque ripple at the output.

IV. CONCLUSION

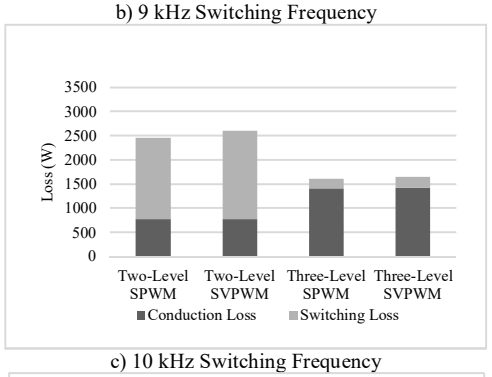
A multidimensional comparison of two VSI topologies is done with two different switching techniques. The three-level NPC VSI topology is superior in both thermal performance and output quality point of views. Conduction losses are dominant in three-level topology. However; due to lower collector-emitter blocking voltage requirement, 650 V IGBT products can be used in three-level design. Therefore; switching losses have minor effect in three-level topology for the same switching frequencies. For the given semiconductors, two-level topology is limited to 12 kHz switching frequency. On the other hand, three-level topology



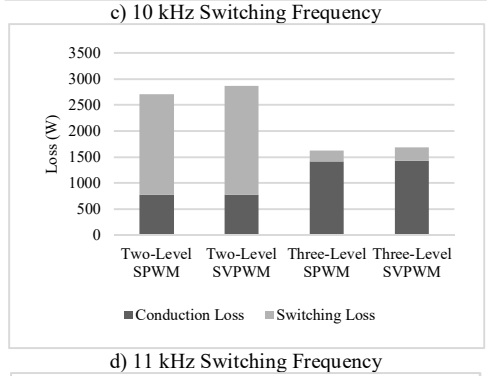
a) 8 kHz switching frequency



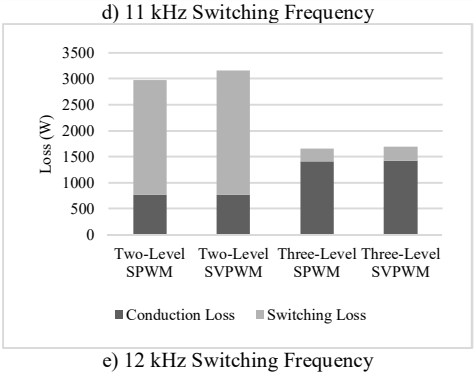
b) 9 kHz Switching Frequency



c) 10 kHz Switching Frequency



d) 11 kHz Switching Frequency



e) 12 kHz Switching Frequency

Fig. 14. Loss distribution of topologies and switching techniques

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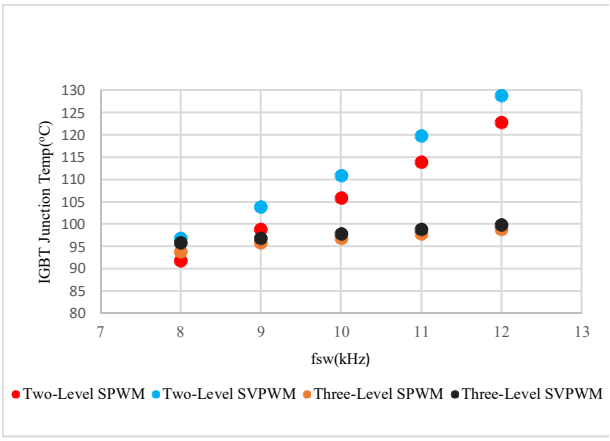

Fig. 15. Junction temperatures of IGBTs in each topology and switching technique

can reach up to 22 kHz for the same maximum junction temperature limitation. Therefore; three-level topology is superior for applications such that high fundamental frequency is needed. However; this inference is valid for conventional Si IGBT diode pairs. With the recent developments in semiconductor technologies, higher switching frequency operation in such power levels with two-level topology is possible as SiC MOSFETs have better switching performance than conventional Si IGBTs [1].

Thermal performance effect of switching techniques is not significant in both topologies. This can be seen from the efficiency comparison results given in Table VIII for a power factor of 0.83. On the other hand, three-level NPC topology has a better efficiency performance in whole switching frequency range. SVPWM has a better output current THD performance compared with SPWM in both topologies. Therefore; SVPWM technique can be preferable due to low THD at the output. Additionally, due to better DC bus utilization, SVPWM can also be preferable in order to decrease DC bus voltage level and switching losses. Although three-level SVPWM is able to achieve a superior performance in all dimensions, topology has few drawbacks. Floating capacitor voltage and manipulation of higher number of switches make the three-level topology more challenging compared to the two-level topology. Also the high number of switches increases initial cost.

TABLE VIII. EFFICIENCY RESULTS FOR TWO TOPOLOGIES AND SWITCHING TECHNIQUES

Topology	**Switching Technique**	**Efficiency (%) with f_{sw} (kHz)**					**P.F.**
		8	**9**	**10**	**11**	**12**	
Two-level	SPWM	98.3	98.1	97.9	97.7	97.5	0.83
Two-level	SVPWM	98.2	98.0	97.8	97.6	97.4	0.83
Three-level NPC	SPWM	98.7	98.7	98.7	98.6	98.6	0.83
Three-level NPC	SVPWM	98.7	98.6	98.6	98.6	98.6	0.83

REFERENCES

[1] Kumar, K.; Bertoluzzo, M.; Buja, G., "Impact of SiC MOSFET traction inverters on compact-class electric car range," in Power Electronics, Drives and Energy Systems (PEDES), 2014 IEEE International Conference on , vol., no., pp.1-6, 16-19 Dec. 2014.

[2] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," Industry Applications, IEEE Transactions on, vol. 41, no. 3, pp. 855 – 865, 2005.

[3] A. Wintrich, U. Nicolai, and T. Reimann, "Semikron application manual," 2011.

[4] A. Bubert, S.-H. Lim, and R. W. De Doncker, "Comparison of 2-level B6C and 3-level NPC inverter topologies for electric vehicles," in Proc. IEEE Southern Power Electron. Conf. (SPEC), Puerto Varas, Chile, 2017, pp. 1–6

[5] A. Choudhury, P. Pillay, M. Amar and Sheldon. S. Williamson, "Performance comparison study of two and three-level inverter for electric vehicle application," in Proc. on IEEE Transportation Electrification Conf. and Expo, Dearborn, USA, June 2014, pp. 1-6.

[6] Peng, F.Z.: 'A generalized multilevel inverter topology with self voltage balancing', IEEE Trans. Ind. Appl., 2001, 37, pp. 611–618

[7] J. Pou, D. Boroyevich, and R. Pindado, "New feedforward space-vector PWM method to obtain balanced ac output voltages in a three-level neutral-point-clamped converter," IEEE Trans. Power Electron., vol. 49, pp. 1026–1034, Oct. 2002

[8] A. Choudhury, P. Pillay, and S. Williamson, "DC-link voltage balancing for a three-level electric vehicle traction inverter using an innovative switching sequence control scheme," IEEE J. Emerging Selected Topics Power Electron., vol. 2, no. 2, pp. 296-307, June 2014.

[9] Haibing Hu; Wenxi Yao; Zhengyu Lu, "Design and Implementation of Three-Level Space Vector PWM IP Core for FPGAs," Power Electronics, IEEE Transactions on , vol.22, no.6, pp.2234-2244, Nov. 2007

[10] G. Mademlis, Y. Liu, J. Zhao, "Comparative Study of the Torque Ripple and Iron Losses of a Permanent Magnet Synchronous Generator Driven by Multilevel Converters," XIII International Conference on Electrical Machines (ICEM), pp. 1406-1412, 2018

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