

# Matrix-Based Approach for Open-Circuit Fault-Tolerant Analysis and PWM Design of Active Neutral-Point-Clamped Converters

Yuzhuo Li<sup>1</sup>, Member, IEEE, Hao Tian<sup>1</sup>, Member, IEEE, and Yunwei Ryan Li<sup>1</sup>, Fellow, IEEE

**Abstract**—Active neutral-point-clamped converter adds open-circuit fault-tolerant (OCFT) capability compared with the widely used original neutral-point-clamped (NPC) topology. However, such capability is hard to utilize due to difficulties in pulse-width modulation (PWM) design and the randomness of failure points, particularly in high-level converters. Current research mainly focused on low-level topologies with a limited number of fault scenarios; moreover, the analysis and design are performed in a nonsystematic way. In this article, the OCFT operations of active NPC (ANPC) converters with multiple fault switches are investigated and the systematic PWM design process is proposed. First, different matrices are proposed for the ANPC converters to capture the complicated topology information and achieve an exhaustive analysis of the topological redundancy. Then, a step-by-step process is proposed to derive the suitable OCFT PWM patterns. The five-level ANPC converter is investigated as an example. Its experimental results validate that the proposed approach can 1) properly predict the behavior of converters systematically so that the tolerable faults and intolerable can be identified during the design procedure, and 2) the inherent fault-tolerant capability of the five-level ANPC converter can be guaranteed through the proposed method, and 3) multiswitch open-circuit faults can be easily dealt with by implementing suitable carrier-based PWM schemes.

**Index Terms**—Matrix model, neutral-point-clamped converter, open circuit fault tolerance, pulsedwidth-modulation design.

## I. INTRODUCTION

**R**ELIABILITY analysis and resilient operation design have been of great importance for better integration of power converters into modern power systems [1]. Different fault-tolerant control and modulation designs for power converters are scattered in different layers of malfunctions, as summarized in Fig. 1: converter-level failures, phase-leg failures, and device-level failures [2]. As one of the device-level failures, open-circuit faults are normally found in the wire-bonded-type

Manuscript received 10 March 2022; revised 9 June 2022; accepted 19 July 2022. Date of publication 26 July 2022; date of current version 6 September 2022. This work was supported in part by the Canada First Excellent Research Fund and in part by the Natural Science and Engineering Research Council of Canada. Recommended for publication by Associate Editor E. Babaei. (Corresponding author: Hao Tian.)

The authors are with the Department of Electrical and Electronic Engineering, University of Alberta, Edmonton, AB T6G 2V4, Canada (e-mail: yuzhuo@ualberta.ca; tianhao1988@gmail.com; yunwei.li@ualberta.ca).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2022.3193972>.

Digital Object Identifier 10.1109/TPEL.2022.3193972

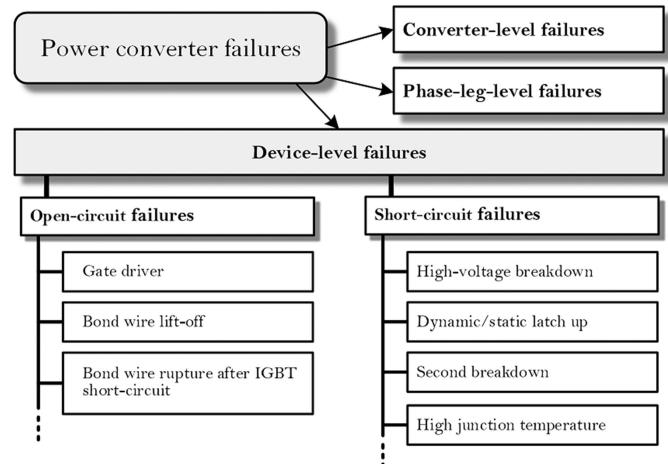


Fig. 1. Failures and causes for power switching devices.

power-electronics modules and could be triggered by gate driver failures, bond wire lift-OFF, bond wire rupture after device short-circuit fault. They are normally deep coupling with the converter topologies and have direct impacts on the healthy operation, degrade the reliability, and cause distorted outputs. Considering multilevel converters (MLCs) generally have a higher number of switches, the ability to tolerate device failure has been considered as an attractive feature, and topologies with such capability are gaining attention [3]. Among the topologies, the active neutral-point-clamped (ANPC) topologies, the variant of widely used neutral-point-clamped (NPC) topology, has been considered as an attractive option for applications requiring high reliability, such as aviation systems, medium-voltage drive systems, and pump storage applications [4].

In recent years, considerable research can be found for open-circuit fault-tolerant (OCFT) analysis and modulation design for specific types of ANPC multilevel converters [5]–[12]. For instance, in [5], the three-level ANPC inverter was thoroughly analyzed and fault-tolerant strategies were proposed. It could help enable continuous operating of the inverters and drive systems under single and multiple device open-failure conditions. A more general analysis for n-level ANPC converters was published later as in [6], where both single- and double-switch open-circuit faults were exhaustively examined. In [7], the fault-tolerant capability of an advanced three-level active T-Type converter was investigated under single-switch

fault conditions. A more recently published work utilized the Markov model to fast investigate the reliability of various ANPC converters [9].

Traditionally, due to the deep-coupling between the device-level OCFT method and the converter topologies, the topology fault-tolerant analysis, and the associated modulation design is highly dependent on the engineering expertise of each converter and normally result in a case-by-case procedure. An exhaustive table is normally presented to extensively investigate the applicable switching states one by one [5], [6], [13], [14]. With the circuit complexity increasing, this task could become quite difficult, and traditional ways become less attractive due to inefficiency. On the other hand, most OCFT modulation schemes of ANPC converters are highly dependent on the individual topology forms and lack systematic methodology [8], [10]–[12]. Both the analysis and design could become less efficient and involve much higher research efforts for higher-level or more complex converter circuits, such as 4/5-level ANPC cases, especially for multi-switch-fault conditions [6]. Just take a four-level ANPC topology as an example: as discussed in [9], there are 1118 relevant states of its Markov chains; and this number raises exponentially with the number of switches.

The abovementioned challenges inspire motivations to find a different way for ANPC converters with OCFT operation. Extended from [15]–[18], which mainly deals with the topology derivation and simplification, this article is mainly focused on the thorough investigation of OCFT operations of multilevel ANPC converters with multiple fault switches and the systematic pulse-width modulation (PWM) design process. In detail, the contributions can be summarized as follows.

- 1) The unified matrix modeling method of open-circuit fault ANPC MLCs is proposed to help achieve exhaustive analysis and design, without the time-consuming establishment of switching state tables/lists.
- 2) By following the proposed PWM design process, the applicable PWM patterns for fault conditions can be systematically derived to help maintain the output performance.
- 3) Random enumeration and nonsystematic case-by-case iterative design processes can be avoided during the implementation by directly implementing the normal condition CB-PWM for faulty ANPC converter.
- 4) In addition to general forms of ANPC MLCs, the proposed method can potentially be implemented for other ANPC-based derivatives by minor modifications, e.g., simplified ANPC topologies and hybridclamped topologies.

Since the fault detection is out of the scope of this article, in the following discussions, the fault device localization is assumed to be done by some existing methods, e.g., device measurement through smart gate drivers [19], [20] and output waveform diagnosis [21]. And these methods can be easily embedded into the proposed method, serving as the external information required by the OCFT analysis and PWM design.

In the following sections, both the theoretic discussions (see Section II), analysis (see Section III), PWM design method (see Section IV), and case study experiments (see Section VI) will be provided to validate this method. Besides, the extension for

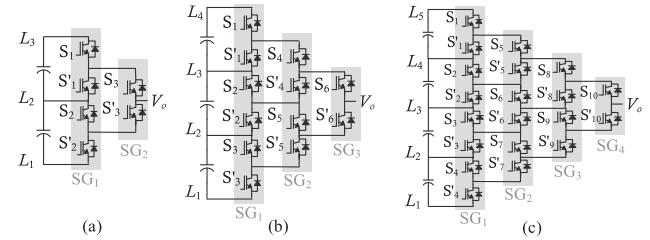


Fig. 2. General topology of (a) three-level ANPC converter, (b) four-level ANPC converter, and (c) five-level ANPC converter.

other topologies will also be discussed (see Section VII). Finally, Section VIII concludes this article.

## II. MATRIX MODELS OF ANPC MULTILEVEL TOPOLOGIES

To systematically investigate the ANPC converters, we capture the complicated structures and the high number of redundant switching states by the matrix models.

### A. General Matrix Models

The general  $N$ -level ANPC converter can be modeled as [17]

$$V_o = \mathbf{S} * \mathbf{L}_N \quad (1)$$

where the output voltage is indicated by  $V_o$ , the switching network matrix is  $\mathbf{S}$ , and the dc-link level matrix is  $\mathbf{L}_N$ . Since the switching network of ANPC topology normally consists of multiple columns of switches, it can be naturally decomposed into several switching groups (e.g.,  $SG_1, SG_2, \dots$ ), as indicated in the shadow areas of Fig. 2. In such a way, the matrix  $\mathbf{S}$  can be decomposed as the product of concatenated submatrix. Each submatrix represents one switching group.

Take the general form of the three-level ANPC converter [see Fig. 2(a)] as an example. Its general matrix model can be expressed as

$$V_{out\_3L} = \underbrace{\begin{bmatrix} s_3 & s'_3 \end{bmatrix}}_{SG_2} \underbrace{\begin{bmatrix} s_1 & s'_1 & 0 \\ 0 & s_2 & s'_2 \end{bmatrix}}_{SG_1} \mathbf{L}_3 \quad (2)$$

where  $s_i$  indicates the state of devices: 1)  $s_i = 1$ , if the switch is ON state, 2)  $s_i = 0$ , if the switch is OFF state.  $s_1, s'_1, s_2$ , and  $s'_2$  form the switching group  $SG_1$ ,  $s_3$  and  $s'_3$  form the switching group  $SG_2$ .  $\mathbf{L}_3 = [L_3 \ L_2 \ L_1]^T$  indicates the dc-link levels.

Take the general form of a four-level ANPC converter [see Fig. 2(b)] as another example

$$V_{out\_4L} = \underbrace{\begin{bmatrix} s_6 & s'_6 \end{bmatrix}}_{SG_3} \underbrace{\begin{bmatrix} s_4 & s'_4 & 0 \\ 0 & s_5 & s'_5 \end{bmatrix}}_{SG_2} \underbrace{\begin{bmatrix} s_1 & s'_1 & 0 & 0 \\ 0 & s_2 & s'_2 & 0 \\ 0 & 0 & s_3 & s'_3 \end{bmatrix}}_{SG_1} \mathbf{L}_4 \quad (3)$$

where  $s_1-s_6$  and  $s'_1-s'_6$  indicate the switching states of associated devices in the topology.  $\mathbf{L}_4 = [L_4 \ L_3 \ L_2 \ L_1]^T$  indicates the dc-link levels.

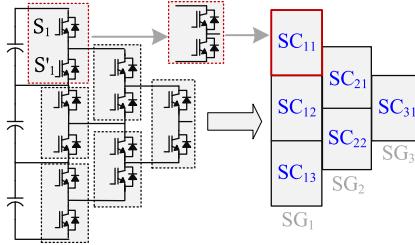


Fig. 3. Switching cell form of ANPC converter.

For the five-level ANPC converter [as shown in Fig. 2(c)], the general matrix model is

$$V_{\text{out\_}5L} = \underbrace{\begin{bmatrix} s_{10} & s'_{10} \end{bmatrix}}_{\mathbf{SG}_4} \underbrace{\begin{bmatrix} s_8 & s'_8 & 0 \\ 0 & s_9 & s'_9 \end{bmatrix}}_{\mathbf{SG}_3} \underbrace{\begin{bmatrix} s_5 & s'_5 & 0 & 0 \\ 0 & s_6 & s'_6 & 0 \\ 0 & 0 & s_7 & s'_7 \end{bmatrix}}_{\mathbf{SG}_2} \underbrace{\begin{bmatrix} s_1 & s'_1 & 0 & 0 & 0 \\ 0 & s_2 & s'_2 & 0 & 0 \\ 0 & 0 & s_3 & s'_3 & 0 \\ 0 & 0 & 0 & s_4 & s'_4 \end{bmatrix}}_{\mathbf{SG}_1} \mathbf{L}_5 \quad (4)$$

where  $s_i$  indicates the state of devices: 1)  $s_i = 1$ , if the switch is ON state; 2)  $s_i = 0$ , if the switch is OFF state.  $\mathbf{L}_5 = [L_5 \ L_4 \ L_3 \ L_2 \ L_1]^T$  indicates the dc-link levels [see Fig. 2(c)],  $s_1-s_{10}$  and  $s'_1-s'_{10}$  indicate the switching states of associated devices in the topology.

### B. Block-Based Representation

By comparing the general matrix models of the three-level and four-level cases, it is observed that this matrix model can preserve the complete structure information of topologies. However, the matrix dimension is directly determined by the output-level numbers and the equation tends to be quite complicated even for the four-level case. Therefore, it is beneficial to establish some special matrix models with lower complexity.

In [15] and [22], the concept of switching cells is introduced for ANPC converters as the half-bridge inside the topology. Take the general four-level ANPC converter as an example. Each half-bridge can be represented as a block, e.g.,  $SC_{11}$  denotes the bridge with  $s_1$  and  $s_2$ . In such a way, the complicated ANPC circuit can be simplified into a block-based version (as shown in Fig. 3) to facilitate the following discussion.

### C. Status Matrix Model

The status matrix model can be established to represent the possible operation status, and for a four-level ANPC converter, it can be expressed as

$$\begin{aligned} \mathbf{S}(k) &= \mathbf{SU}(k) - \mathbf{SL}(k) \\ &= \begin{bmatrix} s_1(k) & s_4(k) & s_6(k) \\ s_2(k) & s_5(k) & \\ s_3(k) & & \end{bmatrix} - \begin{bmatrix} s'_1(k) & s'_4(k) & s'_6(k) \\ s'_2(k) & s'_5(k) & \\ s'_3(k) & & \end{bmatrix} \\ &= \begin{bmatrix} s_{11}(k) & s_{21}(k) & s_{31}(k) \\ s_{12}(k) & s_{22}(k) & \\ s_{13}(k) & & \end{bmatrix} \end{aligned} \quad (5)$$

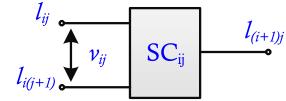


Fig. 4. Potential voltages of the three terminals of a single switching cell.

where  $\mathbf{S}(k)$  represents the status matrix of ANPC topology at time  $k$ ,  $\mathbf{SU}(k)$  (or  $\mathbf{SL}(k)$ ) represents the state matrix of all the upper (or lower) switches of switching cells at time  $k$ . The states of switches in  $\mathbf{SU}(k)$  and  $\mathbf{SL}(k)$  are assigned by using bilogic: 1) if the switch is turned ON, then, the value of the state is “1”, 2) if the switch is turned OFF, then, the value of the state is “0”. While the elements in state matrix  $\mathbf{S}(k)$  are trilogic and have three states: “1,” “0,” “−1,” representing the operation states of associated switching cells in the topology.

In practice, as demonstrated in [15], certain switching cells inside the topology can be operated at a high switching frequency (HSF) or low switching frequency (LSF), resulting in various PWM patterns. These PWM patterns could be indicated by the form of status matrix models as well. This can be realized by assigning certain elements of the matrix as constant values for each operation period, e.g., between  $L_1$  and  $L_2$ .

### D. Level Matrix Model

The potential voltages of the three terminals of a single switching cell are defined first, as shown in Fig. 4 [16]. The  $l_{ij}$  and  $l_{i(j+1)}$  denote the potential voltages of two input terminals of  $SC_{ij}$  ( $l_{i(j+1)} \geq l_{ij}$ ). The  $l_{(i+1)j}$  denotes the potential voltage of one output terminal of  $SC_{ji}$  and satisfies the following equation:

$$l_{(i+1)j}(k) = \begin{cases} l_{ij}(k) & , \text{if } s_{ij}(k) > 0 \\ l_{i(j+1)}(k) & , \text{if } s_{ij}(k) < 0 \\ (l_{ij}(k) + l_{i(j+1)}(k))/2 & , \text{if } s_{ij}(k) = 0. \end{cases} \quad (6)$$

Then, the level matrix  $\mathbf{L}(N, k) = [l_{ij} = (k)]_{N \times N}$  of  $N$ -level ANPC can be derived based on  $\mathbf{S}(k)$  to obtain the instantaneous voltage information in certain operation statuses. Note that the first column of elements in  $\mathbf{L}(N, k)$  should be arranged based on the potential voltages of input dc sources.

For instance, the level matrix of a four-level ANPC converter can be expressed as

$$\mathbf{L}(k) = \begin{bmatrix} l_{11}(k) & l_{21}(k) & l_{31}(k) & l_{41}(k) \\ l_{12}(k) & l_{22}(k) & l_{32}(k) & \\ l_{13}(k) & l_{23}(k) & l_{33}(k) & \\ l_{14}(k) & & & \end{bmatrix}. \quad (7)$$

And the level matrix of a five-level ANPC converter can be expressed as

$$\mathbf{L}(k) = \begin{bmatrix} l_{11}(k) & l_{21}(k) & l_{31}(k) & l_{41}(k) & l_{51}(k) \\ l_{12}(k) & l_{22}(k) & l_{32}(k) & l_{42}(k) & \\ l_{13}(k) & l_{23}(k) & l_{33}(k) & & \\ l_{14}(k) & l_{24}(k) & & & \\ l_{15}(k) & & & & \end{bmatrix}. \quad (8)$$

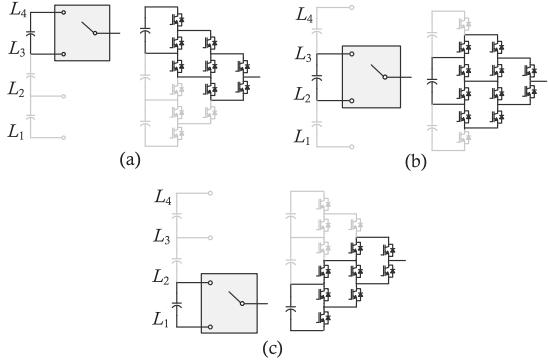


Fig. 5. In total, four-level ANPC converter with (a) operation range from  $L_4$  to  $L_3$ , (b) operation range from  $L_3$  to  $L_2$ , and (c) operation range from  $L_2$  to  $L_1$ .

### E. Vector-Form Model

To represent the equivalent input–output features of the topology, (3) can be further simplified into

$$V_{\text{out\_}4L} = [s_{e1} \ s_{e2} \ s_{e3} \ s_{e4}] \mathbf{L}_{4L} \quad (9)$$

where  $s_{e1}$ – $s_{e4}$  can be expressed as

$$\begin{aligned} s_{e1} &= s_6 s_4 s_1 \\ s_{e2} &= s_6 s_4 s'_1 + s_6 s'_4 s_2 + s'_6 s_5 s_3 \\ s_{e3} &= s_6 s'_4 s'_1 + s'_6 s_5 s'_2 + s'_6 s'_5 s_3 \\ s_{e4} &= s'_6 s'_5 s'_3 \end{aligned}$$

and denote the composite switching states associated with each dc-link level, and the value is “1” or “0”. As Fig. 5 shows, for instance,  $s_{e1}$  of four-level ANPC topology is determined by the product of  $s_6$ ,  $s_4$ , and  $s_1$ , and if  $s_{e1}$  is “1,” then, the  $L_4$  can be generated by the converter as the output level. Similarly,  $s_{e2}$  is determined by  $s_6$ ,  $s'_6$ ,  $s_5$ ,  $s_4$ ,  $s'_4$ ,  $s_2$ ,  $s'_1$ , which can be related to the generation of  $L_3$  for converter output. And  $s_{e3}$  and  $s_{e4}$  is related to  $L_2$  and  $L_1$ , respectively.

The vector form of five-level ANPC converter should be

$$V_{\text{out\_}5L} = [s_{e1} \ s_{e2} \ s_{e3} \ s_{e4} \ s_{e5}] \mathbf{L}_5 \quad (10)$$

where

$$\begin{aligned} s_{e1} &= s_{10} s_8 s_5 s_1 \\ s_{e2} &= s_{10} s_8 s_5 s'_1 + s_{10} s_8 s'_5 s_2 + s_{10} s'_8 s_6 s_2 + s'_10 s_9 s_6 s_2 \\ s_{e3} &= s_{10} s_8 s'_5 s'_2 + s_{10} s'_8 s_6 s'_2 + s_{10} s'_8 s'_6 s_3 \\ &\quad + s'_{10} s_9 s_6 s'_2 + s'_{10} s_9 s'_6 s_3 + s'_{10} s'_9 s_7 s_3 \\ s_{e4} &= s_{10} s'_8 s'_6 s'_3 + s'_{10} s_9 s'_6 s'_3 + s'_{10} s'_9 s_7 s'_3 + s'_{10} s'_9 s'_7 s_4 \\ s_{e5} &= s'_{10} s'_9 s'_7 s'_4 \end{aligned}$$

and  $s_{e1}$ – $s_{e5}$  denote the composite switching states associated with five dc-link levels  $\mathbf{L}_5 = [L_5 \ L_4 \ L_3 \ L_2 \ L_1]^T$ .

### III. MATRIX-BASED ANALYSIS OF CONVERTER REDUNDANCY AND DEVICE OPEN-CIRCUIT FAULTS

In the previous section, the status matrix model, level matrix model, and vector-form model have simpler forms compared

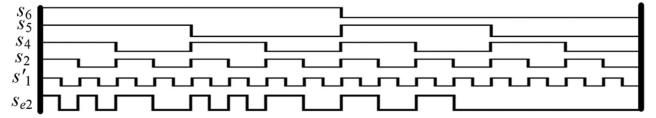


Fig. 6. Logic form values of  $s_{e2}$  based on (9) by exhaustive investigation of associated states in four-level topology ( $s'_6$  and  $s'_4$  are omitted since their values are complementary of  $s_6$  and  $s_4$ , respectively). High level means logic value “1”, low level means logic value “0”.

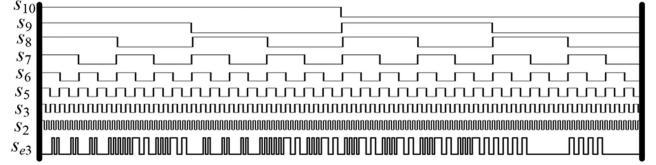


Fig. 7. Timing diagram of the binary code values of  $s_{e3}$  (the third level) in (10) by exhaustive investigation of associated states in five-level topology. High level means value “1”, low level means value “0”.

to the general matrix models. While status matrix model is a compact way of reorganization of the general matrix model and contains all the internal information of the converter. The level matrix model is derived based on the status matrix to further reveal the level information of the converter. The vector-form model captures the input–output information and ignores the internal details of the converter. In this section, three matrix models are utilized for the thorough fault-tolerant operation analysis of converters: 1) vector-form models are used for redundancy analysis and 2) status and level matrix models are used for open-circuit faults analysis.

#### A. Analysis of Converter Redundancy

To exhaustively investigate the redundancies inside the ANPC converters, the simplified matrix model can be implemented. Take four-level ANPC as an example, in (9),  $s_{e2}$  consists of the sum of three terms and can be translated into binary code. The applicable states are the ones that result in  $s_{e2} = 1$ , i.e., the converter can generate the second level.

To test all combinations of the associated switches in  $s_{e2}$ , one can simply test all values of the binary number ( $s_6 \ s_5 \ s_4 \ s_2 \ s'_1$ ) from (11111) to (00000). The results are shown in Fig. 6, which contains 12 states that result in  $s_{e2} = 1$ . Based on the same approach, there is only one state for the first or fourth level and 12 states for the third level.

The redundancies can be exhaustively investigated for higher-level cases, like the five-level ANPC converter. For instance, in (10),  $s_{e3}$  consists of the sum of six terms. To thoroughly investigate all the possibilities, one can simply test all combinations of the associated switches in  $s_{e3}$ , i.e., testing all values of the binary number ( $s_2 \ s_3 \ s_5 \ s_6 \ s_7 \ s_8 \ s_9 \ s_{10}$ ) from (1111 1111) to (0000 0000). And the associated  $s'_i$  can be set as complementary states. The results are shown in Fig. 7, which shows 96 states that result in  $s_{e3} = 1$ . Based on the same approach, there is one state for first or first level and there are 32 states for generating the second or fourth level.

In practice, different locations of the fault switch may result in different fault features and fault effects, e.g., degraded output

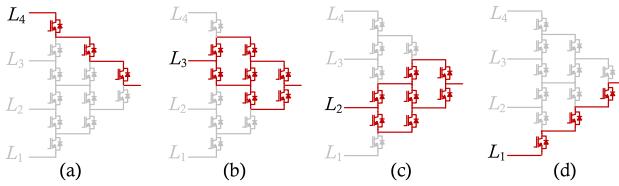


Fig. 8. Locations for possible faults in a four-level ANPC converter: (a) output fourth level, (b) output third level, (c) output second level, and (d) output first level.

TABLE I  
CRITICAL LEVEL OF DIFFERENT SWITCHES OF FOUR-LEVEL ANPC  
CONVERTER BY VECTOR-FORM MODEL

	$S_1$	$S_1'$	$S_2$	$S_2'$	$S_3$	$S_3'$	$S_4$	$S_4'$	$S_5$	$S_5'$	$S_6$	$S_6'$
$L_4$	1						1				1	
$L_3$		1/3	1/3		1/3		1/3	1/3			2/3	1/3
$L_2$		1/3		1/3	1/3		1/3	1/3	1/3	1/3	2/3	
$L_1$						1			1		1	

capability. And this can be thoroughly analyzed by vector-form models. For instance, there are different locations for possible faults in a four-level ANPC converter, as shown in Fig. 8. Recall (9) for four-level ANPC converter. For each output level, there is the composite switching state equation. Here, we can use these equations to help us clearly show their impact on the operation. An index is defined as Critical Level: the ratio between the loss of redundancies induced by the open circuit fault and the prefault redundancies.

In equation  $s_{e1} = s_6 s_4 s_1$ , we can observe that all three switches ( $S_6 S_4 S_1$ ) are necessary for  $L_4$  generation, and any faults will eliminate the redundancy, making the composite switching state equation  $s_{e1}$  equal to 0. The critical level of each of these three switches should be 1 by definition.

As for  $L_3$ , we have equation  $s_{e2} = s_6 s_4 s'_1 + s_6 s'_4 s_2 + s'_6 s_5 s_3$ , where faulty  $S_1'$  or  $S_2$  results in the loss of redundancies, i.e., the number of terms in  $s_{e2}$  is reduced by 1, therefore, the critical level of  $S_1'$  or  $S_2$  is 1/3.

A similar calculation can be done for the rest of the switches and demonstrated in Table I. The distribution of the critical levels indicates the different effects and importance of the different fault locations. In general, we can classify the open-circuit faults of ANPC converter into two major types: 1) one is those switches with a critical level equal to 1, 2) the other one is the rests. As for the four-level case, the latter type can be further divided based on the distributions of critical levels: ii-a) faults on  $S'_1$  (or  $S_3, S_4', S_5$ ) may reduce the redundancies of two levels; ii-b) faults on  $S_2$  or  $S_2'$  only affect one level, therefore, are less critical. The calculation of critical levels for a five-level ANPC converter can be derived by definition and can be found in Appendix Table II.

Without waveform degradation, a general four-level ANPC topology can allow four open-circuit switches at most. This number is increased to eight for a general five-level ANPC topology. And this can be obtained by the proposed matrix analysis. For instance, during the converter redundancy analysis, we can find out those binary numbers representing combinations of the associated switches and examine the bits of binary numbers, then, select the combinations with the least of “1s”.

## B. Matrix-Based Analysis of Device Open-Circuit Faults

To systematically analyze the postfault operation, matrix models of the states can be utilized: if there are open-switch faults in a four-level ANPC topology, the associated elements in  $\mathbf{SU}(k)$  or  $\mathbf{SL}(k)$  will be assigned as “0”. For a three-switch open-circuit case ( $S_1', S_2', S_4'$ ), the resulting state matrix  $\mathbf{S}(k)$  should be derived from (4) with elements  $s_1'(k) = s_2'(k) = s_4'(k) = 0$  as

$$\mathbf{S}(k) = \mathbf{SU}(k) - \mathbf{SL}(k)$$

$$= \begin{bmatrix} s_1(k) & s_4(k) & s_6(k) \\ s_2(k) & s_5(k) & \\ s_3(k) & & \end{bmatrix} - \begin{bmatrix} 0 & 0 & s'_6(k) \\ 0 & s'_5(k) & \\ s'_3(k) & & \end{bmatrix}. \quad (11)$$

With improper modulation schemes, the converter may not output the desired levels. In normal conditions, eight switches can be used to generate PWM waveforms consisting of fourth level and third level [see Fig. 5(a)]. For instance, one possible operation pattern can be: ( $S_1, S_1'$ ) and ( $S_4, S_4', S_5, S_6, S_6'$ ) are operated at LSF. The level matrix can be derived as follow:

$$\mathbf{L}_1(k) = \begin{bmatrix} L_4 & L_3 \text{or} L_4 & L_3 \text{or} L_4 & L_3 \text{or} L_4 \\ L_3 & L_3 & L_3 & \\ L_2 & L_2 & L_2 & \\ L_1 & & & \end{bmatrix} \quad (12)$$

which indicates the converter under this modulation scheme can generate fourth level and third level. However, this scheme could fail under fault conditions. With the three open-circuit switches ( $S_1', S_2', S_4'$ ), (12) should be modified into

$$\mathbf{L}_2(k) = \begin{bmatrix} L_4 & L_4 & L_4 & L_4 \\ L_3 & L_3 & L_3 & \\ L_2 & L_2 & L_2 & \\ L_1 & & & \end{bmatrix} \quad (13)$$

which indicates only the fourth voltage level can be generated.

To guarantee the complete output capability, PWM schemes should have tolerance of open-circuit switches. Based on [15], another PWM pattern can also be implemented:  $S_6$  and  $S_6'$  are modulated to generate the PWM waveforms, while the rest switches are maintained fixed states. The associated level matrix under same open-circuit fault can be derived as follow:

$$\mathbf{L}_3(k) = \begin{bmatrix} L_4 & L_4 & L_4 & L_3 \text{or} L_4 \\ L_3 & L_3 & L_3 & \\ L_2 & L_2 & L_2 & \\ L_1 & & & \end{bmatrix} \quad (14)$$

which demonstrates a complete output capability, and the open-circuit fault will not degrade the output capability. With the help of matrix model  $\mathbf{S}(k)$  and  $\mathbf{L}(k)$ , the same analysis process can also be done for the rest operation zones of the fourth-level ANPC converter, i.e., from first to third voltage levels. And this leads to the PWM pattern that enables HSF ( $S_3, S_3', S_5, S_5', S_6, S_6'$ ), and rest switches are operated at LSF.

## C. Demonstrations of Converter Circuits

To further demonstrate the matrix-based analysis, its circuit diagrams are provided in this section as a supplement.

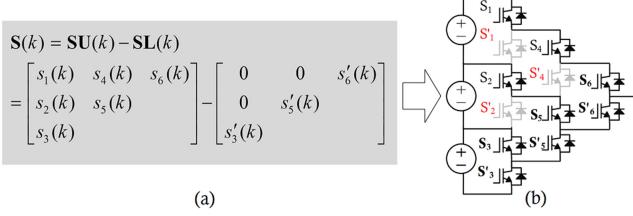


Fig. 9. (a) State matrix of the postfault four-level ANPC topology. (b) Four-level ANPC topology with three open-circuit switches ( $S_1'$ ,  $S_2'$ ,  $S_4'$ ).

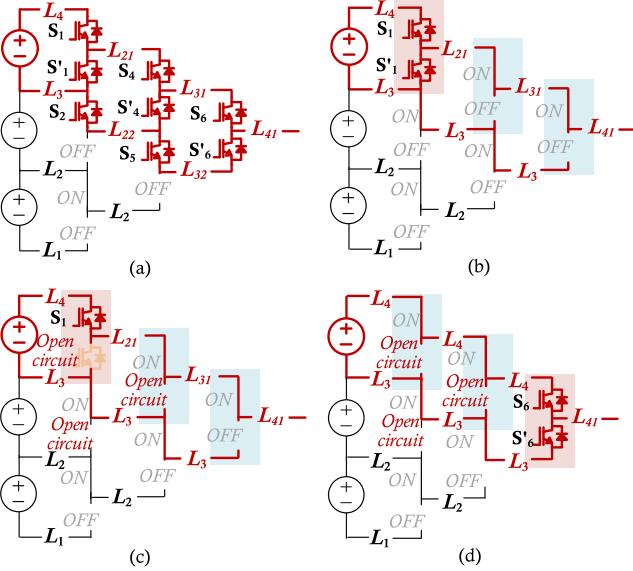


Fig. 10. (a) Available switches for generation of third and fourth voltage levels in four-level ANPC under normal conditions. (b) One possible modulation scheme with  $S_1$ ,  $S_1'$  operating at PWM frequency, other switches are maintained fix states. (c) Implementation of the modulation scheme in (b) with three switches ( $S_1'$ ,  $S_2'$ ,  $S_4'$ ) are open-circuit. (d) Implementation of another modulation scheme with the tolerance of open-circuit switches ( $S_1'$ ,  $S_2'$ ,  $S_4'$ ).

First, the corresponding postfault converter circuit of (11) is shown in Fig. 9(b). The switches associated with the fourth level and third level are displayed in Fig. 10(a). The operation pattern corresponding to (12) is shown as in Fig. 10(b), while Fig. 10(c) shows the faulty condition corresponding to (13). Fig. 10(d) shows another pattern that corresponds to (14).

Then, for the operation zone from second to third voltage level, the operation can follow pattern Fig. 11(a), while the pattern Fig. 11(b) can be used for the operation zone from first to second voltage level.

Combining Fig. 10(d) and Fig. 11(a) and (b), the complete PWM pattern [see Fig. 11(c)] can be obtained with the tolerance of open-circuit switches ( $S_1'$ ,  $S_2'$ ,  $S_4'$ ) during whole operation zones. It can be observed that the proposed matrix-modeling approach provides complete topological descriptions for the ANPC topologies and serves as a more systematic analysis process than the conventional circuit-diagram-based method.

#### IV. SYSTEMATIC PWM DESIGN

For OCFT modulation design, both space-vector-based modulation and carrier-based PWM (CBPWM) can be found in the literature [3], [8], [11], [12], [23]. Due to the inherent scalability

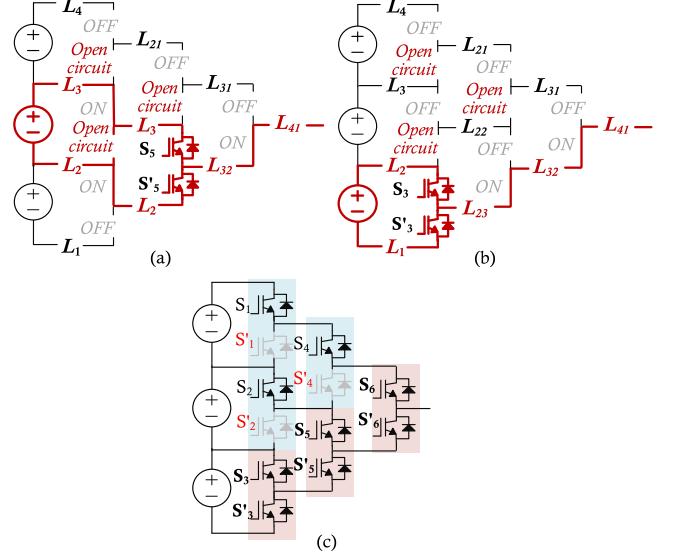


Fig. 11. Postfault four-level ANPC with: (a) implementation of the applicable scheme for generation of second and third voltage levels in, (b) implementation of the applicable scheme for generation of first and second voltage levels, and (c) a PWM pattern that can guarantee a complete output capability.

regarding high-level topologies, CHPWM schemes are getting increasingly research attention recently. For instance, in [5], the reconfiguration of CHPWM was proposed for a five-level capacitor self-voltage balancing inverters to maintain a balanced normal line-to-line voltage under device failures. Another one like in [8], a modified level-shift PWM was proposed for the five-level T-type ANPC converter to endure the single-switch open-circuit faults. However, the systematic OCFT modulation design for high-level ANPC topologies is still not quite clearly covered in the literature.

To systematically address this problem, a four-step process is proposed, as shown in Fig. 12(a), which is based on the authors previous work in [18].

The first step is to derive the vector-form matrix model of ANPC converters, which follows the same way in Section II [the details of the matrix-based modeling and fault-tolerant analysis process are summarized in Fig. 12(b)]. Then,  $s_{ei}$  can be used to find out, which switches contribute to generating a specific output level in  $\mathbf{L}_N = [L_N \dots L_i \dots L_2 \ L_1]^T$ .

In the second step, the faults and PWM patterns are coded. The switching states are defined as a binary variable State in (16). Then, the device fault indicator of open-circuit fault is defined as a binary variable  $Fault_{OC}$  in (17), where the bits regarding open-circuit switches are assigned as “0,” others are set as “1.” Then, the device states with faults can be assigned as in (18). Also, a pattern code is used for each PWM pattern, which can be defined as in (19). If the  $i$ th switching cell is LSF,  $p_i$  is set as “0”; if the cell is HSF,  $p_i$  is set as “1.”

The third step is to select the applicable OCFT PWM patterns. This step is based on logic operations and can be processed in an offline way to form a comprehensive and systematic lookup table of any possible patterns. In detail, a selection code can be defined based on the high/low part of the fault indicator: (20), where  $Fault_H = (f_1 \ f_2 \ f_3 \dots f_i \dots)$ ,  $Fault_L = (f_1' \ f_2' \ f_3' \dots f_i' \dots)$ .

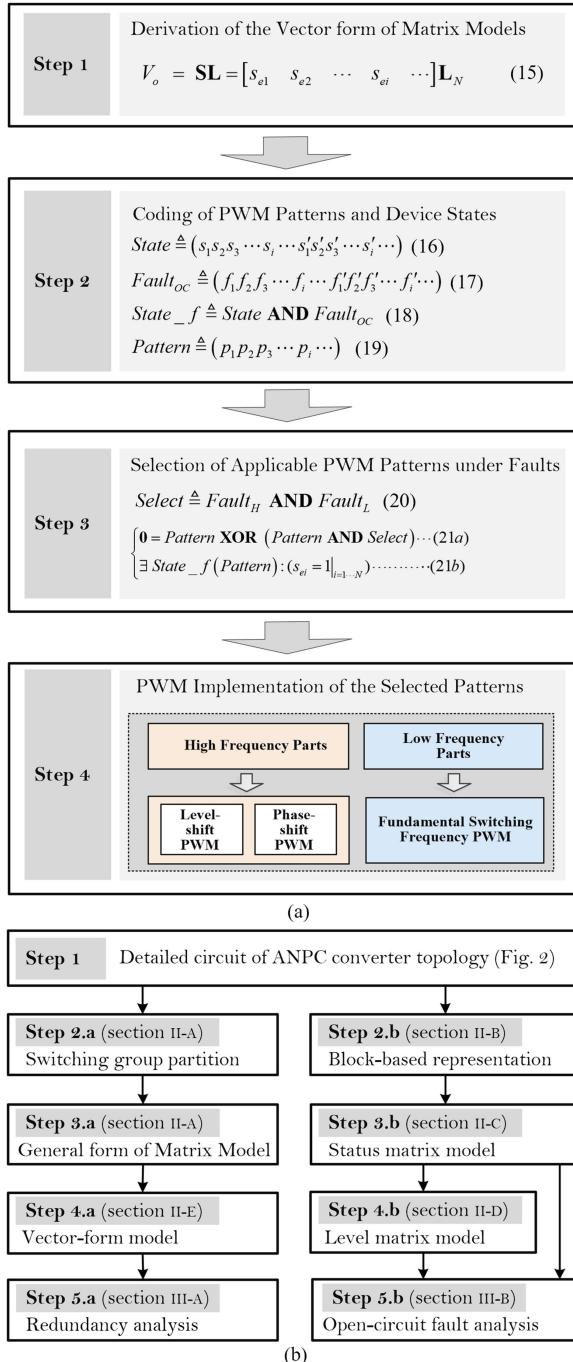


Fig. 12. Flow chart of the proposed: (a) fault tolerant PWM design for ANPC topology based on the matrix method and (b) matrix-based modeling and fault-tolerant analysis process.

And (21) should be met for all of the applicable PWM patterns under faults, where  $\mathbf{0}$  is zero matrix and it is used to check if the Pattern has the fault-condition HSF cell. The bottom equation is to check if variable  $State\_f$  under Pattern can guarantee  $s_{ei}$  equal to “1” for every  $i \in \{1, 2, \dots, N\}$ . If (21) is fulfilled, then, all the voltage levels of the converter can be generated by this pattern.

The fourth step is to implement the chosen patterns for fault-tolerant operation, which can be modularly achieved by using the carrier-based PWM design method. Since all the fault-tolerant

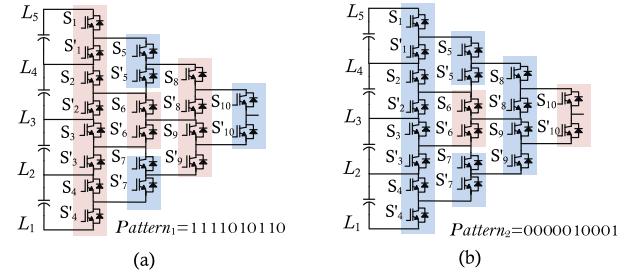


Fig. 13. Two PWM patterns with different arrangements of cells.

carrier-based PWM patterns should be subset of the normal ANPC cases, therefore, the same PWM design method in [15] and [22] is still valid and can be implemented without changes.

The detailed waveforms and examples will be presented in the following case study.

## V. CASE STUDY FOR 5L-ANPC PWM DESIGN

In this section, a case study will be presented and show the implementation of the proposed method for directly finding out the applicable patterns under fault conditions. In particular, the multiswitch open-circuit faults are considered for a five-level ANPC converter [18]. Since its vector form model has been provided in Section II-E, the step 1 of the PWM design will be omitted in this section.

### A. Step-2: Coding for Devices and Patterns

Based on the matrix model, the device states of the five-level case are coded as

State

$$= (s_1 s_2 s_3 s_4 s_5 s_6 s_7 s_8 s_9 s_{10} s'_1 s'_2 s'_3 s'_4 s'_5 s'_6 s'_7 s'_8 s'_9 s'_{10}). \quad (22)$$

And the pattern is coded as

$$Pattern = (p_1 p_2 p_3 p_4 p_5 p_6 p_7 p_8 p_9 p_{10}). \quad (23)$$

Based on [15], there could be over 1000 PWM patterns for the five-level topology, therefore, only two of them are demonstrated as detailed examples here: Pattern<sub>1</sub> [see Fig. 13(a)] and Pattern<sub>2</sub> [see Fig. 13(b)].

Without losing the universality, three multiswitch fault cases are considered here, as shown in Fig. 14(a.1)–(a.3) and (b.1)–(b.3). And these faults can be coded as listed with associated  $State\_f$  in Fig. 14. Case 1 is a two-switch fault, while case 2 and 3 are three-switch faults that could easily lead to very time-consuming workloads with the conventional approach.

### B. Step-3: Selection of Applicable PWM Patterns

The selection codes for case 1–3 should be calculated

$$\begin{aligned} Select_1 &= (1111010111) \\ Select_2 &= (1111010110) \\ Select_3 &= (1111000111). \end{aligned} \quad (24)$$

Then, to find out the eligibility of the patterns, equation (21) is used to check with all the variables (Pattern<sub>1</sub>, Pattern<sub>2</sub>, State \_

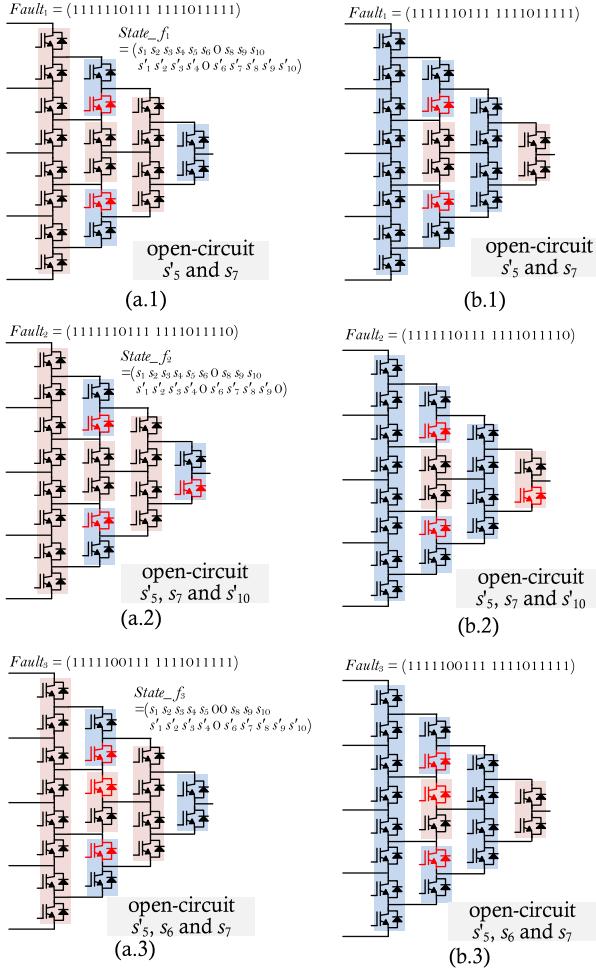


Fig. 14. Three fault cases with multiple open-circuit switches in five-level ANPC topology. (a) Using pattern 1 under (a.1) fault case 1, (a.2) fault case 2, (a.3) fault case 3. (b) Using pattern 2 under (b.1) fault case 1, (b.2) fault case 2, (b.3) fault case 3.

$f_y$ ,  $\text{Select}_y, y = 1, 2, 3$ . Based on the (21a), it can be determined the Pattern<sub>1</sub> is not applicable for fault case 3 and the Pattern<sub>2</sub> is not applicable for fault case 2 and 3. The calculation results can be found in Appendix Table III.

To find out the eligibility of the PWM patterns under fault cases, the (21b) can be utilized. Recall the matrix model (10), under fault conditions, the elements of open-circuit switches can be assigned as “OFF”, i.e., “0”. For example, under fault case 1, the redundancies associated with output levels can be dramatically decreased, and the model will be modified into

$$\left\{ \begin{array}{l} s_{e1}|_{\text{State\_}f_1} = s_{10}s_8s_5s_1 \\ s_{e2}|_{\text{State\_}f_1} = s_{10}s_8s_5s'_1 + s_{10}s'_8s_6s_2 + s'_{10}s_9s_6s_2 \\ s_{e3}|_{\text{State\_}f_1} = s_{10}s'_8s_6s'_2 + s_{10}s'_8s'_6s_3 + s'_{10}s_9s_6s'_2 \\ \quad + s'_{10}s_9s'_6s_3 \\ s_{e4}|_{\text{State\_}f_1} = s_{10}s'_8s'_6s'_3 + s'_{10}s_9s'_6s'_3 + s'_{10}s'_9s'_7s_4 \\ s_{e5}|_{\text{State\_}f_1} = s'_{10}s'_9s'_7s'_4. \end{array} \right. \quad (25)$$

In (25),  $s_{e3}|_{\text{state\_}f_1}$  is consisted of the sum of four terms, resulting in 16 states for generating the third level, as shown in Fig. 15(in normal-condition, there are 96 states for  $s_{e3}|_{\text{state\_}f_1} = 1$ ).

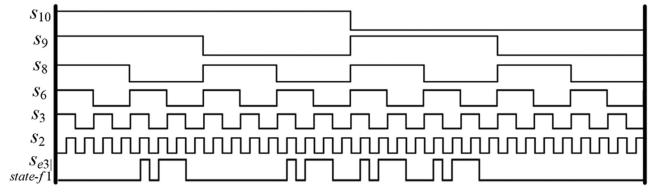


Fig. 15. Timing diagram of the binary code values of  $s_{e3}|_{\text{state\_}f_1}$  (the third level) in (25) by exhaustive investigation of associated states in fault-condition five-level topology. High level means value “1”, low level means value “0”.

With Pattern<sub>1</sub> under fault case 1, (21b) can be satisfied if switches ( $s_5, s_{10}$ ) in LSF cells are assigned as “11” during [ $L_5, L_4$ ]. Similarly, it can be seen that the rest regions can also satisfy (21b). Therefore, Pattern<sub>1</sub> is applicable under fault case 1. Based on the same approach, Pattern<sub>2</sub> is not applicable. The results of the examination are summarized in Appendix Table IV. Based on the proposed logic process, both patterns can be used for case 1 fault but cannot be applied for case 2 and case 3 faults in theory. It is possible to exhaustively investigated more switch fault cases in five-level or other ANPC topologies based on the same methodology and here we omitted and left for readers.

### C. Step-4: PWM Implementation

With pattern selected, carrier-based PWM for the normal five-level ANPC can be directly implemented, which can be modularly designed based on [15], [22], e.g., the level-shift PWM. Four carriers should be used in the comparisons with modulation reference, and then, the resulting logics are assigned to different HSF/LSF cells based on the utilized pattern. In detail, the modulation logic of Pattern<sub>1</sub> can be demonstrated, as in Fig. 16(a) [18]. The PWM generation algorithm does not need to be changed with or without the faults, therefore, its applicability under faults could be verified. Similarly, the modulation logic of Pattern<sub>2</sub> can be determined, as in Fig. 16(b) based on [18].

## VI. EXPERIMENTAL VERIFICATIONS

To further verify the proposed method, the OCFT operation of the five-level ANPC converter is experimentally validated. In the experiment, case 1–3 open-circuit faults with Pattern<sub>1</sub> and Pattern<sub>2</sub> are carried out in the single-phase platform shown in Fig. 17 [18]. Since the fault diagnosis is not the focus of this article, all device faults are predetermined and assumed to be detected by means of the fault detection functions integrated in the industrial gate drivers [21], such as the desaturation protections. The fault-tolerant operations are realized through latching the error signals of faulty devices and overwriting the original modulation signals with “OFF” signal from the controller side so that these devices will act like in open-circuit conditions. To monitor the status of the switches, six channels of the scope are used for ( $s_4$ ,  $s'_5$ ,  $s_6$ ,  $s_7$ ,  $s_8$ ,  $s_{10}$ ), while one channel is for output PWM pulses, one is for the load current. In practice, the freewheeling operation is quite important for this type of converters and could also be affected by the open-circuit faults. In our study, when the IGBT is faulty, if we assume the diode

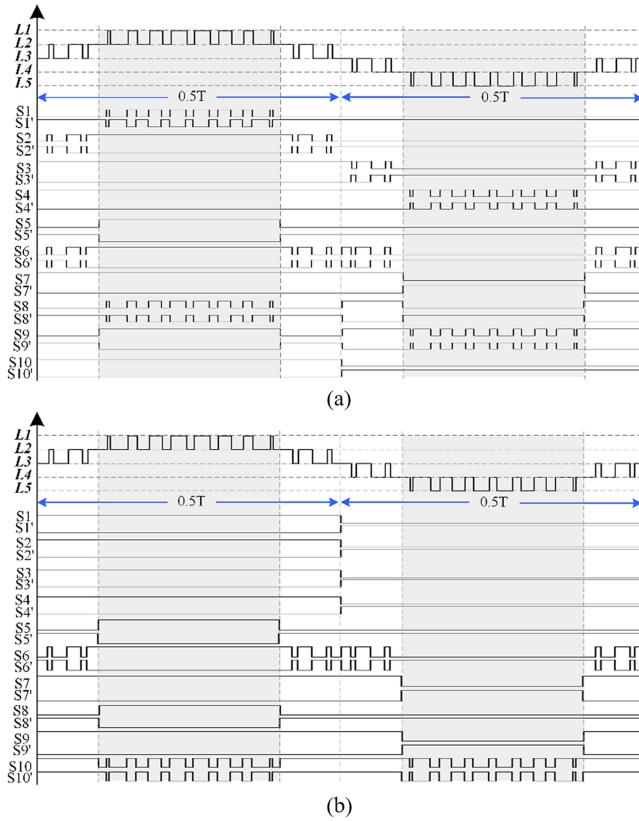


Fig. 16. PWM schemes for studied PWM pattern examples for (a) Pattern<sub>1</sub>, (b) Pattern<sub>2</sub>. (a) Detailed diagram of the PWM scheme designed for Pattern<sub>1</sub>. (b) Detailed diagram of the PWM scheme designed for Pattern<sub>2</sub>.

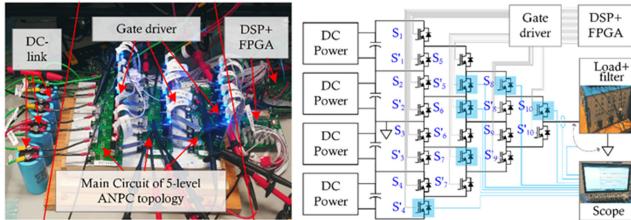


Fig. 17. Single-phase five-level experimental platform with the line frequency 60 Hz, while the carrier/switching frequency is 1560 Hz. The dc links of the converter are clamped by the dc power supply, and the total voltage is 120 V. The RL load is chosen with value: 55 ohm/30 mH.

is still working, then, the converter freewheeling mode would have no difference compared to prefault condition [24]. If the diode is not working, then, the converter will work just exactly like the simplified ANPC converter (certain switches are eliminated from the original converter). In this way, the converter will lose some redundant current paths, but can still work properly.

#### A. Case 1: Device Open-Circuit Faults of ( $s'_5, s_7$ )

Based on the work in [15], each pattern utilizes device differently during the operation regions and different device utilizations result in different fault-tolerant features. Taking Pattern<sub>1</sub> as an example its device utilizations are demonstrated in Fig. 18(a.1)–(a.4). As can be seen in Fig. 18(a.1)–(a.4) with fault case 1, the device open-circuit faults can be tolerated by

applying the PWM Pattern<sub>1</sub>. In theory, the current paths of the converter are not blocked, therefore, the output waveforms will not be affected during the four operation regions. Similar observation can be found with Pattern<sub>2</sub> as well, as shown in Fig. 18(b.1)–(b.4). The experimental results in Fig. 19 are showing the same fact: both the patterns can tolerate the fault case 1 and guarantee the output performance as in normal operating conditions.

#### B. Case 2: Device Open-Circuit Faults of ( $s'_5, s_7, s'_10$ )

With fault case 2 using Pattern<sub>1</sub>, the open-circuit faults can impact the current paths during the region [L4, L3] [see Fig. 20(a.2)] and [L2, L1] [see Fig. 20(a.4)], therefore, cannot ensure the output quality. The situation is different for Pattern<sub>2</sub>, and the open-circuit faults of ( $s'_5, s_7, s'_10$ ) will interfere with the high-frequency cells during the region [L5, L4] [see Fig. 20(b.1)] and [L2, L1] [see Fig. 20(b.4)], therefore, cannot be utilized during the fault case 2. The experimental results in Fig. 21 verify the above analysis: two patterns cannot maintain the same output performance as prefault in fault case 2. Obvious distortions can be observed in the output voltage and load current waveforms. Note that the converter can still generate correct waveforms in [L4, L3] with Pattern<sub>1</sub> under fault case 2 if the output current is positive and compatible with the conducting direction of the antiparallel diode of the fault switch ( $s'_10$ ). Due to the half-cycle symmetry in ANPC topologies, the output current could be negative in the [L3, L2] and/or [L2, L1]. And distortions can be caused when the antiparallel diode of the fault switch ( $s'_10$ ) blocks the current, as shown in Fig. 21(a).

#### C. Case 3: Device Open-Circuit Faults of ( $s'_5, s_6, s_7$ )

As for fault case 3, the open-circuit faults will block the current paths during the region [L5, L4] for both patterns, as shown in Fig. 22(a.1) and (b.1). In addition, it is easy to see that the open-circuit faults of ( $s'_5, s_6, s_7$ ) will interfere the high-frequency cells in both patterns. The disturbed operation regions are [L4, L3] [see Fig. 22(a.2) and (b.2)] and [L3, L2] [see Fig. 22(a.3) and (b.3)]. Therefore, the intended operation cannot be achieved. The experimental results in Fig. 23 verify this: obvious distortions can be seen in the output voltage and load current waveforms in both patterns, which matches the analysis. These cases validate the importance of the proposed approach—properly predict the behaviors of converters systematically so that the tolerable faults and intolerable can be identified during the design procedure.

#### D. Different Operation Conditions

The fault-tolerant operation of 5L ANPC topology under different modulation indexes and load changes are also provided here to further demonstrate the feasibility of the selected PWM schemes. Fig. 24 shows that the applicable OCFT PWM scheme (pattern 2) can achieve normal output performance from low to high modulation index (0.3, 0.6, and 0.9) with multiple open-circuit faults ( $s'_5, s_7$ ). The load changes can also be handled well (e.g., from 55 ohm/30 mH to 27.5 ohm/30 mH). This is because

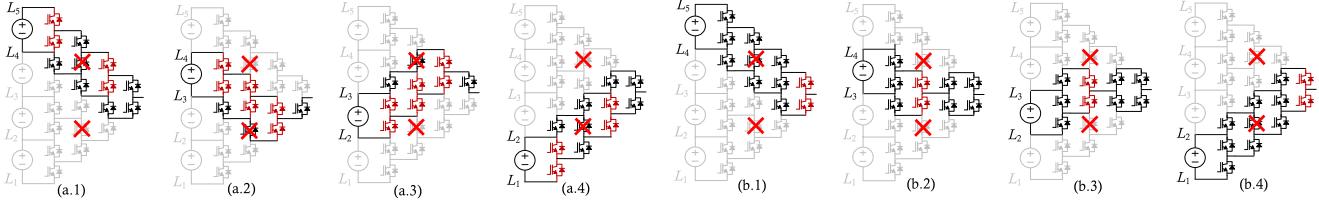


Fig. 18. Fault case 1 with multiple open-circuit switches ( $s'_5, s_7$ ) in five-level ANPC topology: (a.1)–(a.4) using Pattern 1, (b.1)–(b.4) using Pattern 2. From left to right are the utilized switches during four operation regions covering all output levels, e.g., (a.1) is for  $[L_5, L_4]$ , (a.2) is for  $[L_4, L_3]$ , (a.3) is for  $[L_3, L_2]$ , (a.4) is for  $[L_2, L_1]$ .

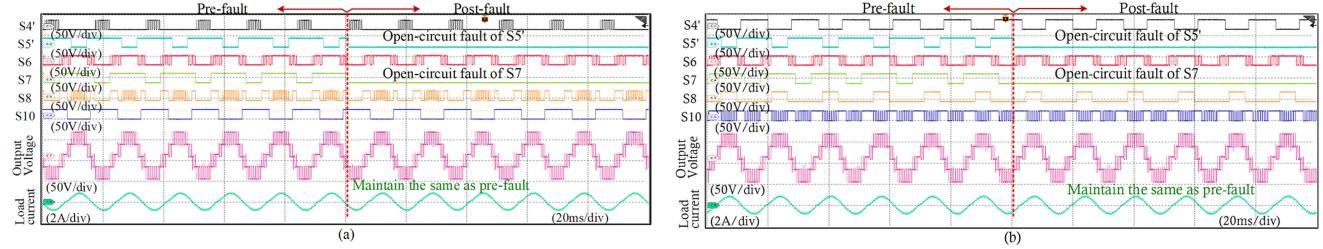


Fig. 19. Experimental results of 5L ANPC topology before and after open-circuit faults with implemented carrier-based PWM scheme under fault case 1 with (a) Pattern 1, (b) Pattern 2. Waveforms from top to bottom: switching states of  $s'_4, s'_5, s_6, s_7, s_8, s_{10}$ , the output PWM voltage, the load current.

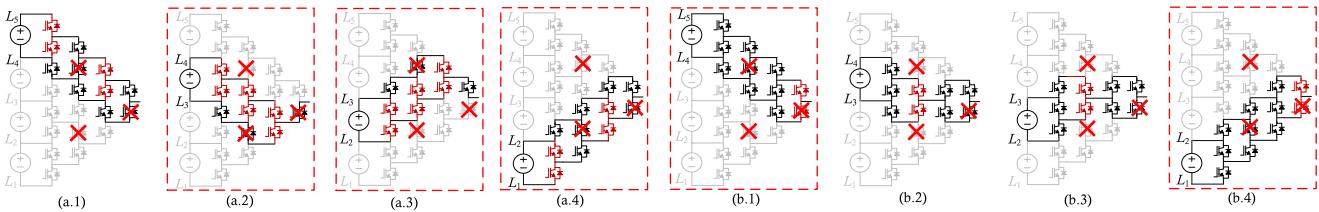


Fig. 20. Fault case 2 with multiple open-circuit switches ( $s'_5, s_7, s'_{10}$ ) in five-level ANPC topology. (a.1)–(a.4) using Pattern 1, (b.1)–(b.4) using Pattern 2. From left to right are the utilized switches during four operation regions covering all output levels, e.g., (a.1) is for  $[L_5, L_4]$ , (a.2) is for  $[L_4, L_3]$ , (a.3) is for  $[L_3, L_2]$ , (a.4) is for  $[L_2, L_1]$ .

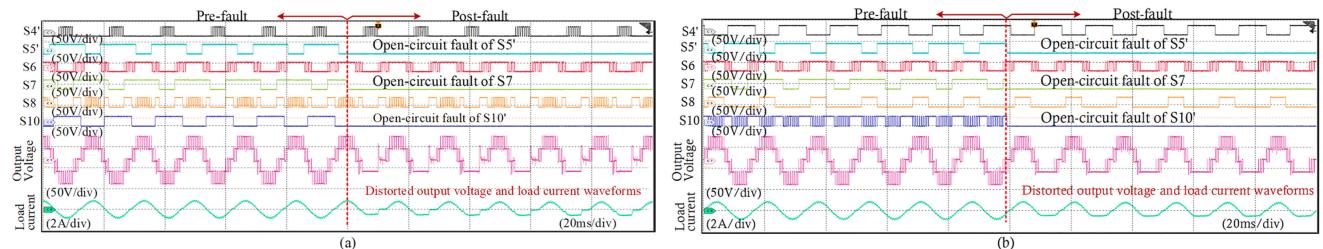


Fig. 21. Experimental results of 5L ANPC topology before and after open-circuit faults with implemented carrier-based PWM scheme under fault case 2 with (a) Pattern 1, (b) Pattern 2. Waveforms from top to bottom: switching states of  $s'_4, s'_5, s_6, s_7, s_8, s_{10}$ , the output PWM voltage, the load current.

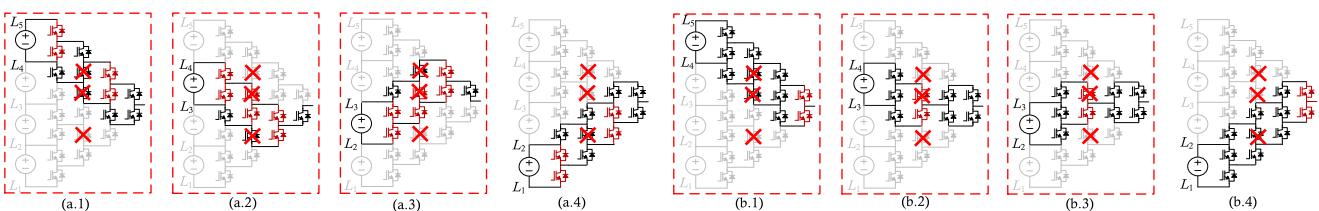


Fig. 22. Fault case 3 with multiple open-circuit switches ( $s'_5, s_7, s'_{10}$ ) in 5-level ANPC topology. (a.1)–(a.4) using Pattern 1, (b.1)–(b.4) using Pattern 2. From left to right are the utilized switches during four operation regions covering all output levels, e.g., (a.1) is for  $[L_5, L_4]$ , (a.2) is for  $[L_4, L_3]$ , (a.3) is for  $[L_3, L_2]$ , (a.4) is for  $[L_2, L_1]$ .

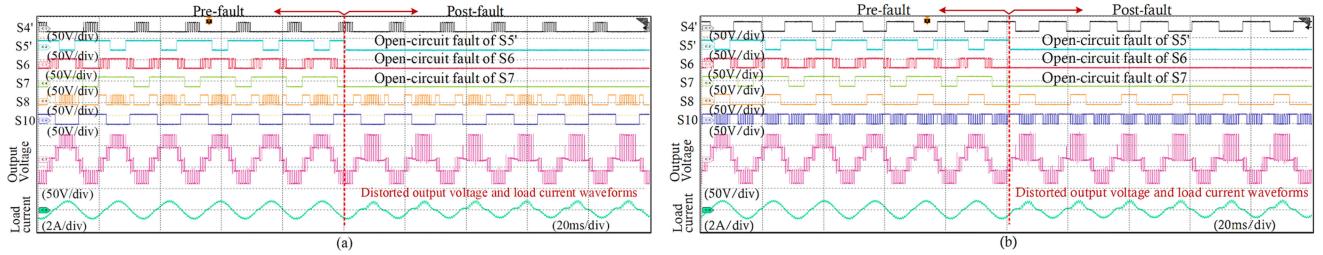


Fig. 23. Experimental results of 5L ANPC topology before and after open-circuit faults with implemented carrier-based PWM scheme under fault case 3 with (a) Pattern 1, (b) Pattern 2. Waveforms from top to bottom: switching states of  $s_4'$ ,  $s_5'$ ,  $s_6$ ,  $s_7$ ,  $s_8$ ,  $s_{10}$ , the output PWM voltage, the load current.

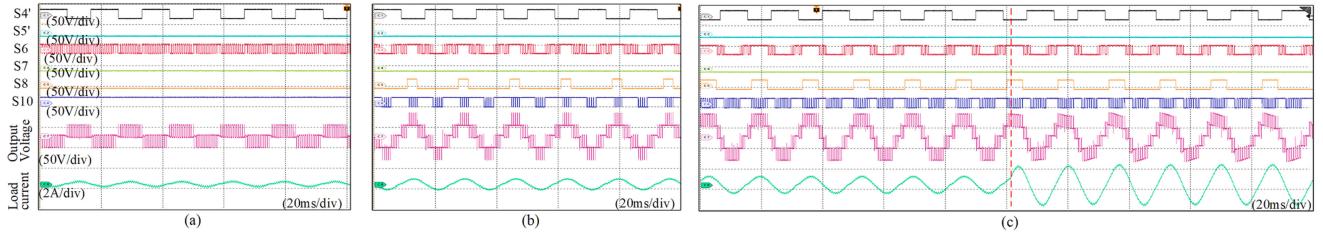


Fig. 24. Experimental results of fault-tolerant operation (fault case 1) of 5L ANPC topology (PWM Pattern 2) under different modulation indexes and load changes. (a) Modulation index is 0.3. (b) Modulation index is 0.6. (c) Modulation index is 0.9 and load changes from 55 ohm/30 mH to 27.5 ohm/30 mH.

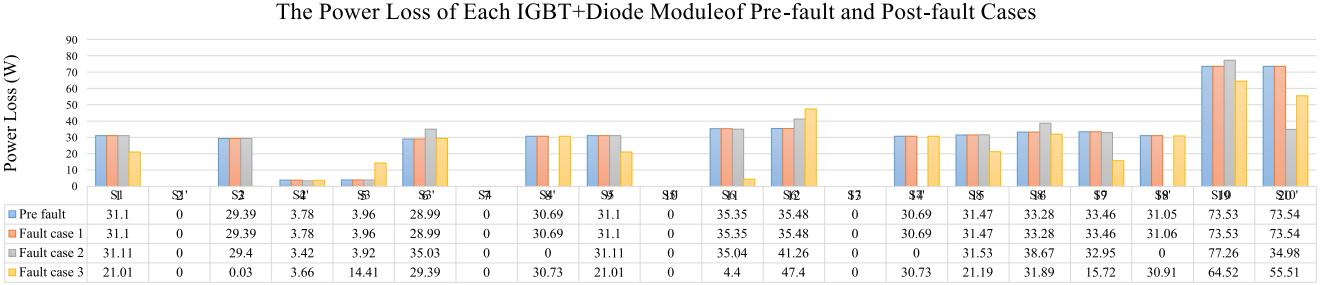


Fig. 25. Power loss distributions of prefault and fault case 1–3 conditions in five-level ANPC converter with PWM pattern 2. (The simulation is done through PLECS tools in MATLAB/Simulink with 1200 V 150 A IGBT, i.e., Infineon DF150R12RT4, at 1560 Hz switching frequency, 0.9 modulation index, 2.4 kV dc-link voltage, 140 A load peak current. Here, we assume all the diodes are in good condition.).

the converter is maintained the same full-range operation capability. The introduced fluctuation of PWM pulses is mainly because of the increased power consumption in single-phase systems [25].

The power loss analysis of the five-level ANPC converter under different conditions is also provided. Fig. 25 shows the details of how different faults result in different power losses on each device. It can be observed that those switches not utilized in prefault conditions will not be used in postfault cases as well. However, for PWM pattern 2, fault case 2 and 3 will alter the current paths of the rest switches, therefore, leading to different loss distributions. For applicable PWM patterns, the same level of losses will be expected since the same switches with the same gating signals based on the same PWM schemes are utilized before and post the faults.

In summary, the experimental results of three fault cases show some promising features as follows:

- 1) the design process is a logic-based offline process and maintained with a relatively low complexity;
- 2) the inherent fault-tolerant capability of a five-level ANPC converter can be guaranteed through the proposed method;
- 3) multiswitch open-circuit faults can be easily dealt with by implementing suitable CB-PWM schemes;
- 4) if the PWM pattern is applicable for the fault case, then, the power losses and the associated loss distributions will be maintained as prefault.

## VII. DISCUSSIONS AND GENERALIZATIONS

In addition to the general forms of ANPC converters, the proposed OCFT analysis and PWM design method can potentially be generalized for other ANPC-based topologies, i.e., the simplified ANPC topologies with fewer switches, or

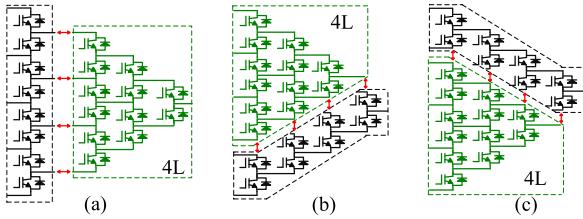


Fig. 26. Decompositions of five-level ANPC topology into a four-level subtopology and the complementary circuit. (a) Vertical decomposition. (b) Upper decomposition. (c) Lower decomposition.

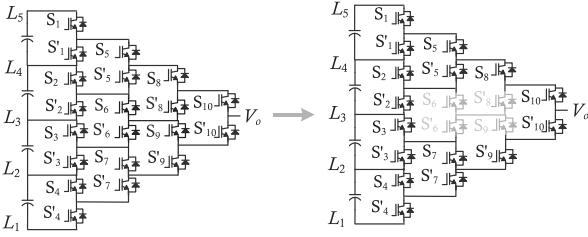


Fig. 27. Simplified ANPC converter is derived from the general form of five-level ANPC topology.

hybrid-clamped multilevel converters that are derived from the basic ANPC topologies.

#### A. Generalization for Higher-Level ANPC Converters

Same as the methods in [15], a hierarchical decomposition concept can be implemented to facilitate the PWM design of post-fault higher-level topologies. For instance, a five-level ANPC topology can be vertically decomposed into a four-level subtopology and the complementary circuit [see Fig. 26(a)]. It can also be decomposed in an upper/lower way, as shown in Fig. 26(b) and (c). And all the operation features (e.g., PWM patterns, modulation schemes, and device faults) of the four-level ANPC converter can be preserved in the four-level subtopology. Meanwhile, the compatible PWM pattern for the complementary circuit can also be chosen. Therefore, only the complementary circuit needs to be considered since the four-level part is kept the same.

#### B. Generalization for Simplified ANPC Converters

The proposed OCFT analysis and PWM design method can be straightforwardly implemented for the simplified ANPC converters by simply assigning certain elements in the matrix models as fixed constant values [16].

For instance, one can derive the simplified five-level ANPC converter by deleting four redundant switches:  $s_6$ ,  $s_6'$ ,  $s_8$ ',  $s_9$ ' of the general topology (see Fig. 27). To analyze the fault-tolerant capability of this simplified topology, the matrix models of the general ANPC topology can still be used, but with the four elements associated with  $s_6$ ,  $s_6'$ ,  $s_8$ ',  $s_9$  in the status matrix assigned as "0". Similarly, the vector form model of general topology can be further modified accordingly. And the database

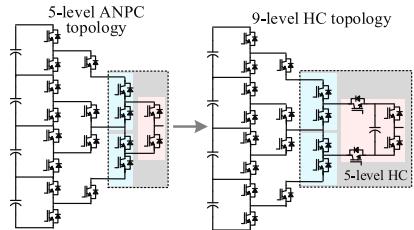


Fig. 28. Hybrid-clamped nine-level converter derived from the five-level HC topology.

of all applicable PWM patterns of this simplified topology can be considered as the subset of the general cases.

#### C. Generalization for Hybrid-Clamped Converters

Many hybrid-clamped multilevel converters can be considered as the extension of the general form of ANPC topologies. Therefore, the analysis and PWM design presented here can also be extended for those topologies.

For instance, by extending the front-end three-level subtopology into the well-studied five-level hybrid-clamped converter [10], the hybrid-clamped nine-level converter can be derived from a simplified five-level ANPC converter [16], [22]. And the flying-capacitor bridge should be operated at PWM frequency. In turn, the original five-level ANPC converter should be operated with an HSF switching cell at its front-end (highlighted as red background in Fig. 28). Therefore, it is easy to conclude that this hybrid-clamped nine-level converter shares the same OCFT-applicable PWM pattern of a simplified five-level ANPC converter, and thus, forms a subset of the general case.

## VIII. CONCLUSION

In this article, the matrix-model approach is proposed for the OCFT analysis and PWM design for ANPC topologies. By implementing the specialized matrix models, the redundancy of the topology can be explored exhaustively. After the systematic coding and calculation, the applicable PWM patterns of an arbitrary ANPC topology with multiple fault switches can be identified. In such a way, the PWM pattern database can be predesigned and directly implemented for postfault operation. Therefore, random enumeration and nonsystematic case-by-case design can be avoided for ANPC converters. Without losing the generality, the four-level and four-level ANPC with multiple fault switches are investigated. The experimental results of the five-level case show that the output levels can be appropriately produced with the selected applicable PWM pattern, especially under multiple switch open-circuit faults. The proposed OCFT approach and PWM design method are not limited to a general form of ANPC converters but have the potentials to be applied for other derivatives of the general ANPC converters. In the future, we would like to further extend the matrix-based method for short circuit analysis and fault-tolerant operation design, which is another great challenge faced by multilevel converters.

## APPENDIX

TABLE II  
CRITICAL LEVEL OF DIFFERENT SWITCHES OF FIVE-LEVEL ANPC CONVERTER  
BY VECTOR-FORM MODEL

	$L_5$	$L_4$	$L_3$	$L_2$	$L_1$
$S_1$	1				
$S'_1$		1/4			
$S_2$		3/4			
$S'_2$			3/6		
$S_3$			3/6		
$S'_3$				3/4	
$S_4$				1/4	
$S'_4$					1
$S_5$	1	1/4			
$S'_5$		1/4	1/6		
$S_6$		2/4	2/6		
$S'_6$			2/6	2/4	
$S_7$			1/6	1/4	
$S'_7$				1/4	1
$S_8$	1	2/4	1/6		
$S'_8$		1/4	2/6	1/4	
$S_9$		1/4	2/6	1/4	
$S'_9$			1/6	2/4	1
$S_{10}$	1	3/4	3/6	1/4	
$S'_{10}$		1/4	3/6	3/4	1

TABLE III  
ELIGIBILITY OF THE PATTERNS THROUGH (21A)

$Pattern_x \text{ XOR } (Pattern_x \text{ AND } Select_y)$	$Select_1$	$Select_2$	$Select_3$
$Pattern_1=1111010110$	00000	00000	00000
	00000	00000	10000
$Pattern_2=0000010001$	00000	00000	00000
	00000	00001	10000

TABLE IV  
SUMMARY OF VARIOUS PWM PATTERNS

Codes	Applicable or Not?			
<b>Case 1</b> $Fault_1 = (111110111111101111)$ open-circuit $s'_5$ and $s_7$				
$State\_f_1 = (s_1 s_2 s_3 s_4 s_5 s_6 0 s_8 s_9 s_{10} s'_1 s'_2 s'_3 s'_4 0 s'_6 s'_7 s'_8 s'_9 s'_{10})$				
$Pattern_1$	1111010110	Applicable		
$Pattern_2$	0000010001	Applicable		
<b>Case 2</b> $Fault_2 = (111110111111101110)$ open-circuit $s'_5$ , $s_7$ and $s'_{10}$				
$State\_f_2 = (s_1 s_2 s_3 s_4 s_5 s_6 0 s_8 s_9 s_{10} s'_1 s'_2 s'_3 s'_4 0 s'_6 s'_7 s'_8 s'_9 0)$				
$Pattern_1$	1111010110	Not applicable, cannot make sure $s_{ei}$ equal to "1" for every $i \in \{1, 2, \dots, N\}$ .		
$Pattern_2$	0000010001	Not applicable, fault switches will affect the operation of the HSF cells		
<b>Case 3</b> $Fault_3 = (111110011111101111)$ open-circuit $s'_5$ , $s_6$ and $s_7$				
$State\_f_3 = (s_1 s_2 s_3 s_4 s_5 00 s_8 s_9 s_{10} s'_1 s'_2 s'_3 s'_4 0 s'_6 s'_7 s'_8 s'_9 s'_{10})$				
$Pattern_1$	1111010110	Not applicable, fault switches will affect the operation of the HSF cells		
$Pattern_2$	0000010001			

## REFERENCES

- [1] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014, doi: [10.1109/TPEL.2014.2304561](https://doi.org/10.1109/TPEL.2014.2304561).

- [2] U. Choi, F. Blaabjerg, and K. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517–2533, May 2015, doi: [10.1109/TPEL.2014.2373390](https://doi.org/10.1109/TPEL.2014.2373390).
- [3] B. Mirafzal, "Survey of fault-tolerance techniques for three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5192–5202, Oct. 2014, doi: [10.1109/TIE.2014.2301712](https://doi.org/10.1109/TIE.2014.2301712).
- [4] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010, doi: [10.1109/TIE.2009.2032430](https://doi.org/10.1109/TIE.2009.2032430).
- [5] J. Li, A. Q. Huang, Z. Liang, and S. Bhattacharya, "Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 519–533, Feb. 2012, doi: [10.1109/TPEL.2011.2143430](https://doi.org/10.1109/TPEL.2011.2143430).
- [6] J. Nicolas-Apruzzese, S. Busquets-Monge, J. Bordonau, S. Alepu, and A. Calle-Prado, "Analysis of the fault-tolerance capacity of the multilevel active-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4773–4783, Nov. 2013, doi: [10.1109/TIE.2012.2222856](https://doi.org/10.1109/TIE.2012.2222856).
- [7] R. Katebi, J. He, and N. Weise, "Investigation of fault-tolerant capabilities in an advanced three-level active T-Type converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 446–457, Mar. 2019, doi: [10.1109/JESTPE.2018.2834367](https://doi.org/10.1109/JESTPE.2018.2834367).
- [8] P. Azer, S. Ouni, and M. Narimani, "A novel fault-tolerant technique for active-neutral-point-clamped inverter using carrier-based PWM," *IEEE Trans. Ind. Electron.*, vol. 67, no. 3, pp. 1792–1803, Mar. 2020, doi: [10.1109/TIE.2019.2903764](https://doi.org/10.1109/TIE.2019.2903764).
- [9] S. Busquets-Monge, R. Rafiezadeh, S. Alepu, A. Filba-Martinez, and J. Nicolas-Apruzzese, "Fast reliability assessment of neutral-point-clamped topologies through markov models," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13449–13459, Dec. 2021, doi: [10.1109/TPEL.2021.3087446](https://doi.org/10.1109/TPEL.2021.3087446).
- [10] M. T. Fard and J. He, "Fault tolerant five-level active NPC inverter for high-reliability photovoltaic applications," in *Proc. IEEE 13th Int. Symp. Diagnostics Elect. Mach., Power Electron. Drives*, 2021, vol. 1, pp. 395–400, doi: [10.1109/SDEMPED51010.2021.9605497](https://doi.org/10.1109/SDEMPED51010.2021.9605497).
- [11] L. M. Halabi, I. M. Alsofyani, and K. B. Lee, "Multi open-/short-circuit fault-tolerance using modified SVM technique for three-level HANPC converters," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13621–13633, Dec. 2021, doi: [10.1109/TPEL.2021.3086445](https://doi.org/10.1109/TPEL.2021.3086445).
- [12] S. Xu, Z. Sun, C. Yao, K. Liu, and G. Ma, "Open-Switch fault-tolerant operation of T-Type active neutral-point-clamped converter using level-shifted PWM," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 7, pp. 2598–2602, Jul. 2021, doi: [10.1109/TCSII.2021.3061483](https://doi.org/10.1109/TCSII.2021.3061483).
- [13] S. Ceballos, J. Pou, E. Robles, J. Zaragoza, and J. L. Martin, "Performance evaluation of fault-tolerant neutral-point-clamped converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2709–2718, Aug. 2010, doi: [10.1109/TIE.2009.2026710](https://doi.org/10.1109/TIE.2009.2026710).
- [14] M. Ma, L. Hu, A. Chen, and X. He, "Reconfiguration of carrier-based modulation strategy for fault tolerant multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2050–2060, Sep. 2007, doi: [10.1109/TPEL.2007.904249](https://doi.org/10.1109/TPEL.2007.904249).
- [15] Y. Li, Y. W. Li, H. Tian, N. R. Zargari, and Z. Cheng, "A modular design approach to provide exhaustive carrier-based PWM patterns for multilevel ANPC converters," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5032–5044, Sep./Oct. 2019, doi: [10.1109/TIA.2019.2928240](https://doi.org/10.1109/TIA.2019.2928240).
- [16] Y. Li, H. Tian, and Y. W. Li, "Systematic derivation of simplified active-neutral-point-clamped multilevel converter through matrix models," in *Proc. IEEE 20th Workshop Control Model. Power Electron.*, 2019, pp. 1–8, doi: [10.1109/COMPTEL.2019.8769693](https://doi.org/10.1109/COMPTEL.2019.8769693).
- [17] Y. Li, Y. W. Li, and Z. Quan, "Systematic synthesis and derivation of multilevel converters using common topological structures with unified matrix models," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5639–5659, Jun. 2020, doi: [10.1109/TPEL.2019.2948580](https://doi.org/10.1109/TPEL.2019.2948580).
- [18] Y. Li, "Systematic topology derivation and PWM design of multilevel converters," Doctoral dissertation, Dept. Elect. Comput. Eng., Univ. of Alberta, Edmonton, Canada, 2021.
- [19] S. Kim et al., "An intelligent gate driver with Self-diagnosis and prognosis for SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5422–5426, doi: [10.1109/ECCE47101.2021.9595991](https://doi.org/10.1109/ECCE47101.2021.9595991).
- [20] C. Lihua, F. Z. Peng, and C. Dong, "A smart gate drive with self-diagnosis for power MOSFETs and IGBTs," in *Proc. IEEE 23rd Annu. Appl. Power Electron. Conf. Expo.*, 2008, pp. 1602–1607, doi: [10.1109/APEC.2008.4522939](https://doi.org/10.1109/APEC.2008.4522939).
- [21] P. Lezana, J. Pou, T. A. Meynard, J. Rodriguez, S. Ceballos, and F. Richardieu, "Survey on fault operation on multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2207–2218, Jul. 2010, doi: [10.1109/TIE.2009.2032194](https://doi.org/10.1109/TIE.2009.2032194).

- [22] Y. Li, H. Tian, and Y. W. Li, "Generalized phase-shift PWM for active-neutral-point-clamped multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9048–9058, Nov. 2020, doi: [10.1109/TIE.2019.2956372](https://doi.org/10.1109/TIE.2019.2956372).
- [23] B. Guan and Z. Liu, "Hybrid modulation strategy with neutral point potential balance of T-Type three-level converter under switch open-circuit fault," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 10797–10806, Nov. 2022, doi: [10.1109/TIE.2021.3120477](https://doi.org/10.1109/TIE.2021.3120477).
- [24] J. Nicolás-Apruzzese, S. Busquets-Monge, and J. Bordonau, "Design issues of the multilevel active-clamped converter," in *Proc. IEEE 37th Annu. Conf. Ind. Electron. Soc.*, 2011, pp. 4409–4414, doi: [10.1109/IECON.2011.6120034](https://doi.org/10.1109/IECON.2011.6120034).
- [25] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.



**Yuzhuo Li** (Member, IEEE) received the B.S. and M.S. degrees in control science and engineering from Shandong University, Jinan, China, in 2012 and 2015, respectively, and the Ph.D. degree in energy system from the University of Alberta, Edmonton, Canada, in 2021.

He is currently a Postdoctoral Fellow with the University of Alberta. His main research interests include systematic power converter topology derivation and PWM design.



**Hao Tian** (Member, IEEE) received the B.S. and M.Eng. degrees in electrical engineering from Shandong University, Jinan, China, in 2011 and 2014, respectively, and the Ph.D. degree in energy system from the University of Alberta, Edmonton, Canada, in 2019.

Since 2019, he has been a Postdoctoral Research Fellow with the University of Alberta. His research interests include multilevel topology and PWM, high-power converter control, and power quality of hybrid ac–dc microgrid.



**Yunwei Ryan Li** (Fellow, IEEE) received the B.Sc. degree in electrical engineering from Tianjin University, Tianjin, China, in 2002, and the Ph.D. degree in power electronics from Nanyang Technological University, Singapore, in 2006.

In 2005, he was a Visiting Scholar with Aalborg University, Denmark. From 2006 to 2007, he was a Postdoctoral Research Fellow with Ryerson University, Canada. In 2007, he was with Rockwell Automation Canada before he joined University of Alberta, Canada in the same year. Since then, he has been with University of Alberta, where he is a Professor and Acting Department Chair currently. His research interests include distributed generation, microgrid, renewable energy, high power converters, and electric motor drives.

Dr. Li serves as an Editor-in-Chief for IEEE Transactions on Power Electronics Letters. Prior to that, he was Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON SMART GRID, and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He was the General Chair of *IEEE Energy Conversion Congress of Exposition* in 2020. He is the AdCom Member at Large for *IEEE Power Electronics Society* (PELS) 2021–2023. He received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from IEEE PELS in 2013. He is recognized as a Highly Cited Researcher by the Web of Science Group.