Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM

Wenchao Song, *Student Member, IEEE*, and Alex Q. Huang, *Fellow, IEEE*

***Abstract*—Cascaded H-bridge multilevel converter (CHMC) is a promising topology for flexible ac transmission systems such as static synchronous compensator (STATCOM) applications. Attention was drawn to the issue of converter reliability due to the large number of power devices used in CHMC applications. This paper proposed an effective fault-tolerant strategy by using H-bridge building block (HBBB) redundancy in CHMC-based STATCOM. The operating principle and the control strategy of the fault tolerance are proposed and discussed. The controller design consideration for the fault-tolerant STATCOM is presented. The proposed fault-tolerant control strategy is implemented on a seven-level CHMC-based STATCOM simulation platform and a five-level CHMC-based STATCOM hardware prototype. Simulation and experimental results are illustrated to verify the feasibility of the proposed fault-tolerant design with the HBBB redundancy.**

***Index Terms*—Cascaded H-bridge multilevel converter (CHMC), fault tolerance, flexible ac transmission systems (FACTS), H-bridge building block (HBBB) and redundancy, static synchronous compensator (STATCOM).**

I. Introduction

STATIC SYNCHRONOUS COMPENSATOR (STATCOM) is a popular flexible ac transmission systems (FACTS) controller for the power system to support the voltage, increase the transmission capability, enhance the voltage stability, and improve the transient stability by injecting/absorbing the reactive power to/from the power system [1]. Recently, the cascaded H-bridge multilevel converter (CHMC) has become an increasingly attractive converter topology for STATCOM applications due to its simple structure and modularity. The CHMC requires the fewest numbers of components among all multilevel converter topologies. The modularized design of H-bridge building block (HBBB) makes it much easier to implement the converter with a large number of levels and achieve higher power capability and flexibility [2]–[4]. Fig. 1(a) shows a typical HBBB used in the CHMC application. Fig. 1(b) shows the circuit diagram of the CHMC with separate dc sources. Each HBBB can generate three-level voltage output, and the CHMC with N HBBBs can generate $(2N + 1)$-level voltage output.

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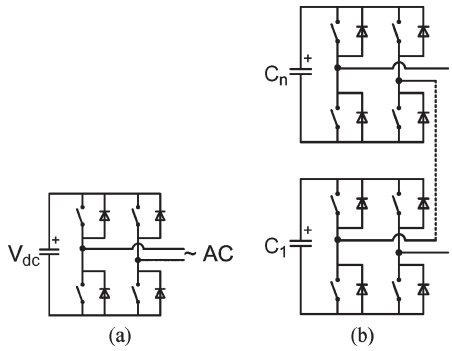

Fig. 1. (a) One HBBB. (b) CHMC.

Reliability is essential for high-power applications and thus is a major concern in CHMC applications, where a large number of power switching devices are used. It is important to restore the normal operation under fault conditions because the failed operation of STATCOM could cause tremendous losses for the power grid, particularly when STATCOM is injecting reactive power to the grid to support the voltage. As higher level multilevel converters are required in the higher power rating application, a large number of power switching devices are used. Each of these devices is a potential failure point, which will dramatically reduce the reliability of the system. It is therefore a key issue to design a fault-tolerant CHMC-based STATCOM system to enhance the system reliability.

Relevant research of the fault-tolerant design for multilevel converters mainly focuses on motor drive systems [5], [6]. References [7] and [8] introduce the fault-tolerant solutions of the capacitor-clamped and the asymmetric multilevel converters, which, in fact, sacrifice the output level. References [9] and [10] propose one multilevel converter topology with redundant switches and one adopted capacitor-clamped topology for the fault-tolerant design to maintain the output voltage level when switch fault occurs. Too many additional switches are applied, which limits the practical value in industry. References [11] and [12] discuss the operations of cascaded H-bridge multilevel inverters with faulty cells for a motor drive system. Additional switches are used to bypass the faulty cells. Despite that their control strategies are applied to minimize the load voltage distortion and balance the line-to-line output voltage, some phase output levels are lost. Applicable for increasing the reliability of a motor drive system, this solution is, however, unsuitable for power utility applications such as STATCOM.

Based on the control strategy presented in [13], this paper proposes a fault-tolerant control strategy to achieve the $N+1$ redundancy in a CHMC-based STATCOM system. Redundant HBBB is designed and applied to deal with the switching device failure and improve the reliability and availability. Compared with the aforementioned solutions, this strategy saves the bypass and isolated switches by using the failure character of high-power devices while keeping the same output converter voltage. The output quality–total harmonic distortion is also improved because of the increasing output level by using the redundant HBBB. The operating principle and the controller design method are introduced and illustrated in this paper. The fault-tolerant control strategy is designed and verified by simulations. The hardware demonstration is built to verify the proposed control strategy, and the experimental results prove the feasibility of the fault-tolerant design and control strategy.

II. Redundancy and Reliability

For a typical fault-tolerant system, the basic ability is to continue operation in a failure event. One of the useful approaches in a fault-tolerant design system is redundancy. Many fault-tolerant systems mirror all the operations, i.e., every operation should be performed on two or more duplicate systems, so if one fails, the other can take over. For modular systems with redundancy, the structure of the system is usually a mixture of series and parallel modules. In traditional two-level converters with high output voltages, the redundancy is achieved by a series connection of more power devices. In this way, redundancy can be achieved when one device fails short. Converter operation is not affected, and no additional control is needed to maintain normal operations since the failed device acts like a short circuit. We name it "device redundancy." By this method, the reliability will increase greatly, but the number of devices will double. For example, for a three-phase five-level CHMC, a normal operation requires $6 \times 4 = 24$ power device sets (considering the main switch and antiparallel diode as one device set). With the duplicate redundancy, we would need 48 devices. Normally, because of the cost, size, and complexity concerns, duplicate systems or modules are not easy to apply. Therefore, the topology configuration redundancy is considered as a practical solution.

The modularized HBBB is very suitable for the fault-tolerant design because all HBBBs are modular and identical in the CHMC application. One additional HBBB can be added to the CHMC as a backup to keep the normal operation even in the case of one HBBB failure. We call this redundancy "HBBB redundancy." The HBBB redundancy is achieved if one uses a $(2N+1)$-level CHMC to implement the STATCOM instead of a $(2N-1)$-level CHMC. In this way, each phase has one additional HBBB. Redundancy is realized if we can bypass the HBBB which contains the failed device so that the cascaded failure is prevented and normal operation is maintained.

There are two major advantages of using this redundancy approach: One is the savings in the number of power devices compared with the device redundancy. For example, a five-level CHMC plus one redundant HBBB will be implemented as a seven-level CHMC. The total number of power devices will be $9 \times 4 = 36$ instead of 48 for the duplicated system. Another major advantage is that, during normal operation, the output voltage waveform will be seven levels instead of five levels. This will improve the output voltage waveform quality in the normal operation. Meanwhile, the power devices are overdesigned, and more devices are applied in a fault-tolerant system. The balance of reliability enhancement and cost augment should be considered.

TABLE I
Reliability Comparison of a CHMC With and Without Redundancy

Conditions of HBBBs per phase	Reliability per phase	Numbers of devices per phase	Size&cost
2 HBBBs (5-level) without redundancy	85.1%	8	Small
3 HBBBs (7-level) with one HBBB redundancy	99.3%	12	Medium
2 HBBBs (5-level) with the duplicate power device redundancy	99.7%	16	Big

To further analyze the reliability of a CHMC application, it is supposed that a CHMC application is designed to have N HBBBs/phase. If the reliability of one power device set in a time interval is R and only the single switch fault can be tolerant for simplicity, the reliability of a one-phase CHMC with N HBBBs is R^{4N}; the number of power device sets per phase is $4N$. The reliability of a one-phase CHMC with $N+1$ HBBBs (one HBBB redundancy) is $[R^4 + 4(1-R)R^3]^{(N+1)}$; the number of power device sets per phase is $4(N+1)$. The reliability of a one-phase CHMC with the device redundancy is $(2R-R^2)^{4N}$; the number of power device sets per phase is $8N$.

For example, if the reliability of each power device set is $R = 98\%$, the comparison of a five-level CHMC without redundancy, a seven-level CHMC with one HBBB redundancy, and a five-level CHMC with the device redundancy is shown in Table I. Although this simple comparison does not take into account the effect to the reliability introduced by the extra components to detect the failure event, it can prove that the reliability improves by using the different redundant strategies.

From the aforementioned comparison, the reliability is improved greatly with the application of redundancy. At the same time, the numbers of devices used for converters also increase. Both the device redundancy and the HBBB redundancy can benefit the reliability of the CHMC greatly. However, compared with device redundancy, the method of HBBB redundancy will reduce the number of devices, then the cost and size, particularly for the high-level CHMC application. The HBBB redundancy can achieve the applicable balance between the reliability improvement and the cost augment. The HBBB redundancy with the acceptable extra size and cost is therefore an effective and applicable way to improve the reliability of CHMC applications.

III. HBBB Bypass and Control Strategy

When one power semiconductor device failed, the key to achieve the aforementioned proposed HBBB redundancy is to

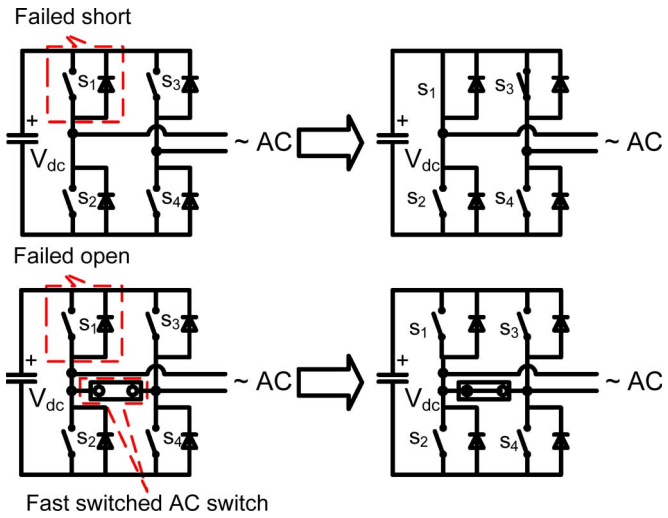

Fig. 2. HBBB bypass schemes after the device failures.

bypass and protect the failed HBBB. This requires that the failed HBBB dc side is open and that the ac side is short.

Nowadays, state-of-the-art high-power semiconductor devices such as integrated gate-commutated thyristors (IGCTs) and high-voltage insulated-gate bipolar transistors (IGBTs) have the potential to substitute conventional gate turn-off thyristors in high-power industrial applications due to their lower cost, higher power density, and higher performance because of the snubberless operation at higher switching frequencies (up to 1 kHz) [14], [15]. Due to its fast switching capability, ease of use, and the reliable press pack, the IGCT and the press-pack IGBTs are the desired semiconductor device candidates for the utility active and reactive power compensation applications. Both IGCTs and press-pack IGBTs will act as the short circuit after the destruction because of their press-pack structures.

For the wire bond package semiconductor devices such as module package IGBTs, the failure state after the destruction is open. One fast-switched ac switch is needed to bypass the failed HBBB in this case. For the press-pack semiconductor devices such as the IGCT and the press-pack IGBT, the failure mode is short. It is possible to use the failed-state character of the power device to bypass the failed HBBB without any additional bypass power switch. Since the press-pack semiconductor devices are widely used in high-power applications, the short failure mode of the device will be mainly analyzed in this paper.

Fig. 2 shows the two bypass schemes for the failed HBBB. For the failed open semiconductor device application, all the switches are turned off after the failure detection, and then the bypass ac switch is turned on simultaneously to isolate the failed HBBB. For the failed short semiconductor device application, if one top/bottom switch is failed short, the complementary switch in the same leg is turned off instantaneously with the fault detection to protect the dc capacitor. Then, turn on another top/bottom switch in the other leg, and turn off the other complementary switch to form a zero state. For instance, if the power switch S1 is failed short, when a fault is detected, the two top switches are given the ON signals, and the two bottom switches are given the OFF signals.

TABLE II
DETECTION OF FAILED DEVICES IN HBBB

S1	S2	Voltage on S1	Current through S1	Failure detection	Action
ON	OFF	H	L	S1 failed open	All switches OFF and bypass switch ON
OFF	OFF	L	L	S1 anti-parallel Diode conduct	None
OFF	OFF	L	H	S1 failed short	S2, S4 OFF; S3 ON
OFF	ON	L	H	S1 failed short	S2, S4 OFF; S3 ON

Sensing a device failure and bypassing the failed HBBB promptly and accurately are very important to prevent failure propagation. Fault detection and diagnostic methods were presented in recent research [16]–[18]. In the strategy described in Fig. 2, a failure event of a semiconductor device can unambiguously be detected by the combination logic of the switching command, the complementary switching command, the voltage-sensing signal across the device, and the current-sensing signal through the device. The developing power semiconductor switch will have the built-in voltage- and current-sensing functions. The commercial IGBT driver modules have the integrated fault detection and feedback function. These capabilities could be used to achieve this goal. Table II illustrates the device failure detection in one HBBB. Since the four switches in one HBBB are identical, the failure detection and the bypassing strategy are similar; only one switch failure detection and the bypass strategy are discussed.

For example, when the switching command is off but the sensed voltage across the device is low and the sensed current through the device is high, then the short failure of this power semiconductor device is detected, and a fault signal is generated to indicate the controller to do the following: 1) bypass the HBBB using this strategy shown in Fig. 2 and 2) change the main CHMC control to the fault-tolerant CHMC operation. Because one HBBB is bypassed, the $(2N+1)$-level converter is degraded to a $(2N-1)$-level converter. A major challenge therefore is to make sure that the main control system can gracefully migrate from a $2N+1$ system to a $2N-1$ system while the fault-tolerant system is still performing its normal operation such as generating reactive power to support the voltage for a STATCOM system.

Take a three-phase seven-level output STATCOM as an example. When one HBBB in one phase is bypassed, the output level of this phase is lost. To keep the equivalent normal output, the converter degrades from the seven-level operation to the five-level operation; then, the individual dc bus voltage needs to be charged to a higher value in order to keep the total dc bus voltage the same as the original value in all three phases. It is possible to be applied in FACTS applications for the active and reactive power compensation because the converter can obtain active power from the power grid to charge the dc-link capacitors without using the additional active power sources.

Because the loss of one HBBB will reduce the converter output voltage by $1/N$ at the time that a failure happens, the large current will be generated due to the voltage difference and the inductor impedance without the proper control. This resulting large transient current is one important issue that should be considered in this fault-tolerant design. The voltage

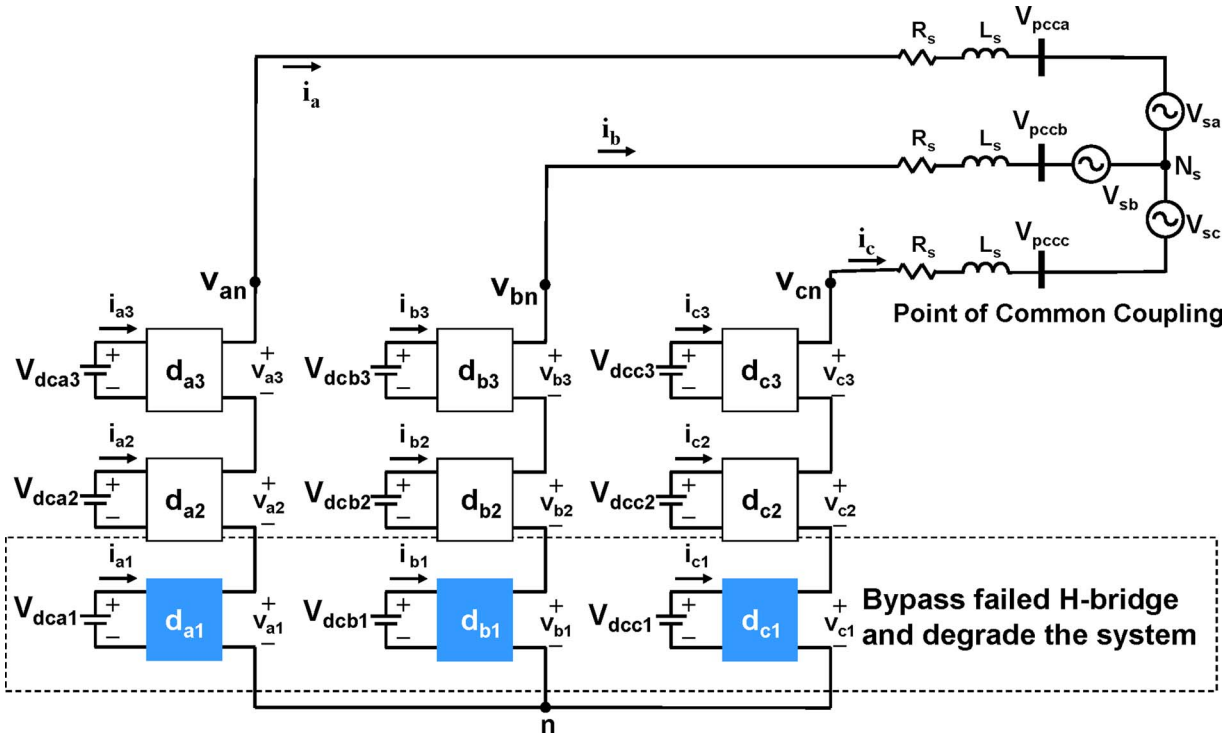

Fig. 3. Reconfiguration of the three-phase seven-level to five-level CHMC-based STATCOM.

control loop and the current control loop should be carefully designed. The current limit control and the dc voltage reference slope are introduced to smooth the transient current. The modulation index of the converter should be designed properly in both the normal operation and the fault-tolerant operation to provide enough voltage to eliminate the high transient current. The details of these design considerations will be discussed in Section V.

IV. Case Study and Controller Design

To study the validity of the proposed HBBB-redundancy-based fault-tolerant control strategy, a five-level plus one HBBB redundancy CHMC-based STATCOM system is considered. In other words, it is a seven-level CHMC-based STATCOM system.

Fig. 3 shows the system configuration of the seven-level CHMC-based STATCOM. This system is designed to have one HBBB redundancy. The seven-level CHMC can degrade to the five-level CHMC when one device is failed short. The specification of the studied STATCOM system is tabulated in Table III. If the transformer is used at the point to common coupling (PCC), the transformer will contribute the reactor inductance and resistance. All control parameters are suitable for the seven-level system and the five-level system. The dc bus voltage and dc capacitor design is based on a commercial semiconductor device in the high-power application market. Based on the selection of power devices, the five-level configuration can achieve the design rating. One HBBB is added to achieve the redundant fault-tolerant design and the better harmonics performance with the seven-level output.

Fig. 3 also shows the control scheme to balance the three-phase output and maintain the output of the converter in the event of a device failure. Because of the ability of redundancy, the system can perform the function of a STATCOM continuously after a fault event until the next planned outage service.

TABLE III
Specification of the Studied STATCOM Simulation System

7-level CHMC based STATCOM	
Configuration	Balanced 3-phase 3-wire
Individual DC bus voltage in 7 level	1450 V
Individual DC bus voltage in 5 level	2175 V
Total DC bus voltage	4350 V
Rated reactive current	1000A
DC capacitor capacitance	16.2mF
Equivalent loss of each HBBB	1.5kW
Individual Switching frequency	1020 Hz
Coupling reactor inductance	0.69mH
Coupling reactor ESR	26mΩ
Point of the Common Coupling (PCC) line to line voltage	4160V
Power Rating of STATCOM	7.2MVA
Digital delay of controller	100us

Modeling the HBBB-based converter, the average model and the small signal model of a CHMC-based STATCOM in the $dq0$ frame can be obtained by the modeling process described in [19]. Based on the derived small signal models, the closed-loop decoupled control can be designed. Fig. 4 shows the converter model and the controller design strategy of a CHMC-based STATCOM system.

The current and dc capacitor voltage information can be obtained from the STATCOM system to the controller. The output of the converter is controlled by the duty cycle and the suitable pulsewidth modulation (PWM) scheme based on the closed-loop controller design. The current loops are designed to achieve a high bandwidth control to regulate the current. The I_d channel is utilized to control the dc bus voltage with a

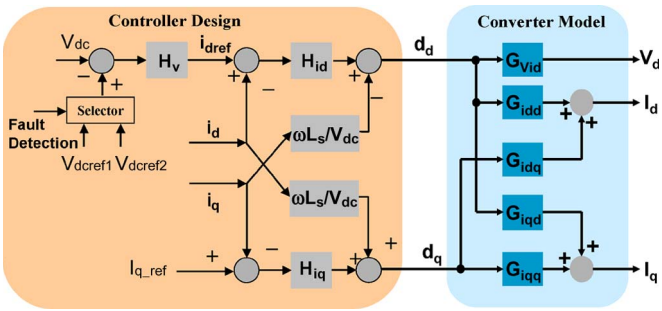

Fig. 4. Modeling and control diagram of a CHMC-based STATCOM.

slow-voltage-loop regulator, and the I_q channel is directly utilized to respond to the reactive compensation command. The closed-loop current loop is regulated by the proportional-integral (PI) regulator H_{id} and H_{iq}. The closed-loop voltage loop is regulated by the PI regulator H_v. The phase-shifted carrier PWM is used to switch the power devices in different H-bridges.

Based on the model development, the converter model of a STATCOM can be described as follows.

The duty-cycle-to-current transfer functions are

$$G_{idd}(s) = \frac{\hat{i}_d}{\hat{d}_d} = G_{iqq}(s) = \frac{\hat{i}_q}{\hat{d}_q} = \frac{K_{idd}\left(\frac{s}{\omega_Z}+1\right)}{\left(\frac{s}{\omega_p}\right)^2 + \frac{s}{Q\omega_p}+1}. \quad (1)$$

The current loop gain is

$$T_{id} = G_{idd}H_{id}. \quad (2)$$

The duty-cycle-to-capacitor-voltage transfer function is

$$G_{Vid}(s) = \frac{\hat{V}_{\rm dc}}{\hat{d}_d} = \frac{-\frac{I_d}{C}}{s+\frac{1}{R_L C}}. \quad (3)$$

The voltage loop gain is

$$T_V = G_{Vid}H_{id}H_v. \quad (4)$$

The digital delay of the controller is modeled to emulate the real digital control system

$$G_D = \frac{1-sT_D/2}{1+sT_D/2} \quad (5)$$

with

$$K_{idd} = \frac{V_{\rm dc}R_S}{R_S^2+(\omega L_S)^2} \qquad Q = \frac{\sqrt{R_S^2+(\omega L_S)^2}}{2R_S}$$
$$\omega_p = \frac{\sqrt{R_S^2+(\omega L_S)^2}}{L_S} \qquad \omega_Z = \frac{R_S}{L_S} \quad (6)$$

where

$V_{\rm dc}$	total dc capacitor voltage;
L_S	coupling reactor inductance;
R_S	coupling reactor equivalent series resistance;
C	dc capacitor capacitance;
P_L	equivalent converter loss of each HBBB;
$R_L = V_{\rm dc}^2/P_L$	equivalent converter loss resistor.

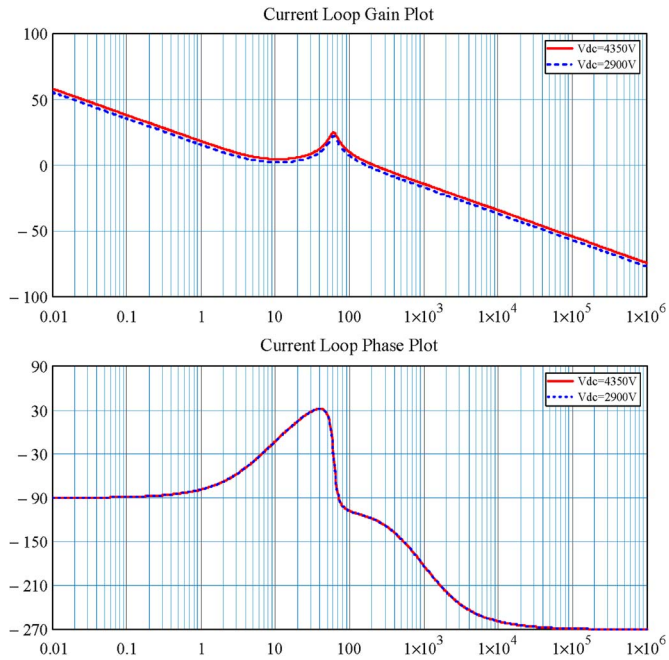

Fig. 5. Open-loop current loop Bode plot in the fault-tolerant transition.

Based on the STATCOM model development and controller design, the control (duty cycle) to the reactive current and the dc capacitor voltage open-loop Bode plots can be expressed to determine the stability and transient performance. The bandwidth of the current loop is designed at 200 Hz, which is about 1/5 of the switching frequency, to avoid noise disturbance. The phase margin of the current loop is 60° to get the good transience and stability performance. The bandwidth of the voltage loop is 20 Hz, which is much slower than the inner current loop bandwidth. The phase margin of the voltage loop is also designed to 60°.

From (1) and (3), when the STATCOM controller changes the operating mode from the seven-level output operation to the five-level output operation, the total dc capacitor voltage will not change based on the proposed control strategy. Since the equivalent resistor for the converter loss dominates the zero of the voltage loop in the range of 0.1 Hz, its effect to the voltage loop can be neglected. The current loop and the voltage loop will not change from the seven-level operation to the five-level operation; thus, the control design is suitable for both the seven-level and the five-level operation by using the proposed fault-tolerant control strategy.

Although the steady-state operations can be guaranteed, it is important to analyze the stability and transient performance during the fault-tolerant transition from the seven-level operation to the five-level operation.

From (1) and (2), the current loop in the fault-tolerant transition is determined by the change of the total dc capacitor voltage. The open-loop current loop Bode plot during the fault-tolerant transition is shown in Fig. 5. When the dc capacitor voltage varies between 2900 and 4350 V during the fault-tolerant transience, the controller bandwidth is around 200 Hz, and the 60° phase margin can be achieved.

From (3) and (4), the voltage loop in the fault-tolerant transition is determined by the change of the d-axis current.

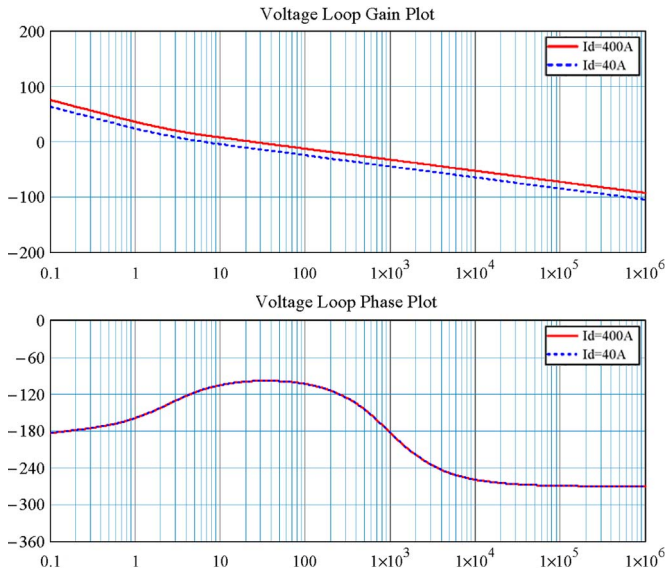

Fig. 6. Open-loop voltage loop Bode plot in the fault-tolerant transition.

When the d-axis current varies between 40 and 400 A, the crossover frequency is around 7–20 Hz, and a phase margin that is higher than 60° can be achieved. The open-loop voltage loop Bode plot during the fault-tolerant transition is shown in Fig. 6.

When the fault-tolerant STATCOM controller is well designed based on the aforementioned analysis, this seven-level CHMC-based STATCOM can stably operate in both normal seven-level output operation and five-level output operation with the application of the fault-tolerant design in the controller. Even in the fault-tolerant transition from the seven-level operation to the five-level operation, the proposed control will provide good stability and transient performance. This controller design method is applicable for the CHMC-based STATCOM fault-tolerant design.

V. Simulation Results

The control performance of the study system is verified by simulation. The simulation investigation is implemented in Saber.

Fig. 7 shows the results of the dynamic response of the studied STATCOM operating in full capacitive mode to inject reactive power to the power grid.

At 50 ms, a fault is detected in one HBBB of one phase, and the failed HBBB is bypassed. Then, the controller bypasses the two other HBBBs in the other two phases. The total system changes to a five-level CHMC operation. The control strategy degrades the system from the seven-level output to the five-level output. Since the total dc capacitor voltage does not change, the healthy dc bus voltages are charged. To avoid overcurrent during the fault-tolerant transience to charge the dc capacitor, the current limit control is applied. In this simulation, the peak current limit is set to 2000 A. While the output reactive power command does not change, the duty cycle will increase to meet the reactive power requirement due to the feedback controller operation. From the simulation results, we can find that the duty cycle increases just after the fault detection to keep the converter output, therefore to maintain the reactive current generation. The duty cycle recovers to the normal value after the dc capacitor charge. With the proper normal-operating duty cycle and closed-loop controller design, overcurrent can be avoided. A slope of the dc voltage reference is introduced to improve the dynamic performance of the output current. The slope time step in this simulation is 30 ms.

The relationship of the maximum duty cycle and the normal-operation duty cycle is shown as

$$N \times D_{\text{normal}} = (N-1) \times D_{\text{TransMax}} \tag{7}$$

$$D_{\text{TransMax}} = \frac{N}{N-1} D_{\text{normal}} \tag{8}$$

where D_{normal} is the duty cycle in the normal operation and D_{TransMax} is the maximum duty cycle in fault tolerance. When the converter output level is high (N is large), the change of the duty cycle is relatively small. In this simulation, the normal capacitive mode operation is 0.8, and the maximum duty cycle during the fault-tolerant transience is 1.2. When the total capacitor voltage charges up to the normal value, the duty cycle decreases to 0.8 again.

Because the converter needs energy to charge the capacitor, the active power flows into the converter from the power grid; the current does not lead the PCC voltage by exactly 90° and has little distortion because the STATCOM is absorbing active power from the power grid during the charging time. During the fault clear period, the reactive power injecting to the grid is maintained.

Fig. 8 shows the results of the dynamic response of the STATCOM operating in full inductive mode to absorb reactive power from the power grid. The control strategy is the same. The absorbing reactive power is maintained during the fault detection and fault recovery. The STATCOM system is transferred to another safe operating mode smoothly.

The results in Figs. 7 and 8 indicate that the proposed fault-tolerant control strategy operates successfully in the event of a device failure, and HBBB redundancy is realized. Because the controller is well designed, the stability of the STATCOM operation is achieved in the seven-level output mode, the five-level output mode, and the fault-tolerant transient mode. By applying the dc capacitor voltage reference slope and the proper current loop controller design, overcurrent is avoided under the current limit control.

VI. Experimental Results

To verify the proposed fault-tolerant control strategy, a five-level CHMC-based STATCOM hardware prototype has been built in a laboratory, as shown in Fig. 9.

IGBT-based PM50RSA120 intelligent power modules are used as HBBB-based converters. Each HBBB is controlled by an Altera FLEX 10K30A field-programmable-gate-array (FPGA)-based digital local controller through a driver board and optical fibers. The switching signals are generated by the digital central controller. The central controller includes a TMS320C6701 DSP board and an AED-106 FPGA

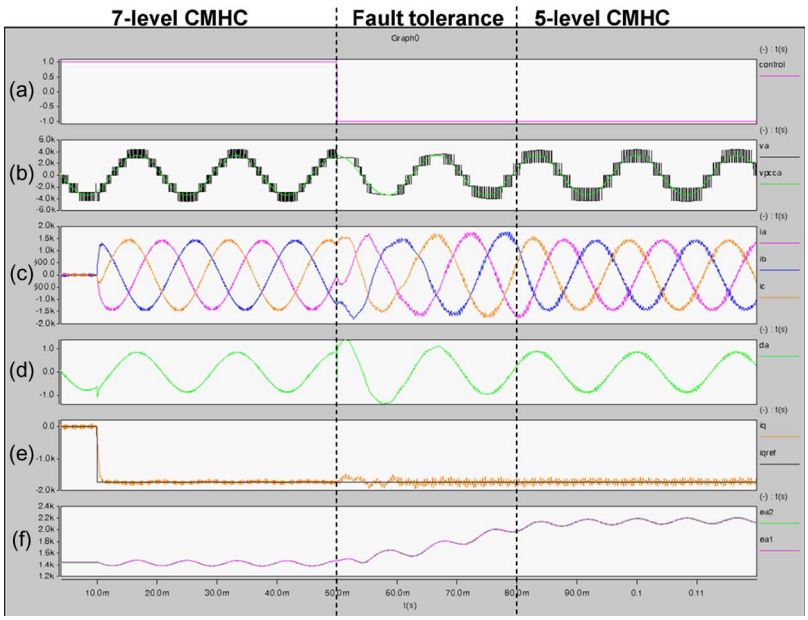

Fig. 7. Simulation of the fault-tolerant STATCOM operation in full capacitive mode. (a) Fault detection signal. (b) Output voltage of the converter and voltage at the PCC. (c) Three-phase current. (d) Duty cycle of the converter output. (e) Reactive current and reactive current reference. (f) DC capacitor voltage.

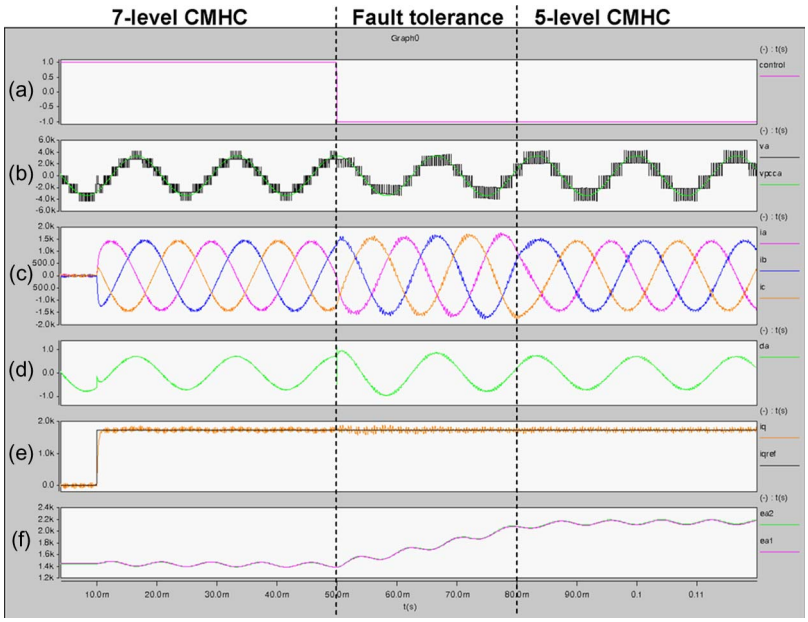

Fig. 8. Simulation of the fault-tolerant STATCOM operation in full inductive mode. (a) Fault detection signal. (b) Output voltage of the converter and voltage at the PCC. (c) Three-phase current. (d) Duty cycle of the converter output. (e) Reactive current and reactive current reference. (f) DC capacitor voltage.

daughterboard. The controller system is a fully optical interface and fully compatible with any optical-triggered device-based power converter.

For the experimental test, the five-level CHMC-based STATCOM will degrade to a three-level STATCOM after the detection of the failure and bypass the failed HBBB. The controller is designed based on the specification of the experimental STATCOM prototype which is shown in Table IV.

Six IGBT-based H-bridges are built in a laboratory to achieve the basic three-phase five-level multilevel converter. Since the fault-tolerant strategy is suitable for all different-level-output CHMC applications, the experimental setup is capable of verifying the proposed fault-tolerant control strategy. The switching frequency is 300 Hz because of the calculation capability limitation of the applied FPGA resource utilization. Since the PWM method is not considered in the controller design, it will not affect the operation performance of the fault-tolerant control design of the STATCOM system.

The controller design is following the controller design method presented in Section IV. The current loop bandwidth is designed to 50 Hz, and the voltage loop bandwidth is designed to 5 Hz. The phase margins are designed to greater than 60° for both five-level and three-level operations. The controller is carefully designed to provide enough phase margin in the fault-tolerant transition from the five-level to three-level operation.

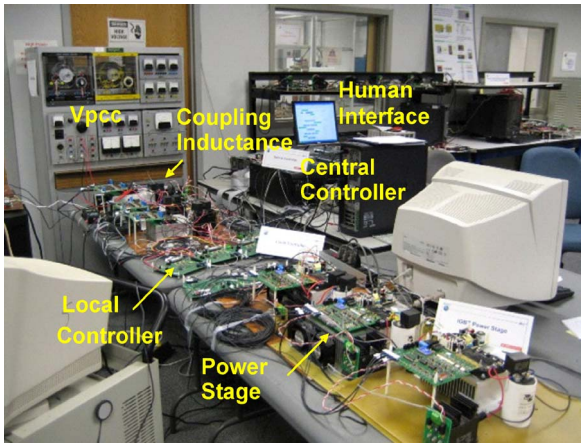

Fig. 9. Five-level CHMC-based STATCOM prototype.

TABLE IV
SPECIFICATION OF THE STUDIED EXPERIMENTAL STATCOM SYSTEM

5-level CHMC based STATCOM	
Configuration	Balanced 3-phase 3-wire
Individual DC bus voltage in 5 level	29 V
Individual DC bus voltage in 3 level	58 V
Total DC bus voltage	58 V
Rated reactive current	4A
DC capacitor capacitance	2700uF
Equivalent loss of each HBBB	1W
Individual Switching frequency	300 Hz
Coupling reactor impedance	2.5mH
Coupling reactor resistance	180mΩ
PCC phase voltage	35V
Digital delay of controller	100us

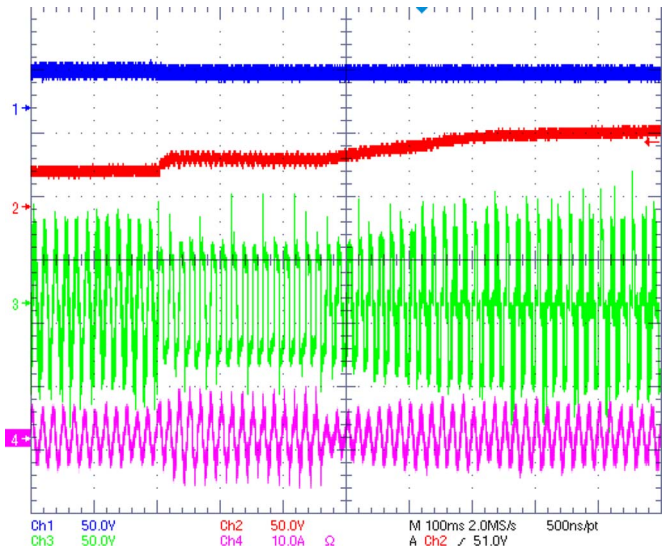

Fig. 10. STATCOM fault-tolerant operation in the capacitive mode: (1) dc capacitor voltage 1; (2) dc capacitor voltage 2; (3) converter output; and (4) reactive current.

Figs. 10 and 11 show the experimental results of the fault-tolerant design control strategy in the capacitive mode and the inductive mode of STATCOM separately.

Although one HBBB is lost because of the device failure, the STATCOM can still inject/absorb reactive power to/from the power grid to keep the normal operation following the control commands by charging the dc capacitor voltage and adjusting

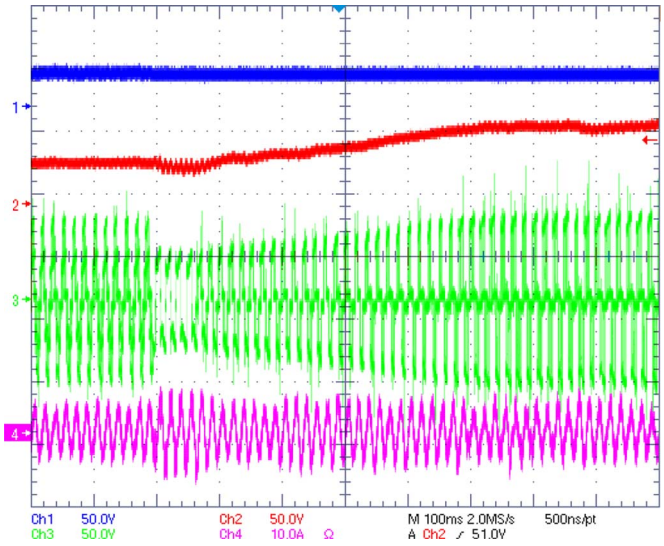

Fig. 11. STATCOM fault-tolerant operation in the inductive mode: (1) dc capacitor voltage 1; (2) dc capacitor voltage 2; (3) converter output; (4) reactive current.

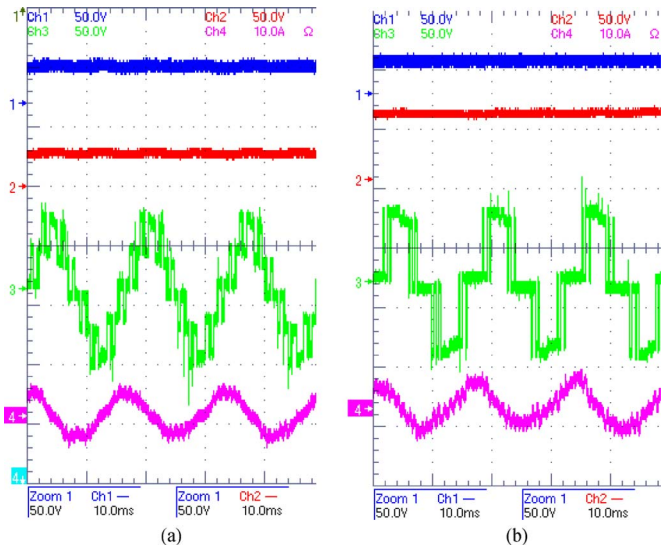

Fig. 12. STATCOM capacitive mode operation in the (a) five-level output and (b) three-level output.

the duty cycle of the converter output. The current waveforms are not consistent because the current sensor tolerance is large compared with the small current rating. In the experimental tests, the large reactive current happens during the first few cycles of the fault-tolerant transition. Based on the aforementioned discussion of (8), the duty cycle will double and saturate in this five-level output to the three-level output transition. The duty cycle is limited to 1.2 for a few cycles. The converter output is saturated too from the test results. After the dc capacitor voltage is charged up, the feedback control will adjust the duty cycle under the limit, and then, the reactive current recovers to the normal operation. Because the inductive mode needs a smaller duty cycle, the overcurrent time interval is shorter than that of the capacitive mode. The charging time in the experimental test is longer than that in the simulation because of the usage of the large dc capacitor and the small charging current. The application hardware limits the accuracy of the

experimental test results, but the feasibility of the fault-tolerant design for the CHMC-based STATCOM can be verified.

Fig. 12 shows the zoom-in capacitive operation waveforms of the STATCOM at the five-level output operation and the three-level output operation. The reactive current is maintained even if the STATCOM loses one HBBB and two output levels.

From the experimental results, it can be seen that the dc capacitor voltage is charged from 29 to 58 V after the fault detection, and the reactive current is maintained because of the implementation of the fault-tolerant strategy for the STATCOM operation. During the fault-tolerant transition, the current loop is working well to keep the reactive current by changing the duty cycle when the dc capacitor voltage is low; thus, the large overcurrent is avoided.

The experimental results verify the feasibility of the proposed fault-tolerant control strategy.

VII. Conclusion

A fault-tolerant control strategy to achieve HBBB redundancy in a CHMC-based STATCOM system has been proposed and verified by simulations and experiments. As a result, the reliability of the STATCOM is enhanced greatly with the redundant HBBB, and at the same time, the output voltage waveform quality is improved. The extra cost and size are relatively small compared with the high output level. Even losing two output levels, the output (reactive power) still can be maintained by the proper control design. The controller design considerations are discussed to provide a good stability and transient performance during the fault-tolerant transition. The simulation and experimental test results verify the feasibility of the proposed fault-tolerant design. The proposed fault-tolerant control strategy is suitable for an any-level CHMC topology. This fault-tolerant control strategy can also be applied to other CHMC-based FACTS applications, such as static synchronous series compensation and unified power flow controllers.

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