

Comparative Analysis Between Two-Level and Three-Level DC/AC Electric Vehicle Traction Inverters Using a Novel DC-Link Voltage Balancing Algorithm

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Abstract—This paper presents an extensive comparative study between a two- and three-level inverter for electric vehicle traction applications. An advanced control strategy for balancing the two dc-link capacitors is also proposed. In this paper, the main focus is on the total voltage harmonic distortion (%THD_v), the analytical derivation of the three-level capacitor currents, and the voltage balancing of two capacitor voltages. For generating the gate signals, space vector pulse width modulation (SV-PWM) is used. The developed voltage-balancing scheme helps to reduce the number of converter switching sequences, compared with the conventional SV-PWM strategy, and keeps the voltage difference between the two dc-link capacitors at the desired voltage level. The developed test-bench is used for a permanent magnet synchronous machine drive for electric vehicle (EV) applications. Detailed simulation studies are performed using MATLAB/Simulink block set and experimental verification is achieved using dSpace based real-time simulator. Both the simulation and experimental results show a significant improvement in reduction of total harmonic distortion (%THD_v) for the three-level inverter.

Index Terms—Electric vehicles (EVs), inverters, motor drives, permanent magnet motors, propulsion, traction.

I. INTRODUCTION

BECAUSE of the increased global awareness to reduce carbon emission from different sources, internal combustion engine (ICE) vehicles engine-driven cars are found to be one of the potential sources. To reduce this type of carbon emission electric vehicles (EVs) are one of the potential solutions. Generally majority of the electrical vehicle manufacturer uses two-level traction inverter to drive their machines, which is a well-developed technique.

However, to reduce the size of passive components in drive train, better control of electric machines and to increase

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power density of inverter, it may be required to increase the switching frequency of converter to several kilohertz level. Two-level inverters have higher switching losses at higher switching frequencies, which lead to poor inverter efficiency. However, multilevel inverters, which were previously being used for high- and medium-power applications, can now be used for EV applications. It has a low switching loss at higher switching frequencies compared with two-level inverter and also produces low acoustic noise. Multilevel inverters have attracted special attention in high-power applications in the last three decades, after its introduction in 1981 [1].

Because of low-voltage ratings of the switches used for multilevel inverters compared with two-level inverters for same dc bus voltages, switching losses goes down as the switching frequency increases [2], [3]. There are other additional advantages like a reduction in total harmonic distortion (%THD) due to an increase in the number of steps, which then reduces the electro-magnetic interference (EMI) emission. Boost inductor size can also be reduced with line filter for reduced harmonic distortion. Voltage stress also reduces due to a reduction in dv/dt across the power switches. Hence, many EV manufacturing companies are now trying to replace their two-level inverters with three-level inverters, to drive their electric machines. This also allows them to increase the dc bus voltage level of the inverter. However, it has a potential drawback of unbalanced dc-link capacitor voltages. The permanent magnet synchronous motor (PMSM) is one of the most preferred choices for electric and plug-in hybrid EV applications, owing to its fast torque response and high torque to weight ratio, compared with the induction motor.

Recently, much literature has been published, such as [2], [3], and [8], on the comparative study between two-level (see Fig. 2) and three-level (see Fig. 1) inverters. They are mainly based on switching loss calculations as well as voltage and current harmonics. These comparisons do not depict all modes of operation, with change in speed or torque demand of the machine. Analytical calculations of three-level inverter capacitor currents have also been neglected in these papers. In this paper, an analytical derivation is presented for three-level inverter capacitor current, based on two-level inverter current model [4]. Thereafter, a reduced switching loss-based strategy for dc-link voltage-balancing algorithm is proposed for the three-level inverter. This algorithm keeps the

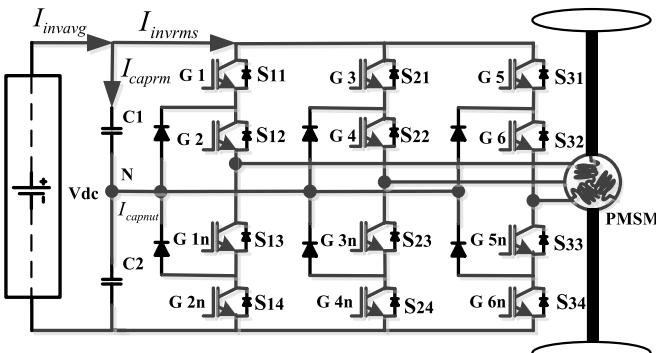


Fig. 1. Schematic representation of a typical 3-level neutral point clamped (NPC) DC/AC traction inverter.

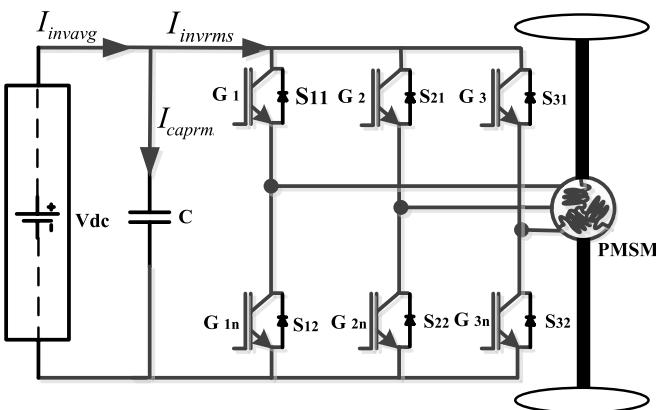


Fig. 2. Schematic representation of a typical 2-level DC/AC traction inverter.

voltage difference between the two dc-link capacitor voltages below 5% of the total dc-link voltage. Capacitor current is sensed from the two capacitors and compared with analytical calculations as well as hardware prototype test results. Thereafter, the phase voltage THD from the simulation and hardware results is compared for both the two-level as well as three-level inverter, which shows significant improvement in the total harmonic distortion for the three-level inverter.

The problem of dc-link capacitor voltage balancing has been studied by many researchers during last few years and different solutions have been proposed. There are many topologies, which have been proposed for balancing the two dc-bus capacitor voltages, depending on application requirements [5]–[32]. Some researchers proposed to have two separate rectifiers to supply the dc-link capacitors separately [10]. Therefore we need two separate converters, which intern will increase the system cost. This type of converter can be replaced by connecting two back-to-back NPC converters [11], [12].

Pulse width modulation (PWM)-based control topologies are also proposed to resolve this problem. There are basically two kinds of PWM control strategies that can be found in literature; carrier-based PWM and space-vector-based PWM (SV-PWM) techniques. In the carrier-based topology, a zero-sequence voltage is generally added in the output voltage [13]–[18]. Moreover, most SV-PWM strategies operate in

such a way, so as to optimize the redundant voltage vectors, to balance the dc-link voltage. In this paper, the nearest three vector (NTV) scheme is considered, which is a part of SV-PWM technique [18]. In the NTV scheme, either the upper or the lower capacitor voltage is used, which makes the two capacitor voltages stable. However, to make the switching strategy symmetrical, the use of all the switching states makes the switching frequency different for different subsectors, as the numbers of redundant voltage vectors are not equal in all subsectors [20]. Some techniques described in literature try to overcome this problem by dividing the first and second subsector into two parts, which makes the switching frequency for each sector equal [21], [22], [31]. However, it makes the number of subsectors six, instead of four.

Researchers also tried to balance the capacitor voltages using virtual voltage vectors, which is known as, nearest three virtual vector (NTV^2) topology [25]. This also creates more number of subsectors and no results are shown for transient stability for motor drive applications. All the topologies mentioned above use redundant vector states as well as varying positive and negative redundant voltage vectors, depending on the capacitor voltage difference. Furthermore, they use a PI controller at the output of the voltage difference, to generate the duty cycle [23], [25]. More recently, some papers have proposed taking the neutral point current as a reference, instead of the capacitor voltages. This reduces the neutral point current to zero or keeps it in a particular band limit, to control and balance the dc-link voltage. This strategy also uses sharing of the ON-time of positive and negative voltage vector [24]. This increases the total harmonic distortion of the generated voltage, owing to variation of the switch ON-time. Certain research work shows the combination of NTV and nearest three virtual vectors (NTV^2) schemes, to get the benefit of low switching frequency from the NTV scheme. It also leads to better controllability, to keep the neutral point balanced at all load conditions, compared with the NTV^2 scheme [23], [24].

The dc-link voltage balancing topologies, described before, can be summarized in two categories: passive and active balancing circuits. In passive balancing, external hardware components are generally being used, which increase the system cost and space requirement. All the active balancing circuits use PWM control, which also takes care of the voltage balancing issue. However, all the control topologies proposed in the literature either increases the number of switching or lead the system to asymmetrical switching. These types of control strategies increase the inverter losses and harmonic distortions. Moreover, neither of the control strategies proposed has focused on EV applications, which have much more dynamics, compare with other systems.

The proposed control topology used a reduced number of switching sequence compared with the conventional one and also keeps the two capacitor voltage difference at desired level. It helps to reduce the total inverter switching losses and voltage distortion. Details simulation and experimental studies are carried out to shows the performance of the proposed system for wide speed and torque range. Results are then compared with a two-level inverter based permanent magnet synchronous machine drives.

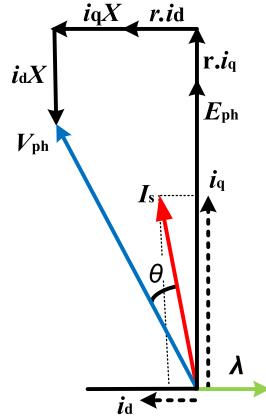


Fig. 3. Phaser diagram of PMSM machine.

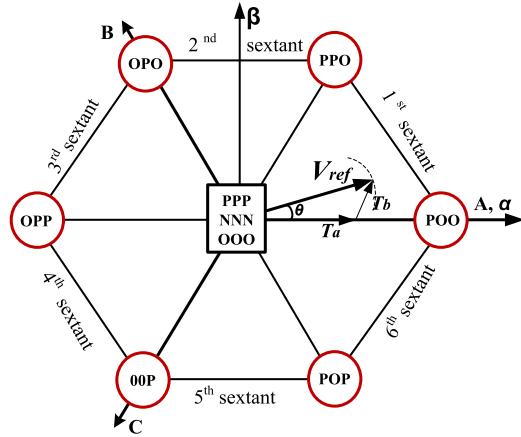


Fig. 4. Space-vector diagram for two-level inverter.

II. PRINCIPLE OF OPERATION

A. Machine Modeling and Performance Analysis

The machine model equations can be represented as follows:

$$v_d = r \cdot i_d + p(\phi_d + \lambda) - \omega_e \phi_q \quad (1)$$

$$v_q = r \cdot i_q + p\phi_q + \omega_e(\phi_d + \lambda) \quad (2)$$

$$\phi_d = L_d \cdot i_d \quad (3)$$

$$\phi_q = L_q \cdot i_q \quad (4)$$

$$T_e - T_l = J \cdot p \cdot \omega + B_m \cdot \omega \quad (5)$$

$$T_e = (3p/2) \cdot (\lambda \cdot i_q - (L_q - L_d) \cdot i_d \cdot i_q) \quad (6)$$

where v_d and v_q are the d - and q -axis components of the stator voltage, respectively, i_d and i_q are the d - and q -axis components of stator currents, respectively, r is the stator resistance, ϕ_d and ϕ_q are the stator flux linkages in the d - and q -axis, respectively, L_d and L_q are the d - and q -axis inductances, λ is the rotor magnet flux linkage, owing to the permanent magnet on the rotor side, p is the machine pole pair, and ω_e is the reference field speed.

Fig. 3 shows the phasor diagram of the PMSM machine, where I_s is the reference current vector and ϕ is the power factor angle between v_{ph} and I_s .

B. SV-PWM for Two-Level and Three-Level Inverter

Fig. 4 shows the vector diagram for a two-level inverter. When the reference vector is on the first sextant, it can be

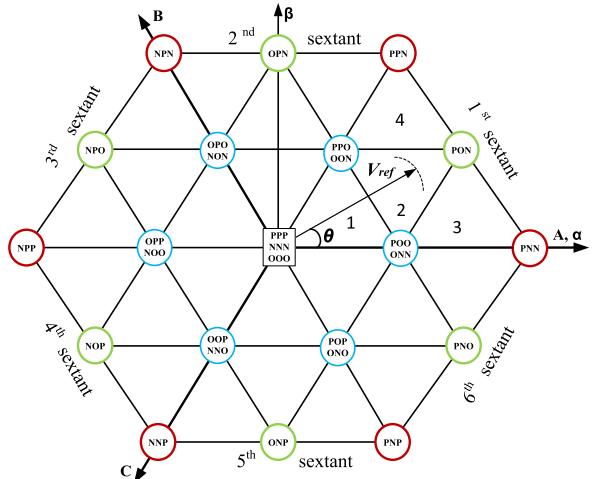


Fig. 5. Space-vector diagram for three-level NPC inverter.

TABLE I
DIFFERENT SWITCHING STATES

Switching State	Switch Status, Phase x ($a/b/c$)				Pole Voltage (V_{x0})
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
P	1	1	0	0	$V_{dc}/2$
O	0	1	1	0	0
N	0	0	1	1	$-V_{dc}/2$

represented by the three nearest voltage vectors, as shown in (7). The total time duration, for which the vectors will be applied, is also shown in (8)

$$V_{ref} \cdot T_S = V_1 T_a + V_2 T_b + V_0 T_z \quad (7)$$

where $T_S = T_a + T_b + T_z$

V_1 and V_2 are the two nearest voltage vectors and V_0 is zero-voltage vector; T_a , T_b , and T_z are the respective time durations for the applied voltage vectors

$$T_a = (m \cdot T_s) \frac{\sin(\frac{\pi}{3} - \theta)}{\sin(\frac{\pi}{3})}$$

$$T_b = (m \cdot T_s) \frac{\sin(\theta)}{\sin(\frac{\pi}{3})}$$

$$T_z = T_s - (T_a + T_b) \quad (8)$$

where $m = \sqrt{3}V_m/V_{dc}$ and T_s is the switching time. For three-level inverter, as shown in Fig. 1, the inverter has four switches for each leg. There exist two diodes in each leg, whose neutral points are connected to the common connection point of the two dc-link capacitors. Hence, there exist a total 27 switching combinations, out of which three are null or zero vectors, and 24 are active vectors, as shown in the vector diagram of Fig. 5. Table I shows the different switching combinations and output pole voltages. Table II shows the list of different null, small, medium, and large voltage vectors.

Similar to two-level SV-PWM, in a three-level inverter, the reference voltage vector is generated with a combination of the available switching states of that sector. From Fig. 5, it can

TABLE II
DIFFERENT SWITCHING COMBINATIONS

Switching vector combination	Voltage level
PPP,NNN,OOO	0 (Null)
PPO,OON,POO,ONN,POP,ONO,OOP, NNO,OPP,NOO,OPO,NON	$V_{dc}/3$ (Small)
PON,OPN,NPO,NOP,ONP,PNO	$V_{dc}/\sqrt{3}$ (Medium)
PNN,PPN,NPN,NPP,NNP,PNP	$2V_{dc}/3$ (Large)

TABLE III
SWITCHING STATES FOR THREE-LEVEL INVERTER IN SECTOR 1

Sub-sector	T ₁	T ₂	T ₃
1	$T_s(\sin(\pi/3-0))$	$T_s(1-2\sin(\pi/3+0))$	$T_s(2\sin(0))$
2	$T_s(1-2\sin(0))$	$T_s(2\sin(\pi/3+0)-1)$	$T_s(1-2\sin(\pi/3-0))$
3	$T_s(2\sin(\pi/3+0))$	$T_s(2\sin(0))$	$T_s(2\sin(\pi/3-0)-1)$
4	$T_s(2\sin(0)-1)$	$T_s(2\sin(\pi/3-0))$	$T_s(2-2\sin(\pi/3+0))$

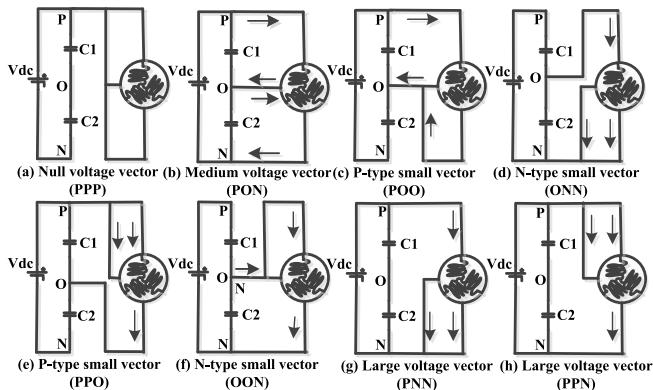


Fig. 6. Effects of different voltage vectors on dc-link capacitor voltage.

be seen that the reference voltage vector is placed in sector two, where the available vectors are POO/ONN, PPO/OON, and PON. So V_{ref} can be represented as

$$V_{ref} \cdot T_S = T_a \cdot V_1 + T_b \cdot V_2 + T_c \cdot V_3 \quad (9)$$

where $T_s = T_a + T_b + T_c$.

Time duration for all the three voltage vectors are shown in Table III. All other sectors, duty cycles, or time duration for different voltage vectors can also be calculated accordingly. Because of the repetitive sequence of all other sectors from 0° to 60° , similar equations can be derived.

C. Problems Associated With DC-Link Capacitor Voltage Balancing

As can be seen from Fig. 6 and Table II, in each sextant, there exists four types of vector combinations. They affect differently on dc-link capacitor voltages. Fig. 6 shows the effect of those vectors on the two capacitor voltages. Null (a) and large voltage vectors (g and h) do not affect the dc-link voltage balancing, as they are not connected to the neutral point. Hence, only the small (c, d, e, and f) as well as medium voltage (b) vectors are mainly responsible for the balancing problem.

The positive small voltage vectors, like POO/PPO, help to discharge the upper capacitor (c and e), while the negative voltage vectors, such as OON/OON (d and f) help to discharge the lower capacitor. Hence, by selecting a proper switching sequence, the two dc-link capacitor voltages can be balanced dynamically.

III. PROPOSED DC-LINK VOLTAGE BALANCING ALGORITHM

To overcome the problem with variable switching frequency for different subsectors, as stated in the introduction, and to increase the controllability of the dc-link capacitors, for wide speed and torque range with reduced switching losses, a new switching sequence is proposed, as shown in Table IV. The total number of switching in each subsector is five, which is less than the conventional switching schemes. Also, since the switching sequences are selected depending on the difference in the capacitor voltages at each time period T_s , this scheme is more useful and robust for PMSM drive applications in both transient as well as steady-state conditions. It can also be observed that, in each sequence, one of the switching combinations does not change (for instance, for subsector two in sector one, first bit, P is constant), which further reduces the switching losses.

However, once the duty cycle is specified according to this strategy, because of the change in the capacitor voltage, the switching sequence may change in between the total switching time period T_s , which may lead to asymmetrical switching. To overcome this problem, the change in switching state is allowed only at the start of each switching cycle, T_s . A logic block detects the change in switching time period, as shown in Fig. 7. Detailed simulation and experimental test results are exhibited, to compare the performance of the proposed system, and the results are compared with those obtained from a two-level inverter.

IV. ANALYTICAL CALCULATION OF CAPACITOR CURRENT

A. Two-Level Inverter Capacitor Current

According to the analytical calculations shown for capacitor current in [4], an analytical expression for the capacitor current is derived from the inverter positive bus current. Average value to the inverter current, which is mainly supplied by battery, can be computed by finding out the average value of total inverter current ($I_{inv,avg}$), as

$$I_{inv,avg} = \left(\frac{3}{\pi} \right) \int_0^{\frac{\pi}{3}} (I_{po0} \cdot T_a + I_{ppo} \cdot T_b) d\alpha$$

$$I_{inv,avg} = \frac{\sqrt{3}}{2} \cdot m \cdot I_m \cos(\varphi). \quad (10)$$

In a similar manner, the total RMS inverter current ($I_{inv,rms}$) can be calculated, as

$$I_{inv,rms} = I_m \sqrt{\left(\frac{3}{\pi} \right) \int_0^{\frac{\pi}{3}} (I_{po0}^2 \cdot T_a + I_{ppo}^2 \cdot T_b) d\alpha}$$

$$I_{inv,rms} = I_m \cdot \sqrt{\frac{m \cdot (4 \cdot \cos^2(\varphi) + 1)}{2 \cdot \pi}}. \quad (11)$$

TABLE IV
PROPOSED DC-LINK VOLTAGE BALANCING SEQUENCE

Sector	Sub-sector	Balancing Ability	Switching Sequence
1	1	$V_{dc1} > V_{dc2}$	OOO-POO-PPO-POO-OOO
		$V_{dc2} > V_{dc1}$	NNN-ONN-OON-ONN-NNN
	2	$V_{dc1} > V_{dc2}$	POO-PPO-PON-PPO-POO
		$V_{dc2} > V_{dc1}$	ONN-OON-PON-OON-ONN
	3	$V_{dc1} > V_{dc2}$	POO-PON-PNN-PON-POO
		$V_{dc2} > V_{dc1}$	ONN-PNN-PON-PNN-ONN
	4	$V_{dc1} > V_{dc2}$	PPO-PPN-PON-PPN-PPO
		$V_{dc2} > V_{dc1}$	OON-PON-PPN-PON-OON
2	1	$V_{dc1} > V_{dc2}$	OOO-OPO-PPO-OPO-OOO
		$V_{dc2} > V_{dc1}$	NNN-NON-OON-NON-NNN
	2	$V_{dc1} > V_{dc2}$	PPO-OPO-OPN-OPO-PPO
		$V_{dc2} > V_{dc1}$	OON-NON-OPN-NON-OON
	3	$V_{dc1} > V_{dc2}$	PPO-PPN-OPN-PPN-PPO
		$V_{dc2} > V_{dc1}$	OON-OPN-PPN-OPN-OON
	4	$V_{dc1} > V_{dc2}$	OPO-OPN-NPN-OPN-OPO
		$V_{dc2} > V_{dc1}$	NON-NPN-OPN-NPN-NON
3	1	$V_{dc1} > V_{dc2}$	OOO-OPO-OPP-OPO-OOO
		$V_{dc2} > V_{dc1}$	NNN-NON-NOO-NON-NNN
	2	$V_{dc1} > V_{dc2}$	OPP-OPO-NPO-OPO-OPP
		$V_{dc2} > V_{dc1}$	NOO-NPO-NON-NPO-NOO
	3	$V_{dc1} > V_{dc2}$	OPO-NPO-NPN-NPO-OPO
		$V_{dc2} > V_{dc1}$	NON-NPN-NPO-NPN-NON
	4	$V_{dc1} > V_{dc2}$	OPP-NPP-NPO-NPP-OPP
		$V_{dc2} > V_{dc1}$	NOO-NPO-NPP-NPO-NOO
4	1	$V_{dc1} > V_{dc2}$	OOO-OOP-OPP-OOP-OOO
		$V_{dc2} > V_{dc1}$	NNN-NNO-NOO-NNO-NNN
	2	$V_{dc1} > V_{dc2}$	OOP-OPP-NOP-OPP-OOP
		$V_{dc2} > V_{dc1}$	NNO-NOO-NOP-NOO-NNO
	3	$V_{dc1} > V_{dc2}$	OPP-NPP-NOP-NPP-OPP
		$V_{dc2} > V_{dc1}$	NOO-NOP-NPP-NOP-NOO
	4	$V_{dc1} > V_{dc2}$	OOP-NOP-NNP-NOP-OOP
		$V_{dc2} > V_{dc1}$	NNO-NNP-NOP-NNP-NNO
5	1	$V_{dc1} > V_{dc2}$	OOO-OOP-POP-OOP-OOO
		$V_{dc2} > V_{dc1}$	NNN-NNO-ONO-NNO-NNN
	2	$V_{dc1} > V_{dc2}$	OOP-POP-ONP-POP-OOP
		$V_{dc2} > V_{dc1}$	NNO-ONO-ONP-ONO-NNO
	3	$V_{dc1} > V_{dc2}$	OOP-ONP-NNP-ONP-OOP
		$V_{dc2} > V_{dc1}$	NNO-NNP-ONP-NNP-NNO
	4	$V_{dc1} > V_{dc2}$	POP-PNP-ONP-PNP-POP
		$V_{dc2} > V_{dc1}$	ONO-ONP-PNP-ONP-ONO
6	1	$V_{dc1} > V_{dc2}$	OOO-POO-POP-POO-OOO
		$V_{dc2} > V_{dc1}$	NNN-ONN-ONO-ONN-NNN
	2	$V_{dc1} > V_{dc2}$	POP-POO-PNO-POO-POP
		$V_{dc2} > V_{dc1}$	ONO-ONN-PNO-ONN-ONO
	3	$V_{dc1} > V_{dc2}$	POP-PNP-PNO-PNP-POP
		$V_{dc2} > V_{dc1}$	ONO-PNO-PNP-PNO-ONO
	4	$V_{dc1} > V_{dc2}$	POO-PNO-PNN-PNO-POO
		$V_{dc2} > V_{dc1}$	ONN-PNN-PNO-PNN-ONN

Here, $I_{POO} = I_m \cos(\alpha - \varphi)$, $I_{PPO} = -I_m \cos(\alpha - \varphi - 4\pi/3)$, and T_a , T_b are referred from (8). Now, as the total inverter current is composed of the average load current, supplied by battery, and RMS value of ripple current, which is supplied by capacitor, the RMS capacitor current (I_{caprms}) can be

calculated as

$$I_{caprms} = \sqrt{I_{invrms}^2 - I_{invavg}^2}$$

$$I_{caprms} = \frac{I_m}{2} \sqrt{-3 \cdot m^2 \cos^2(\varphi) + \frac{2 \cdot m(4 \cdot \cos^2(\varphi) + 1)}{\pi}}. \quad (12)$$

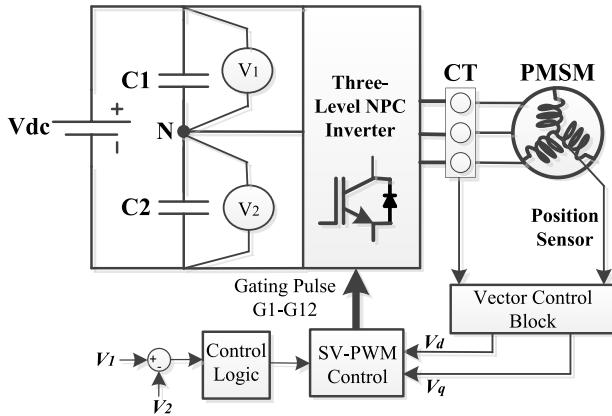


Fig. 7. Three-level inverter and control strategy model.

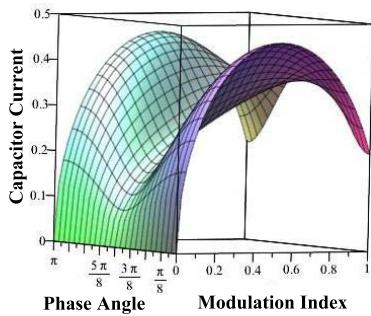


Fig. 8. Two-level inverter capacitor current RMS value.

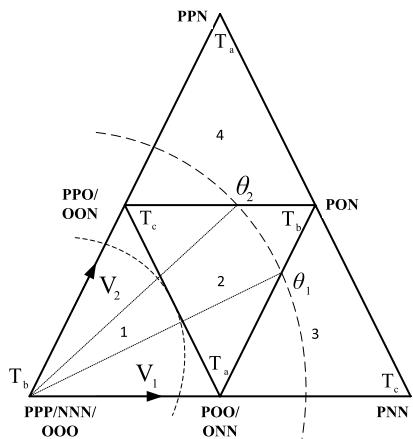


Fig. 9. Sector-I, with four subsectors.

As is clear from (12), RMS value of capacitor current is a function of modulation index, m , and the power factor angle, φ . Fig. 8 shows the variation in RMS ripple current, owing to change in m and φ , while keeping the peak load current (I_m) at unity. It can be observed that capacitor current reaches its peak value, when m reaches approximately 0.5.

B. Three-Level Inverter Capacitor Current

Fig. 9 shows the vector diagram of sector I, with four subsectors. When m is in between 0 and 0.5, the reference vector lays in subsector one; and above that value, it will

use subsector 2, 3, or 4. As seen in subsector I, there exist four small voltage vectors, which are redundant. Either the positive one can be used, which uses the upper capacitor, or the negative one could be used, which uses the lower capacitor. In a switching cycle, to keep the voltage in the two capacitors balanced both the voltage vectors are used equally, which is valid for other subsectors as well. To calculate the capacitor current, sector I is divided into two regions. Region I includes subsector 1 and region II includes subsectors 2, 3, and 4. For this analysis, the first capacitor current is considered. As in the balanced condition, both the capacitor voltages should be equal; the two capacitor currents will be symmetrical as well.

1) *Region I*: As shown in Fig. 9 subsector 1, to keep the two capacitor voltages balanced, POO/OON and PPO/OON vectors have to be used equally. As ONN and OON vectors are using only the lower capacitor, to calculate the upper capacitor RMS current, only the POO and PPO vectors are considered. The RMS capacitor current calculation is shown in (13) and (14), with the same procedure followed, as that for the two-level inverter. The time period for which redundant voltage vectors (POO/PPO) will be applied can be calculated by their corresponding time period shown in Table III and multiplication with 0.5, to equally distribute the time period between the upper and lower capacitors. For null, medium and large voltage vectors, full time period will be considered, because only one voltage vector is available

$$\begin{aligned} I_{\text{invavg}} &= \left(\frac{3}{\pi}\right) \int_0^{\frac{\pi}{3}} ((I_{\text{poo}} \cdot T_a \cdot 0.5) + (I_{\text{ppo}} \cdot T_c \cdot 0.5) \\ &\quad + (0 \cdot T_b)) d\alpha \\ \therefore I_{\text{invavg}} &= \frac{2.7206 \cdot I_m \cdot m \cdot \cos(\varphi)}{\pi} \end{aligned} \quad (13)$$

$$\begin{aligned} I_{\text{invrms}} &= \sqrt{\left(\frac{3}{\pi}\right) \int_0^{\frac{\pi}{3}} ((I_{\text{poo}}^2 \cdot T_a \cdot 0.5) + (I_{\text{ppo}}^2 \cdot T_c \cdot 0.5) + (0 \cdot T_b)^2) d\alpha} \\ \therefore I_{\text{invrms}} &= I_m \sqrt{0.31830 \cdot m \cdot (2 \cdot \cos^2(\varphi) + 0.5)}. \end{aligned} \quad (14)$$

From (13) and (14), RMS capacitor current can be calculated as

$$\begin{aligned} I_{\text{caprms}} &= I_m \sqrt{-m \cdot (0.7499 \cdot m \cdot \cos^2(\varphi) - 0.6366 \cdot \cos^2(\varphi) - 0.1591)}. \end{aligned} \quad (15)$$

Here, $I_{\text{PPO}} = I_m \cos(\alpha - \varphi)$, $I_{\text{POO}} = -I_m \cos(\alpha - \varphi - 4\pi/3)$, $\alpha = \omega t$, and φ is the phase angle leg.

2) *Region II*: When the reference vector is in region-II, the trajectory will cross the three subsectors 2, 3, and 4. Let us assume the reference voltage vector will cross the subsectors at θ_1 and θ_2 ; hence, the calculation for total average and RMS current of the inverter positive dc-bus can be seen in (16) and (17), shown at the bottom of the next page. The total RMS ripple current supplied by capacitor is shown in (18), at the bottom of the next page. Fig. 10 shows the variation in capacitor currents during change in m . It can be observed that the peak capacitor current is same as two-level capacitor current value. Hence, during the design of capacitor current rating for the three-level inverter, the RMS current rating

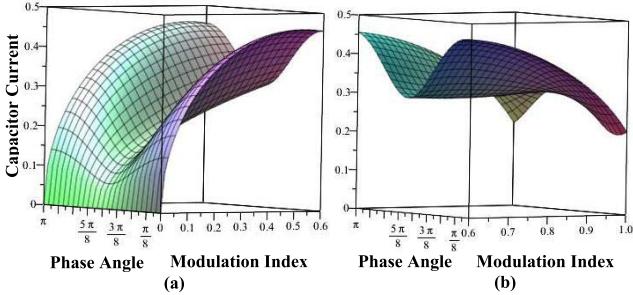


Fig. 10. RMS capacitor current in three-level inverter, for (a) $m = 0$ to 0.6 and (b) 0.6–1.0.

will be considered the same as that of the two-level inverter. However, the voltage will be half of the dc-link voltage.

From (16) and (17), RMS capacitor current can be calculated as (18).

Here, $\theta_1 = \pi/3 - \sin^{-1}(1/2 \cdot m)$, $\theta_2 = \pi/3 - (\pi/3 - \sin^{-1}(1/2 \cdot m))$, $I_{pon} = I_m \cos(\alpha - \varphi)$, $I_{pnn} = I_m \cos(\alpha - \varphi)$ and $I_{ppn} = -I_m \cos(\alpha - \varphi - 4\pi/3)$.

When m lies between regions I and II, it uses vectors from both subsector 1 and 2. For the sake of simplicity of

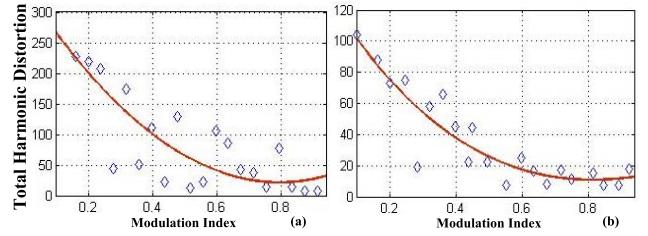


Fig. 11. (a) Two-level and (b) three-level inverter phase voltage total harmonic distortion (%THD_v) comparison.

calculation, the third region is not considered for RMS capacitor current calculation. This is clearly depicted in regions I and II. For this reason, a discontinuity is observed at around $m = 0.6$. Moreover, film capacitors are used for dc-link capacitors, which have very low ESR. So, effects of ESR are also not considered for this paper.

V. SIMULATION RESULTS

All the simulations are performed in MATLAB/Simulink platform. Figs. 11 and 12 show the total harmonic distortion

$$\begin{aligned} I_{\text{invavg}} &= \left(\frac{3}{\pi} \right) \left(\int_0^{\theta_1} (I_{\text{poo}} \cdot T_a \cdot 0.5 + I_{\text{pnn}} \cdot T_c + I_{\text{pon}} \cdot T_b) d\alpha + \int_{\theta_1}^{\theta_2} (I_{\text{poo}} \cdot T_a \cdot 0.5 + I_{\text{pon}} \cdot T_b + I_{\text{ppo}} \cdot T_c \cdot 0.5) d\alpha \right. \\ &\quad \left. + \int_{\theta_2}^{\frac{\pi}{3}} (I_{\text{ppo}} \cdot T_c \cdot 0.5 + I_{\text{pon}} \cdot T_b + I_{\text{ppn}} \cdot T_a) d\alpha \right) \\ \therefore I_{\text{invavg}} &= \frac{I_m}{m} \left(m^2 \cdot \left(0.866 \cdot \cos(\varphi) + \arcsin \left(\frac{0.5}{m} \right) \cdot (0.477 \cdot \sin(\varphi) - 6.36e^{-10} \cos(\varphi)) \right) \right. \\ &\quad \left. + m \cdot 0.119 \cdot \sin(\varphi) \cdot \sqrt{4 \cdot m^2 - 1} - 0.2067 \cdot \sin(\varphi) \right) \end{aligned} \quad (16)$$

$$I_{\text{inrvms}} = \sqrt{\left(\frac{3}{\pi} \right) \left(\int_0^{\theta_1} (I_{\text{poo}}^2 \cdot T_a \cdot 0.5 + I_{\text{pnn}}^2 \cdot T_c + I_{\text{pon}}^2 \cdot T_b) d\alpha + \int_{\theta_1}^{\theta_2} (I_{\text{poo}}^2 \cdot T_a \cdot 0.5 + I_{\text{pon}}^2 \cdot T_b + I_{\text{ppo}}^2 \cdot T_c \cdot 0.5) d\alpha \right.} \\ \left. + \int_{\theta_2}^{\frac{\pi}{3}} (I_{\text{ppo}}^2 \cdot T_c \cdot 0.5 + I_{\text{pon}}^2 \cdot T_b + I_{\text{ppn}}^2 \cdot T_a) d\alpha \right)} \\ I_{\text{inrvms}} = \frac{I_m}{m} \cdot \sqrt{\left(m^3 (0.159 - 0.275 \cdot \sin(2 \cdot \varphi) + 0.636 \cdot \cos^2(\varphi)) + m^2 (\sqrt{4 \cdot m^2 - 1} \cdot (-3.18 \cdot e^{-11} \cdot \cos^2(\varphi) \right.} \\ \left. + 0.318 \cdot \sin(2 \cdot \varphi) + 0.358 \cdot \sin(2 \cdot \varphi)) + \sqrt{4 \cdot m^2 - 1} \cdot (-3.18 \cdot e^{-11} \cdot \cos^2(\varphi) - 3.18 \cdot e^{-12} \right.} \\ \left. - 0.034 \cdot \sin(2 \cdot \varphi)) - 0.059 \cdot \sin(2 \cdot \varphi) \right)} \quad (17)$$

$$I_{\text{caprms}} = \frac{I_m}{m} \cdot \sqrt{\left(m^4 \cdot \left(\arcsin \left(\frac{0.5}{m} \right)^2 \cdot (-0.227 + 0.227 \cdot \cos^2(\varphi) + 3.039 \cdot e^{-10} \cdot \sin(2 \cdot \varphi)) + \arcsin \left(\frac{0.5}{m} \right) \right. \right. \right.} \\ \left. \left. \left. \cdot (-0.416 \cdot \sin(2 \cdot \varphi) + 1.102 \cdot e^{-9} \cdot \cos^2(\varphi)) - 0.75 \cdot \cos^2(\varphi) \right) + m^3 \cdot (0.159 - 0.275 \cdot \sin(2 \cdot \varphi) \right. \right. \\ \left. \left. + 0.636 \cdot \cos^2(\varphi)) + m^2 \cdot \left(\sqrt{4 \cdot m^2 - 1} \cdot (-3.18 \cdot e^{-11} \cdot \cos^2(\varphi) + 0.113 \cdot \cos^2(\varphi) \cdot \arcsin \left(\frac{0.5}{m} \right) \right. \right. \right.} \\ \left. \left. \left. - 0.113 \cdot \arcsin \left(\frac{0.5}{m} \right) + 0.759 \cdot e^{-10} \cdot \sin(2 \cdot \varphi) \cdot \arcsin \left(\frac{0.5}{m} \right) + 0.034 \cdot \sin(2 \cdot \varphi) + \arcsin \left(\frac{0.5}{m} \right) \right. \right. \right. \\ \left. \left. \left. \cdot (-1.316 \cdot e^{-10} \cdot \sin(2 \cdot \varphi) - 0.197 \cdot \cos^2(\varphi) + 0.197 + 0.056 \cdot \cos^2(\varphi) - 0.056 + 0.537 \cdot \sin(2 \cdot \varphi)) \right) \right) \right. \\ \left. + \sqrt{4 \cdot m^2 - 1} \cdot (-0.04 \cdot \cos^2(\varphi) + 0.049 - 0.034 \cdot \sin(2 \cdot \varphi)) + 0.028 \cdot \cos^2(\varphi) - 0.059 \cdot \sin(2 \cdot \varphi) - 0.028 \right)} \quad (18)$$

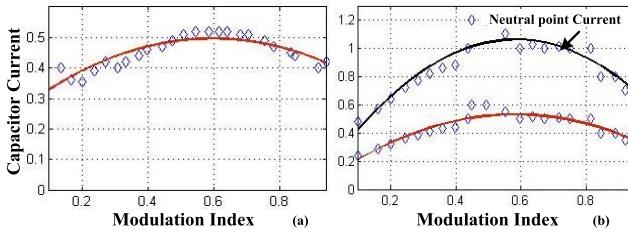


Fig. 12. (a) Two-level (a) and (b) three-level inverter RMS capacitor current comparison.

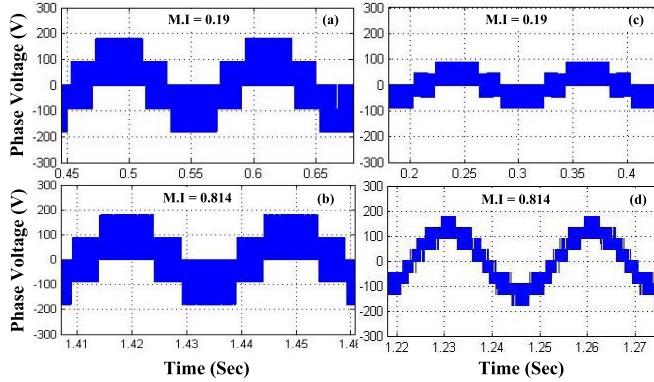


Fig. 13. Simulation results for (a) and (b) two- and (c) and (d) three-level inverter phase voltages, with low and high modulation index.

(%THD) for phase voltages applied to the machine as well as the variation in capacitor RMS current for changes in m in two- and three-level inverter. It can be observed that, in case of the three-level inverter, the harmonic distortion is almost 50% lower than that of the two-level inverter, for the same m . This significant reduction in harmonic distortion will reduce the passive component sizes, like the load side filter inductor and the EMI filter, which is used at the source side. This will also help to reduce the machine losses significantly. Capacitor current is also shown for both the inverters. It can be observed that capacitor current peak occurs near $m = 0.5$, which agrees with the analytical expression derived for capacitor current, in Section IV.

It can also be observed that the neutral current shown for three-level inverter is almost double compared with the capacitor current. The reason is that, when $m < 0.5$, the control strategy tries to use the two capacitors equally; hence, either the upper or lower capacitor current is going to flow through the neutral point, or it flows to the source from the neutral point. Again, when $m > 0.5$, the medium vector uses the neutral point. Thus, the total current that flows in the neutral wire is almost double of each individual capacitor current.

Fig. 13 shows the phase voltages for both the inverters, with low ($m = 0.19$) and high ($m = 0.814$) modulation indices. From the waveforms, it can be observe that, at low m , to produce the same reference voltage, the three-level inverter uses the lower voltage step, compared with the two-level inverter, whereas for a higher m , the three-level inverter uses more number of steps, which makes it close to sinusoidal.

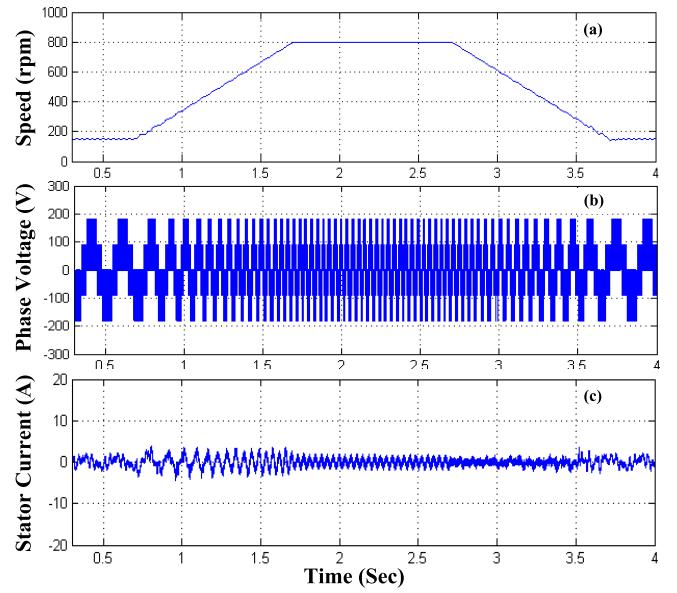


Fig. 14. Simulation results for two-level inverter, with change in speed from 15.70 to 83.77 rad/s, at no-load. (a) Motor speed. (b) Phase voltage. (c) Stator current.

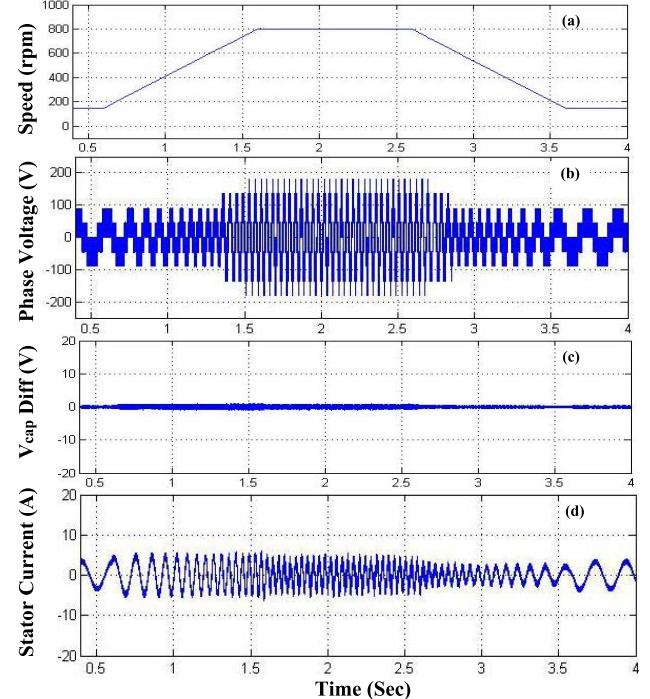


Fig. 15. Simulation results for three-level inverter, with change in speed from 15.70 to 83.77 rad/s, at no-load. (a) Motor speed. (b) Phase voltage. (c) Capacitor voltage difference. (d) Stator current.

Fig. 14 shows the performance of two-level inverter with change in speed from 15.70 to 83.77 rad/s, under no-load condition.

Fig. 15 shows the machine performance for three-level inverter with a similar speed change. It can be observed that, with increase in m for the three-level inverter, the phase-voltage steps increase, which brings the phase-voltage more toward a sinusoidal wave-shape, compared with the two-level

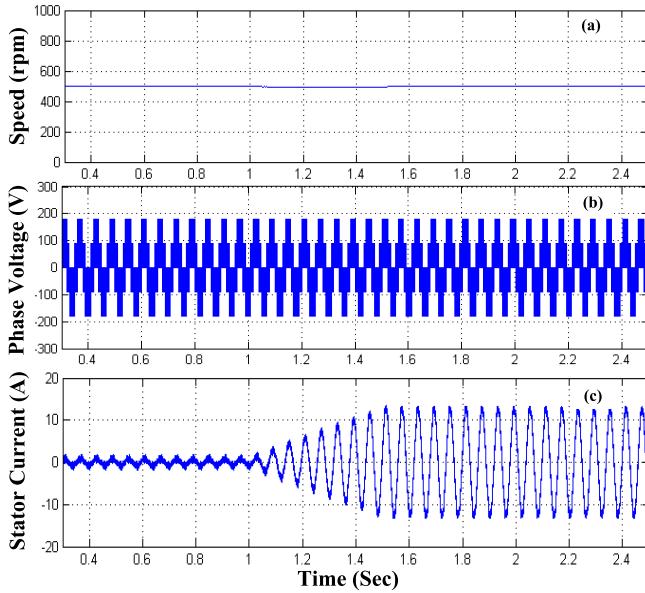


Fig. 16. Simulation results for two-level inverter, with change in load torque from 0 to 22 Nm. (a) Motor speed. (b) Phase voltage. (c) Stator current.

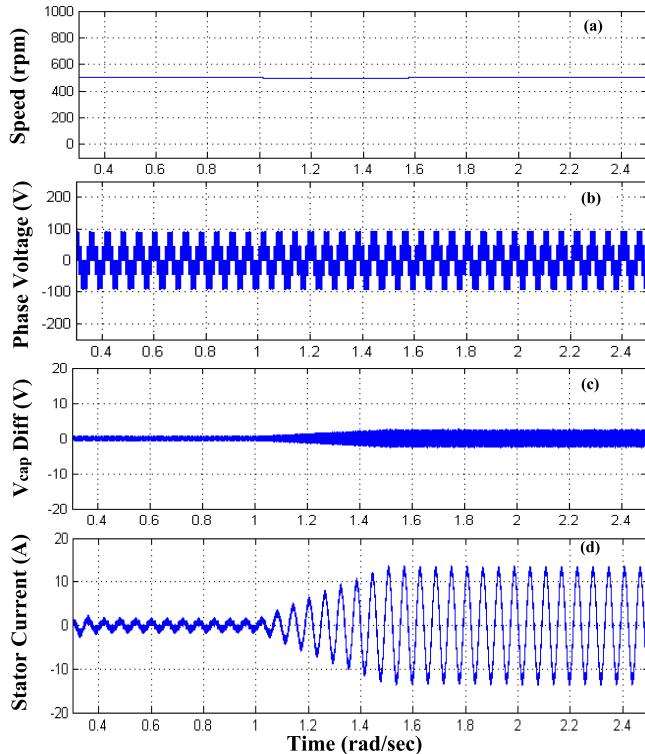


Fig. 17. Simulation results for three-level inverter, with change in load torque from 0 to 22 Nm. (a) Motor speed. (b) Phase voltage. (c) Capacitor voltage difference. (d) Stator current.

inverter. Also, owing to the increased number of voltage steps, overall dv/dt stress across power switches gets reduced. The capacitor voltage difference is even stable at transient condition and it is around 2.0 V, which is less than 1% of the total dc-link voltage.

Figs. 16 and 17 show the performance of both inverters, owing to change in load torque, from 0 to 22 Nm, while speed is kept constant at 52.359 rad/s. From the waveforms, it can

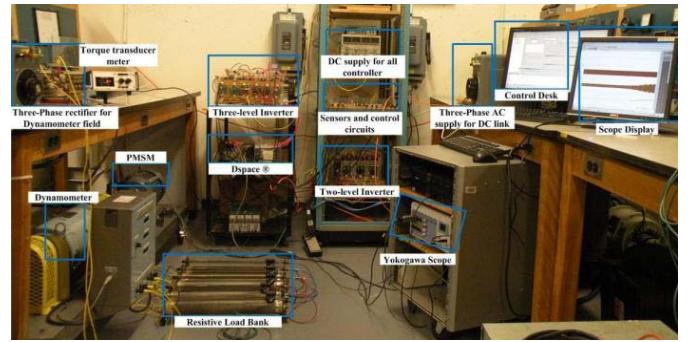


Fig. 18. Experimental laboratory setup for two- and three-level inverter.

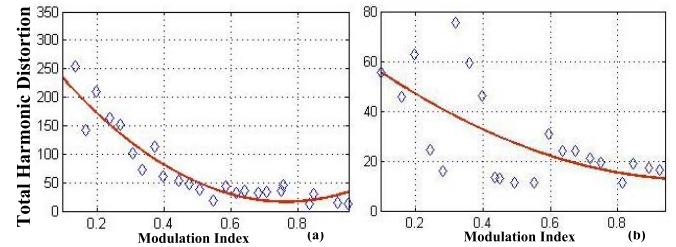


Fig. 19. (a) Two-level and (b) three-level inverter phase voltage total harmonic distortion (%THD_V) comparison.

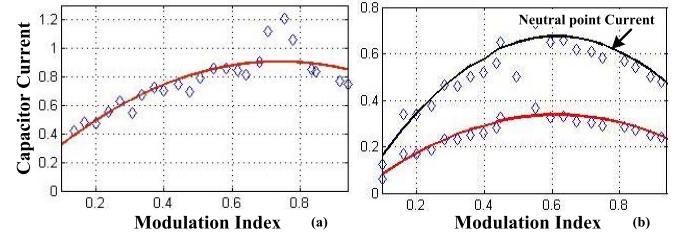


Fig. 20. (a) Two-level and (b) three-level inverter RMS capacitor current comparison.

be observed that, although the wave-shapes are similar, due to lower m , the three-level inverter voltage steps are lower than the two-level inverter. For the three-level inverter dc-link capacitor voltage difference at full load is around 4.0 V, which is again less than 2% of the total dc-link voltage. Simulation results show good steady state and transient performance of both two-level and proposed three-level SV-PWM based dc-bus voltage-balancing algorithms.

VI. EXPERIMENTAL SETUP AND TEST RESULTS

Fig. 18 shows the experimental setup for the two- and three-level inverters, which feed a surface PMSM. The control strategies are implemented using dSpace-based real-time operating system. Simulation step time was kept constant at 25 μ s and switching frequency was kept constant at 3.0 kHz. During the experimental procedure, the dc-link voltage was kept constant at 270 V. Figs. 19 and 20 show the experimental results of total harmonic distortion and capacitor current for both the inverters. It can be observed that total harmonic distortion for three-level inverter is less than 50% compared with the two-level inverter. The peak capacitor currents occur near $m = 0.5$, as proven in the analytical and simulation study. If the equations derived in Section IV are considered, it can

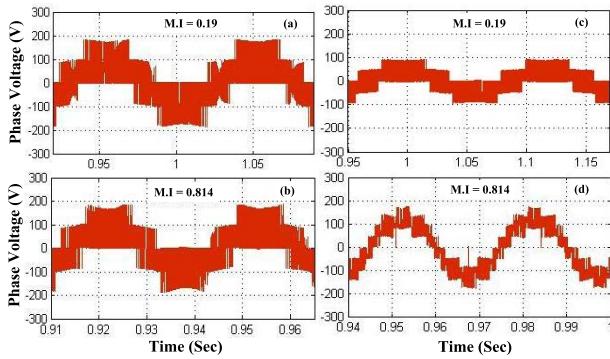


Fig. 21. Experimental results for (a) and (b) two-level and (c) and (d) three-level inverter phase voltages with low and high modulation index.

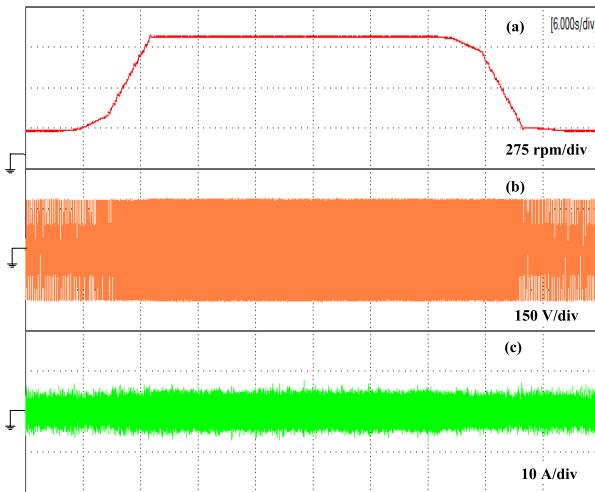


Fig. 22. Experimental results for two-level inverter with change in speed from 15.70 to 83.77 rad/s; at no load. (a) Motor speed. (b) Phase voltage. (c) Stator current.

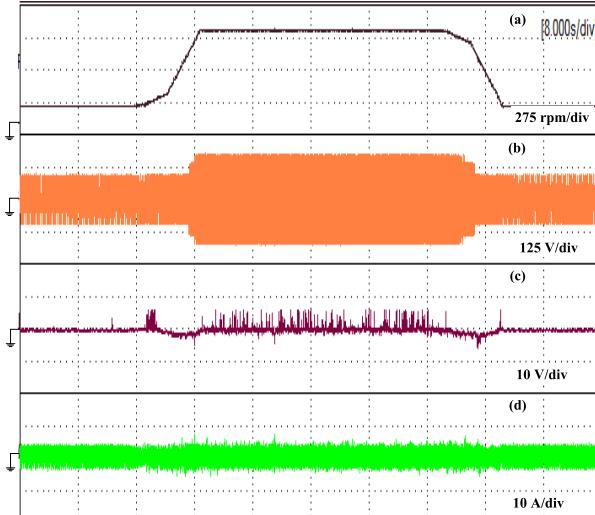


Fig. 23. Experimental results for three-level inverter, based on the new dc-link voltage balancing algorithm, with change in speed from 15.70 to 83.77 rad/s; at no load. (a) Motor speed. (b) Phase voltage. (c) Difference in two capacitor voltages. (d) Stator current.

be observed that the capacitor current wave-shape depends on m , peak load current, as well as power-factor. Thus, if the load current is kept constant, then capacitor current peak occur

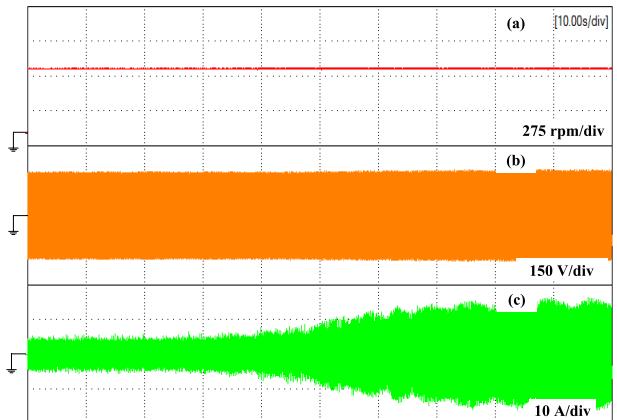


Fig. 24. Experimental results for two-level inverter with change in load torque from 0 to 22.0 Nm. (a) Motor speed. (b) Phase voltage. (c) Stator current.

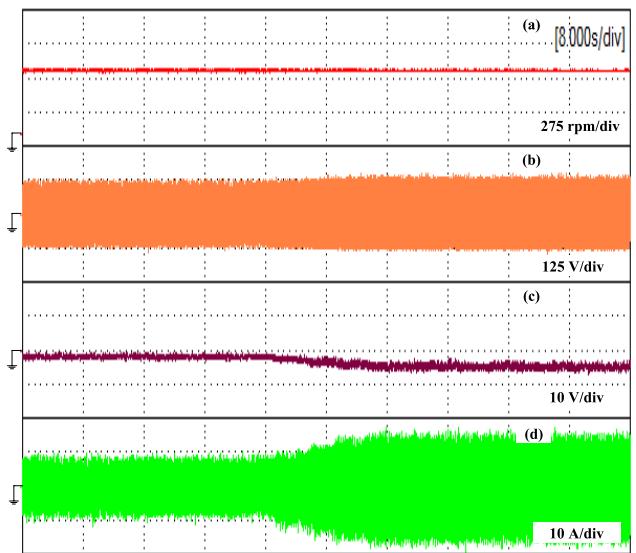


Fig. 25. Experimental results for three-level inverter using the new dc-link voltage balancing algorithm, with change in load torque from 0 to 22.0 Nm. (a) Motor speed. (b) Phase voltage. (c) Difference in two capacitor voltages. (d) Stator current.

at $m = 0.5$. However, in case of the machine no-load losses, such as friction and windage losses, keep increasing with speed. Hence, the current supplied by the inverter increases with higher m , which in turn, shifts the peak capacitor current to greater than 0.5. This occurrence can be observed from the wave-shapes collected from the experimental data.

Fig. 21 shows the experimental wave shapes for both the inverters output voltages, for low as well as high m . It is clear, that the obtained wave-shapes are agreeable with the simulation results, shown earlier in Fig. 13. At higher m , the three-level inverter has more number of steps, compared with two-level inverter, which helps to reduce the total harmonic distortion and voltage transients occurs across the switching devices.

Figs. 22 and 23 show the performance of the machine with change of speed from 15.70 to 83.77 rad/s, under no-load conditions for both two- and three-level inverters. As is clear, the number of voltage steps has increased with speed, for the three-level inverter. Furthermore, the dc-link capacitor voltage

TABLE V
MACHINE PARAMETERS

PMSM rating	6.0 kW
Stator Resistance (r)	0.1718 Ω
Stator Self Inductances (L_d, L_q)	0.00336 H, 0.00336 H
Flux Linkage (λ)	0.591 Wb/m ²
Motor Inertia (J)	0.03334 kg-m ²

difference is maintained at less than 1% of the total dc-bus voltage.

Figs. 24 and 25 show the performance of the machine with change in load torque, from 0 to 22 Nm. Experimental test results show good transient and steady state performance of the system for both inverter topologies. The dc-bus capacitor voltage difference for the three-level inverter is also less than 2% of the total dc-link voltage, which shows good controllability of the proposed system.

Table V shows all the machine parameters for permanent magnet synchronous machine, used for simulation and experimental studies.

VII. CONCLUSION

This paper presented a detailed comparative study between a two-level and a three-level dc/ac EV traction inverter, with analytical calculation of capacitor currents and total harmonic distortion of phase voltages. A novel dc-link voltage balancing strategy, with low switching losses is proposed, which keeps the voltage difference between the two dc-link capacitors at a desired level. This balancing strategy was developed based on NTV scheme, for a neutral point clamped three-level dc/ac traction inverter. Simulation and experimental test results show a 50% reduction in total harmonics for the three-level inverter using the proposed control strategy. Moreover, performance of the proposed balancing scheme is examined by carrying out extensive simulations and experimental studies on a surface-mounted permanent magnet synchronous machine for wide speed and torque variations. Results show satisfactory performance of the proposed system.

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