

# HD74LS155

## Dual 2-line-to-4-line Decoders / Demultiplexers

REJ03D0440-0200

Rev.2.00

Feb.18.2005

This circuit features dual 1-line-to-4-line demultiplexer with individual strobes and common binary-address input. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

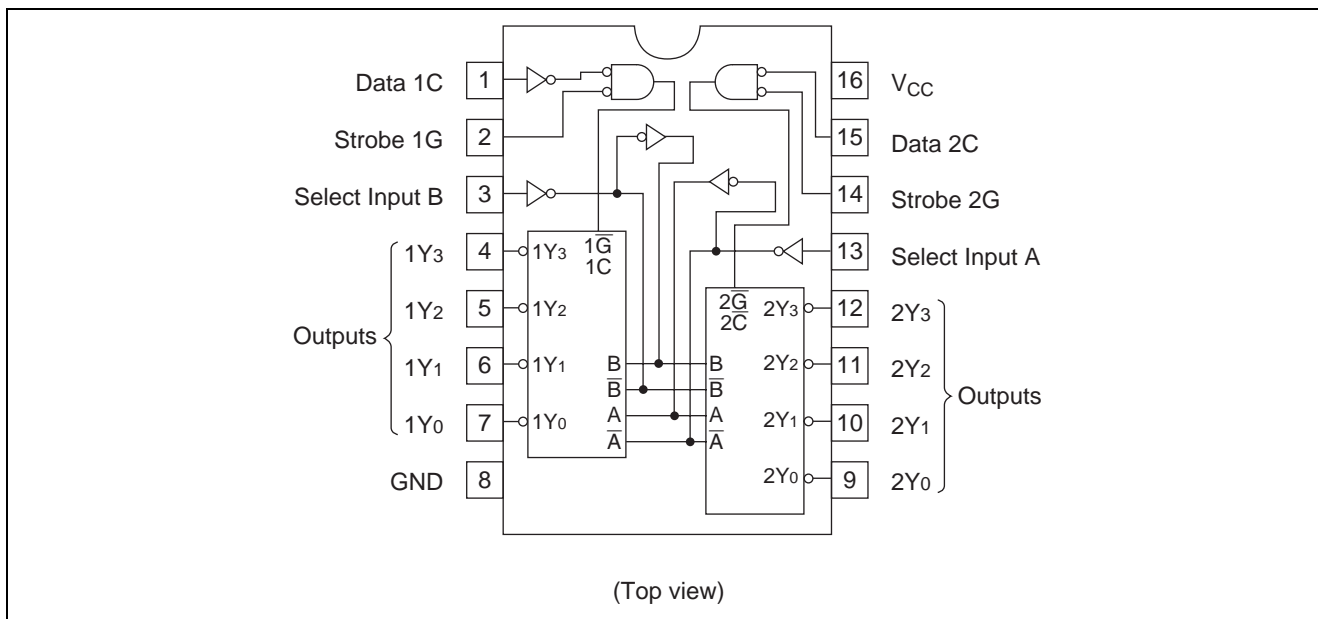
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS155P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



## Function Table

### • 2-line-to-4-line Decoder / 1-line-to-4-line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data	1Y <sub>0</sub>	1Y <sub>1</sub>	1Y <sub>2</sub>	1Y <sub>3</sub>
B	A	1G	1C				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

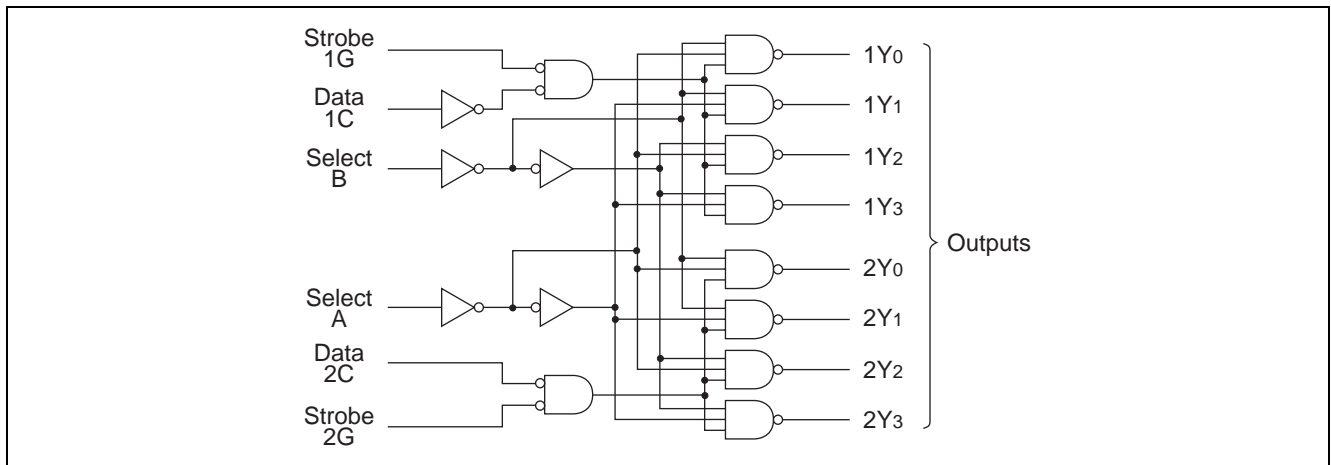
Inputs				Outputs			
Select		Strobe	Data	2Y <sub>0</sub>	2Y <sub>1</sub>	2Y <sub>2</sub>	2Y <sub>3</sub>
B	A	2G	2C				
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

### • 3-line-to-8-line Decoder / 1-line-to-8-line Demultiplexer

Inputs				Outputs							
Select			Strobe Data	0	1	2	3	4	5	6	7
C	B	A	G	2Y <sub>0</sub>	2Y <sub>1</sub>	2Y <sub>2</sub>	2Y <sub>3</sub>	1Y <sub>0</sub>	1Y <sub>1</sub>	1Y <sub>2</sub>	1Y <sub>3</sub>
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

- Notes: 1. C ; input 1C and 2C connected together  
 2. G ; inputs 1G and 2G connected together  
 3. H ; high level, L ; low level, X ; irrelevant

## Block Diagram



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	μA
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	°C

## Electrical Characteristics

( $T_a = -20$  to  $+75$  °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	$V_{IH}$	2.0	—	—	V	
	$V_{IL}$	—	—	0.8	V	
Output voltage	$V_{OH}$	2.7	—	—	V	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -400$ μA
	$V_{OL}$	—	—	0.4	V	$I_{OL} = 4$ mA, $V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V
Input current	$I_{IH}$	—	—	20	μA	$V_{CC} = 5.25$ V, $V_I = 2.7$ V
	$I_{IL}$	—	—	-0.4	mA	$V_{CC} = 5.25$ V, $V_I = 0.4$ V
	$I_I$	—	—	0.1	mA	$V_{CC} = 5.25$ V, $V_I = 7$ V
Short-circuit output current	$I_{OS}$	-5	—	-42	mA	$V_{CC} = 5.25$ V
Supply current**	$I_{CC}$	—	6.1	10	mA	$V_{CC} = 5.25$ V
Input clamp voltage	$V_{IK}$	—	—	-1.5	V	$V_{CC} = 4.75$ V, $I_{IN} = -18$ mA

Notes: \*  $V_{CC} = 5$  V,  $T_a = 25$  °C

\*\*  $I_{CC}$  is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

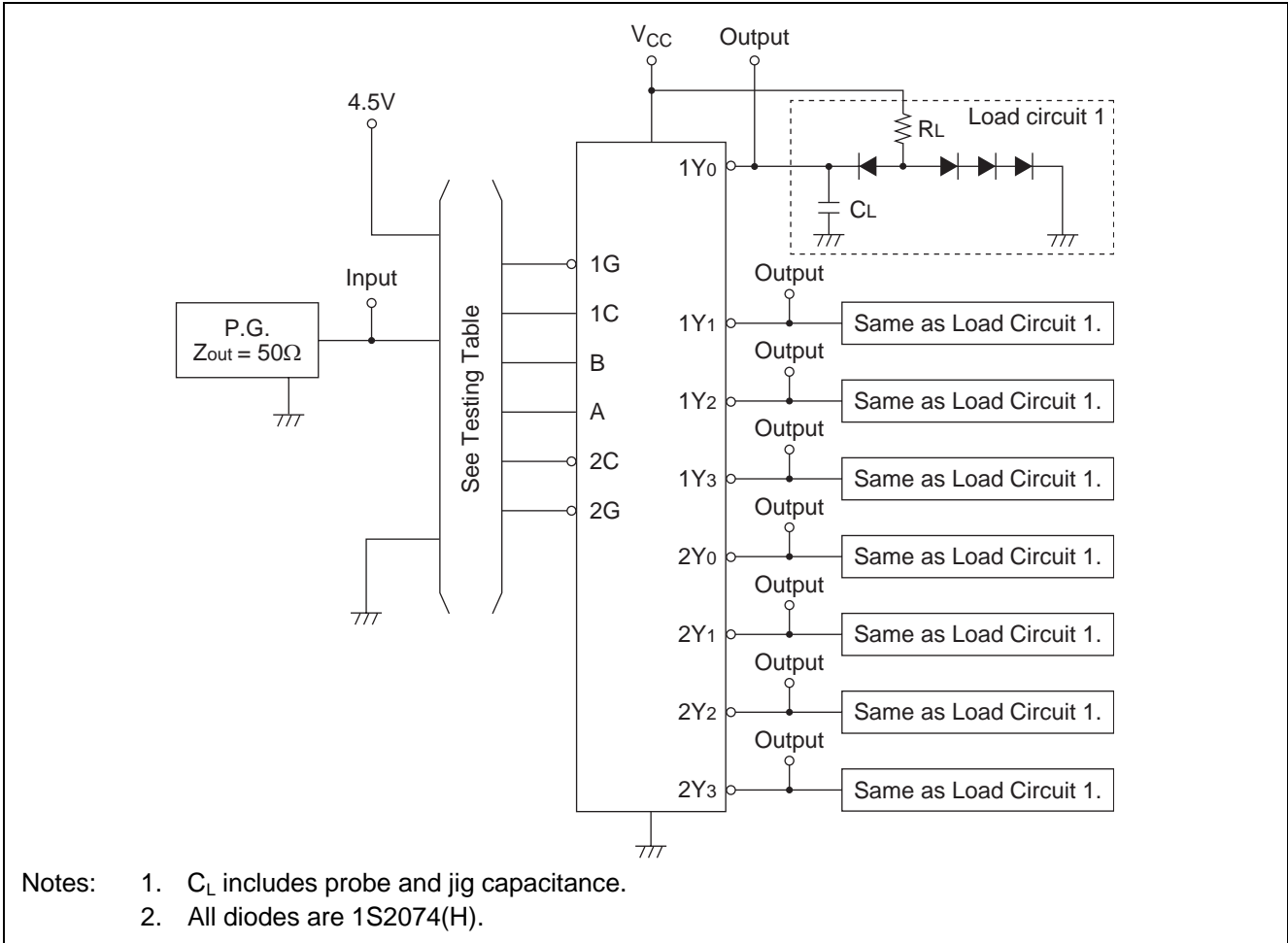
# Switching Characteristics

( $V_{CC} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )

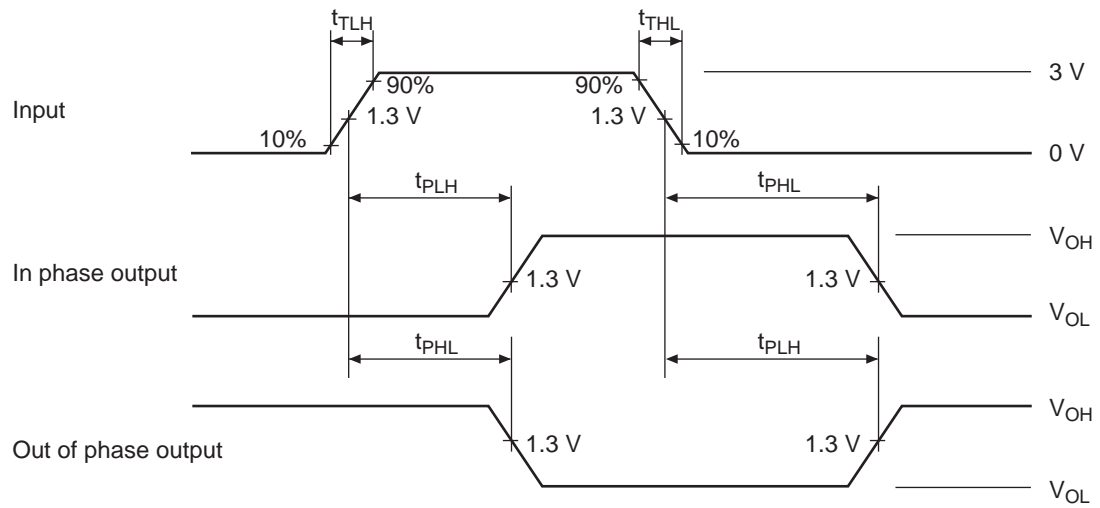
Item	Symbol	Inputs	Output	Levels of logic	min.	typ.	max.	Unit	Condition
Propagation delay time	$t_{PLH}$	A, B, 2C 1G or 2G	Y	2	—	10	15	ns	$C_L = 15\text{ pF}$ , $R_L = 2\text{ k}\Omega$
	$t_{PHL}$				—	19	30	ns	
	$t_{PLH}$	A or B	Y	3	—	17	26	ns	
	$t_{PHL}$				—	19	30	ns	
	$t_{PLH}$	1C	Y	3	—	18	27	ns	
	$t_{PHL}$				—	18	27	ns	

## Testing Method

### Test Circuit

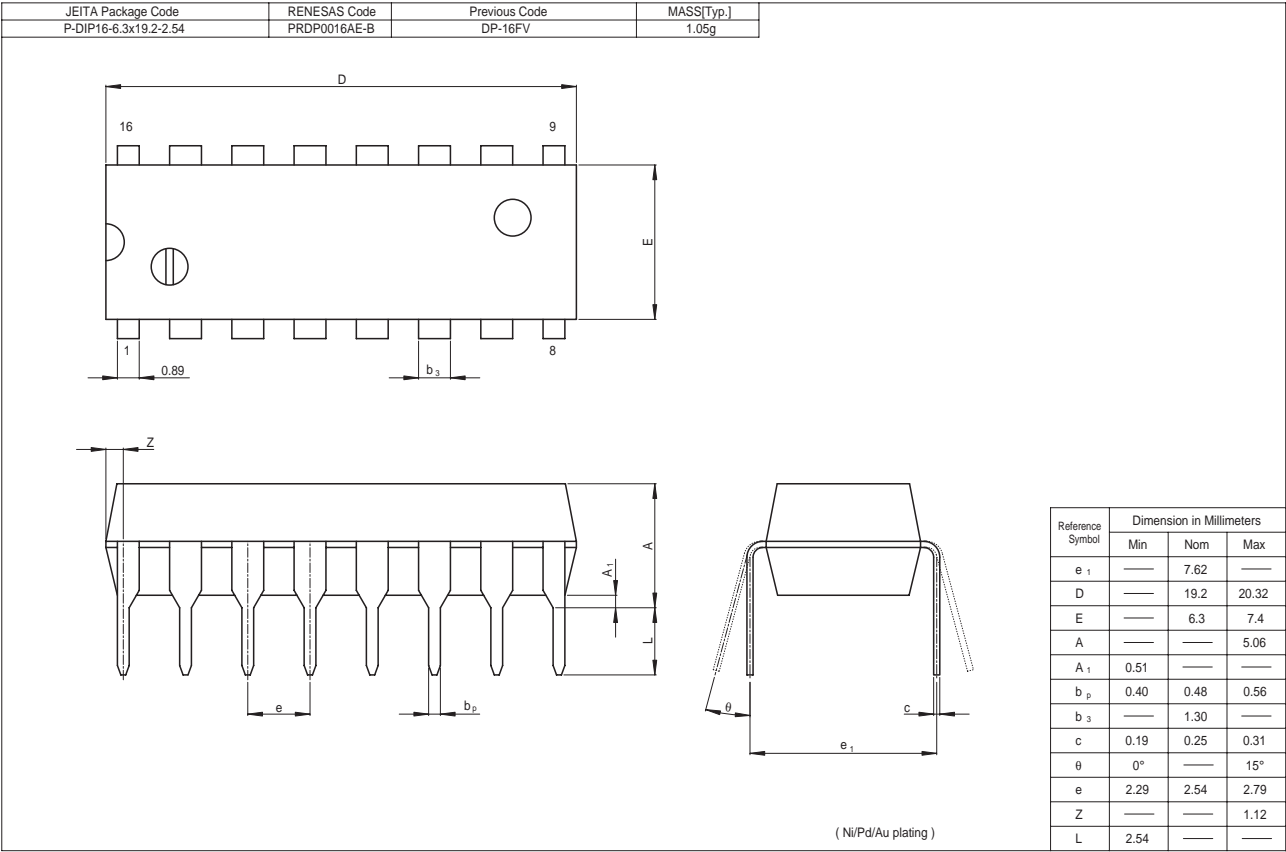


Waveform



Note: Input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz, duty cycle 50%

Package Dimensions



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