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6 # Clock signal
7 set_property PACKAGE_PIN W5 [get_ports clk]
8     set_property IOSTANDARD LVCMOS33 [get_ports clk]
9     create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
10
11 # Switches
12 set_property PACKAGE_PIN V17 [get_ports {bcd0[0]}]
13     set_property IOSTANDARD LVCMOS33 [get_ports {bcd0[0]}]
14 set_property PACKAGE_PIN V16 [get_ports {bcd0[1]}]
15     set_property IOSTANDARD LVCMOS33 [get_ports {bcd0[1]}]
16 set_property PACKAGE_PIN W16 [get_ports {bcd0[2]}]
17     set_property IOSTANDARD LVCMOS33 [get_ports {bcd0[2]}]
18 set_property PACKAGE_PIN W17 [get_ports {bcd0[3]}]
19     set_property IOSTANDARD LVCMOS33 [get_ports {bcd0[3]}]
20 set_property PACKAGE_PIN W15 [get_ports {bcd1[0]}]
21     set_property IOSTANDARD LVCMOS33 [get_ports {bcd1[0]}]
22 set_property PACKAGE_PIN V15 [get_ports {bcd1[1]}]
23     set_property IOSTANDARD LVCMOS33 [get_ports {bcd1[1]}]
24 set_property PACKAGE_PIN W14 [get_ports {bcd1[2]}]
25     set_property IOSTANDARD LVCMOS33 [get_ports {bcd1[2]}]
26 set_property PACKAGE_PIN W13 [get_ports {bcd1[3]}]
27     set_property IOSTANDARD LVCMOS33 [get_ports {bcd1[3]}]
28 set_property PACKAGE_PIN V2 [get_ports {bcd2[0]}]
29     set_property IOSTANDARD LVCMOS33 [get_ports {bcd2[0]}]
30 set_property PACKAGE_PIN T3 [get_ports {bcd2[1]}]
31     set_property IOSTANDARD LVCMOS33 [get_ports {bcd2[1]}]
32 set_property PACKAGE_PIN T2 [get_ports {bcd2[2]}]
33     set_property IOSTANDARD LVCMOS33 [get_ports {bcd2[2]}]
34 set_property PACKAGE_PIN R3 [get_ports {bcd2[3]}]
35     set_property IOSTANDARD LVCMOS33 [get_ports {bcd2[3]}]
36 set_property PACKAGE_PIN W2 [get_ports {bcd3[0]}]
37     set_property IOSTANDARD LVCMOS33 [get_ports {bcd3[0]}]
38 set_property PACKAGE_PIN U1 [get_ports {bcd3[1]}]
39     set_property IOSTANDARD LVCMOS33 [get_ports {bcd3[1]}]
40 set_property PACKAGE_PIN T1 [get_ports {bcd3[2]}]
41     set_property IOSTANDARD LVCMOS33 [get_ports {bcd3[2]}]
42 set_property PACKAGE_PIN R2 [get_ports {bcd3[3]}]
43     set_property IOSTANDARD LVCMOS33 [get_ports {bcd3[3]}]

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