```
# Clock signal
set_property PACKAGE_PIN W5 [get_ports clk]
    set_property IOSTANDARD LVCMOS33 [get_ports clk]
    create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

# Switches
set_property PACKAGE_PIN V17 [get_ports {bcd0[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd0[0]}]
set_property PACKAGE_PIN V16 [get_ports {bcd0[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd0[1]}]
set_property PACKAGE_PIN W16 [get_ports {bcd0[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd0[2]}]
set_property PACKAGE_PIN W17 [get_ports {bcd0[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd0[3]}]
set_property PACKAGE_PIN W15 [get_ports {bcd1[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd1[0]}]
set_property PACKAGE_PIN V15 [get_ports {bcd1[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd1[1]}]
set_property PACKAGE_PIN W14 [get_ports {bcd1[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd1[2]}]
set_property PACKAGE_PIN W13 [get_ports {bcd1[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd1[3]}]
set_property PACKAGE_PIN V2 [get_ports {bcd2[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd2[0]}]
set_property PACKAGE_PIN T3 [get_ports {bcd2[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd2[1]}]
set_property PACKAGE_PIN T2 [get_ports {bcd2[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd2[2]}]
set_property PACKAGE_PIN R3 [get_ports {bcd2[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd2[3]}]
set_property PACKAGE_PIN W2 [get_ports {bcd3[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd3[0]}]
set_property PACKAGE_PIN U1 [get_ports {bcd3[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd3[1]}]
set_property PACKAGE_PIN T1 [get_ports {bcd3[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd3[2]}]
set_property PACKAGE_PIN R2 [get_ports {bcd3[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {bcd3[3]}]
```