CSE4117 Fall 2019 Final Exam Question 1

Due and Demo Date 23.01.2020 Thursday from 11:00 to 17:00

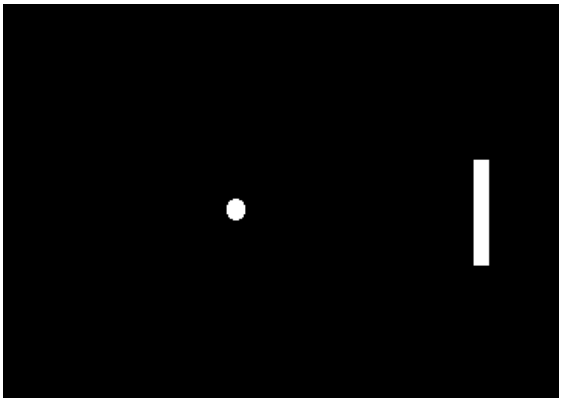
This exam will form 40/100 of your final exam grade.

Part A (14 Pts)

In this question, you will design a PONG game on a VGA monitor.

Your game must include a racket and a **circular** ball.

The game is lost when the ball exits the right side of the screen. The ball will bounce from the left, top and bottom side of the screen. At the start of the game, the ball will start from the center of the screen. When the game is lost, the ball will immediately return to the center of the screen and the game will restart again.

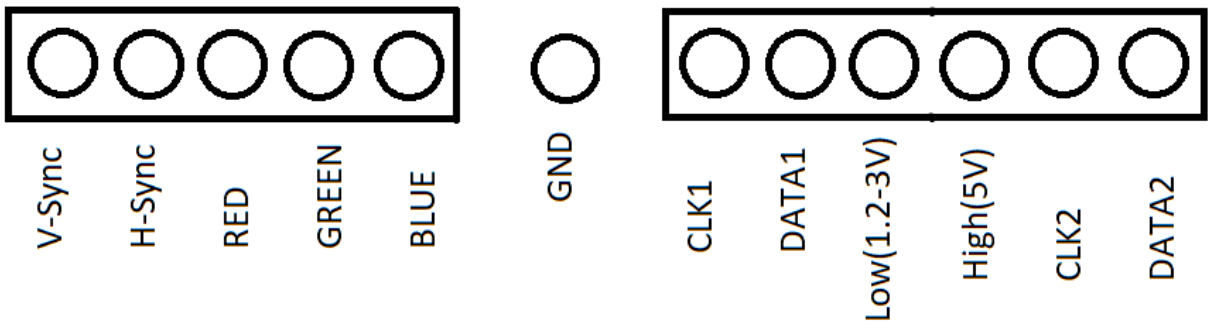


At the subsequent restarts of the game, the ball will shoot off from the angles 45, 135, 225 and 315 degrees sequentially.

Half a minute after the game starts, the speed of the ball will double and the size of the racket will halve, if the game is not already lost.

Up and down movements of the racket should be controlled by the push buttons on the FPGA kit. These push buttons are debounced, so no need to worry about debouncing them.

Your ball must be circular. How a circular ball is created in a Verilog context is explained in your Verilog Textbook. (FPGA PROTOTYPING BY VERILOG EXAMPLES, Pong Chu, pp 325)



Pin Laylout of the Card given to you. You need not use the signals on the right (ie. Clk1, data1 etc.)

Part B (10 Pts)

This question will be done by using Logisim only (ie, no Verilog). It is a continuation of Q1 in your 2nd homework:

You will design system which will add a timer and one more four-digit 7-segment display to the system you have designed on the 2nd homework.

The timer will have a 16-bit register. At every second, it will increment this register and send an interrupt to the CPU. After receiving the interrupt, the CPU will read this register and display it on the second 7-segment display.
The timer will count the seconds by counting the clock.
You must use the latest CPU shown in the class which is capable of handling interrupts. You must also use a PIC.
Your system must work at 4KHz clock of Logisim. When the system starts, I must be able to see the timer incrementing at every second in one seven segment display, while I must be able to perform additions by using the switchboard and the other 4-bit 7-segment display.

All the results will be displayed in hexadecimal (which is easier for you)

Part C (16 Pts)

You have to redo the 2nd question of the 2nd homework i.e. the "pocket calculator" in Verilog. The calculations must be executed in software on the CPU (ie. In assembly code, not in Verilog)