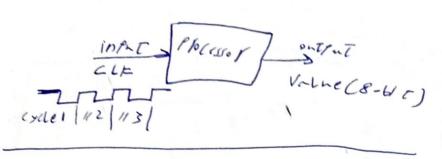
8-BIT microplocessed Lessin using VHDL



mainty components

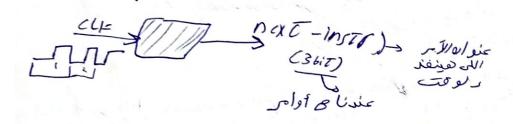
-> PlogY-m Counter [16]

-> Instruction mimols [cach isser 8-610]

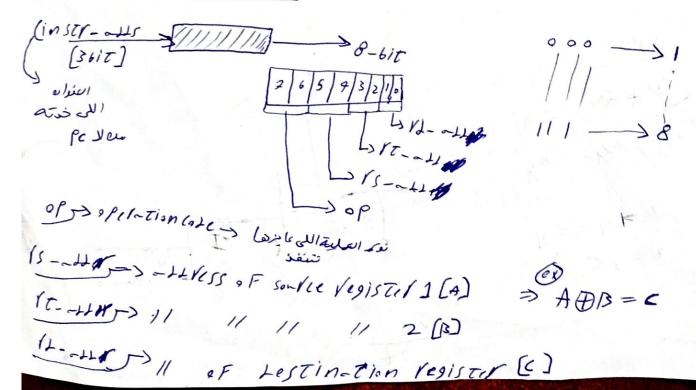
-> 4 registers (e-ch reg 8-617) -> ALU.

-> control unic.

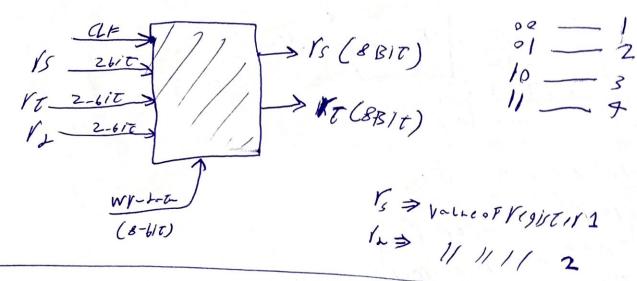
1 floghem constil (PC)



2) Instruction memory



Registeds File



@ ALU

BGO For

Solward [A & B = c]

Solward [A + B = c]

Solward [A + B = c]

Solward [A + PL. all = B]

Sol

EV .	
5 CONTROL WAIT	
1	
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Same = all	ess of Lection
SSI Const-nt date = add 10	contraction legs
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convice	Tolde of 192 To Consision
and and	diess of des levister - Cant data Colster 2.
m / v c	"CUBJ2" TO KILLE CONLO
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~ 24°C>V////	Lestination Flom Leant Lestination to Laco 1 sciloster 2. Laco of Lestination to Constant Late 1 scientes 2. Lestination to 1 scientes 1 scientes 2. Les 1 scientes 2 legister to Value con be alled to le
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55) LeFault Lestination alles	
DS) HISTINATION address	/Fsell=1 => x= 3
	PP-117
Mhx (2)	/F sel=1 => x= ~ } J== b ≠ 500/ [P=1]
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b 8612	
and default data (B)	IF Sel=1=> 9 == 6 (ye=a) 500
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grantput buta	26
Clane un	
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Bail is to larget ble also,	date // date
- 476	The state of the s
	address 2
	(7-hit) constant
	(2-pit) (000000 8 Tagain)
	& Lacain]

Control Wast

2615 alu-of 145 reg- 75 T) > selection line of muxy

[HS reg-75 T) > selection line of muxe inst/2-610

