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Synplify Pro® for Lattice Release Notes

Verification Continuum™

Version Q-2020.03L-SP1, November 2020

Release Note Topics

About this Release

Release Q-2020.03L-SP1 includes software improvements and enhancements to the Synplify Pro® for Lattice product.

Feature and Enhancement Summary

The following table summarizes features and enhancements.

Feature	Description
Q-2020.03L-SP1 Features	
Text-based Find and Filter	The new HDL Analyst traverses the text-based netlist quickly, to extract and display hierarchical instance data. This reduces the time taken to display the design hierarchy and view custom instances on demand. For details, see User Guide->Analyzing with HDL Analyst->Finding Objects->Browsing to Find Objects in HDL Analyst Views->Browsing With the New HDL Analyst
Q-2020.03 Features	
Extensions to cdpl_queue command	See *cdpl_queue* on page 2 for details.

Command Additions Summary

This section summarizes synthesis commands added or changed during this release.

cdpl_queue

Use the cdpl_queue command to set a CDPL queue, get the configuration setting of the CDPL queue, or clear the CDPL queue settings. Depending on the memory requirements of each configuration, you can specify different queues for different configuration files. For more information, see *Command Reference -> Tcl Synthesis Commands -> cdpl_queue*.

Recommended Versions of Compatible Tools

The FPGA design tool is tested with specific versions of other compatible Synopsys tools.

Compatible Versions of Synopsys Tools

The table lists the recommended version of VCS:

Tool	Recommended Version
VCS®	Q-2020.03-1

Platforms

The software is supported on the platforms listed below:

Windows	• Windows 10 Professional or Enterprise (64-bit) • Windows 7 Professional or Enterprise (64-bit) • Windows Server 2016 (64-bit) • Windows Server 2012 R2 (64-bit)[1] • Windows Server 2008 R2 (64-bit)
Linux	All Linux platforms require 32-bit compatible libraries. • CentOS 6.6 or later/7.1 or later (64-bit) • Red Hat Enterprise Linux 6.6 or later/7.1 or later (64-bit) • SUSE Linux Enterprise 12-SP4 (64-bit)

1. This is the final release that supports Windows Server 2012 R2 platform

Documentation

The following product documents are included with the Synopsys FPGA design tool. Documents can be accessed through the Online help (HTML) and as PDF documents.

Document	Access
User Guide	Online help, PDF
Reference Manual	Online help, PDF
Attribute Reference Manual	Online help, PDF
Command Reference Manual	Online help, PDF
Language Support Reference Manual	Online help, PDF
Messages Reference Manual	Online help

Known Problems and Solutions

The following are the known problems and the solutions for them.

Windows Certificate Installer Message

If you get a Windows certificate message during installation, it is because of a Synopsys Common Licensing (SCL) change, issued in December 2018. The change introduced Tamper Resistant Licensing (TRL) cryptography, implemented as part of the ongoing enhancement of the security of the Synopsys software. The installer checks if the required certificates are installed and issues a message if an update is needed.

Solution: Contact Synopsys support for the licensing certificate.

Software Does Not Open After Installation

If your software does not open after installation, check if you need to update your Synopsys Common Licensing (SCL) certificates. A SCL change was issued by Synopsys in December 2018, that contained TRL cryptography. This change was implemented as part of the ongoing process of enhancing the security of the Synopsys software.

Solution: To find out if you are missing any required certificates, go to the /bin directory of your installation and run the following:

```
whatscl.exe  --check-cert
```

If certificates are listed as missing, contact Synopsys support to update the required licensing certificates.

Change in Behavior for Sequential Optimizations

In the N-2018.03-SP1 release, the default behavior of the RAM implementations change. If sequential optimizations are disabled (set_option no_sequential_opt 1), you may see block RAM utilization increase (LUT utilization may decrease) in area estimation and in FPGA synthesis.

Default behavior:

Version	RAMs with read address registered	RAMs with output registered
N-2018.03 or older	Block RAM	LUT RAM (select RAM)
N-2018.03-SP1 or later	Block RAM	Block RAM

Solution: A new option has been added to control the behavior of block RAM packing when sequential optimizations are disabled.

```
set_option no_sequential_opt_bram_mapping inreg|both
```

inreg - Read address registered RAMs will be packed to block RAMs (prior default behavior).

both - (Default) Both read address registered and output registered RAMs are packed to block RAMs.

The following is a list of what is impacted by disabling sequential optimization.

- If you are disabling sequential optimizations with GSV for better naming correlation, you may not see RAM output registers that were seen in the GSV database in prior versions.
- No gated clock conversion and no ICG latch removal
- May increase area
- Limited design performance
- May increase congestion

False Flagging of Product Executables as Malware

On Microsoft Windows, some endpoint protection systems could flag executables as similar to malware threats. These are false positives, as Synopsys thoroughly scans all released files.

Solution: If your endpoint system blocks a Synopsys file, white-list it so that it is not flagged. Also, open a CASE so that Synopsys can investigate.

The encryptP1735.pl script is Incompatible with Windows DOS or PowerShell

If the encryptP1735.pl encryption script is run on Windows from DOS or PowerShell, it might fail.

Solution: Run the script on Linux. To run it on Windows, use a UNIX-like environment such as Cygwin.

Adobe Reader Error About Opening PDF Files (Linux)

Random links in the document PDFs on the Linux platform do not work. Adobe Reader generates an error message about not being able to find the appropriate PDF file. This does not happen on Windows platforms.

Solution: This is a problem with Adobe Reader on Linux. Work around it by first opening all the PDFs, and then trying the link again.

GUI Processing Can Fail on Windows 7 for the Synthesis Tool

The synthesis tool GUI might intermittently stop responding on Windows 7.

Solution: To resolve this issue, apply the hotfix from Microsoft by going to support.microsoft.com/kb/2718841/.

Limitations

The following limitations apply to supported features in the Synplify Pro tool.

Fault Injection Feature for Mixed HDL Designs

When using fault injection techniques for mixed HDL designs, RTL instrumentation is not supported. Only SRS instrumentation is supported for mixed HDL designs.

Page Could Not Be Found Message When Invoking Online Help

When online help is first invoked, it creates a cached version of the compiled help file in a local hierarchy to allow you to save preferences, bookmarks, and full-text search information. This cached version records the path to the installed version. If the same product version is subsequently re-installed in a new directory, invoking online help displays a message, "*The page could not be found*," because the cached version does not recognize the path to the re-installed product.

Solution: Go to the platform-specific directory and clear the cached help files:

Windows:
C:\Users*username*\AppData\Local\assistant\Synopsys*product*

Linux:
~/.local/share/data/assistant/Synopsys/Synplify/

- Delete any/all directories named “online*” from the cache directory.
- Restart help. This creates a new cache and correctly displays the online help.

Online Search Does Not Handle Hyphens as Expected

If the search term includes a hyphen (for example, *byte-enable*), online help does not produce the search hits you expect, because it searches for *byte* and *enable*. This limitation does not affect underscores. It is limited to online help search and does not affect search in PDF documents.

Solution: Here are some workarounds:

- Basic Search—Use the \ character before the hyphen to escape the hyphen
- Try the index
- Basic Search—Try using the * wildcard
- Basic Search, and Advanced Search with exact term—Try the term with a space in place of the hyphen

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save the project file from the synthesis GUI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project GUI.