The ECP3 Versa Board design will compile all the way through and can be downloaded to the ECP3 Versa Board. Please refer to Step 5a to 5i starting from page 12 of UG45.pdf to get the demo working. Note the LED states in Table 5 to see that the demo is working.

After running the tools, users can exercise the following tools:

1. Spreadsheet View: Look at the pins and timing constraints tabs
2. Package View
3. Device View
4. Netlist View
5. NCD View
6. Timing Analysis View
7. Power Calculator
8. Programmer
9. Run Manager

Demo also covers various timing constraints: FREQUENCY, MULTICYCLE, MAXDELAY and BLOCK PATHS. There are some unconstrained paths but they are combinatorial paths and reset/clock enable lines.