Synplify Pro® for Lattice Release Notes

Version N-2018.03L-SP1-1, April 2019

Release Note Topics

About this Release

Release N-2018.03L-SP1-1 includes software improvements and enhancements to the Synplify Pro® for Lattice product. For details, see the Feature and Enhancement Summary section below.

Feature and Enhancement Summary

The following table summarizes features and enhancements.

Feature	Description
Feature in the N-2018.03L-SP1 Release	
Compiler Enhancements	The syn_smhigheffort attribute uses a higher threshold and correspondingly higher effort when the tool extracts a state machine on individual state registers. Use this attribute when state machine extraction is enabled, but the state machine is not automatically extracted.
	Attribute Reference Guide->syn_smhigheffort
Feature in the N-2018.03L Release	
Clock Conversions in Pre-map State	Clock conversion now takes place in the pre-mapping stage, based on the compiler primitives. In the Synplify Pro N-2017.09 release, gated clock conversion was happening in the mapper flow but now it happens in the pre-mapper flow.
	Due to this, the clock conversion report in the log (.srr) file is moved to the pre-mapper section of the log file.
	User Guide->Clock Conversion->Restrictions on Using Gated Clocks->Clock Conversions for the Traditional Flow

Recommended Versions of Compatible Tools

The FPGA design tool is tested with specific versions of other compatible Synopsys tools.

Compatible Versions of Synopsys Tools

The table lists the recommended version of VCS:

Tool	Recommended Version
VCS	M-2017.03-SP2-2

Platforms

The software is supported on the platforms listed below:

Windows	• Windows 10 Professional or Enterprise (64-bit)
	• Windows 8.1 Professional or Enterprise (64-bit)
	• Windows 7 Professional or Enterprise (64-bit)
	• Windows Server 2016 (64-bit)
	• Windows Server 2012 R2 (64-bit)
	• Windows Server 2008 R2 (64-bit)
Linux	All Linux platforms require 32-bit compatible libraries. • CentOS 6.6 or later/7.1 or later (64-bit)
	• Red Hat Enterprise Linux 6.6 or later/7.1 or later (64-bit)
	• SUSE Linux Enterprise 11-SP1 or later/12 or later (64-bit)

Documentation

The following product documents are included within the Synopsys FPGA design tool. Documents can be accessed through the Online help (HTML) and as PDF documents.

Document	Access
User Guide	Online help, PDF
Reference Manual	Online help, PDF
Attribute Reference Manual	Online help, PDF
Command Reference Manual	Online help, PDF
Language Support Reference Manual	Online help, PDF
Messages Reference Manual	Online help

Known Problems and Solutions

The following are the known problems and the solutions for them.

The encryptP1735.pl Script Fails on Windows

The encryption standard encryptP1735 works only with Linux/Cygwin.

Solution: This script is not compatible with DOS or PowerShell. It must be run in a UNIX-like environment such as Cygwin.

Gated Clock Conversion is not Recommended with High Reliability

If you have enabled gated clock conversion and you are implementing a high reliability design, you might get an error or unexpected results during the technology mapping phase.

Solution: : If you intend to create a high-reliability design, disable gated clock conversion from the GUI or through a command:

- From the GUI, go to Implementation Options -> GCC and disable the checkbox for Clock Conversion.
- Add this command in the project file or type it at the tool Tcl prompt:

  set_option -fix_gated_and_generated_clocks 0

Locked FSMs

FSMs are locked in an illegal state.

Solution: If you have uninitialized FSMs, turn off the FSM compiler throughout the synthesis flow.

False Flagging of Product Executables as Malware

On Microsoft Windows, some endpoint protection systems could flag executables as similar to malware threats. These are false positives, as Synopsys thoroughly scans all released files.

Solution: If your endpoint system blocks a Synopsys file, white-list it so that it is not flagged. Also, open a CASE so that Synopsys can investigate.

Limitations

The following limitations apply to supported features in the Synplify Pro tool.

Page Could Not Be Found Message When Invoking Online Help

When online help is first invoked, it creates a cached version of the compiled help file in a local hierarchy to allow you to save preferences, bookmarks, and full-text search information. This cached version records the path to the installed version. If the same product version is subsequently re-installed in a new directory, invoking online help displays a message, "*The page could not be found,*" because the cached version does not recognize the path to the re-installed product.

Solution: Go to the platform-specific directory with the cached help files:

Windows:
C:\Users*username*\AppData\Local\assistant\Synopsys\Synplify\

Linux:
~/.local/share/data/assistant/Synopsys/Synplify/

    — Delete any "online*" directories from the cache directory.

    — Restart help. This creates a new cache, and correctly displays the online help.

Adobe Reader Error About Opening PDF Files (Linux)

Random links in the document PDFs on the Linux platform do not work. Adobe Reader generates an error message about not being able to find the appropriate PDF file. This does not happen on Windows platforms.

Solution: This is a problem with Adobe Reader on Linux. Work around it by first opening all the PDFs, and then trying the link again.

Online Search Does Not Handle Hyphens as Expected

If the search term includes a hyphen (for example, byte-enable), search in online help does not produce the search hits you expect, because it searches for byte and enable. This limitation does not affect underscores. It is also limited to online help search and does not affect search in PDF documents.

Solution: Here are some workarounds:

    — Basic Search: Use the \ character before the hyphen to escape the hyphen

    — Try the index

    — Basic Search: Try using the * wildcard

    — Basic Search and Advanced Search with exact term: Try the term with a space in place of the hyphen

GUI Processing Can Fail on Windows 7 for the Synthesis Tool

The synthesis tool GUI might intermittently stop responding on Windows 7.

Solution: To resolve this issue, apply the hotfix from Microsoft by going to http://suppport.microsoft.com/kb/2718841/.

Crossprobing Source Code Files Created with Third-Party Editors

When using source code files created with third-party editors, you sometimes cannot crossprobe to the correct line number in the source file.

Solution: Open the file in the FPGA synthesis tool text editor.

Editing Externally Created Project (prj) Files

If Tcl commands or script files were used to build your project, you might not be able to save this Project file from the synthesis GUI in downstream tools, because they contain hard-coded file paths.

Solution: Generally, use the same method to save a project as you did to create the project. In this case, save the project file to an external text editor and not in the project GUI.