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Hardware/Software Codesign - HS 09

Solution for Exercise Sheet 8

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8.1 Design Space, Pareto Points

The task graph in Figure 1 shows a system specification with four tasks, T1 ...T4. The tasks can be executed on different components. Table 1 displays the execution times for the tasks on the different components as well as the component cost. For example, the MIPS processor costs 200 units and can run tasks T1 in 5 ms and task T4 in 2 ms. Table 1 shows also the number of components available for each component type (MIPS, DSP, FPGA and ASIC). All components execute tasks sequentially – at any given time a component executes at most one task. Task execution is non-preemptive – once a task is started, it runs to completion.

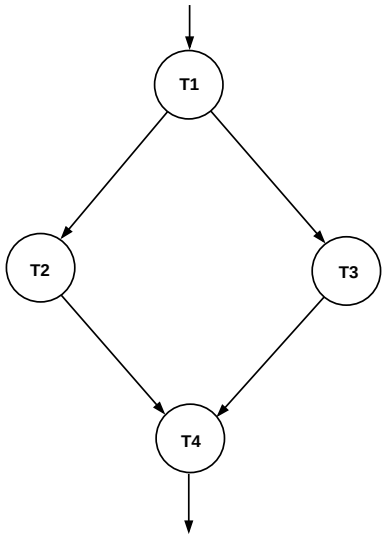

Figure 1: Task graph

component	*number*	*cost*	*execution time*			
			T1	T2	T3	T4
MIPS	1	200,-	5 ms	—	—	2 ms
DSP	1	120,-	—	20 ms	18 ms	5 ms
FPGA	1	240,-	—	12 ms	10 ms	—
ASIC	1	400,-	—	—	800 μs	—

Table 1: Available components with cost and execution times for tasks $T1 \ldots T4$.

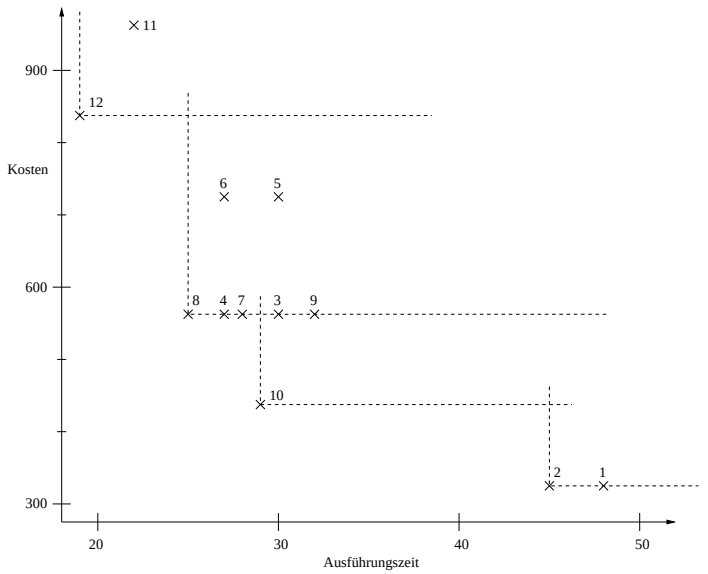

Figure 2: Sinnvolle Entwurfspunkte bei beschränkten Ressourcen.

(a) Construct the design space by listing all possible design points. A design point consists of an *allocation* (selection of components), a *binding* (assignment of tasks to selected components) and a *schedule* (execution order for the tasks). Determine the total cost and execution time for each design point.

Solution: *Siehe Abbildung 2 und Tabelle 2. Die entsprechenden Ablaufpläne sind trivial. Werden T_2 und T_3 auf derselben Ressource ausgeführt, dann müssen die Tasks sequentiell hintereinander gestartet werden, ansonsten parallel. Hinweis: die Konfigurationen 9 und 10 geben nur Sinn, sofern der FPGA dynamisch rekonfigurierbar ist.*

	1	2	3	4	5	6	7	8	9	10	11	12
T_1	MIPS	MIPS	MIPS	MIPS	MIPS	MIPS	MIPS	MIPS	MIPS	MIPS	MIPS	MIPS
T_2	DSP	DSP	DSP	DSP	DSP	DSP	FPGA	FPGA	FPGA	FPGA	FPGA	FPGA
T_3	DSP	DSP	FPGA	FPGA	ASIC	ASIC	DSP	DSP	FPGA	FPGA	ASIC	ASIC
T_4	DSP	MIPS	DSP	MIPS	DSP	MIPS	DSP	MIPS	DSP	MIPS	DSP	MIPS
Kosten	320.-	320.-	560.-	560.-	720.-	720.-	560.-	560.-	560.-	440.-	960.-	840.-
t_{exec}	48 ms	45 ms	30 ms	27 ms	30 ms	27 ms	28 ms	25 ms	32 ms	29 ms	22 ms	19 ms

Table 2: Sinnvolle Entwurfspunkte bei beschränkten Ressourcen

(b) Draw the design points in a cost-time diagram. Which design points are Pareto points?

Solution: *Die Punkte 2, 8, 10, 12 sind Pareto-optimal.*

(c) Consider an allocation without resource constraints. That means we are given an arbitrarily high number of components of each type (MIPS, DSP, FPGA and ASIC). Are there new design points? Does the set of Pareto points change?

Solution: *Siehe Abbildung 3 und Tabelle 3. Die Punkte 2, 8, 13, 15 sind nun Pareto-optimal.*

(d) How many design points exist at least if a task graph comprises n tasks, each task can be executed on at least three component types, and there are no resource constraints?

Solution: 3^n

	13	14	15	16
T_1	MIPS	MIPS	MIPS	MIPS
T_2	DSP1	DSP1	FPGA1	FPGA1
T_3	DSP2	DSP2	FPGA2	FPGA2
T_4	MIPS	DSP1/2	MIPS	DSP
Kosten	440.-	440.-	680.-	800.-
t_{exec}	27 ms	30 ms	19 ms	22 ms

Table 3: Zusätzliche Paretopunkte bei unbeschränkten Ressourcen.

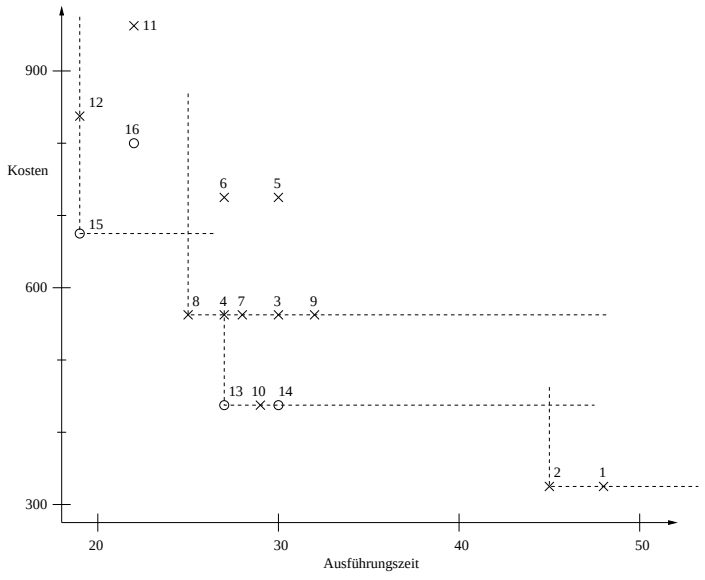

Figure 3: Zusätzliche Entwurfspunkte bei unbeschränkten Ressourcen