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Hardware/Software Codesign - HS 09

Exercise Sheet 8

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8.1 Design Space, Pareto Points

The task graph in Figure 1 shows a system specification with four tasks, T1 ...T4. The tasks can be executed on different components. Table 1 displays the execution times for the tasks on the different components as well as the component cost. For example, the MIPS processor costs 200 units and can run tasks T1 in 5 ms and task T4 in 2 ms. Table 1 shows also the number of components available for each component type (MIPS, DSP, FPGA and ASIC). All components execute tasks sequentially – at any given time a component executes at most one task. Task execution is non-preemptive – once a task is started, it runs to completion.

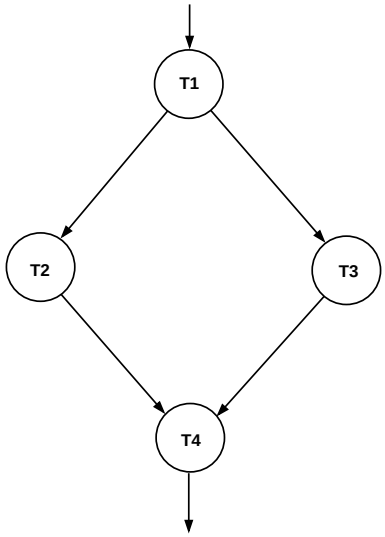

Figure 1: Task graph

component	*number*	*cost*	*execution time*			
			T1	T2	T3	T4
MIPS	1	200,-	5 ms	—	—	2 ms
DSP	1	120,-	—	20 ms	18 ms	5 ms
FPGA	1	240,-	—	12 ms	10 ms	—
ASIC	1	400,-	—	—	800 μs	—

Table 1: Available components with cost and execution times for tasks $T1 \ldots T4$.

(a) Construct the design space by listing all possible design points. A design point consists of an *allocation* (selection of components), a *binding* (assignment of tasks to selected components) and a *schedule* (execution order for the tasks). Determine the total cost and execution time for each design point.

(b) Draw the design points in a cost-time diagram. Which design points are Pareto points?

(c) Consider an allocation without resource constraints. That means we are given an arbitrarily high number of components of each type (MIPS, DSP, FPGA and ASIC). Are there new design points? Does the set of Pareto points change?

(d) How many design points exist at least if a task graph comprises n tasks, each task can be executed on at least three component types, and there are no resource constraints?