High Performance, Low Power, ISM Band FSK/GFSK/OOK/MSK/GMSK Transceiver IC

Silicon Anomaly

ADF7023

This anomaly sheet describes the known bugs, anomalies, and workarounds for the ADF7023 transceiver and relates to Silicon Revision 1.2, which has corresponding silicon revision readback codes of 0x70, 0x23, 0x01, 0x02. See the ADF7023 data sheet for details on how to read the silicon revision codes.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADF7023 FUNCTIONALITY ISSUES

Silicon Revision Readback	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
Product Code MSB = 0x70 Product Code LSB = 0x23 Silicon Revision Code MSB = 0x01 Silicon Revision Code LSB = 0x02	ADF7023BCPZ	Release	Rev. 0	5

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FUNCTIONALITY ISSUES

Table 1. RC Oscillator Accuracy [er001]

Background	The RC oscillator can be used to control the wake-up timing of the ADF7023 low power modes. Its typical accuracy is specified as 1.5% after a calibration at 25°C.
Issue	The calibration range of the RC oscillator is not sufficient to ensure a 1.5% typical accuracy on all devices. This can result in the postcalibration accuracy on some devices being significantly greater than 1.5%.
Workaround	For applications requiring accurate low power mode timing, the 32.768 kHz external oscillator should be used.
Related Issues	None

Table 2. External PA and LNA Enable on ADCIN_ATB3 and ATB4 [er002]

Background	External PA and LNA enable signals from the ADF7023 can be configured on the ADCIN_ATB3 and ATB4 pins, respectively. The specified typical V_{OH} is 1.8 V and the specified typical V_{OL} is 0.1 V.
Issue	The output voltage levels of the PA and LNA enable signals on ADCIN_ATB3 and ATB4 do not meet the specified V_{OH} and V_{OL} specifications in the ADF7023 data sheet. The actual V_{OH} and V_{OL} levels are shown in Table 3 below.
Workaround	An external level translator or buffer may be required to ensure that the appropriate logic trigger points of the external circuitry are met.
Related Issues	[er003]

Table 3. Typical Output Voltage Levels on ADCIN_ATB3 and ATB4 ([er002])

Parameter	Typical	Unit	Conditions
ADCIN_ATB3, Output High Voltage, V_{OH}	2.2	V	V_{DD} = 3.6 V. I_{OH} = 100 µA
ADCIN_ATB3, Output Low Voltage, V_{OL}	0.64	V	V_{DD} = 3.6 V, I_{OL} = 0.2 µA
ADCIN_ATB3, Output Low Voltage, V_{OL}	2.04	V	V_{DD} = 3.6 V, I_{OL} = 1.0 µA
ATB4, Output High Voltage, V_{OH}	2.2	V	V_{DD} = 3.6 V, I_{OH} = 100 µA
ATB4, Output Low Voltage, V_{OL}	0.53	V	V_{DD} = 3.6 V, I_{OL} = 0.2 µA
ATB4, Output Low Voltage, V_{OL}	2.08	V	V_{DD} = 3.6 V, I_{OL} = 1.0 µA
ADCIN_ATB3, Output High Voltage, V_{OH}	1.38	V	V_{DD} = 1.8 V, I_{OH} = 100 µA
ADCIN_ATB3, Output Low Voltage, V_{OL}	0.65	V	V_{DD} = 1.8 V, I_{OL} = 0.2 µA
ADCIN_ATB3, Output Low Voltage, V_{OL}	1.8	V	V_{DD} = 1.8 V, I_{OL} = 1.0 µA
ATB4, Output High Voltage, V_{OH}	1.38	V	V_{DD} = 1.8 V, I_{OH} = 100 µA
ATB4, Output Low Voltage, V_{OL}	0.55	V	V_{DD} = 1.8 V, I_{OL} = 0.2 µA
ATB4, Output Low Voltage, V_{OL}	1.8	V	V_{DD} = 1.8 V, I_{OL} = 1.0 µA

Table 4. External PA and LNA Enable on XOSC32KP_GP5_ATB1 and XOSC32KN_ATB2 [er003]

Background	External PA and LNA enable signals from the ADF7023 can be configured on the XOSC32KP_GP5_ATB1 and XOSC32KN_ATB2 pins.
Issue	The PA and LNA enable signals on XOSC32KP_GP5_ATB1 and XOSC32KN_ATB2 are nonfunctional.
Workaround	Use the external PA and LNA enable signals on ADCIN_ATB3 and ATB4.
Related Issues	[er002]

Table 5. Optimum Uncalibrated Image Attenuation [er004]

Background	The typical uncalibrated image attenuation is specified as 40 dB at 433 MHz and 36 dB at 868 MHz/915MHz.
Issue	To achieve the typical uncalibrated image attenuation values specified in the datasheet, it is required to use recommended default values for IMAGE_REJECT_CAL_PHASE (Address 0x118) and IMAGE_REJECT_CAL_AMPLITUDE (Address 0x119).
Workaround	To achieve the specified uncalibrated image attenuation at 433 MHz, set IMAGE_REJECT_CAL_AMPLITUDE = 0 and IMAGE_REJECT_CAL_PHASE = 14. To achieve the specified uncalibrated image attenuation at 868 MHz/915 MHz, set IMAGE_REJECT_CAL_AMPLITUDE = 8 and IMAGE_REJECT_CAL_PHASE = 55.
Related Issues	None

Table 6. Receiver Sensitivity at 910 MHz [er005]

Background	The 910 MHz channel falls exactly on the 35th harmonic of the 26 MHz crystal reference.
Issue	When the ADF7023 receiver is configured for reception at 910 MHz ± (IF bandwidth × 2), the receiver sensitivity can be degraded by up to 20 dB.
Workaround	The degradation in receiver sensitivity at 910 MHz± (IF bandwidth × 2) can be significantly improved by using the following configuration: 1. Disable the AGC by setting AGC_LOCK_MODE (in Register RADIO_CFG_7, Address 0x113) = 0x01. 2. Set the receiver gain to maximum by setting AGC_MODE (Address 0x35D) = 0x36. 3. Disable the ADC by writing 0x0F to MCR Register 0x324.
Related Issues	None.

NOTES

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