# Conclusion

In this project we have worked with areas in both system engineering and software hardware co.-design, with special focus on the last part.

We have learned modeling at higher level with SySML and transformation to SystemC. Our experience with automated transformation is that you have to be dedicated in order to learn the details.

By using SystemC in practice, we come to the fact that the learning curve for the simulation tool is quite steep and particularly benefits of applying SystemC in projects that veer toward ASIC solutions do not match the time effort. Presence of an auto generate tool would compensate the mentioned disadvantage by gaining shorter implementation time through auto-generated VHDL code.

On the other hand, it is important to emphasize that the situation will immediately be different when we talk HW & SW co-design principles in which we operate within the FPGA design rules, where the HW platform is often out of reach until late stage in the development process. SystemC is of great importance in this case. A HW platform can be simulated using SystemC and provides the basis for SW development without having the HW platform available.

One thing the pareto analyse don’t mention is risk, and the pareto analysis we made don’t focus on risk, but only cost and performance. Our proposal is making a pareto analysis for each quality pair which is most important for the system.

**Suggestions to improvements**

**The excellence of the project - description of parts where you are especially proud**