# Scope and Objective

The primary objective for this project is to analyze an architecture from a specification and map this architectural solution to a selected platform. The architectural solution will contain an simulation of the most important modules. Design space exploration, partitioned technique and profiling *[Gajski]* will be used in order to archive the best trade-off between cost, performance and dependability. Some of these quality constraints riposte each other, and therefore it is essential that the architecture reflects the quality attribute which is most important for the defined product.

Stakeholders always want a dependable system, which perform the best and cost the less. Ours objective will be to find the best platform that fulfills the stakeholders requirements. Therefore different platform architecture will be considered including MIPS and FPGA, and each platform will be analyzed to archive the best trade-off between system quality attributes defined by the stakeholders.

While this project has limited time schedule, the architectural design and implementation will focus on modeling at the TLM level in SystemC. These simulations will also be used as proof of concept, and the further syntheses from behavior to structure defined by *[Gajski]*. As mentioned above the project has limited time schedule, and therefore only the most important steps in the syntheses will be described.

From a learning perspective, group members have indicated that a major learning area is going from higher level UML/SysML abstraction where the overall system architecture is defined, to a specific platform. The whole syntheses from higher level abstraction to implementation and the steps needed is one of the interesting focus areas for the project, as well as risk level management *[INCOSE]* at higher abstraction.

[Anders]

Provide a proof-of-concept for a solution detailed in the project definition. Focus on architectural design and prototyping in SystemC til TLM niveau.

Evaluerer hvilke platforme (inklusiv FPGA) der er muligt, fordele og ulemper, om nogen kan fravælges fra start af, m.m.

Opret liste over -ability (Usability, Power, Cost, …), deres betydning og hvordan de forskellige platforme møde de krav. Reference til pålidelig SW og arkitektur (SW arkitektur i praksis).

Evaluer risk of failure (ikke mode men –ability krav) on the different platforms.

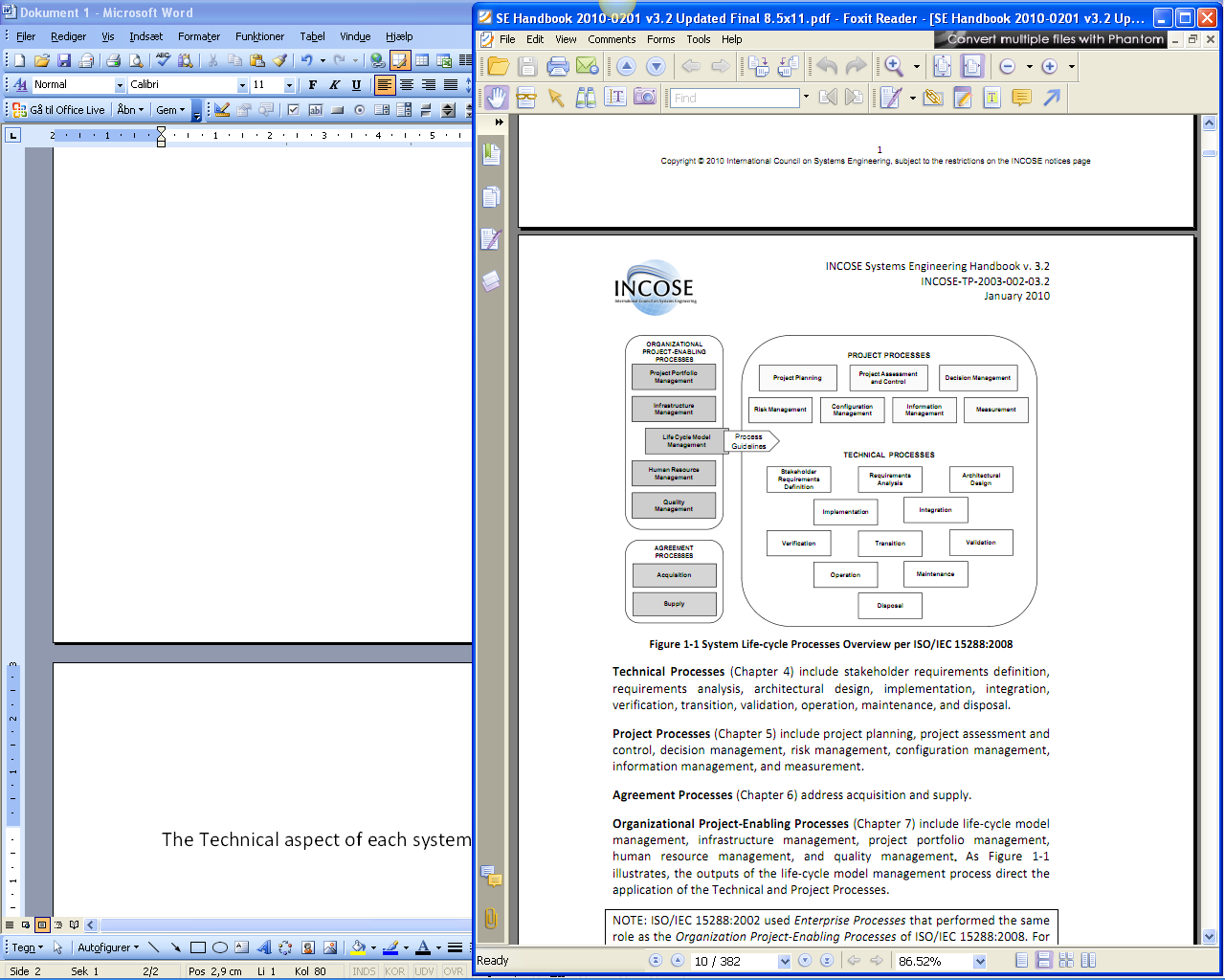
# Specification



# Methodology and tools

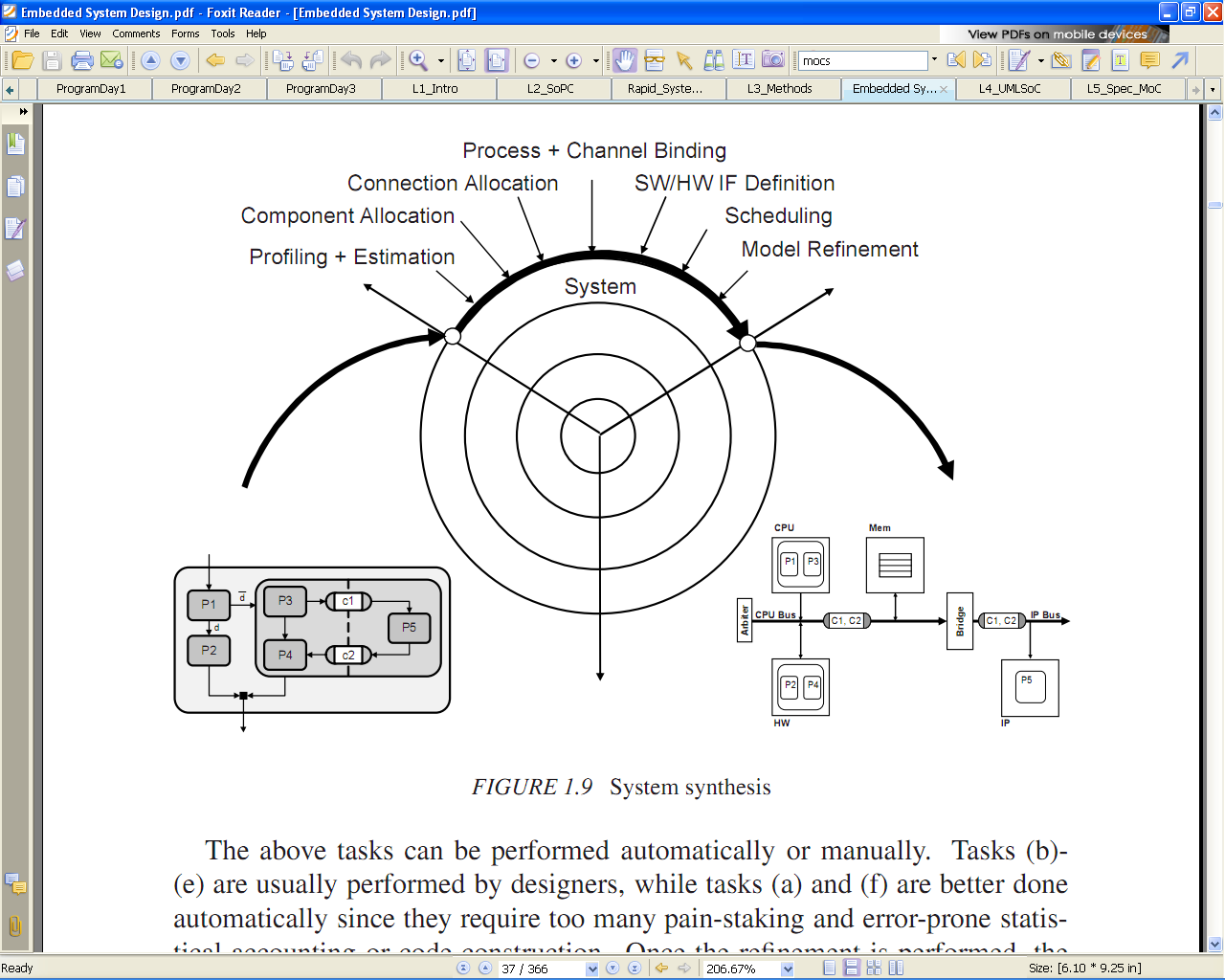
1. Subversion (Google code), Microsoft Word 2007, Visio 2003 (også til tidsplan)
2. SysML/UML,
3. SystemC til simulering.
4. INCOSE vs. Y-chart (top down).

The Technical aspect of any system can be described by *[INCOSE]*’s technical process as shown in the following figure.



We follow the INCOSE guidelines through this project and wherever necessary, use other appropriate methods and approaches such as Y-chart, SysML and SystemC to support, model and evaluate the process.

The technical process begins with Stakeholder Requirements Definition followed by Requirement analyses. These will base the inputs for Architectural design. At this point a system level synthesis described by *[Gajski]* would be utilized to support implementation.



SystemC will be applied to verify the architectural design and generate an executable requirement. This will help us to simulate different designs and compare their metrics to choose the best fit.

The figure bellow is an visualization of the described process above.



# Working group contract

* Møde tirsdag efter behov.
* Første møde tirsdag d. 1/2-2010

# Planning

* Inden tirsdag gennemlæser vi dette dokument og gør os klart hvad vi ønsker at opnå med projektet så vi er klar til at formalisere det tirsdag.
* AHP ”flytter” hvad der måtte være af kravspecifikation fra project proposal til dette dokument.

# Noter

Hvis man vælger en FPGA med en oscillator og en custom IP til modulation, kan der så opnås et bedre strømforbrug end at vælge en lille microcontroller og en ekstern tranceiver?

Måle worst-case SNR ved at gå længst væk i huset og aktivere. Dermed kan sendestyrke (strømforbrug) minimeres – en del af konfiguration af ny panikknap.

Possibility:

TI MSP430F200x + TI CC110 = 0,7uA + 200nA sleep mode at 1,8 – 3,3V

# Refrences

|  |  |
| --- | --- |
| *[INCOSE]* | INCOSE System Engineering Handbook v.3.2 |
| *[Gajski]* | Embedded System Design, Modeling, Sunthesis and Verification by Daniel D. Gajski |
|  |  |