Practical Objective for Course(s) BSCS-401, CSSE-303, CS-501; Digital Computers Logic & Design

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Lab Objective – 3: Logic Gates and Their Functions

Please refer the Lecture session conducted over "Logic Gates and Their Functions".

Caution:

Use the given Assignment Template only, and follow the Submission Procedure given in Syllabus Document strictly.
Be aware of Assignment Submission Ethics. Submit handwritten work.
Do not use MS-Excel to develop Truth Table, also you are not allowed to use circuit drawing softwares for this Objective.
Do not attach this Objective Document along with your work submission.

Write List-wise that what's new thing you have learned from this Assignment?

Consider the following Logic Map (MALVINO-Pg.37).

1. Identify INPUTs and OUTPUTs.
2. Determine the Final Equations for each: C_P, E_P, L_M, E_R, L_I, E_I, L_A, E_A, SU, E_U, L_B, L_O
3. Trace and Write the Formula at each NODE, INPUT & OUTPUT Terminal of each Gate.
4. Develop complete Truth Table with all possible combinations.
5. Develop Truth Table with selected any 10 random INPUT instances extracted from Truth Table with far-sequence. Apply all instances on given Logic Map, and verify OUTPUT Logic.
6. Apply the same selected 10 INPUT instances on equations determined in (2) above, to verify output obtained after Logic Trace. Show verification status also.