BRAC University
Semester: Fall 2024, Faculty: YAP
Course: CSE 251

Assignment: 03	Deadline: 04 Jan., 2025 (11:59 PM)	Marks: 90

Instruction:

- Clearly write the solutions, along with the questions, on white paper with black ink (no need to use color pen, don't use pencils).
- Use CamScanner, Adobe Scan, Microsoft Office Lens, or any other software to scan the pages and make a single PDF file.
- After creating the PDF, make sure that (a) no pages are missing, (b) all of the pages are legible, and (c) your student ID on each page is visible.
- Please note, collaboration ≠ copying. You are allowed to discuss the questions and clear confusion you might have, but you have to write your solutions independently and be able to explain your answers during a random viva.
- [Very Important] Rename the PDF in the following format: "Section A4 StudentID FullNameWithoutSpace.pdf". For example, if my student ID is 12345678 and my name is Yeasin Arafat, the filename should be A4 12345678 YeasinArafat.pdf

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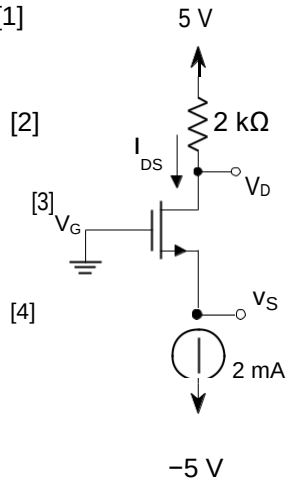
■ Question 1 of 8 [CO3] [10 marks]

Refer to the MOSFET in the figure below where V_T = 1 V and $K = k_n' W/L$ = 4 mA/V^2 – for questions (a-c).

(a) [CO1] Identify the value of the gate voltage v_G and the drain-source current i_{DS}. [1]

(b) [CO2] Calculate the drain voltage V_D. [2]

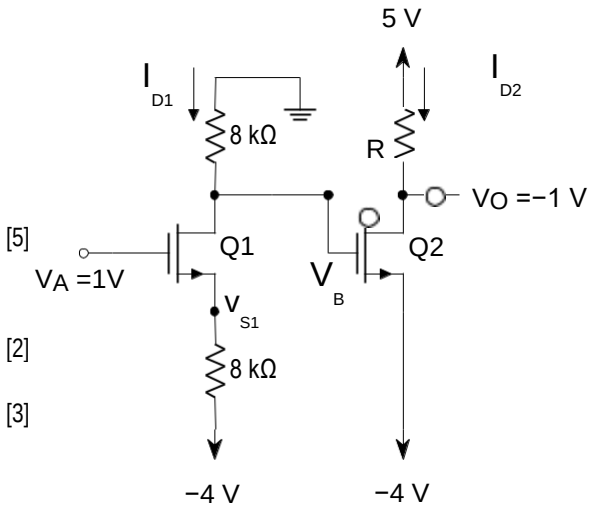
(c) [CO2] Analyze the circuit to find the source voltage V_S. [Use the method of assumed states.] [3]



(d) [CO3] Consider a MOSFET inverter (SR model) with the following circuit parameters: V_{CC} =10 V, R_L =10 kΩ. Also, for the MOSFET, V_T =1 V and $1/(k_n' V_{OV})$ = 5. Determine a W/L sizing for the MOSFET so that the inverter output of logical 0 can switch OFF the next MOSFET inverter connected to it. [4]

■ Question 2 of 8 [10 marks]

Refer to the MOSFET circuit in the adjacent figure where V_T = 1 V and k_n' =250 μA/V^2 W/L = 1/8 for both Q1 and Q2.



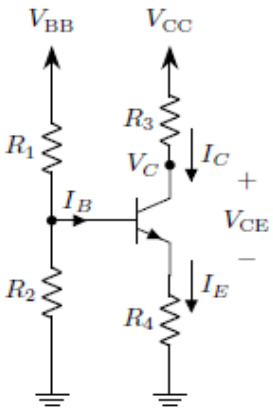
(a) [CO2] Assuming Triode mode of operation, find the the voltage v_{S1} and V_B. [5]

(b) [CO2] Calculate the current I_{D1}. [2]

(c) [CO2] Use the value of V_B obtained in (a) to find the value of resistor R so that V_O =−1 V. [3]

Question 3 of 8 [10 marks]

Refer to the BJT circuit in the adjacent figure where, V_{BB} =5 V, V_{CC} =15 V, $4R_1 = R_2 = 40R_3 = 80R_4$ =80 kΩ. Also, assume that the common emitter current gain $\beta = 100$.



(a) **[CO1] Draw** the equivalent circuit of an npn-BJT during active mode. [2]

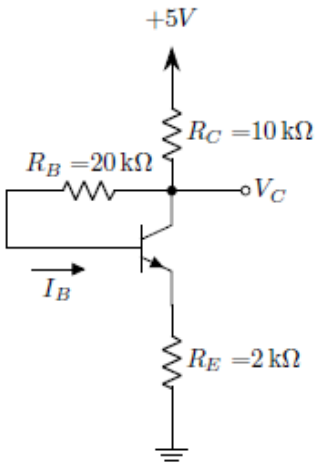
(b) **[CO2] Calculate** I_B, I_C, I_E, V_{CE} and V_C using the method of assumed states. [Hint: Try to find the Thevenin's equivalent circuit of the left hand side circuit from the B terminal and ground] [3]

(c) **[CO2]** If V_{BB} is changed from 5V to 5.3V, what happens to the outputs of the circuits? Calculate I_B, I_C, I_E, V_{CE} and V_C again. Now for a 0.3 V increase in input V_{BB}, what is the change of I_C? Use $\Delta I_C = I_{C,\text{new}} - I_{C,\text{old}}$. [4]

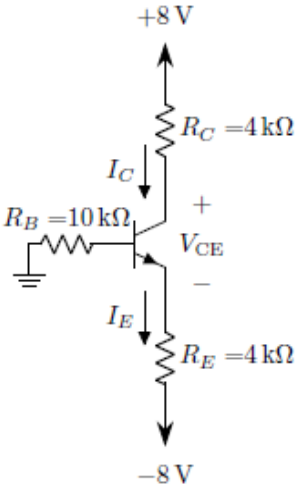
(d) **[CO1]** Explain any use case of the differences in voltage increase between input and output. What could the use case be to such a phenomenon? [1]

■ **Question 4 of 8** [10 marks]

(a) **[CO2]** For the transistors in the figure (a) and (b) below, $\beta = 75$. **Find** the labelled voltages and currents. (Assume v_{BE0} =0.7 V, for active mode and $v_{CE(\text{sat})}$ =0.2 V) [6]

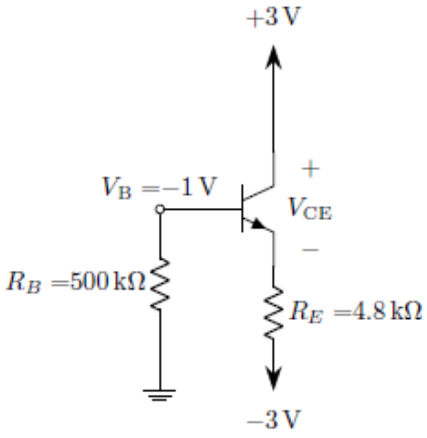


(a) Circuit-1



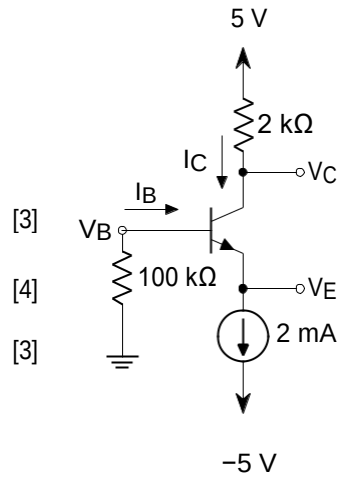
(b) Circuit-2

(b) **[CO2]** In the circuit shown in adjacent figure, the values of measured parameters are shown. Determine β, α and the other labeled currents and voltages. [4]



■ Question 5 of 8 [CO3] [10 marks]

Refer to the BJT in the adjacent figure where v_{BE0} = 0.7 V, $v_{CE(sat)}$ = 0.2 V and β = 100.



(a) [CO1] Identify the value of the BJT currents I_B, I_C and I_E. [3]

(b) [CO2] Calculate the base and collector voltages V_B and V_C . [4]

[

(c) CO2] Analyze the circuit to find the emitter voltage V_E. [Use the method of assumed states.] [3]

■ Question 6 of 8 [10 marks]

(d)

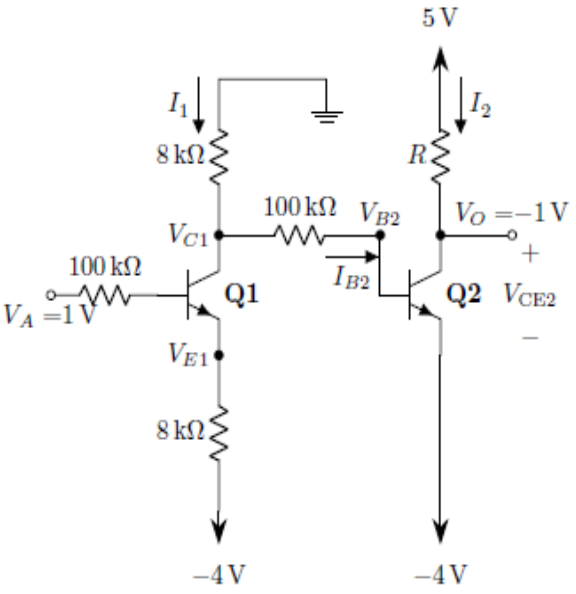
Refer to the BJT circuit in the adjacent figure where $v_{BE0} = 0.7$ V, $v_{CE(sat)} = 0.2$ V and $\beta = 100$. for both the BJTs.

(a) **[CO2]** Assuming **Saturation** mode of operation, and $I_{B2} = 0$, find the the voltage V_{C1} and current V_{E1}. [6]

(b) **[CO2] Calculate** the voltage value V_{B2}, so that $V_O = -1$ V. [Hint: Try to identify the mode of operation of Q2 with the help of V_{CE2}. Thereafter, find the value of V_{B2}.] [1]

(c) **[C02]** Find the value of resistor R so that $V_O = -1$ V. [1]

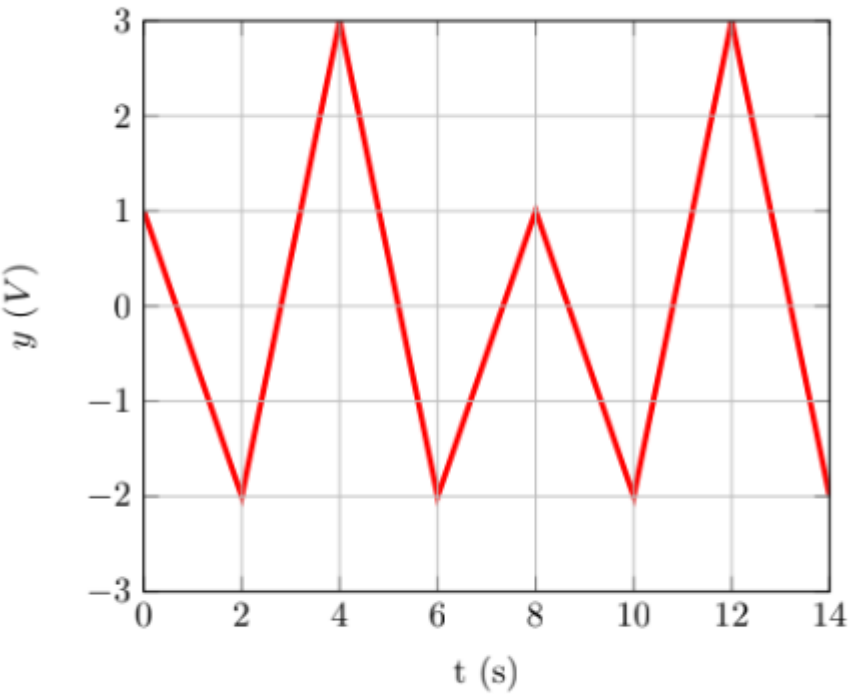
(d) **[C01] Explain** why the solution of the circuit, as per the above questions, is not perfectly accurate but an approximation of the true solution. **State** the process in which you may find the true solution. [2]



Question 7 of 8 [20 marks]

Part 1: The input of a full-wave rectifier is a **square wave** voltage with peak V_M= 15 V and frequency 0.5 Hz, and output load resistance is R = 5 kΩ. Silicon diodes are used in this circuit for which the forward drop is V_{D0} = 0.7 V.

- **i.** Briefly explain the purpose of a rectifier and describe its operation. [3]
- **ii.** Describe the purpose of using a filter capacitor in a rectifier. [2]
- **iii.** Show the input and output waveforms. [4]
- **iv.** Draw the output waveforms if we add a filter capacitor, C = 1000 uF in parallel with R. [3]
- **v.** Draw the VTC curve [2]



(b) Input of the FW rectifier

Part 2: A voltage waveform $V_i = 15\sin(2000\pi t)$ V is fed into a Half-wave rectifier with a load resistance $R = 5$ kΩ. Silicon diodes are used in this circuit for which the forward drop is $V_{D_0} = 0.7$ V.

(a) **Illustrate** the input and output waveforms in separate graphs. Label the graph and **indicate** the voltage levels properly. [2]

(b) **Calculate** the DC/Average value of the output. [1]

(c) A capacitor is now added to reduce the fluctuation of the output voltage, which makes the peak to peak ripple voltage **4%** of the maximum output voltage V_P. **Deduce** is the value of the capacitor from the given data.[2]

(d) The input of a Full-wave rectifier is shown in Figure 1(b) above and output load resistance is $R = 10$ kΩ. Germanium diodes are used in this circuit for which the forward drop is $V_{D_0} = 0.3$ V. **Show** the input and output waveforms [1]

■ **Question 8 of 8** [10 marks]

(a) Briefly explain the operation principle of a MOSFET as a switch with appropriate illustrations showing gate bias voltage [4]
(b) Draw the IV curve of a MOSFET considering the S-model only [2]
(c) Design a circuit using ideal MOSFETs (S-model) and BJTs to implement the logic function: [1.5+1.5+1.5+1.5]

$$(1)\ \mathbf{F} = \overline{(\overline{A.C} + \overline{(\overline{A} + \overline{B})})}$$

$$(2)\ \mathbf{F} = (\overline{A + \overline{B}}).\ \overline{(\overline{B} + B.\overline{C})}$$