The University of Bahawalpur

Faculty of Engineering

Department of Computer Systems Engineering

LAB No.4

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| Name: | Instructor |
| Roll No. | Date |

**Objective:**

1. Design An ALU data path that performs the following operations in parallel on two 16 signed inputs A and B and assigns the value of one of the outputs to 16bit C. The selection of operation is based on a 2 bit selection line. Code the design in Verilog using Xilinx 10.1
2. Develop a test bench to verify the design.

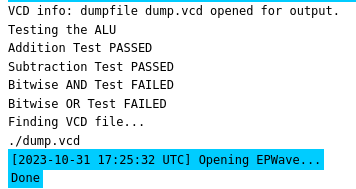
**Pre Lab:**

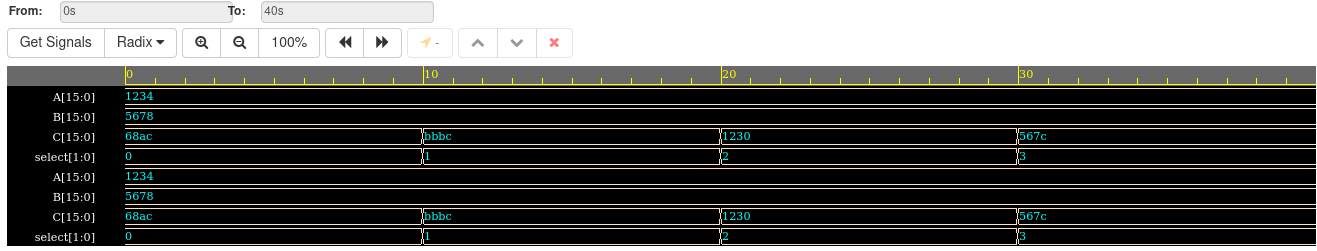
Following are the steps that should be followed for the required Design :

1. Draw a design diagram by writing its inputs and outputs.
2. Connect inputs and outputs where you want to tie according to the design requirement.
3. Write down the Verilog code for Your design
4. Execute the result, You will get a block diagram
5. Develop the test bench

**code:**

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| Design.v | Testbench.v |
| module ALU (  input [15:0] A,  input [15:0] B,  input [1:0] select,  output reg [15:0] C  );  always @(\*) begin  case (select)  2'b00: C = A + B; // Addition  2'b01: C = A - B; // Subtraction  2'b10: C = A & B; // Bitwise AND  2'b11: C = A | B; // Bitwise OR  default: C = 16'h0000; // Default to zero  endcase  end  endmodule | module testbench;  reg [15:0] A, B;  reg [1:0] select;  wire [15:0] C;  // Add $dumpfile and $dumpvars here  initial begin  $dumpfile("dump.vcd"); // Specify the VCD file name  $dumpvars(0, testbench); // Dump all variables in this module  end  ALU uut (  .A(A),  .B(B),  .select(select),  .C(C)  );  initial begin  $display("Testing the ALU");  A = 16'h1234; // Sample input A  B = 16'h5678; // Sample input B  // Test addition (select = 00)  select = 2'b00;  #10;  if (C == 16'h68AC)  $display("Addition Test PASSED");  else  $display("Addition Test FAILED");  // Test subtraction (select = 01)  select = 2'b01;  #10;  if (C == 16'hBBBC)  $display("Subtraction Test PASSED");  else  $display("Subtraction Test FAILED");  // Test bitwise AND (select = 10)  select = 2'b10;  #10;  if (C == 16'h0220)  $display("Bitwise AND Test PASSED");  else  $display("Bitwise AND Test FAILED");  // Test bitwise OR (select = 11)  select = 2'b11;  #10;  if (C == 16'h58FC)  $display("Bitwise OR Test PASSED");  else  $display("Bitwise OR Test FAILED");  $finish;  end  endmodule |

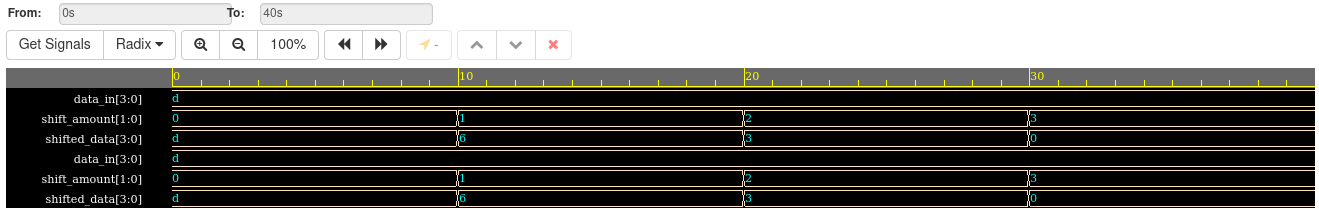
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**Lab Task:**

1. **Design a Barrel shifter and verify the design by test bench.**

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| Design.vs | Testbench.vs |
| module barrel\_shifter (  input wire [3:0] data\_in,  input wire [1:0] shift\_amount,  output wire [3:0] shifted\_data  );  assign shifted\_data = (shift\_amount == 2'b00) ? data\_in :  (shift\_amount == 2'b01) ? data\_in >> 1 :  (shift\_amount == 2'b10) ? data\_in >> 2 :  4'b0000;  endmodule | module testbench;  reg [3:0] data\_in;  reg [1:0] shift\_amount;  wire [3:0] shifted\_data;  barrel\_shifter uut (  .data\_in(data\_in),  .shift\_amount(shift\_amount),  .shifted\_data(shifted\_data)  );  initial begin  $dumpfile("dump.vcd");  $dumpvars(0, testbench);  data\_in = 4'b1101;  shift\_amount = 2'b00; // No shift  #10;  shift\_amount = 2'b01; // Right shift by 1  #10;  shift\_amount = 2'b10; // Right shift by 2  #10;  shift\_amount = 2'b11; // Clear (right shift by 4)  #10;  $finish;  end  endmodule |

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**LAB ASSIGNMENT**

**Q. How you can Convert the text into speech signal in Matlab?**

**Simulate your code and show plots of speech signal.**