# IPC

**The Institute for**

**Interconnecting**

**and Packaging**

**Electronic Circuits**

# IPC-2221

# Generic Standard on Printed Board Design

**IPC-2221**

**Standardization**

In May 1995 the IPC's Technical Activities Executive Committee adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

**Standards Should:**
• Show relationship to DFM & DFE
• Minimize time to market
• Contain simple (simplified) language
• Just include spec information
• Focus on end product performance
• Include a feed back system on use and problems for future improvement

**Standards Should Not:**
• Inhibit innovation
• Increase time-to-market
• Keep people out
• Increase cycle time
• Tell you how to make something
• Contain anything that cannot be defended with data

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The material in this standard was developed by the IPC-D-275 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) of the Institute for Interconnecting and Packaging Electronic Circuits.

**IPC-2221**

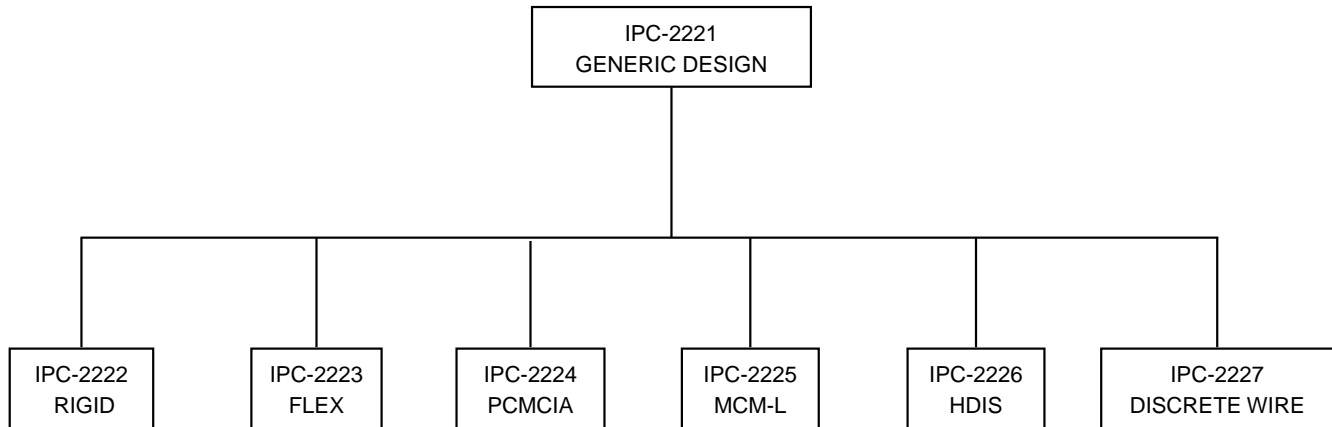# Generic Standard on Printed Board Design

Developed by the IPC-D-275 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) of the Institute for Interconnecting and Packaging Electronic Circuits

Users of this standard are encouraged to participate in the development of future revisions.

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                    │   HIERARCHY OF IPC DESIGN SPECIFICATIONS    │
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| IPC-2222 RIGID | IPC-2223 FLEX | IPC-2224 PCMCIA | IPC-2225 MCM-L | IPC-2226 HDIS | IPC-2227 DISCRETE WIRE |
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**FOREWORD**

This standard is intended to provide information on the generic requirements for organic printed board design. All aspects and details of the design requirements are addressed to the extent that they can be applied to the broad spectrum of those designs that use organic materials or organic materials in combination with inorganic materials (metal, glass, ceramic, etc.) to provide the structure for mounting and interconnecting electronic, electromechanical, and mechanical components. It is crucial that a decision pertaining to the choice of product types be made as early as possible. Once a component mounting and interconnecting technology has been selected the user should obtain the sectional document that provides the specific focus on the chosen technology.

It may be more effective to consider alternative printed board construction types for the product being designed. As an example the application of a rigid-flex printed wiring board may be more cost or performance effective than using multiple printed wiring boards, connectors and cables.

IPC's documentation strategy is to provide distinct documents that focus on specific aspect of electronic packaging issues. In this regard document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0).

Included in the set is the generic information which is contained in the first document of the set and identified by the four digit set number. The generic standard is supplemented by one or many sectional documents each of which provide specific focus on one aspect of the topic or the technology selected. The user needs, as a minimum, the generic design document, the sectional of the chosen technology, and the engineering description of the final product.

As technology changes specific focus standards will be updated, or new focus standards added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of ''Suggestions for Improvement'' forms located at the end of each document.

# Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC-D-275 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

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## Figures

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# Generic Standard on Printed Board Design

## 1.0 SCOPE

This standard establishes the generic requirements for the design of organic printed boards and other forms of component mounting or interconnecting structures. The organic materials may be homogeneous, reinforced, or used in combination with inorganic materials; the interconnections may be single, double, or multilayered.

**1.1 Purpose** The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of a specific interconnecting structure sectional standard (see 1.2) to produce detailed designs intended to mount and attach passive and active components.

The components may be through-hole, surface mount, fine pitch, ultra-fine pitch, array mounting or unpackaged bare die. The materials may be any combination able to perform the physical, thermal, environmental, and electronic function.

**1.2 Documentation Hierarchy** This standard identifies the generic physical design principles, and is supplemented by various sectional documents that provide details and sharper focus on specific aspects of printed board technology. Examples are:

IPC-2222   Rigid organic printed board structure design
IPC-2223   Flexible printed board structure design
IPC-2224   Organic, PC card format, printed board structure design
IPC-2225   Organic, MCM-L, printed board structure design
IPC-2226   High Density Interconnect (HDI) structure design
IPC-2227   Organic board design using discrete wiring

The list is a partial summary and is not inherently a part of this generic standard. The documents are a part of the PWB Design Document Set which is identified as IPC-2220. The number IPC-2220 is for ordering purposes only and will include all documents which are a part of the set, whether released or in-process proposal format at the time the order is placed.

**1.3 Presentation** All dimensions and tolerances in this standard are expressed in SI (metric) units. Users of this and the corresponding performance and qualification specifications are expected to use metric dimensions.

**1.4 Interpretation** "**Shall**," the imperative form of the verb, is used throughout this standard whenever a require-

ment is intended to express a provision that is mandatory. Deviation from a "**shall**" requirement may be considered if sufficient data is supplied to justify the exception.

The words "should" and "may" are used whenever it is necessary to express non-mandatory provisions. "Will" is used to express a declaration of purpose.

To assist the reader, the word "**shall**" is presented in bold characters.

**1.5 Definition of Terms** The definition of all terms used herein **shall** be as specified in IPC-T-50.

**1.6 Classification of Products** This standard recognizes that rigid printed boards and printed board assemblies are subject to classifications by intended end item use. Classification of producibility is related to complexity of the design and the precision required to produce the particular printed board or printed board assembly.

Any producibility level or producibility design characteristic may be applied to any end-product equipment category. Therefore, a high-reliability product designated as Class "3" (see 1.6.2), could require level "A" design complexity (preferred producibility) for many of the attributes of the printed board or printed board assembly (see 1.6.3).

**1.6.1 Board Type** This standard provides design information for different board types. Board types vary per technology and are thus classified in the design sectionals.

**1.6.2 Performance Classes** Three general end-product classes have been established to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there may be an overlap of equipment between classes. The printed board user has the responsibility to determine the class to which his product belongs. The contract **shall** specify the performance class required and indicate any exceptions to specific parameters, where appropriate.

*Class 1 General Electronic Products* Includes consumer products, some computer and computer peripherals, as well as general military hardware suitable for applications where cosmetic imperfections are not important and the major requirement is function of the completed printed board or printed board assembly.

*Class 2 Dedicated Service Electronic Products* Includes communications equipment, sophisticated business machines, instruments and military equipment where high

performance and extended life is required, and for which uninterrupted service is desired but is not critical. Certain cosmetic imperfections are allowed.

*Class 3 High Reliability Electronic Products* Includes the equipment for commercial and military products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated, and must function when required such as for life support items, or critical weapons systems. Printed boards and printed board assemblies in this class are suitable for applications where high levels of assurance are required and service is essential.

**1.6.3 Producibility Level** When appropriate this standard will provide three design complexity levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

Level A   General Design Complexity—Preferred
Level B   Moderate Design Complexity—Standard
Level C   High Design Complexity—Reduced

The producibility levels are not to be interpreted as a design requirement, but a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the numerous tables are to be used as a guide in determining what the level of producibility will be for any feature. The specific requirement for any feature that must be controlled on the end item **shall** be specified on the master drawing of the printed board or the printed board assembly drawing.

## 2.0 APPLICABLE DOCUMENTS

The following documents form a part of this document to the extent specified herein. If a conflict of requirements exist between IPC-2221 and those listed below, IPC-2221 takes precedence.

**2.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)[1]**

**IPC-A-22**   UL Recognition Test Pattern

**IPC-T-50**   Terms and Definitions for Interconnecting and Packaging Electronic Circuits

**IPC-L-109**   Specification for Resin Preimpregnated Fabric (Prepreg) for Multilayer Printed Boards

**IPC-MF-150**   Metal Foil for Printed Wiring Applications

**IPC-CF-152**   Composite Metallic Material Specification for Printed Wiring Boards

**IPC-FC-232**   Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring

**IPC-D-279**   Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

**IPC-D-310**   Guidelines for Phototool Generation and Measurement Techniques

**IPC-D-317**   Design Guidelines for Electronic Packaging Utilizing High-speed Techniques

**IPC-D-322**   Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes

**IPC-D-325**   Documentation Requirements for Printed Boards

**IPC-D-330**   Design Guide Manual

**IPC-D-350**   Printed Board Description in Digital Form

**IPC-D-356**   Bare Substrate Electrical Test Data Format

**IPC-D-422**   Design Guide for Press Fit Rigid Printed Board Backplanes

**IPC-TM-650**   Test Methods Manual
Method 2.4.22   Bow and Twist

**IPC-ET-652**   Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

**IPC-CM-770**   Printed Board Component Mounting

**IPC-SM-780**   Component Packaging and Interconnecting with Emphasis on Surface Mounting

**IPC-SM-782**   Surface Mount Design and Land Pattern Standard

**IPC-SM-785**   Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

**IPC-MC-790**   Guidelines for Multichip Module Technology Utilization

**IPC-CC-830**   Qualification and Performance of Electrical Insulating Compound for Printed Board

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1. The Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062-6135

**IPC-SM-840** Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

**IPC-2510 Series**

**IPC-2511** Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer Methodology

**IPC-2513** Drawing Methods for Manufacturing Data Description (formerly IPC-D-351)

**IPC-2514** Printed Board Manufacturing Data Description (formerly IPC-D-350)

**IPC-2515** Bare Board Product Electrical Testing Data Description (formerly IPC-D-356)

**IPC-2516** Assembled Board Product Manufacturing (formerly IPC-D-355)

**IPC-2518** Parts List Product Data Description (formerly IPC-D-354)

**IPC-2615** Printed Board Dimensions and Tolerances

**IPC-4101** Laminate/Prepreg Materials Standard for Printed Boards

**IPC-6011** Generic Performance Specification for Printed Boards

**IPC-6012** Qualification and Performance Specification for Rigid Printed Boards

**IPC-100002** Universal Drilling & Profile Master Drawing

**IPC-100047** Composite Test Pattern Basic Dimension Drawing - Ten Layer

**IPC-100103** Master Drawing for Capability Test Board (Ten Layer Multilayer Board without Blind or Buried Vias)

**SMC-TR-001** An Introduction to Tape Automated Bonding Fine Pitch Technology

**2.2 Joint Industry Standards[1]**

**J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies

**J-STD-003** Solderability Tests for Printed Boards

**J-STD-005** Requirements for Soldering Pastes

**J-STD-006** Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

**J-STD-012** Implementation of Flip Chip and Chip Scale Technology

**J-STD-013** Implementation of Ball Grid Array and Other High Density Technology

**2.3 Military[2]**

**MIL-G-45204** Gold Plating (Electrodeposited)

**2.4 Federal[2]**

**QQ-N-290** Nickel Plating (Electrodeposited)

**QQ-A-250** Aluminum Alloy, Plate and Sheet

**QQ-S-635** Steel

**2.5 American Society for Testing and Materials[3]**

**ASTM-B-152** Copper Sheet, Strip and Rolled Bar

**ASTM-B-579** Standard Specification for Electrodeposited Coating of Tin-Lead Alloy (Solder Plate)

**2.6 Underwriters Labs[4]**

**UL-746E** Standard Polymeric Materials, Material used in Printed Wiring Boards

**2.7 IEEE[5]**

**IEEE 1149.1** Standard Test Access Port and Boundary-Scan Architecture

**2.8 ANSI[6]**

**ANSI/EIA 471** Symbol and Label for Electrostatic Sensitive Devices

**3.0 GENERAL REQUIREMENTS**

The information contained in this section describes the general parameters to be considered by all disciplines prior to and during the design cycle.

Designing the physical features and selecting the materials for a printed wiring board involves balancing the electrical, mechanical and thermal performance as well as the reliability, manufacturing and cost of the board. The tradeoff checklist (see Table 3-1) identifies the probable effect of

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2. Application for copies should be addressed to Standardization Documents Order Desk, Building 4D, 700 Robbins Avenue, Philadelphia, PA 19111-5094

3. American Society for Testing and Materials, 100 Barr Habor Drive, West Conshohocken, PA 19428-2959

4. Underwriters Labs, 333 Pfngsten Road, Northbrook, IL 60062-2002

5. IEEE, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331

6. ANSI, 655 15th Street N.W., Suite 300, Washington, DC 20005-5794

changing each of the physical features or materials. The items in the checklist need to be considered if it is necessary to change a physical feature or material from one of the established rules. Cost can also be affected by these parameters as well as those in Table 5-1.

**3.1 Information Hierarchy**

**3.1.1 Order of Precedence**   In the event of any conflict in the development of new designs, the following order of precedence **shall** prevail:

1. The procurement contract

2. The master drawing or assembly drawing (supplemented by an approved deviation list, if applicable)

3. This standard

4. Other applicable documents

**3.2 Design Layout**   The layout generation process should include a formal design review of layout details by as many affected disciplines within the company as possible, including fabrication, assembly and testing. The approval of the layout by representatives of the affected disciplines will ensure that these production-related factors have been considered in the design.

The success or failure of an interconnecting structure design depends on many interrelated considerations. From an end-product usage standpoint, the impact on the design by the following typical parameters should be considered.

• Equipment environmental conditions, such as ambient temperature, heat generated by the components, ventilation, shock and vibration.

• If an assembly is to be maintainable and repairable, consideration must be given to component/circuit density, the selection of board/conformal coating materials, and component placement for accessibility.

• Installation interface that may affect the size and location of mounting holes, connector locations, lead protrusion limitations, part placement, and the placement of brackets and other hardware.

• Testing/fault location requirements that might affect component placement, conductor routing, connector contact assignments, etc.

• Process allowances such as etch factor compensation for conductor widths, spacings, land fabrication, etc. (see Section 5 and Section 9).

• Manufacturing limitations such as minimum etched features, minimum plating thickness, board shape and size, etc.

• Coating and marking requirements.

• Assembly technology used, such as surface mount, through hole, and mixed.

• Board performance class (see 1.6.2).

• Materials selection (see Section 4).

• Producibility of the printed board assembly as it pertains to manufacturing equipment limitations.
  – Flexibility (Flexural) Requirements
  – Electrical/Electronic
  – Performance Requirements

• ESD sensitivity considerations

**3.2.1 End-Product Requirements**   The end-product requirements **shall** be known prior to design start-up. Maintenance and serviceability requirements are important factors which need to be addressed during the design phase. Frequently, these factors affect layout and conductor routing.

**3.3 Schematic/Logic Diagram**   The initial schematic/logic diagram designates the electrical functions and interconnectivity to be provided to the designer for the printed board and its assembly. This schematic should define, when applicable, critical circuit layout areas, shielding requirements, grounding and power distribution requirements, the allocation of test points, and any preassigned input/output connector locations. Schematic information may be generated as hard copy or computer data (manually or automated).

**3.4 Parts List**   A parts list is a tabulation of parts and materials used in the construction of a printed board assembly. All end item identifiable parts and materials **shall** be identified in the parts list or on the field of the drawing. Excluded are those materials used in the manufacturing process, but may include reference information; i.e., specifications pertinent to the manufacture of the assembly and reference to the schematic/logic diagram.

All mechanical parts appearing on the assembly pictorial **shall** be assigned an item number which **shall** match the item number assigned on the parts list.

Electrical components, such as capacitors, resistors, fuses, IC's, transistors, etc., **shall** be assigned reference designators, (Ex. C5, CR2, F1, R15, U2, etc.). Assignment of electrical reference designators **shall** be the same as (match) those assignments given to the same components on the Logic/schematic diagram.

It is advisable to group like items; e.g., resistors, capacitors, IC's, etc., in some sort of ascending or numerical order.

The parts list may be handwritten, manually typed on to a standard format, or computer generated.

**3.5 Test Requirement Considerations**   Normally, prior to starting a design, a testability review meeting should be held with fabrication, assembly, and testing. Testability

**Table 3-1   PWB Design/Performance Tradeoff Checklist Considerations[1]**

| Physical Feature | Class[2] | Parameter | If Value of Physical Feature is Increased | | | |
|---|---|---|---|---|---|---|
| | | | Parameter is: | | Resulting Performance or Reliability is: | |
| | | | Increased | Decreased | Enhanced | Degraded |
| Dielectric Thickness to Ground | EP | Lateral Crosstalk | X | | | X |
| | EP | Vertical Crosstalk | X | | | X |
| | EP | Characteristic Impedance | X | | | X |
| | MP | Physical Size/Weight | X | | | X |
| Line Spacing | EP | Lateral Crosstalk | | X | X | |
| | M/Y | Electrical Isolation | X | | X | |
| Coupled Line Length | EP | Lateral Crosstalk | X | | | X |
| | EP | Vertical Crosstalk | X | | | X |
| Line Width | EP | Lateral Crosstalk | | X | X | |
| | EP | Vertical Crosstalk | X | | | X |
| | EP | Characteristic Impedance | X | | Design Driven | |
| | R | Signal Conductor Integrity | X | | X | |
| | M/Y | Electrical Continuity | X | | X | |
| Dual Stripline | EP | Lateral Crosstalk | | X | X | |
| | EP | Vertical Crosstalk | | X | X | |
| | EP | Reflections | | X | X | |
| | MP | Physical Size/Weight | | X | | |
| | M/Y | Electrical Continuity | | X | | X |
| Line Thickness | EP | Lateral Crosstalk | X | | | X |
| | R | Signal Conductor Integrity | X | | X | |
| Vertical Line Spacing | EP | Vertical Crosstalk | | X | X | |
| $Z_0$ of PWB vs. $Z_0$ of Device | EP | Reflections | | X | X | |
| PTH Grid Spacing | MP | Physical Size/Weight | X | | X | |
| Signal Layer Quantity | MP | Physical Size/Weight | X | | | X |
| | M/Y | Layer-to-Layer Registration | | X | | X |
| Component I/O Pitch | MP | Physical Size/Weight | X | | X | |
| Board Thickness | R | PTH Integrity | | X | | X |
| | M/Y | PTH Plating Thickness | | X | | X |
| Copper Plating Thickness | R | PTH Integrity | X | | X | |
| Overplate (Nickel -Kevlar only) | R | PTH Integrity | X | | X | |
| Hole Diameter | M/Y | PTH Plating Thickness | X | | X | |
| Dielectric Thickness | EP | Lateral Crosstalk | X | | | X |
| | EP | Vertical Crosstalk | | X | X | |
| | EP | Characteristic Impedance | X | | | |
| | MP | Physical Size/Weight | X | | | X |
| | R | PTH Integrity | | X | | X |
| | MP | Flatness Stability | X | | X | |
| Insulation Resistance | EP | Lateral Crosstalk | | X | X | |
| | EP | Vertical Crosstalk | | X | X | |
| Dielectric Constant | EP | Characteristic Impedance | X | | | |
| Density Dielectric and Metal | MP | Physical Size/Weight | X | | | X |
| CTE (out-of-plane) | R | PTH Integrity | | X | | X |

**Table 3-1  PWB Design/Performance Tradeoff Checklist Considerations[1] (continued)**

| Physical Feature | Class[2] | Parameter | If Value of Physical Feature is Increased | | | |
|---|---|---|---|---|---|---|
| | | | Parameter is: | | Resulting Performance or Reliability is: | |
| | | | Increased | Decreased | Enhanced | Degraded |
| CTE (in-plane) | R | Solder Joint Integrity | | X | | X |
| | R | Signal Conductor Integrity | | X | | X |
| Resin $T_g$ | R | PTH Integrity | X | | X | |
| | R | Solder Joint Integrity | X | | X | |
| Copper Ductility | R | PTH Integrity | X | | X | |
| | R | Signal Conductor Integrity | X | | X | |
| Copper Peel Strength | R | Solder Land Adhesion (Footprint) | X | | X | |
| Dimensional Instability | M/Y | Layer-to-Layer Misregistration | X | | | X |
| Mechanical Feature Clearances (Internal) | EP/MP/R | Electrical Performance | X | | X | |

1. How to read Table 3-1: As an example, the first row of the table indicates that if the dielectric thickness to ground is increased, the lateral crosstalk also increases and the resultant performance of the PWB is degraded (because lateral crosstalk is not a desired property).

2. EP = Electrical Performance, MP = Mechanical Performance, R = Reliability, M/Y = Manufacturability/Yield

concerns, such as circuit visibility, density, operation, circuit controllability, partitioning, and special test requirements and specifications are discussed as a part of the test strategy. See Appendix A for a checklist of design for testability criteria.

During the design testability review meeting, tooling concepts are established, and determinations are made as to the most effective tool-cost versus board layout concept conditions.

During the layout process, any circuit board changes that impact the test program, or the test tooling, should immediately be reported to the proper individuals for determination as to the best compromise. The testing concept should develop approaches that can check the board for problems, and also detect fault locations wherever possible. The test concept and requirements should economically facilitate the detection, isolation, and correction of faults of the design verification, manufacturing, and field support of the printed board assembly life cycle.

**3.5.1 Printed Board Assembly Testability**  Design of a printed board assembly for testability normally involves systems level testability issues. In most applications, there are system level fault isolation and recovery requirements such as mean time to repair, percent up time, operate through single faults, and maximum time to repair. To meet the contractual requirements, the system design may include testability features, and many times these same features can be used to increase testability at the printed board assembly level. The printed board assembly testability philosophy also needs to be compatible with the overall integrations, testing and maintenance plans for the contract. The factory testers to be used, how integration and test is planned, when printed board assemblies are conformal

coated, the depot and field test equipment capabilities and personnel skill level are all factors that must be considered when developing the printed board assembly test strategy. The test philosophy may be different for different phases of the program. For example, the first unit debug philosophy may be much different than the test philosophy for spares when all the systems have already been shipped.

Before the PWB design starts, requirements for the system testability functions should be presented at the conceptual design review. These requirements and any derived requirements should be partitioned down to the various printed board assemblies and documented. The system and program level test criteria and how they are partitioned down to the printed board assembly requirements are beyond the scope of this document. Appendix A provides an example of a checklist to be used in evaluating the testability of the design.

The two basic types of printed board assembly test are functional test and in-circuit test. Functional testing is used to test the electrical design functionality. Functional testers access the board under test through the connector, test points, or bed-of-nails. The board is functionally tested by applying pre-determined stimuli (vectors) at the printed board assembly's inputs while monitoring the printed board assembly outputs to ensure that the design responds properly.

In-circuit testing is used to find manufacturing defects in printed board assemblies. In-circuit testers access the board under test through the use of a bed-of-nails fixture which makes contact with each node on the printed board assembly. The printed board assembly is tested by exercising all the parts on the board individually. In-circuit testing places less restrictions on the design. Conformal coated printed

board assemblies and many Surface Mount Technology (SMT) and mixed technology printed board assemblies present bed-of-nails physical access problems which may prohibit the use of in-circuit testing. Primary concerns for in-circuit test are that the lands or pins (1) must be on grid (for compatibility with the use of bed-of-nails fixture) and (2) should be accessible from the bottom side (a.k.a. non-component or solder side of through-hole technology boards) of the printed board assembly.

Manufacturing Defects Analyzer (MDA) provide a low cost alternative to the traditional in-circuit tester. Like the in-circuit tester, the MDA examines the construction of the printed board assembly for defects. It performs a subset of the types of tests, mainly only tests for shorts and opens faults without power applied to the printed board assembly. For high volume production with highly controlled manufacturing processes (i.e., Statistical Process Control techniques), the MDA may have application as a viable part of a printed board assembly test strategy.

Vectorless Test is another low cost alternative to in-circuit testing. Vectorless Test performs testing for finding manufacturing process-related pin faults for SMT boards and does not require programming of test vectors. It is a powered-off measurement technique consisting of three basic types of tests:

1. *Analog Junction Test* – DC current measurement test on unique pin pairs of the printed board assembly using the ESD protection diodes present on most digital and mixed signal device pins.

2. *RF Induction Test* – Magnetic induction is used to test for device faults utilizing the printed board assemblies devices protection diodes. This technique uses chip's power and ground pins to make measurements for finding solder opens on device signal paths, broken bond wires, and devices damaged by ESD. Parts incorrectly oriented can also be detected. Fixturing containing magnetic inducers are required for this type of test

3. *Capacitive Coupling Test* – This technique uses capacitive coupling to test for pin opens and does not rely on internal device circuitry but instead relies on the presence of the metallic lead frame of the device to test the pins. Connectors and sockets, lead frames and correct polarity of capacitors can be tested using the technique.

**3.5.2 Boundary Scan Testing** As printed board assemblies become more dense with fine pitch devices, physical access to printed board assembly nodes for in-circuit testing may not be possible. The boundary scan standard for integrated circuits (IEEE 1149.1) provides the means to perform virtual in-circuit testing to alleviate this problem. Boundary scan architecture is a scan register approach where, at the cost of a few I/O pins and the use of special scan registers in strategic locations throughout the design,

the test problem can be simplified to testing of simpler, mostly combinational circuits.

In many applications, the inclusion of scan registers on the inputs and outputs of the printed board assembly allows the board to be tested while installed. If the circuit is more complex, additional sets of scan registers can be included in the design to capture intermediate results and apply test vectors to exercise portions of the design.

A full description of the standard access port and boundary scan architecture can be found in IEEE 1149.1. The full test access port capabilities are not needed to gain significant testability via the scan registers.

The decision to use boundary scan test as part of a test strategy should consider the availability of boundary scan parts and the return on investment for capital equipment and software tools required for implementing this test technique. Boundary scan testing can be conducted using a low cost PC-based tester which requires access to the printed board assembly under test through the edge connector or an existing functional, in-circuit, or hybrid tester that may be adapted to perform boundary scan testing.

**3.5.3 Functional Test Concern for Printed Board Assemblies** There are several concerns for designing the printed board assembly for functional testability. The use of test connectors, problems with initialization and synchronization, long counter chains, self diagnostics, and physical testing are topics which are discussed in detail in the following subsections and are not meant to be tutorials on testability but rather ideas of how to overcome typical functional testing problems.

**3.5.3.1 Test Connectors** Fault isolation on conformal coated boards or most SMT and mixed technology designs can be very difficult because of the lack of access to the circuitry on the board.

If strategic signals are brought out to a test connector or an area on the printed board where the signals can be probed (test points), fault isolation may be much improved. This lowers the cost of detection, isolation and correction.

It is also possible to design the circuit so that a test connector can be used to stimulate the circuit (such as taking over a data bus via the test connector) or disable functions on the printed board assembly (such as disabling a free running oscillator and adding single step capability via the test connector).

**3.5.3.2 Initialization and Synchronization** Some designs or portions of a design do not need any initialization circuitry because the circuit will quickly cycle into its intended function. Unfortunately, it is sometimes very difficult to synchronize the tester with this type of circuit because the tester would need to be programmed to stimulate the circuit until a predetermined signature is found on the outputs of the circuit. This can be difficult to achieve.

With relatively little difference in the design, initialization capability can usually be designed into the circuitry allowing the printed board assembly to be quickly initialized and the circuit and the tester can follow the expected outputs of the printed board assembly.

Free running oscillators also present a problem in testing because of the synchronization problem with the test equipment. These problems can be overcome by (1) adding test circuitry to select a test clock instead of the oscillator; (2) removing the oscillator for test and injecting a test clock; (3) overriding the signal; or (4) designing the clock system so that the clocking can be controlled via a test connector or test points.

**3.5.3.3 Long Counter Chains**  Long counter chains in the design with signals used from many stages of the counter chain present another testability problem. Testability can be very bad if there is no means to preset the counter chain to different values to facilitate testing of the logic that is driven from the high order stages of the counter chain.

Testability is much improved if the counter chain is either broken into smaller counter chains (perhaps no more than 10 stages) which can be individually controlled or if the counter chain can be loaded via the test software. The test software can then verify the operation of the logic that is driven from the counter stages without wasting the simulation and test time that would be required to clock through the complete counter chain.

**3.5.3.4 Self Diagnostics**  Self diagnostics are sometimes imposed either contractually or via derived requirements. Careful consideration should be given to determine how to implement these requirements.

Many times a printed board assembly does not contain functions that lend themselves to self diagnostics at the printed board assembly level but a small group of printed board assemblies, when taken as a unit, do lend themselves to good diagnostics. For example, a complex Fast Fourier Transform (FFT) function may be spread across multiple printed board assemblies. It may be very difficult for any one printed board assembly to self diagnose a problem but it may be very easy to design-in circuitry that self diagnoses the whole FFT function.

The depth of self diagnostics that are needed is usually driven by the line replaceable unit (LRU) which varies with requirements. It may be an integrated circuit or it may be a drawer of electronics depending on the contract, the function of the design, or the system level maintenance philosophy.

For self diagnostics at a printed board assembly level, the printed board assembly is usually put into a test mode and then the printed board assembly applies a known set of test inputs and compares the results with a stored set of

expected responses. If the results do not match the expected responses, the printed board assembly signals the test equipment indicating the printed board assembly failed the self-test. There are many variations on this scheme. Some examples are:

1. The printed board assembly is placed in a feedback loop with the results checked after a predetermined number of cycles.

2. A special test circuit or the Central Processor Unit (CPU) applying the stimuli and comparing the signature of the responses against a known pattern.

3. The printed board assembly performing self-checks when idling and then supplying the results to another (or diagnostic) printed board assembly for verification of the responses, etc.

**3.5.3.5 Physical Test Concerns**  Printed board assembly functional test equipment is usually very expensive and requires highly skilled personnel to operate. If printed board assembly testability is poor, the printed board assembly test operation can be very expensive. There are some simple physical considerations that can decrease the debug time and therefore the overall test costs.

The orientation of polarized parts should be consistent so that the operator does not get confused with parts being oriented 180° out of phase with other parts on the printed board assembly. Non-polarized parts still need to have the pin #1 identified so that the test operator knows which end to probe when guided probe software says to probe a specific pin.

Test connectors are much preferred over test points which require the use of test clips or test hook-up wires. However, test points such as riser leads are preferred over clipping on to the lead of a part. If riser leads are used for temporary testing, such as determining a select-by-test resistor, it is suggested that the risers remain after the installation of the selected component. This allows verification of the selected item without re-fixturing the assembly.

Signals that are not accessible for probing (such as can happen with leadless parts) can greatly increase fault isolation problems. If scan registers are not used, it is recommended that every signal have a land or other test point somewhere on the printed board assembly where the signal can be probed. It is also recommended that lands used for test points be located on grid and placed so that all the probing can be done from the secondary side of the printed board assembly. If it is not feasible to provide capability for probing every signal, then (1) only the strategic signals should have special probing locations and (2) the test vectors need to be increased or other test techniques need to be utilized to assign fault isolation to one component or a small set of components.

Many faults are often due to shorts between the leads of adjacent parts, shorts between a part lead and an external

layer conductor on the printed board or shorts between two printed board conductors on the external layers of the printed board. The physical design must consider these normal manufacturing defects and not impair the isolation of the faults due to lack of access or inconvenient access to signals. As with design for in-circuit testability, probe pad test points should be on grid to allow automated probing to be used in the future.

Partitioning of the design into functions, perhaps digital separated from analog, is sometimes required for electrical performance. Testing concerns also are helped with physical separation of dissimilar functions. Separation of not just the circuitry but also the test connectors or at least grouping the pins on the connectors can help improve testability. Designs that mix digital design with high performance analog design may require testing on two or more sets of test equipment. Separating the signals will not only help the test fixturing but will help the operator in debugging the printed board assembly.

As with in-circuit test fixturing, functional test fixturing can have a significant cost impact. Normally a standard board size or only a few board sizes are used for all designs on a program. Similarly one, or at most a few, test fixtures are typically used for a program. Generating test fixtures can be costly and debugging noise problems in the fixtures or tuning the fixtures to the tester can be expensive. If the test fixturing is not adequately engineered, it may not be possible to accurately measure the board under test. Typically much effort is expended in generating a few test fixtures and it is expected that the fixtures will be used for all the printed board assembly designs. Therefore the test fixturing restrictions must be considered in the printed board assembly design. The fixturing restraints can be significant. Such as (1) requiring ground and voltage supplies on specific connector pins, (2) limiting which pins can be used for high speed signals, (3) limiting which pins can be used for low noise applications, (4) defining power switching limitations, (5) defining voltage and current limitations on each pin, etc.

**3.5.4 In-Circuit Test Concerns for Printed Board Assemblies** In-circuit testing is used to find shorts, opens, wrong parts, reversed parts, bad devices, incorrect assembly of printed board assemblies and other manufacturing defects. In-circuit testing is neither meant to find marginal parts nor to verify critical timing parameters or other electrical design functions.

In-circuit testing of digital printed board assemblies can involve a process that is known as backdriving (see IPC-T-50). Backdriving can also cause devices to oscillate and the tester can have insufficient drive to bring a device out of saturation. Backdriving can be performed only for controlled periods of time, or the junction of the device (with the overdriven output) will overheat.

The two main concerns for designing the printed board and printed board assembly for in-circuit testability are design for compatibility with in-circuit test fixturing and electrical design considerations. These topics are discussed in detail in the following subsections.

**3.5.4.1 In-Circuit Test Fixtures** In-circuit test fixtures are commonly called bed-of-nails fixtures. A bed-of-nails fixture is a device with spring contact probes which contact each node on the board under test. The following guidelines should be followed during printed board assembly layout to promote in-circuit testability in bed-of-nails fixtures:

1. The diameter of lands of plated-through holes and vias used as test lands are a function of the hole size (see 9.1.1). The diameter of test lands used specifically for probing should be no smaller than 0.9 mm. It is feasible to use 0.6 mm diameter test lands on boards under 7700 mm$^2$.

2. Clearances around test probe sites are dependent on assembly processes. Probe sites should maintain a clearance equal to 80% of an adjacent component height with a minimum of 0.6 mm and a maximum of 5 mm (see Figure 3-1).

3. Part height on the probe side of the board must not exceed 5.7mm. Taller parts on this side of the board will require cutouts in the test fixture. Test lands should be located 5 mm away from tall components. This allows for test fixture profiling tolerances during test fixture fabrication (see Figure 3-2).

4. No parts or test lands are to be located within 3 mm of the board edges.

5. All probe areas must be solder coated or covered with a conductive non-oxidizing coating. The test lands must be free of solder resist and markings.

6. Probe the test lands or vias, not the termination/ castellations of leadless surface mount parts or the leads of leaded parts (see Figure 3-3). Contact pressure can cause an open circuit or make a cold solder joint appear good.

7. Avoid requiring probing of both sides of the printed board. Use vias, to bring test points to one side, the bottom side (non-component or solder side of through-hole technology printed board assemblies) of the board. This allows for a reliable and less expensive fixture.

8. Test lands should be on 2.5 mm hole centers, if possible, to allow the use of standard probes and a more reliable fixture.

9. Do not rely on edge connector fingers for test lands. Gold plated fingers are easily damaged by test probes.

10. Distribute the test lands evenly over the board area. When the test lands are not evenly distributed or when
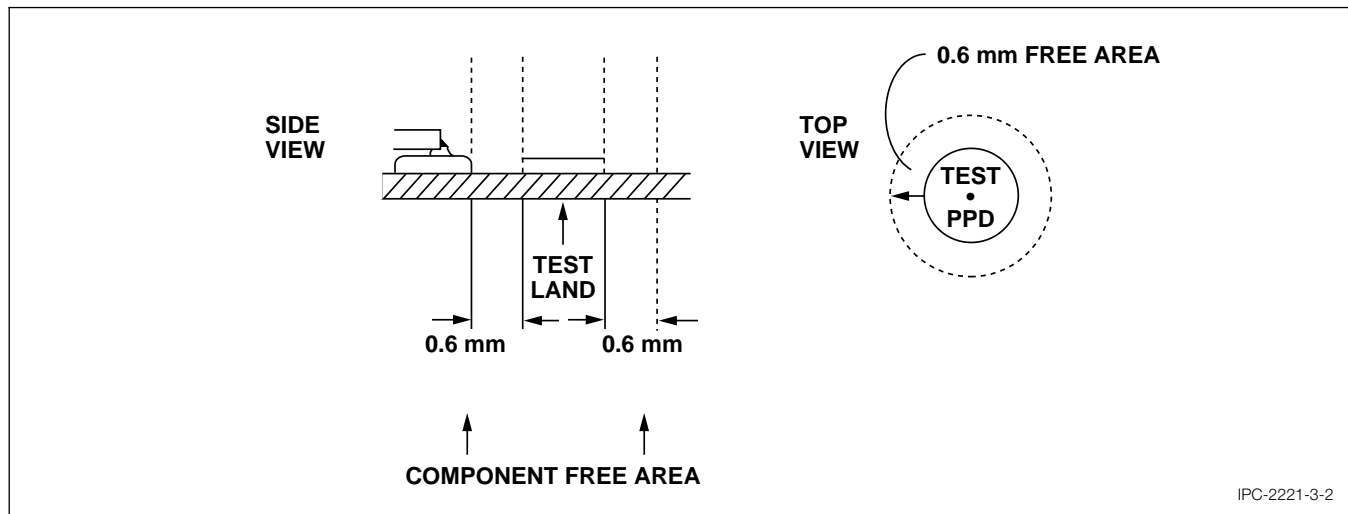
**Figure 3-1    Test Land Free Area for Parts and Other Intrusions**
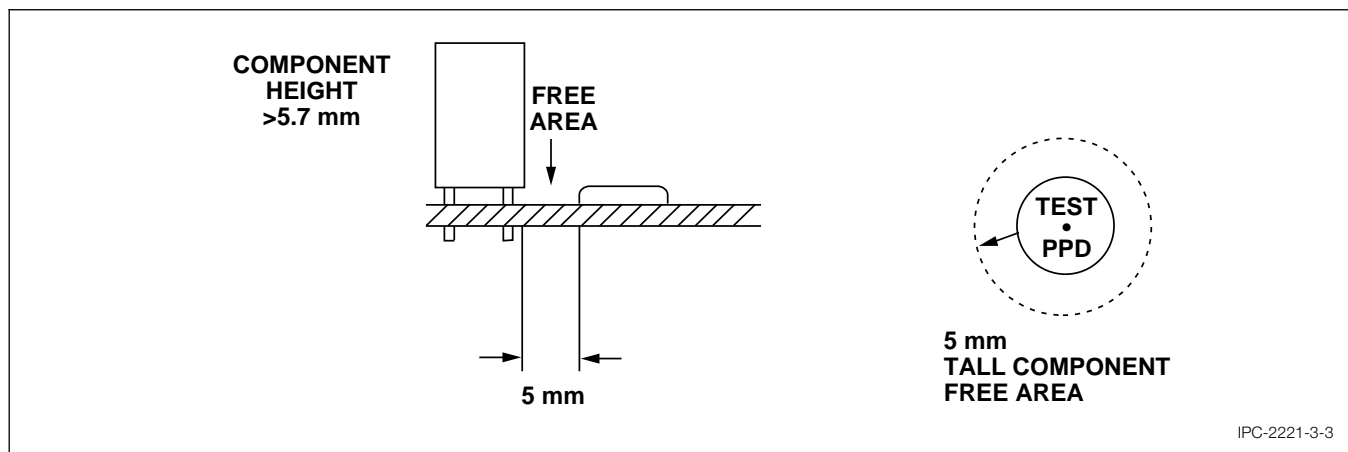


**Figure 3-2    Test Land Free Area for Tall Parts**
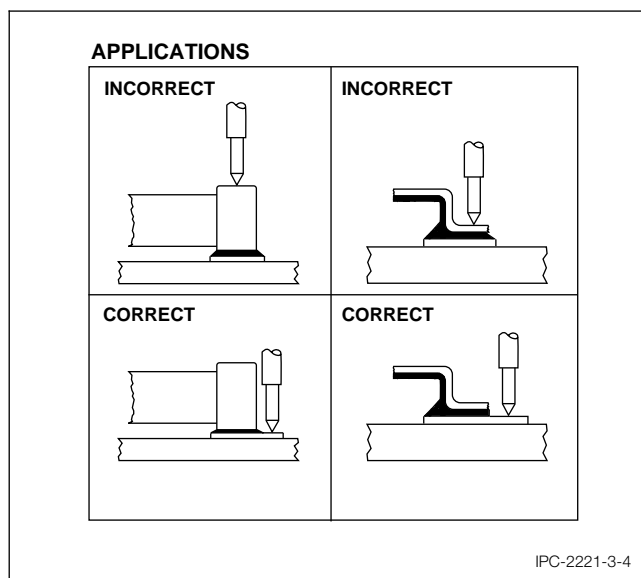


**Figure 3-3    Probing Test Lands**

they are concentrated in one area, the results are board flexing, probing faults, and vacuum sealing problems.

11. A test land must be provided for all nodes. A node is defined as an electrical connection between two or more components. A test land requires a signal name (node signal name), the x-y position axis in respect to the printed board datum point, and a location (describing which side of the board the test land is located). This data is required to build a fixture for SMT and mixed technology printed board assemblies.

12. Mixed technology printed board assemblies and pin grid component boards provide test access for some nodes at the solder side pins. Pins and vias used at test lands must be identified with node signal name and x-y position in reference to the printed board datum point. Use solder mount lands of parts and connectors as test points to reduce the number of generated test lands.

**3.5.4.2 In-Circuit Electrical Considerations** The following electrical considerations should be followed during printed board assembly layout to promote in-circuit testability:

1. Do not wire control line pins directly to ground, $V_{cc}$, or a common resistor. Disabled control lines on a device can make it impossible to use the standard in-circuit library tests. A specialized test with reduced fault coverage and higher program cost is the normal result.

2. A single input vector for tri-stating a device's outputs is preferable for in-circuit testing. Reasons for tri-statable outputs are (1) testers have a limited amount of vectors, (2) the backdrive problems will disappear, and (3) it simplifies the generation of test programs. An example of this which would reduce program cost is tri-statable Programmable Array Logic (PAL) outputs. Use a spare input to a pull-up resistor plus an equation that would enable a normal function in a high state and the device outputs to be tri-stated in a low state.

3. Gate arrays and devices with high pin counts are not testable using an in-circuit tester. Backdrive may not be a problem per pin but the large numbers of pins limit backdrive restrictions. A control line or a single vector to tri-state all device outputs is recommended.

4. Node access and the inability to cover all nodes using standard in-circuit testers is a growing problem. If standard test techniques cannot be applied to detect surface mounted part faults, an alternative method must be developed.

Alternative test strategies must be developed for SMT printed board assemblies with limited nodes. An example of this is a test that will partition the board into groups of clustering components. Each group must have control lines (for testability) and test lands to electrically isolate the cluster from the other devices or groups during test.

Another alternative test method for opens, shorts, and correct devices is boundary scan. This built-in-test-circuitry (electronic bed-of-nails) is gaining momentum in the surface mount printed board assembly area. IEEE Standard 1149.1 is the specification for boundary scan.

**3.5.5 Mechanical**

**3.5.5.1 Uniformity of Connectors** Test fixtures are most often designed for automatic or semiautomatic engagement of edge type or on-board connectors. Connectors should be positioned to facilitate quick engagement and should be uniform and consistent (standardized) in their relationships to the board from one design to another. Similar types of connectors should be keyed, or board geometry used, to ensure proper mating, and prevent electrical damage to the circuitry.

**3.5.5.2 Uniformity of Power Distribution Arrangement and Signal Levels on Connectors** The connector contact position should be uniform for AC and DC power levels, DC common and chassis ground, e.g., contact number 1 is always connected to the same relative circuit power point in each board design. Standardizing contact positions will minimize test fixture cost and facilitate diagnostics.

Signals of widely different magnitude should be isolated to minimize crosstalk.

Logic levels should be located in pre-designated connector contacts.

**3.5.6 Electrical**

**3.5.6.1 Bare Board Testing** Bare board testing **shall** be performed in accordance with IPC-ET-652. If testing will use data from the design area, the configuration and type of data provided will be determined by the method of test selected.

Bare board testing is performed by the printed board supplier and includes continuity, insulation resistance and dielectric withstanding voltage. Suppliers can also perform testing of controlled impedance circuitry. Continuity tests are performed to assure conductors are not broken (opens) or inadvertently connected together (shorts). Insulation resistance and dielectric withstanding voltage testing is performed to assure sufficient conductor spacing and dielectric thickness.

There are two basic types of continuity testing; Golden Board and Intelligent. In Golden Board test, a known good board is tested and its results are used to test all the remaining boards in the lot. If there were an error in the Golden Board, an error in all boards could go undetected. The Intelligent test verifies each board against the design's electrical net list. It will not miss the defects which could be undetected in a Golden Board test.

Designs which do not have all electrical connections available from one side of the board (such as boards with blind or buried vias, components on both sides with via holes solder resist tented or boards bonded to both sides of heatsinks) will require Flip or Clamshell testing. Flip testing tests one side of the board and then the other on two separate fixtures. Connections which require contacting both sides of the board are not evaluated. Clamshell testing uses two fixtures which come in contact with both sides of the board at the same time and is capable of testing all connections. Flip and Clamshell testing costs more than testing performed from one side of the board only.

The following areas **shall** be considered before starting a design.

**3.5.6.2 Testing Surface Mount Patterns** Normally, testing of a bare board involves fixturing where spring loaded

pins contact plated holes. On a surface mount pattern, the ends of the nets are typically not at holes but rather on surface mount lands. There are at least two different strategies for performing testing:

A. Contact the via which is connected to the land and visually inspect to ensure continuity from the via to the land. Vias can be designed such that they are on a common grid which will reduce the need for special fixturing for each part number. The barrels of the plated-through holes that are used for internal electrical connectivity should not be subject to probing unless the force is very low and the point of the probe will not damage the barrel. These barrels can crack or break free from the land on the internal layer if subjected to mechanical stresses.

B. Test to the land itself. This approach will probably require special fixturing since surface mount lands may not all be on a grid. Additionally, computer design systems may place the end-of-net point at a via rather than the land which may require adjustment of test point locations.

**3.5.6.3  Testing of Paired Printed Boards Laminated to a Core**   At least two approaches are available for electrical test:

A. Test the top and bottom of the laminated composite printed board separately. If there are plated holes which provide a side-to-side interconnection, they will require a manual electrical test or visual inspection to ensure hole continuity.

B. Use a clam shell type fixture where both the top and bottom of the composite printed board can be tested together. The use of the first approach will require that the electrical test data be provided in two parts. When networks have terminations on both sides of the printed board, the electrical test data should be split into at least two parts with the end of net occurring at the side-to-side interconnect. "Self learn" testing from a known good board will provide the data automatically in the above format.

**3.5.6.4  Point of Origin**   Electrical test and numerical control data should have a common origin point for ease of constructing electrical test fixtures.

**3.5.6.5  Test Points**   When required by the design, test points for probing **shall** be provided as part of the conductor pattern and **shall** be identified on the drawing set. Vias, wide conductors, or component lead mounting lands may be considered as probe points provided that sufficient area is available for probing and maintaining the integrity of the via, conductor, or component lead mounting joint. Probe points must be free of nonconductive coating materials such as solder resist or conformal coating.

**3.6  Layout Evaluation**

**3.6.1  Board Layout Design**   The design layout from one board design to another should be such that designated areas are identified by function, i.e., power supply section confined to one area, analog circuits to another section, and logic circuits to another, etc. This will help to minimize crosstalk, simplify bare board and assembly test fixture design, and facilitate troubleshooting diagnostics. In addition, the design should:

• Ensure that components have all testable points accessible from the secondary side of the board to facilitate probing with single-sided test fixtures.

• Have feed-throughs and component holes placed away from board edges to allow adequate test fixture clearance.

• Require the board be laid out on a grid which matches the design team testing concept.

• Allow provision for isolating parts of the circuit to facilitate testing and diagnostics.

• Where practical, group test points and jumper points in the same physical location on the board.

• Consider high-cost components for socketing so that parts can be easily replaced.

• Provide optic targets (fiducials) for surface mount designs to allow the use of optic positioning and visual inspection equipment and methods (see 5.4.3).

Surface mounted components and their patterns require special consideration for test probe access, especially if components are mounted on both sides of the board and have very high lead counts.

**3.6.1.1  Layout Concepts**   The printed board layout depicts the physical size and location of all electronic and mechanical components, and the routing of conductors that electrically interconnect the components in sufficient detail to allow the preparation of documentation and artwork.

**3.6.2  Feasibility Density Evaluation**   After approved documents for schematic/logic diagrams, parts lists, and end-product and testing requirements are provided, and before the actual drawing of the layout is begun, a feasibility density evaluation should be made. This should be based on the maximum size of all parts required by the parts list and the total space they and their lands will require on the board, exclusive of interconnection conductor routing.

The total board geometry required for this mounting and termination of the components should then be compared to the total usable board area for this purpose. Reasonable maximum values for this ratio are 70% for Level A, 80% for Level B, and 90% for Level C. Component density values higher than these will be a cause for concern. The lower these values are, the easier it will be to design a cost-effective functional board.

Figure 3-4 provides the usable board area for the standardized board sizes recommended in Figure 5-1.

Table 3-2 gives the area (in 0.5 mm grid elements) a component will occupy on the board for a variety of components. As an example, the 14 lead dual in-line package for through-hole technology occupies a total of 84.0 grid elements. The package outline that encloses the component and land pattern has a grid matrix of 20 x 42 grid elements on 0.5 mm centers. The 20 grid elements establish an outline dimension of 10 mm while the 42 grid elements account for 21 mm. This component area would use up a portion of the board usable area. The component outline does not include grid elements for conductor routing outside the land area. Total component area compared to total usable area provides the conductor routing availability and thus the density percentage.

An alternative method of feasibility density evaluation expresses board density in units of square centimeters per equivalent SOIC. A 16-pin SOIC occupies approximately one $cm^2$ of board area. Figure 3-5 shows a table for determining the SOIC equivalent for a variety of components and the total SOIC equivalents used on the board. This number is then divided into the total square centimeters of usable board area. Reasonable maximum density values are 0.55 $cm^2$ per SOIC for Level A, 0.50 for Level B, and 0.45 for Level C. Density values can increase with additional circuit layers. Also, when using surface mount technology, the potential usable board area is theoretically doubled.

**3.7 Performance Requirements**  Finished printed boards **shall** meet the performance requirements of IPC-6011 and its applicable sectional standard.

| Board Size (Fig. 5-1) | Overall Dimensions | | Usable Dimensions | | Usable Area | | |
|---|---|---|---|---|---|---|---|
| | Height, mm | Width, mm | Height, mm | Width, mm | mm$^2$ | Grid Elements 0.5 mm Grid | cm$^2$ |
| A1 | 80 | 60 | 65 | 50 | 3200 | 12800 | 32 |
| B1 | 170 | | 155 | | 7700 | 30800 | 77 |
| C1 | 260 | | 245 | | 12200 | 48800 | 122 |
| D1 | 350 | | 335 | | 16700 | 66800 | 167 |
| A2 | 80 | 120 | 65 | 110 | 7100 | 28400 | 71 |
| B2 | 170 | | 155 | | 17000 | 68000 | 170 |
| C2 | 260 | | 245 | | 26900 | 107600 | 269 |
| D2 | 350 | | 335 | | 36800 | 147200 | 368 |
| A3 | 80 | 180 | 65 | 170 | 11000 | 44000 | 110 |
| B3 | 170 | | 155 | | 26300 | 105200 | 263 |
| C3 | 260 | | 245 | | 41600 | 166400 | 416 |
| D3 | 350 | | 335 | | 56900 | 227600 | 569 |
| A4 | 80 | 240 | 65 | 230 | 14900 | 59600 | 149 |
| B4 | 170 | | 155 | | 35600 | 142400 | 356 |
| C4 | 260 | | 245 | | 56300 | 225200 | 563 |
| D4 | 350 | | 335 | | 77000 | 308000 | 770 |
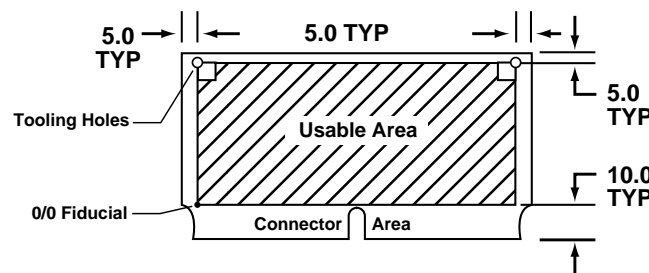


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**Figure 3-4  Example of usable area calculation, mm (Usable area determination includes clearance allowance for edge-board connector area, board guides, and board extractor)**

**Table 3-2   Component Grid Areas**

| Component Description | Type[1] | Number of Grid Elements[2] 0.5 mm Grid | |
|---|---|---|---|
| D07 (without stress relief loop) | THT | 6 x 24 | 144 |
| D07 (with stress relief loop) | THT | 6 x 28 | 168 |
| T05 | THT | 20 x 20 | 400 |
| T024 | THT | 10 x 10 | 100 |
| CK05 | THT | 6 x 12 | 72 |
| CM05, 13000pF | THT | 20 x 44 | 880 |
| CM06, 400pF | THT | 12 x 26 | 312 |
| RC07 | THT | 6 x 20 | 120 |
| RC20 | THT | 10 x 26 | 260 |
| RN60 | THT | 10 x 30 | 300 |
| CQFP-10 T090 | SMT | 16 x 12 | 192 |
| CQFP-28 | SMT | 34 x 34 | 1156 |
| CQFP-144 | SMT | 68 x 68 | 4624 |
| 3216 (1206) | SMT | 4 x 10 | 40 |
| 4564 (1825) | SMT | 14 x 12 | 168 |
| 6032 | SMT | 8 x 18 | 144 |
| DIP-14 | THT | 20 x 42 | 840 |
| DIP-14 | SMT | 22 x 42 | 924 |
| DIP-24 | SMT | 22 x 60 | 1320 |
| DIP-24L | SMT | 26 x 64 | 1664 |
| SOD87/MLL-41 | SMT | 6 x 14 | 84 |
| SOT23 | SMT | 8 x 8 | 64 |
| SOT89 | SMT | 12 x 10 | 120 |
| SOT143 | SMT | 8 x 8 | 64 |
| SQFP 7x7-40 | SMT | 22 x 22 | 484 |
| SOIC-20W | SMT | 28 x 24 | 672 |
| SOIC-36X | SMT | 48 x 24 | 1152 |
| TSOP 10x20 | SMT | 22 x 44 | 968 |
| SOJ 26/350 | SMT | 24 x 34 | 816 |

[1]THT = Through-Hole Technology, SMT = Surface Mount Technology
[2]Grid area includes physical component outlines and land areas. It does not include space for conductor routing.

## 4.0 MATERIALS

**4.1 Material Selection** A designer of printed boards has several material choices to consider, ranging from standard to highly sophisticated and specialized. When specifying materials, the designer must first determine what requirements the printed board must meet. These requirements include temperature (soldering and operating), electrical properties, interconnections (soldered components, connectors), structural strength, and circuit density. It should be noted that increased levels of sophistication may lead to increased material and processing costs.

When constructing a composite from materials with different temperature characteristics, the maximum end-use temperature allowable must be limited to that of the lowest rated material.

Other items that may be important in the comparison of various materials include:

Resin Formula,
Flame Resistance,
Thermal Stability,
Structural Strength,
Electrical Properties,
Flexural Strength,
Maximum Continuous Safe Operating Temperature,
Glass Transition Temperature ($T_g$),
Reinforcing Sheet Material,
Nonstandard Sizes and Tolerances,
Machinability or Punchability,
Coefficients of Thermal Expansion (CTE),
Dimensional Stability, and
Overall Thickness Tolerances.

| PRINTED BOARD DENSITY EVALUATION | | | Date of issue | No. | | Sheet 1 of 1 |
|---|---|---|---|---|---|---|
| | | | | Revised | | |
| DESCRIPTION: SOICs per square centimeter | | | | | | |
| Comp. name | # of comp. | or | IC equiv | Comments | | |
| 8 SOIC | | .50 | | | | |
| 14 SOIC | | 1.00 | | | | |
| 16 SOIC | | 1.00 | | | | |
| 16L SOIC | | 1.00 | | | | |
| 20 SOIC | | 1.25 | | | | |
| 24 SOIC | | 1.50 | | | | |
| 28 SOIC | | 1.75 | | | | |
| 18 PLCC | | 1.13 | | | | |
| 18L PLCC | | 1.13 | | | | |
| 20 PLCC | | 1.25 | | | | |
| 28 PLCC | | 1.75 | | | | |
| 44 PLCC | | 2.75 | | | | |
| 52 PLCC | | 3.25 | | | | |
| 68 PLCC | | 4.25 | | | | |
| 84 PLCC | | 5.25 | | | | |
| SOT 23 | | 0.19 | | | | |
| SOT 89 | | 0.19 | | | | |
| SOMC 1401 | | 1.00 | | | | |
| SOMC 1601 | | 1.00 | | | | |
| 2012 (0805) | | 0.13 | | | | |
| 3216 (1206) | | 0.13 | | | | |
| 3225 (1210) | | 0.13 | | | | |
| 4564 (1812) | | 0.13 | | | | |
| MLL 34 | | 0.13 | | | | |
| MLL 41 | | 0.13 | | | | |
| others (specify) | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

Total IC equivalent _____

| Total board area | (X) | = | cm² cm² |
|---|---|---|---|
| Usable board area | (X) | = | Usable board area Design criteria |

| | ☐ Analog | ☐ Digital |
|---|---|---|
| | Etch & Spac. | / |
| | PWB & GYD Sz | / |

| Devel. by | Date | App'd by | Date |
|---|---|---|---|

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**Figure 3-5   Printed board density evaluation**

**4.1.1 Material Selection for Structural Strength** The first design step in the selection of a laminate is to thoroughly define the service requirements that must be met, i.e., environment, vibration, ''G'' loadings, shock (impact), physical and electrical requirements.

The choice of laminate should be made from standard structures to avoid costly and time consuming proof-out tasks. Several laminates may be candidates, and the choice should be optimized to obtain the best balance of properties.

Materials should be easily available in the form and size required. Special laminate may be costly, and have long lead times. Special laminates should be analyzed against all of the parameters discussed in this section.

Items to be considered are such things as machining, processing, processing costs, and the overall specification of the raw material.

In addition to these parameters, the structural strength of the board must be able to withstand the assembly and operational stresses.

**4.1.2 Material Selection for Electrical Properties**  Some of the critical properties to consider are electrical strength, dielectric constant, moisture resistance, and hydrolytic stability. Table 4-1 lists properties of some of the more common systems. Consult the laminate manufacturer utilized by the fabricator for specific values.

**4.1.3 Material Selection for Environmental Properties**  Table 4-2 shows the properties affected by the environment for some of the more common resin systems. The stated values are typical and will vary among different material suppliers. Consult the laminate manufacturer utilized by the fabricator for specific values.

**4.2 Dielectric Base Materials (Including Prepregs and Adhesives)**

**4.2.1 Bonding Material**  Bonding materials described in the following paragraphs **shall** be used to bond layers of copper foil, bare laminate, copper clad laminate or heat-sinking planes to each other.

**4.2.1.2 Preimpregnated Bonding Layer (Prepreg)**  Prepreg **shall** conform to the types listed in IPC-L-109, IPC-4101, or UL 746E. In most cases, the prepreg should be of the same resin and reinforcement type as the copper clad laminate. The reinforcement style, nominal resin flow, nominal scaled flow thickness, nominal gel time, and nominal resin content are process parameters normally dictated by the printed board manufacturing process.

Unless design constraints dictate, these values **shall** not be included on master drawings, but **shall** only be specified and used in procurement specifications by the printed board manufacturer.

**4.2.2 Adhesives**  Adhesives used in printed board assemblies are drawn from at least five basic resin types covering a wide range of properties. In addition to adhesion quality or bond strength, criteria for adhesive selection include hardness, coefficient of thermal expansion (CTE), service temperature range, dielectric strength, cure conditions and tendency for outgassing. In some cases structural adhesives may be sufficient for thermal bonding applications, see 4.2.5. Each adhesive type has both strong and weak points.

Selection of a resin system for an adhesive or encapsulant is be based on the characteristics of the materials being bonded and their compatibility. Special treatments, such as

**Table 4-1   Typical Properties of Common Dielectric Materials**

| Property | Material | | | | | |
|---|---|---|---|---|---|---|
| | FR-4 (Epoxy E-glass) | Multifunctional Epoxy | High Performance Epoxy | Bismalaimide Triazine/ Epoxy | Polyimide | Cyanate Ester |
| Dielectric Constant (neat resin) | 3.9 | 3.5 | 3.4 | 2.9 | 3.5 - 3.7 | 2.8 |
| Dielectric Constant (reinforcement/ resin)[1] | — | — | — | — | — | — |
| Electric Strength[2] (V/mm) | $39.4 \times 10^3$ | $51.2 \times 10^3$ | $70.9 \times 10^3$ | $47.2 \times 10^3$ | $70.9 \times 10^3$ | $65 \times 10^3$ |
| Volume Resistivity (D-cm) | $4.0 \times 10^6$ | $3.8 \times 10^6$ | $4.9 \times 10^6$ | $4 \times 10^6$ | $2.1 \times 10^6$ | $1.0 \times 10^6$ |
| Water Absorption (wt%) | 1.3 | 0.1 | 0.3 | 1.3 | 0.5 | 0.8 |
| Dissipation Factor (DX) | 0.022 | 0.019 | 0.012 | 0.015 | 0.01 | 0.004 |

[1]For values of dielectric constant, see Table 6-2.
[2]The stated electrical strength values are commonly evaluated under test conditions with a 0.125 mm core laminate thickness. These values should not be considered linear for high voltage designs with a minimum dielectric separation, i.e., less than 0.09 mm.

**Table 4-2  Environmental Properties of Common Dielectric Materials**

| Environmental Property | Material | | | | | |
|---|---|---|---|---|---|---|
| | FR-4 (Epoxy E-glass) | Multifunctional Epoxy (E-glass) | High Performance Epoxy (E-glass) | Bismalaimide Triazine/ Epoxy | Polyimide (E-glass) | Cyanate Ester |
| Thermal Expansion xy-plane (ppm/°C) | 16 - 19 | 14 - 18 | 14 - 18 | $\sim$15 | 8 - 18 | $\sim$15 |
| Thermal Expansion z-axis below $T_g$[3] (ppm/°C) | 50 - 85 | 44 - 80 | $\sim$44 | $\sim$70 | 35 - 70 | 81 |
| Glass Transition Temp. $T_g$ (°C) | 110 - 140 | 130 -160 | 165 - 190 | 175 - 200 | 220 - 280 | 180 - 260 |
| Flexural Modulus (x $10^{10}$ Pa)  Fill[1]  Warp[2] | 1.86  1.20 | 1.86  2.07 | 1.93  2.20 | 2.07  2.41 | 2.69  2.89 | 2.07  2.20 |
| Tensile Strength (x $10^8$ Pa)  Fill[1]  Warp[2] | 4.13  4.82 | 4.13  4.48 | 4.13  5.24 | 3.93  4.27 | 4.82  5.51 | 3.45  4.13 |

[1] Fill - yarns that are woven in a crosswise direction of the fabric.
[2] Warp (cloth) - yarns that are woven in the lengthwise direction of the fabric.
[3] Z-axis expansion above $T_g$ can be as much as four times greater. For FR-4 it is 240-390 ppm. Contact supplier for specific values of the other materials.

primers or activators, may be required to suitably activate surfaces for bonding. The selection process should also consider the exact purpose of the adhesive bond and its use environment. Fungus inert materials are also a consideration. Not all adhesives are suitable for direct application on or near electronic products due to either their chemical or dielectric properties. Incorrect selection of materials may result in product degradation or failure.

In actual application, most adhesive needs can be addressed by a few carefully selected materials. Storage and shelf life limitations apply to most of these materials.

**4.2.2.1 Epoxies**  Epoxy resin formulations are among the most versatile adhesives for electrical insulating and mechanical bonding applications. They offer a wide range of physical and electrical properties, including adhesive and cohesive strengths, hardness, chemical resistance, thermal conductivity and thermal vacuum stability. They are also available with a wide range of cure methods and times. A thorough review of the material is warranted, based on its intended use. Thermal coefficient of expansion and glass transition temperatures should be considered in addition to other properties to preclude problems. Epoxies are available with a variety of modifiers, fillers and reinforcements for specific applications and extended temperature ranges.

**4.2.2.2 Silicone Elastomers**  Silicone elastomers are generally noted for being resilient materials with very goodelectrical and mechanical properties at ambient and extreme temperatures. Several curing methods are available, including moisture, metallic salts and others. Silicone resins which evolve acetic acid should be avoided in elec-

tronic applications. Bond strength, tensile strength, and hardness properties tend to be considerably lower than epoxies. Silicones will swell and dissolve with prolonged exposure to some chemicals. Some of the metallic salts curing silicones will react with TFE, PTFE materials. Conformal coatings, other than silicones, generally will not adhere to cured silicone materials. Silicones are often used as a cushioning overcoat for articles which will be encased in hard potting compounds later.

A number of high purity grades of silicones are available which offer good thermal vacuum stability. Silicone gels are also available, which offer enhanced properties as encapsulants. These materials generally require physical restraint, such as a potting cup or enclosure to maintain their form, once applied.

**4.2.2.3 Acrylics**  Acrylic resins generally provide rapid cures, good electrical and adhesive properties and hardness. Chemical resistance and thermal vacuum stability tend to be considerably lower than the epoxies. The glass transition temperature of these materials also tends to be low.

**4.2.2.4 Polyurethanes**  Polyurethanes are available in almost as many variations as the epoxies. These materials generally offer toughness, high elasticity, a wide range of hardness, and good adhesion. Some of the urethane compounds are outstanding as vibration and shock damping materials. Moisture and chemical resistance is relatively high, but varies with the individual product. Thermal vacuum stability will also vary by the individual product formulation. Many of the urethanes can be used in a relatively thick application as a local vibration damping compound.

**4.2.2.5 Specialized Acrylate-Based Adhesives** This category includes the cyanoacrylates (instant cure) and anaerobic adhesives (cure without air). The cyanoacrylates form strong bonds within seconds without catalysts when only a trace amount of moisture is present on a surface. The anaerobic adhesives cure in the absence of oxygen when a peroxide additive can be decomposed by certain transition metal ions. Both adhesive types can give high initial bond strengths which may be beneficial for wire staking and temporary bonding applications. The instant cure adhesives generally have poor impact resistance and are susceptible to degradation from exposure to moisture and temperatures over 82°C. The anaerobic adhesives have the capability of withstanding higher temperatures but can lose strength with prolonged exposure to chemicals.

**4.2.2.6 Other Adhesives** Many other types and forms of adhesives are available, including polyesters, polyamides, polyimides, rubber resins, vinyl, hot melts, pressure sensitive, etc. Where they are used is determined by the needs of the design and its performance requirements. Selection of specialized items, such as chip bond adhesives, should be done in conjunction with the using facility, in order to ensure full compatibility of the equipment and process.

**4.2.3 Adhesive Films or Sheets** Adhesive films or sheets used for bonding heatsinks, stiffeners, etc., or as insulators, are generally in accordance with IPC-FC-232 or MIL-S-13949.

Film type adhesives find many uses in laminated structures. The ability to pre-cut a film adhesive to fit given shapes or dimensions is a distinct advantage in the fabrication of some laminated parts. Epoxy based film adhesives provide very good bond strength but require elevated temperature cure. Film adhesives are commonly used to bond board heatsinks to printed boards.

Through-hole technology (THT) printed boards and heatsinks may be bonded together with a dry epoxy sheet adhesive to improve heat transfer or resist vibration. These adhesives consist of an epoxy impregnated glass cloth which is cut to the heatsink configuration, assembled between printed board and heatsink, then cured with heat and pressure. The cured adhesive is strong and resists vibration, temperature extremes, and solvents. 0.1 mm should be adequate for most applications; if necessary, specify two thicknesses.

**4.2.4 Electrically Conductive Adhesives** This class of adhesives consists, generally, of a conductive filler, such as graphite (carbon) or silver embedded in a polymeric resin adhesive system. Bonding strength of these materials can be compromised by the filler loading to achieve conductivity. Volume resistivity, a measure of the electrically conductive property of the material, may be varied over a range of values consistent with the intended application. This is accomplished by the type of filler used and the loading.

Epoxies, silicone elastomers and urethanes are the resin systems commonly used to formulate conductive adhesives. The strongest bonds are generally achieved with conductive epoxy, silicone elastomers follow with urethanes a close third. Cure conditions and filler content have a pronounced effect upon tensile strength of these materials. The choice of conductive adhesive for a particular application should consider the strength of bond, the service temperature, the effect of CTE on the bond and the volume resistivity or conductivity required.

**4.2.5 Thermally Conductive/Electrically Insulating Adhesives** Thermally conductive adhesives are filled versions of epoxy, silicone, urethane and some acrylic base materials. The filler is normally dried aluminum oxide or magnesium oxide powder.

**4.2.5.1 Epoxies** The epoxies offer the greatest bond strength and best solvent resistance along with good thermal conductivity and electrical resistance. As with most two part systems, the choice of catalyst has an impact on cure conditions and ultimately could affect the glass transition temperature since it is somewhat dependent upon cure conditions.

**4.2.5.2 Silicone Elastomers** The silicone elastomers are characterized by relatively low bond strengths and less rigidity (lower hardness) than epoxies. They are less resistant to solvent attack than epoxy and are two part systems with variable other properties dependent upon formulation. Thermal conductivity and electrical resistance properties are good.

Silicone elastomers may be obtained as humidity curing or heat curing, the latter offering accelerated cure with applied heat. They cure well in contact with most materials except butyl and chlorinated rubbers, some RTV silicone elastomers and residues of some curing agents. Some bonding applications may require a primer.

**4.2.5.3 Urethanes** Urethanes can be varied through a wide range of hardness, tensile and electrical properties by varying the proportions of curing agent to resin. Consistency can be varied from a soft, rubbery state to a hard, rigid condition by this method. The latitude for formulation optimization over a range of application conditions is an advantage offered by the filled urethanes.

The urethanes are characterized by relatively low bond strengths and less rigidity (lower hardness) than epoxies. They are less resistant to solvent attack than epoxy; are two part systems with variable other properties dependent upon formulation. Thermal conductivity and electrical resistance properties are good.

**4.2.5.4 Use of Structural Adhesives as Thermal Adhesives** In design circumstances where thermal conduction properties are not critical, the use of structural adhesives (see 4.2.2) in place of thermal adhesives may be acceptable as determined by thermal analysis and may be a more cost effective alternative.

**4.3 Laminate Materials** Laminate materials should be selected from material listed in IPC-4101 or IPC-FC-231. When Underwriter's Labs (UL) requirements are imposed, the material used must be approved by UL for use by the printed board manufacturer.

The board design **shall** be such that internal temperature rise due to current flow in the conductor, when added to all other sources of heat at the conductor/laminate interface, will not result in an operating temperature in excess of that specified for the laminate material or maximum sustained operating temperature of the assembly.

Since heat dissipated by parts mounted on the boards will contribute local heating effects, the material selection **shall** take this factor, plus the equipment's general internal rise temperature, plus the specified operating ambient temperature for the equipment into account for maximum operating temperature.

Hot spot temperatures **shall** not exceed the temperatures specified for the laminate material selected. See IPC-2222 for maximum operating temperature specified for laminate materials. Materials used (copper-clad, prepreg, copper foil, heatsink, etc.) **shall** be specified on the master drawing.

**4.3.1 Color Pigmentation** Natural colored stock is preferred, because whenever a pigment is added to change to a color, the possibility exists for the pigment retarding the ability of the impregnating resin to completely wet each and every glass fiber. Without complete wetting, moisture can be trapped.

Colored stock should not be used because the material usually costs more. Production delays may also be incurred because of lack of availability of the colored stock. If colored stock is required, it **shall** be specified on the procurement documentation.

**4.3.2 Dielectric Thickness/Spacing** The minimum dielectric thickness/spacing **shall** be specified on the master drawing.

**4.4 Conductive Materials** The primary function of metallic coatings is to contribute to the formation of the conductive pattern. Beyond this primary function, specific platings offer such additional benefits as corrosion prevention, improved long term solderability, wear resistance, and others.

The thickness and integrity requirements for metallic platings and coatings on as-produced boards **shall** be in accordance with the requirements of Table 4-3 for the appropriate class of equipment. Unless otherwise specified on the master drawing, metallic platings and coatings **shall** meet the requirements specified in 4.4.1 through 4.4.8.

**4.4.1 Electroless Copper Plating** Electroless copper is deposited on the surface and through holes of the printed board as a result of processing the drilled panel through a series of chemical solutions. Typically, this is the first step in the plating process and is usually 0.6 to 2.5 μm thick. Electroless copper can also be used to fully build the required copper thickness, which is referred to as additive plating.

**4.4.2 Semiconductive Coatings** Semiconductive coatings for direct metallization are used as a conductive starter coating prior to electrolytic copper plating and are applied to the hole wall. The coating should be of sufficient quality for subsequent metallic deposition and **shall** be non-migrating. This process is typically fabricator dependent and is not specified on the master drawing.

**4.4.3 Electrolytic Copper Plating** Electrolytic copper can be deposited from several different electrolytes, including copper fluoroborate, copper cyanide, copper sulfate, and copper pyrophosphate. Copper sulfate and copper pyrophosphate are the most commonly used electrolytes for building the copper deposition on the surface and through the holes to the required thickness. This type of plating usually produces the final copper thickness requirement

**4.4.4 Gold Plating** A variety of gold platings are available for depositions on printed boards. These may be electrolytic, electroless, or immersion deposits. The electrolytic deposition may come in 24k soft gold, 23+k hard gold (hardening uses trace amounts of cobalt, nickel, or iron which are co-deposited with the gold), or the plating may be a lower karat alloy (14k-20k) for some applications. Gold plating serves several purposes:

1. To act as a self lubricating and tarnish resistant contact for edge board connectors (see Table 4-3). Hard electrolytic gold plating is most often used for this application.

2. To prevent oxidation of an underlying plating such as nickel and electroless nickel to enhance solderability and extend storage life. Electrolytic, immersion and electroless gold are most often used for this purpose (see Table 4-3 for thickness).

3. To provide a wire bonding surface. This application employs a soft 24k electrolytic gold, see Table 4-3 for thickness.

**Table 4-3   Final Finish, Surface Plating Coating Requirements***

| Finish | Class 1 | Class 2 | Class 3 |
|---|---|---|---|
| Gold (min) for edge-board connectors and areas not to be soldered | 0.8 µm | 0.8 µm | 1.3 µm |
| Gold (max) on areas to be soldered | 0.8 µm | 0.8 µm | 0.8 µm |
| Gold (min) on areas to be wire bonded (ultrasonic) | 0.05 µm | 0.05 µm | 0.15 µm |
| Gold (min) on areas to be wire bonded (thermosonic) | 0.3 µm | 0.3 µm | 0.8 µm |
| Nickel (min) for edgeboard connectors | 2.0 µm | 2.5 µm | 2.5 µm |
| Nickel (min) barrier to prevent formation of copper-tin compounds** | 1.0 µm | 1.3 µm | 1.3 µm |
| Electroless Nickel | 2.5 - 5.0 µm | | |
| Immersion Gold | 0.08 - 0.23 µm | | |
| Unfused tin-lead (min) | 8.0 µm | 8.0 µm | 8.0 µm |
| Fused tin-lead or Solder Coat | Coverage and solderable | Coverage and solderable | Coverage and solderable |
| Solder Coat over Bare Copper | Coverage and solderable | Coverage and solderable | Coverage and solderable |
| Organic Solderability Preservative | Solderable | Solderable | Solderable |
| Bare Copper | None | None | None |
| **Surface and Holes** | | | |
| Copper* (Avg. minimum) | 20 µm | 20 µm | 25 µm |
| Min. thin areas*** | 18 µm | 18 µm | 20 µm |
| **Blind Vias** | | | |
| Copper (Avg. minimum) | 20 µm | 20 µm | 25 µm |
| Min. thin area | 18 µm | 18 µm | 20 µm |
| **Buried Vias** | | | |
| Copper (Avg. minimum) | 13 µm | 15 µm | 15 µm |
| Min. thin area | 11 µm | 13 µm | 13 µm |

*Copper plating thickness applies to surfaces and hole walls.

**Nickel platings used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.

***For Class 3 boards having a drilled hole diameter <0.35 mm and having an aspect ratio >3.5:1, the minimum thin area copper plating in the hole **shall** be 25 µm

4. To provide an electrically conductive surface on printed wiring boards when electrically conductive adhesives are used. A minimum thickness of 0.25 µm is recommended.

5. To act as an etch resist during printed board fabrication. A minimum thickness of 0.13 µm is recommended.

Electrolytically deposited gold is often specified as required to meet MIL-G-45204 with the type and grade selected to satisfy the different applications. A low-stress nickel or electroless nickel **shall** be used between the gold overplating and the basis metal when gold finish is to be used for electrical or wire bonding.

Table 4-4 will help clarify some of the uses for the various alloys.

**Table 4-4   Gold Plating Uses**

| Minimum Purity | Knoop Hardness | Contacts | Wire Bonding | Soldering |
|---|---|---|---|---|
| 99.0 | 130-200 | S | C* | C** |
| 99.0 | 90 max | NR | S | C** |

S - Suitable use     NR - Not recommended     C - Conditional use

* May be used, but will depend on type of wire bonding being used. Run Test prior to wire bonding.

** More than 0.8 µm gold on boards or leads may cause embrittled solder joints.

**4.4.5 Nickel Plating**   Nickel plating serves a dual function in contact plating: 1) It provides an anvil effect under the gold providing an essential extra hardness to the gold; 2) It is an effective barrier layer (when its thickness exceeds 2.5 µm) which prevents the diffusion of copper into gold. This diffusion process can result in a room temperature alloying of the gold, degrading the electrical and corrosion resistance characteristics of the contact.

All electrolytically deposited nickel plating **shall** be low-stress and conform to QQ-N-290, Class 2, except that the thickness **shall** be as specified in Table 4-3.

**4.4.6 Tin/Lead Plating** Tin/Lead Plating is applied in the subtractive fabrication process to provide a copper etch resist and a solderable coating, when required. Typical thickness sufficient for etch resist on 2 oz. copper is 8.0 μm, but it is a fabrication process parameter, not a design requirement. The electrodeposit is generally fused by one of several techniques (hot oil immersion, infrared exposure, exposure to hot vapors or inert liquids). The fusing operation results in the formation of a true alloy on the surface and in the through holes of the printed board. Fusing is required unless the unfused option is selected to maintain flatness. It also promotes improved long-term solderability.

Tin lead plating does not apply to buried plated-through holes which are internal to the printed board and do not extend to the surface.

Tin-lead plating **shall** meet the composition requirements of ASTM-B-579.

**4.4.6.1 Tin Plating** Tin Plating is applied in the subtractive fabrication process to provide a copper etch resist.

**4.4.7 Solder Coating** Solder coating is generally applied by immersing the printed board into molten solder and removing the excess by blowing hot, pressurized air, oil or vapors over the surface of the printed board in a specially designed machine.

Solder coating does not apply to buried or tented plated-through holes which are internal to the printed board and do not extend to the surface.

Unless otherwise specified on the master drawing, the solder used for solder coating **shall** be in accordance with J-STD-006. Solder coating thickness may be specified for particular applications. The performance of solder coating is evaluated, not by a mechanical thickness measurement, but by the ability of the printed board to pass solderability testing per J-STD-003 (see Table 4-3). The user has the responsibility to determine if steam aging, prior to solderability testing, is required.

**4.4.8 Other Metallic Coatings for Edgeboard Contacts** In addition to the coatings cited previously, there are several other options that the designer may want to consider:

• Rhodium - a low resistance contact coating for flush circuits, switches or where a high number of insertions is expected. Expense has precluded its general use.

• Tin/Nickel Alloy- an abrasion resistant coating.

• Palladium/Nickel Alloy- a low resistance contact coating. May be particularly useful for flush circuits.

• Electroless Nickel and Immersion Gold- a low resistance contact coating suitable for low number of insertions.

**4.4.9 Metallic Foil/Film**

**4.4.9.1 Copper Foil** There are two types of copper foil available: (W) - wrought (or rolled), and (ED) - electrodeposited. There are also several copper foil grades. For rigid boards, electrodeposited copper foil is generally used. For flexible boards, wrought foil is generally used. Whichever type is used, the copper foil **shall** conform to the requirements of IPC-MF-150.

The thickness of starting copper conductors **shall** be as defined in Table 4-5 for the appropriate class of equipment (a reduction in copper thickness of inner layers may be expected after processing). See Appendix A of IPC-MF-150 for details of foil properties.

**4.4.9.2 Copper Film** Copper film **shall** be in accordance with Table 4-5.

**Table 4-5   Copper Foil/Film Requirements[1]**

| Copper Type | Class 1-3 |
|---|---|
| Minimum Starting Copper Foil - external | 1/8 oz/ft$^2$ (5 μm) |
| Minimum Starting[2] Copper Foil - internal | 1/4 oz/ft$^2$ (9 μm) |
| Starting Copper Film (semi-additive) | 5 μm |
| Final Copper Film (fully-additive) | 15-20 μm |

1. All dimensional values are nominal and derived from weight measurements.

2. 1/8 oz/ft$^2$ (5 μm) may be used for buried via applications.

**4.4.9.3 Other Foils/Film** When other foils or films (nickel, aluminum, etc.) are used, their characteristics **shall** be specified on the master drawing.

**4.4.9.4 Metal Core Substrates** Substrates for metal core boards **shall** be in accordance with Table 4-6.

**4.4.10 Electronic Component Materials**

**4.4.10.1 Buried Resistors** Incorporating buried resistance technology is considerably more expensive than standard multilayer board fabrication. This is due to the special material copper foil purchasing, additional imaging and etching, and resistance (ohm) value verification.

One of the main printed board attributes that requires buried resistance technology is the availability of component real estate. Some high-density designs do not permit discrete resistors. In these cases, buried resistors are viable because they are considerably smaller and when buried allow surface mount components or surface circuitry to pass over them.

**Table 4-6 Metal Core Substrates**

| Material | Specification | Alloy |
|---|---|---|
| Aluminum | QQ-A-250 | As specified on master drawing |
| Steel | QQ-S-635 | As specified on master drawing |
| Copper | ASTM B-152<br>IPC-MF-150 | As specified on master drawing |
| Copper-Invar-Copper<br>Copper-Moly-Copper | IPC-CF-152 | As specified on master drawing |
| Other | User defined | As specified on master drawing |

An annular resistor is a polymer resistor that can be formed in the empty annulus or "antipad" which surrounds each via hole which passes through the plane or circuit layer. The annular design allows the resistor to be screened with a minimum number of factors which will affect the final resistor value. The primary use of this type of resistor is to replace pull up or pull down resistors that have an acceptable tolerance of ±10% or greater. This resistor may be produced much less expensively than a surface resistor and does not require any room on the printed board surface. The larger resistor tolerance and limited number of resistor types that can be replaced are the primary design limitations.

**4.4.10.2 Buried Capacitors** Distributed capacitance is a design feature which places the power (VCC - voltage common carrier) and ground plane directly facing and in close proximity to each other. A separation of the two planes by 0.1 mm or less will produce a sandwich that will provide a low inductance, high capacitance connection to the active devices on the printed board. This fast switching, low current bypass is most useful in high speed digital applications in which the desire to remove surface capacitors or EMI are key considerations. In most designs two power/ground sandwiches are used to replace the existing power and ground plane layers presently in the printed board. In many cases the bypass capacitors 0.1 µF and smaller may be removed from the printed board.

**4.5 Organic Protective Coatings**

**4.5.1 Solder Resist (Solder Mask) Coatings** Coatings and markings **shall** be compatible with each other and with all other parts and materials used in the printed board, and the printed board assembly process, including the board preparation/cleaning required prior to their application. IPC-SM-840 assigns determination of this compatibility to the board fabricator and assembler.

The use of solder resist coatings **shall** be in accordance with the requirements of IPC-SM-840. When required, Class 3 boards **shall** use IPC-SM-840, Class H solder resist. When Underwriters Laboratories (UL) requirements are imposed, the coatings used must be approved by UL for use by the printed board manufacturer's process.

When solder resist is used as an electrical insulator the dielectric properties of the coating **shall** be sufficient to maintain electrical integrity. There should be no solder resist in areas of the board that make contact with the board guides.

Solder resist coating adhesion to melting metal surfaces (solder coating, tin/lead plating, etc.) cannot be assured, as boards are subjected to temperatures that cause redistribution of the melting metals. When solder resist coating is required over melting metal surfaces, the maximum recommended conductor width, where the coating completely covers the conductor, **shall** be 1.3 mm.

When conductors of melting metal have a width larger than 1.3 mm, the design of the conductor **shall** provide a relief through the metal to the base laminate substrate. The relief should be at least 6.45 mm$^2$ in size and located on a grid no greater than 6.35 mm. When conductor areas of melting metal are to be left uncovered, the design for all class boards **shall** provide that the solder resist **shall** not overlap the melting metal by more than 1.0 mm.

Design requirements may dictate that via holes are protected from access by processing solutions during soldering, cleaning, etc. When protection is required, the via **shall** be covered (tented) with permanent solder resist, other polymer coverlay material (not conformal coating), or filled with an appropriate polymer in order to prevent access by the processing solutions.

Tenting or filling of vias **shall** be accomplished so that the hole is covered or filled from both sides.

When tenting over vias is used, the maximum finished hole diameter of the vias **shall** be 1.0 mm for Class 1 and 2 equipment, and 0.65 mm for Class 3 equipment.

For printed board vias with diameters greater than the maximum, tenting **shall** be agreed to between board user and supplier.

**4.5.1.1 Resist Adhesion and Coverage** Adhesion between solder resist and laminate and between solder resist and foil **shall** be complete for the total stipulated coverage area. Oxide treatment, double-treated copper, protective chemical treatment, or other adhesion promoter may be used. The use of an adhesion promoter may need user approval.

When circuit designs include unrelieved copper areas greater than 625 mm$^2$, the use of a resist adhesion promoter is advisable.

When polymer coatings are required over non-melting metals, such as copper, the design should provide that conductors not covered by the resist **shall** be protected from oxidation, unless otherwise specified.

**4.5.1.2 Resist Clearance** Liquid screened coatings require greater clearances (typically 0.4 - 0.5 mm) than photoimageable resists (typically 0 - 0.13 mm). Clear areas may have to be provided for assembly fiducials.

Data files usually will contain clearances equal to the land. This will allow the board fabricators to adjust the clearance to meet his process capabilities while meeting minimum design clearance requirements specified on the master drawing.

Solder resist-to-land relationship **shall** meet the registration requirements stated on the master drawing.

**4.5.2 Conformal Coatings** When required, conformal coatings **shall** meet the requirements of IPC-CC-830 and **shall** be specified on the master drawing or master assembly drawing. When UL requirements are imposed, the coatings **shall** be approved by UL for use by the printed board manufacturer. The designer should be cognizant of compatability issues. Conformal coating is an electrical insulation material which conforms to the shape of the circuit board and its components. It is applied for the purpose of improving surface dielectric properties and protecting against the effects in a severe environment. Conformal coatings are not required on surfaces or in areas that have no electrical conductors. Conformal coatings, are not normally required on circuit board edges. Conformal coatings are, at best, a vapor permeable barrier.

**4.5.2.1 Conformal Coating Types and Thickness** Conformal coating may be any one of the types indicated. The thickness of the conformal coating **shall** be as follows for the type specified, when measured on a flat unencumbered surface:

| | |
|---|---|
| Type AR - Acrylic Resin | 0.03-0.13 mm |
| Type ER - Epoxy Resin | 0.03-0.13 mm |
| Type UR - Urethane Resin | 0.03-0.13 mm |
| Type SR - Silicone Resin | 0.05-0.21 mm |
| Type XY - Paraxylylene Resin | 0.01-0.05 mm |

There are three primary chemical categories in use for conformal coating materials: silicone elastomers, organics, and parylene. All three types provide various levels of protection from solvents, moisture, corrosion, arcing, and other environmental factors that can jeopardize are circuits operation performance (see Table 4-7). Many surface mount technologies cannot perform adequately without the use of a conformal coating due to the tight spacing of leads and land traces.

Conformal coatings may be used in greater thicknesses as shock and vibration dampening agents. This type of application brings with it the risk of mechanical stress to glass and ceramic sealed parts during cold temperature excursions, which may require the use of buffer materials. Heavy build up of conformal coatings under DIPs may also result in mechanical stress of soldered connections during thermal cycling, unless precautions are taken.

**4.5.3 Tarnish Protective Coatings** Protective coatings may be applied to bare copper on the unassembled board in order to maintain solderability or appearance for extended periods. These coatings may be dispersed during the soldering operation or may require a separate removal process prior to the soldering operation. The coating requirement **shall** be designated on the master drawing.

**4.5.3.1 Organic Solderability Protective Coatings** OSP coatings are specifically used to protect the unplated copper lands during storage or dual soldering operations for surface mount components. OSP coatings are useful where flatness is required on surface mount lands. The OSP coating must meet solderability requirements. No specific thickness is required, but resistance to tarnishing and retention of solderability after thermal or environmental exposures is required. When OSP coatings are used, solderability retention, their use and storage life requirement criteria **shall** be documented.

**4.6 Marking and Legends** When specified on the master drawings, boards and assemblies **shall** be marked by appropriate non-conductive inks, labels, etched characters, or other methods. Marking should be used to provide reference designators, part or serial numbers, revision level, orientation or polarization symbols, bar codes, electrostatic discharge (ESD) status, etc.

The marking locations should be such to avoid placing information under components, in hidden locations after assembly or installation, or on conductive surfaces. Marking should not be placed on surfaces covered with melting metals or opaque coatings. Etched markings may effect electrical characteristics such as capacitance.

Whenever practical, fixed format information such as part number, revision level, layer number, and orientation symbols should be incorporated on the artwork master and be considered during printed board layout. Coupons should include this same information. Variable format information, such as serial numbers, fabricator information, date codes, etc., should be placed in an appropriate area utilizing permanent nonconductive, non-nutrient, and high contrast inks, labels, laser scribes, or other means with sufficient durability to survive assembly and cleaning.

Markings **shall** be of sufficient size, clarity, and location to allow legibility during the processing, inspection, storage,

**Table 4-7   Conformal Coating Functionality**

| Type | Advantages | Disadvantages |
|------|-----------|---------------|
| Silicone elastomers | Resistant to extreme temperature cycling. Good intermittent solvent splash resistance. Low modulus, easily removed, flexible. Works well over most solder resists and no clean fluxes. Easily reworked. | Low mechanical abrasion resistance. Half the dielectric strength of organics. Can impair solderability after coating. |
| Organics | High dielectric strength. Excellent mechanical abrasion resistance. Excellent solvent resistance. Excellent moisture resistance. | Can only be used to 125°C. Difficulty of rework varies. Coefficient of thermal expansion needs to be matched. Required compatibility check with solder resist. Required compatibility check with flux chemistry. |
| Parylene | Extremely high dielectric strength. Excellent conformability around parts. Excellent penetration of polymer. Excellent moisture/chemical resistance. | High raw material cost. Applied in a vacuum chamber (batch process). Masking seals must be air-tight. Thin film leakage difficult to visually detect. |

installation, and field repair of a board or assembly. Usually, a minimum character height of 1.5 mm with a line width of 0.3 mm is adequate.

Every attempt should be made to provide enough space for the marking and it is recommended that space be reserved when component placement is determined per 8.1. Avoid the use of marking inks in close proximity to surfaces that must be solderable as the resin systems used in these inks may impair solderability.

Liquid screened markings require clearances that are typically 0.4 - 0.5 mm from solderable surfaces. Caution should be used when calling for liquid screened markings. Their legibility is affected by high surface irregularities.

ESD or Underwriters Laboratories requirements may include special marking considerations which **shall** become a part of the master drawing.

**4.6.1 ESD Considerations**  Completed circuit card assemblies **shall** be marked in accordance with the assembly drawing with their full identification. Circuit card assemblies which contain electrostatic discharge sensitive devices **shall** be marked in accordance with EIA Standard RS-471.

The marking **shall** be etched or applied by the use of a permanent ink or a permanent label which will withstand assembly processing and visible just prior to removal of the assembly for maintenance. Additional markings, if required, **shall** be specified on the assembly drawing.

**5.0 MECHANICAL/PHYSICAL PROPERTIES**

**5.1 Fabrication Considerations**  Table 5-1 lists fabrication assumptions and considerations.

**5.1.1 Bare Board Fabrication**  Due to the equipment involved in printed board fabrication, there are certain limits that should be taken into account in order to maximize manufacturability and, thereby, minimize costs. Also

human factors, such as strength, reach and control, preclude the use of full-size panels in most printed board manufacturing facilities.

**5.2 Product/Board Configuration**  The physical parameters of the printed board should be consistent with the mechanical requirements of the electronic system. Tolerances, as defined in Sections 3 and 5, should be optimized to provide the best fit between the board size, shape, and thickness and mechanical hardware used to mount the product.

**5.2.1 Board Type**  The decision for board type (single-sided, double-sided, multilayer, metal core, etc.) should be made prior to starting layout procedures and be based on assembly performance requirements, heat dissipation, mechanical rigidity requirements, electrical performance (shielding, impedance matching, etc.) and anticipated circuit density (see 3.6.2).

**5.2.2 Board Size**  Boards should be of uniform size whenever possible to facilitate bare board and assembly test fixturing, and minimize the number of fixtures required. An example of board standardization is shown in Figure 5-1. The board size should also be compatible with standard manufacturing panel sizes in order to achieve lowest cost and maximum number of boards per panel. This will also help facilitate bare board testing (see IPC-D-322).

**5.2.3 Board Geometries (Size and Shape)**

**5.2.3.1 Material Size**  The largest size for a printed board fabrication panel is a function of the economic use of sheet laminate common to the marketplace (see IPC-D-322).

The use of a panel size smaller than the largest sub-multiple of the full-size sheet is recommended. One common panel size is 460 mm x 610 mm. Secondary standard panel sizes should be sub-multiples of the full-size sheet.

It is recommended that the designer be aware of the printed board manufacturer's process panel size in order to optimize the board-to-panel yield, and cost relationships. The

**Table 5-1  Fabrication Considerations**

| Fabrication Design Assumptions | Benefits(★), Drawbacks(⇓), Impacts of Not Following Assumptions(⊗), Other Comments(✎) |
|---|---|
| **Hole/Land Ratio:** Land size at least 0.6 mm greater than the hole size | ★Provides sufficient land area to prevent breakout, i.e., hole intersecting edge of land (insufficient annular ring) <br> ⇓ Large lands may interfere with minimum spacing |
| **Teardrop at Connection of Run with Land** | ★Provides additional area to prevent breakout. <br> ★May improve reliability by preventing cracking at land/run boundary in vibration or thermal cycling. <br> ⇓ May interfere with minimum space requirements |
| **Board Thickness:** 0.8 mm to 2.4 mm typical (over copper) | ⊗Thinner boards tend to warp & require extra handling with through-hole technology components. Thicker boards have lower yield because of layer to layer registration. Some components may not have long enough leads for thicker boards. |
| **Board Thickness to Plated Hole Diameter:** Ratios ≤ 5:1 are preferred | ★Smaller ratios result in more uniform plating in hole, easier cleaning of holes and less drill wander. <br> ★Larger holes are less susceptible to barrel cracking. |
| **Symmetry across Board Thickness:** top half should be a mirror image of bottom half to achieve a balanced construction | ⊗Asymmetrical boards tend to warp. <br> ✎The location of ground/power planes, the orientation of signal runs and the direction of the fabric weave affect board symmetry. |
| **Board Size** | ★Smaller boards warp less and have better layer to layer registration. <br> ⇓ Foil lamination or floating layer lay-ups should be considered for large panels with small features <br> ✎Panel utilization determines cost. |
| **Conductor Spacing:** ≤ 0.1 mm | ⊗Etchant fluid does not circulate efficiently in narrower spaces resulting in incomplete metal removal. |
| **Circuit Feature (Conductor Width):** ≤ 0.1 mm | ⊗Smaller features are more susceptible to breakage and damage during etching. |

use of the larger panel sizes is typically the most effective from a labor cost per unit area of end-product board processed. However, the use of large panels may pose difficulties in achieving fine lines and feature positional accuracy due to an increase in base material movement.

**5.2.4 Bow and Twist**  Proper board design, with respect to balanced circuitry construction distribution and component placement, is important to minimize the degree of bow and twist of the printed board. Additionally, the cross-sectional layout, which includes core thicknesses, dielectric thicknesses, inner layer planes, and individual copper layer thicknesses, should be kept as symmetrical as possible about the center of the board.

Unless otherwise specified on the master drawing, the maximum bow and twist **shall** be 0.75% for boards that use surface mount components and 1.5% for all other board technologies. Panels that contain multiple printed boards to be assembled on the panel and later separated **shall** also meet these bow and twist requirements.

If symmetrical construction and tighter tolerances are not sufficient to meet critical assembly or performance requirements, stiffeners or other support hardware may be necessary.

Values are measured per IPC-TM-650, Method 2.4.22.

**5.2.5 Structural Strength**  The wide variety of materials and resins available places a serious analytical responsibility on the designer when structural properties are impor-

tant. The structural properties of laminates are influenced by environmental conditions that vary with the lay-up and composition of the base materials. Physical and electrical properties vary widely over temperature and loading ranges. The ultimate properties of printed board materials are of marginal use to the designer trying to employ the printed board as a structural member. The concern to meet electrical performance requirements, which are impacted by deformation and elongation of the printed board, should consider lower values of ultimate material strength than those listed in the technical literature for determining structural needs.

**5.2.6 Composite (Constraining-core) Boards**  When structural, thermal, or electrical requirements dictate the use of a constraining-core board, the physical performance properties **shall** be evaluated using similar conformance specimen to those designed for standard rigid boards. The coupons for the constraining-core board **shall** include the core material.

Whether for thermal or constraining characteristics, the board configuration may be symmetrical or asymmetrical. There are some advantages in an asymmetrical design in that the electrical properties or functions are separated from the mechanical or heat dissipation functions (see Figure 5-2).

The drawback of the asymmetrical design is that due to the differences of the coefficient of thermal expansion of the printed board and the core material, the completed board

| Board No. | Printed Board Size ± 0.4 |
|---|---|
| A1 | 60 x 80 |
| A2 | 60 x 170 |
| A3 | 60 x 260 |
| A4 | 60 x 350 |
| B1 | 120 x 80 |
| B2 | 120 x 170 |
| B3 | 120 x 260 |
| B4 | 120 350 |
| C1 | 180 x 80 |
| C2 | 180 x 170 |
| C3 | 180 x 260 |
| C4 | 180 x 350 |
| D1 | 240 x 80 |
| D2 | 240 x 170 |
| D3 | 240 x 260 |
| D4 | 240 x 350    [Not recommended for Best Panel Utilization] |

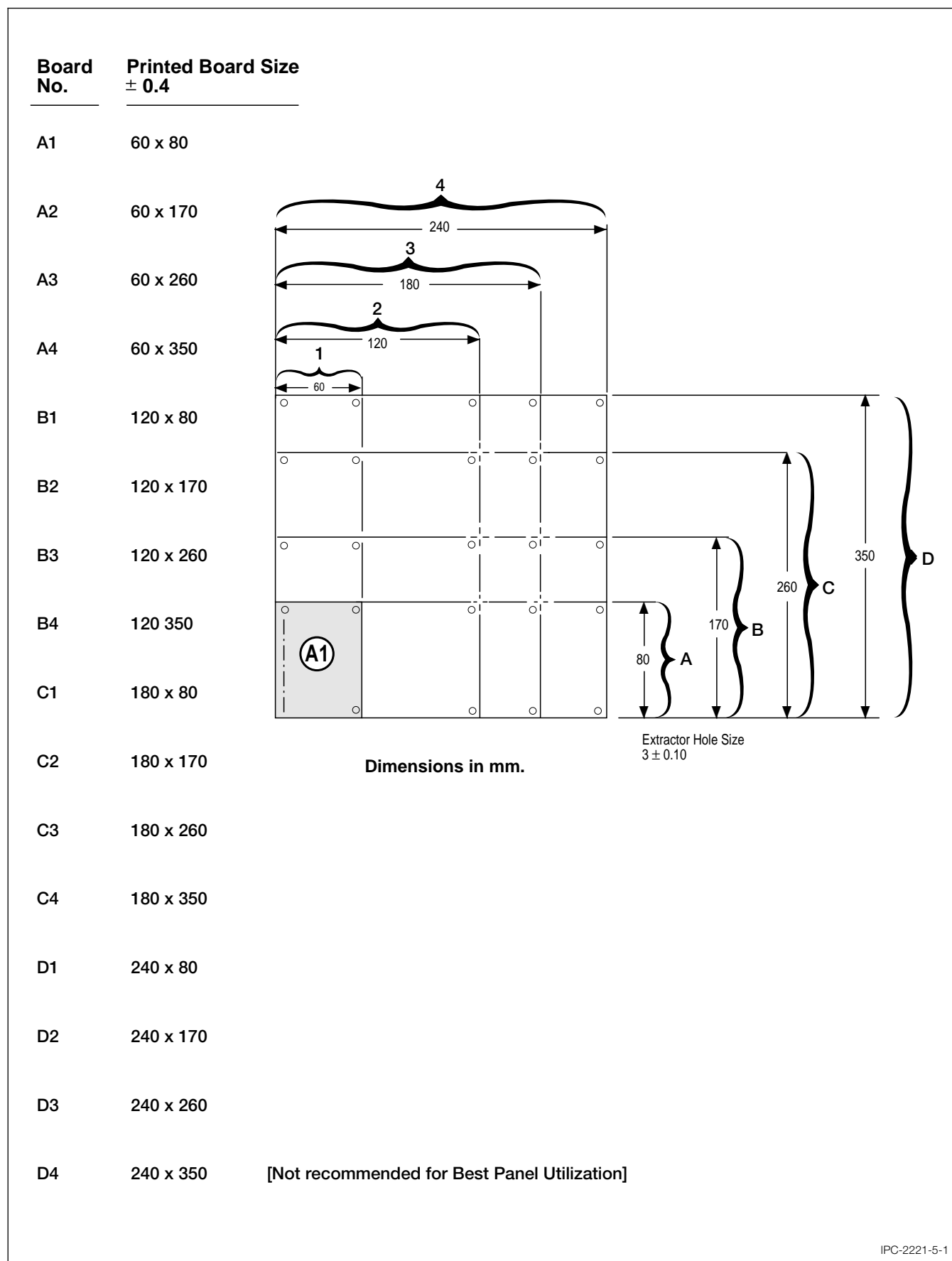Dimensions in mm.

Extractor Hole Size
3 ± 0.10

IPC-2221-5-1

**Figure 5-1    Example of printed board size standardization, mm**
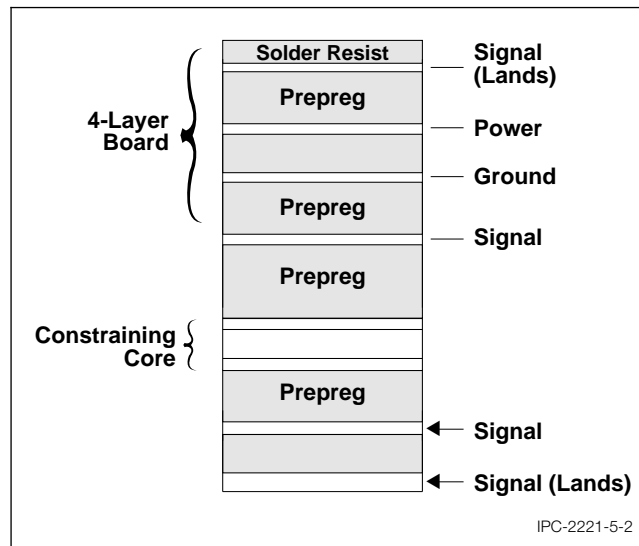
**Figure 5-2   Typical asymmetrical constraining-core configuration**



**Figure 5-3A  Multilayer Metal Core Board with Two Symmetrical Copper-Invar-Copper Constraining Cores (when the Copper-Invar-Copper planes are connected to the plated-through hole, use thermal relief per Figure 9-4)**



**Figure 5-3B   Symmetrical Constraining Core Board with a Copper-Invar-Copper Center Core**

may distort during assembly soldering/reflow operations or while in system use due to temperature change. Some compensation can be achieved by having an additional copper plane added to the back of the interconnection product. The extra copper plane increases the expansion coefficient slightly, but a positive effect is that it enhances thermal conductivity.

A more desirable construction may be that of the symmetrical cored board (see Figure 5-3A and 5-3B). Figure 5- 3A shows the two restraining cores laminated into the multilayer board where they serve as part of the electrical function, in this case, power and ground. The center core construction as shown in Figure 5-3B has a single thicker restraining core which usually has only the thermal plane and restraining function. To achieve restraint in the usable range, the combined thickness of the copper-Invar-copper in the multilayer board should be approximately 25% of the board thickness. The two-restraining-core board is more often used because the core layers may be imaged, etched and connected to the plated through hole; the thicker center core must be machined. Better thermal cycle survival is exhibited by the two-restraining-core board.

A special constraining-core board may be made by bonding a multilayer printed board to each side of a thick containing metal core after the boards have been completed. A more complex variation may also be fabricated wherein the constraining metal core is laminated between two partially completed multilayer printed boards. The composite board is then sequentially drilled, plated and etched to form plated-through hole connections between the two boards. Coupons should be provided to test the integrity of the composite structure.

Metal core boards add significantly to the thermal mass of the assembly. This may force the preheating and soldering
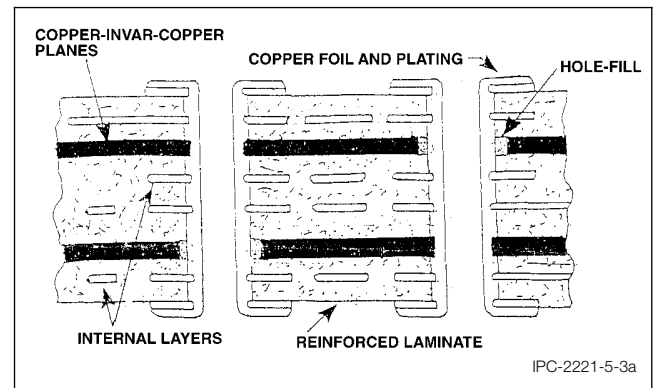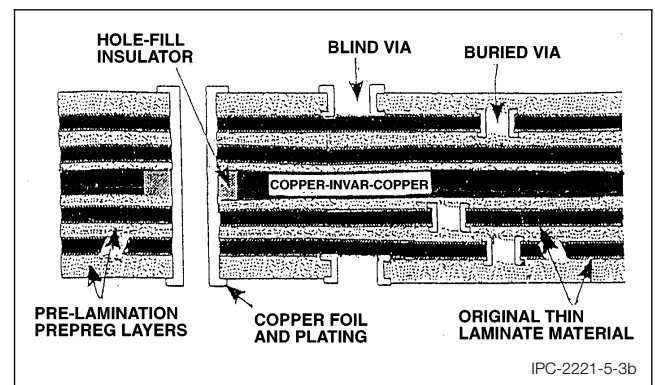
process to be operated at abnormally high limits. These designs should be thoroughly evaluated under production conditions prior to release. Laminate ruptures and discoloration and grainy or textured solder are typical effects that have been observed.

**5.2.7 Vibration Design**   The design of printed boards that will be subjected to vibration while in service requires that special consideration be given to the board prior to board layout. The effect on the board assembly caused by the vibration can seriously reduce the reliability of the assembly. The interrelationship between the unit, printed board assemblies, their mounting and the environmental conditions make necessary the need for a vibration analysis of the complete system very early in the design. The effect from vibration on any item within a unit can make the vibration analysis very complex.

Vibration analysis should be done on each piece of electronic hardware which contains printed board assemblies. The complexity of the analysis should depend on the vibration level to which the hardware will be subjected in service. The design of the printed boards will depend on the

level of vibration transmitted to the board. Particular attention should be given to printed boards subjected to random vibration.

The following criteria should be used as guidelines for determining if the level of vibration to which the boards will be subjected is a level which would require complex vibration analysis of the board:

- The random spectral density is at, or above, $0.1G^2/Hz$ in the frequency range of 80 to 500 hertz or an unsupported board distance of greater than 76.2 mm.

- A sinusoidal vibration level at, or above, 3 Gs at a frequency of 80 to 500 Hz.

- The board assembly will be subjected to Reliability Development Growth Testing (RDGT) at a spectral density at, or above, $0.07\ G^2/Hz$ for more than 100 hours in conjunction with temperature cycling.

The following guidelines should be observed during the design of printed boards to eliminate vibration induced failures of the printed board assemblies:

- The board deflection, from vibration, should be kept below 0.08 mm per mm of board length (or width) to avoid lead failure on multiple lead devices.

- Positive support of all components with a weight of more than 5.0 gm per lead should be considered when the board will be subjected to vibration (see 5.3.2).

- Board stiffeners and/or metal cores should be considered to reduce the board deflection.

- Cushioned mounting of relays should be considered for their usage in high level vibration environments.

- Vibration isolators should be considered for mounting of units whenever practical.

- The mounting height of freestanding components should be kept to a minimum.

- Non-axial leaded components should be side-mounted.

Because of the interrelationship of the many components that makeup a system, the use of the above guidelines does not ensure the success of a unit subjected to a vibration test. A vibration test of a unit is the only way to ensure that a unit will be reliable in service.

### 5.3 Assembly Requirements

**5.3.1 Mechanical Hardware Attachment**  The printed board **shall** be designed in such a manner that mechanical hardware can be easily attached, either prior to the main component mounting effort, or subsequently. Sufficient physical and electrical clearance should be provided for all mechanical hardware that requires electrical isolation. In general, mounting hardware should protrude no more than 6.4 mm below the board surface to allow sufficient clearances for assembly equipment and solder nozzles.

**5.3.2 Part Support**  All parts weighing 5.0 gm, or more, per lead **shall** be supported by specified means (see 8.1.12), which will help ensure that their soldered joints and leads are not relied upon for mechanical strength.

The reliability of printed boards that will be subject to shock and vibration in service require consideration of the following criteria:

- The worst-case levels of shock and vibration environment for the entire structure in which the printed board assembly resides, and the ultimate level of this environment that is actually transmitted to the components on the board. (Particular attention should be given to equipment that will be subjected to random vibration.)

- The method of mounting the board in the equipment to reduce the effects of the shock and vibration environment, specifically the number of board mounting supports, their interval, and their complexity.

- The attention given to the mechanical design of the board, specifically its size, shape, type of material, material thickness, and the degree of resistance to bowing and flexing that the design provides.

- The shape, mass and location of the components mounted on the board.

- The component lead wire stress relief design as provided by its package, lead spacing, lead bending, or a combination of these, plus the addition of restraining devices.

- The attention paid to workmanship during board assembly, so as to ensure that component leads are properly bent, not nicked, and that the components are installed in a manner that tends to minimize component movement.

- Conformal coating may also be used to reduce the effect of shock and vibration on the board assembly (see 4.5.2).

Where circuit design permits, the selection of components to be mounted on boards subjected to severe shock and vibration should favor the use of components that are lightweight, have low profiles and inherent strain-relief provisions. Where discrete components must be used, preference should be given to surface mount and/or axially-leaded types that present a relatively low profile that can be mounted and easily clamped or bonded in intimate contact with the board surface.

The use of irregularly-shaped components, especially those having a large mass and a high center of gravity, should be avoided where practical. If their use cannot be avoided, they should be located toward the outer perimeter of the board, or where hardware or mounting reduces flexing. Depending on the severity of this problem, the use of mechanical clamping, adhesive bonding, or embedding may be required.

**5.3.3 Assembly and Test**  Consideration, similar to that mentioned above for printed board fabrication, must be

given to printed board assembly and test equipment utilization in order to improve manufacturing yields and to minimize end-product costs. Table 5-2 provides limits associated with the use of typical printed board assembly equipment.

**Table 5-2　Normal Assembly Equipment Limits**

| Operation | Typical Maximum Part Size |
|---|---|
| Auto Insertion | 450 x 450 mm |
| Wave Solder | 400 mm x open |
| In-Circuit Test* | 400 x 400 mm |

* Maximum size also determined by the number of electrical nodes to be tested.

## 5.4 Dimensioning Systems

**5.4.1 Dimensions and Tolerances** Historically, printed board designs have used bilateral tolerances for size and position, which is acceptable per IPC-2615 with some restriction in regard to datum references; however, the use of geometric dimensioning and tolerancing (GDT) has many advantages over size and bilateral tolerancing:

- It allows at least 57% more tolerance area with true positioning than with bilateral tolerancing (see Figure 5-4).

- It provides for maximum producibility while assuring the mechanical function of the printed board. It allows "bonus" or extra tolerances when the maximum/least material concept is used.

- It ensures that design requirements, as they relate to actual function, are specifically stated and carried out, especially when automated assembly techniques are to be used.

- It ensures interchangeability of mating parts.

- It provides uniformity and convenience in drawing delineation and interpretation, thus reducing controversy and guesswork.

For these reasons, the use of geometric dimensioning and tolerancing is encouraged.

**5.4.2 Component and Feature Location** Grid systems are used to locate components, plated-through holes, conductor patterns, and other features of the printed board and its assembly so they need not be individually dimensioned. When printed board features are required to be off a grid, they **shall** be individually dimensioned and toleranced on the master drawing.

The use of electronic media precludes the necessity for individual component dimensioning.

Grid systems are always basic and have no tolerance, and therefore all features located on a grid **shall** be toleranced elsewhere on the master drawing. Grid systems **shall** be located with respect to a minimum of two printed board datums.



**Bilateral Tolerance Zone**

The shaded square represents the tolerance zone of a hole with a positioned tolerance of 0.13 ± .

**Positional Tolerance Zone**

By using the positional tolerance shown in Detail A, a 0.18 diameter tolerance zone is established. The tolerance zone is increased 57%.

**Bonus Tolerance Based on Maximum Material Concept**

By modifying the positional tolerance to apply at maximum material condition, as shown in detail B, the tolerance zone increases as the measured hole size deviates from its minimum size (maximum material condition). In this example, the tolerance zone can increase to 0.25.
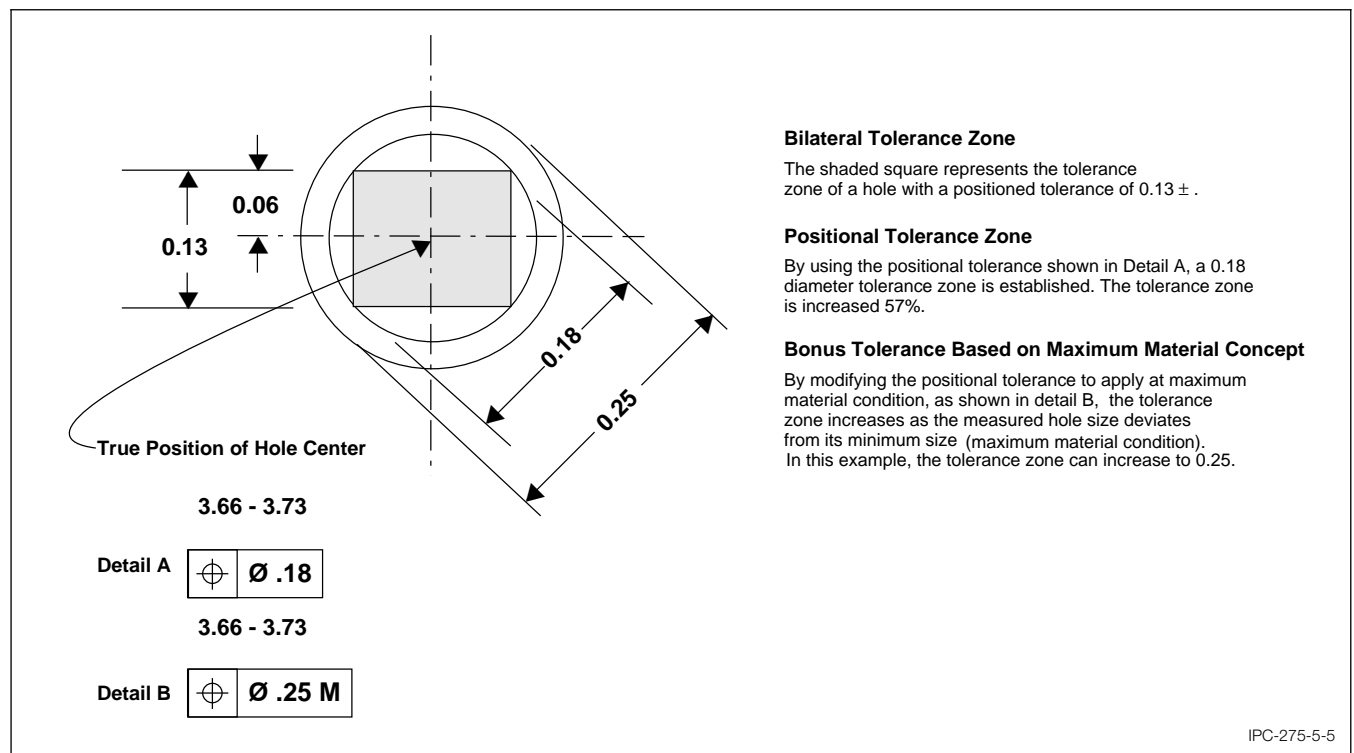
IPC-275-5-5

**Figure 5-4　Advantages of positional tolerance over bilateral tolerance, mm**

The selected grid increment or the use of electronic media **shall** be specified on the master drawing. The component terminal location for through-hole components or the component center location for surface mount components is established by either the selected grid increment or the electronic media.

Typical grid increments are multiples of 0.5 mm for through-hole components, and 0.05 mm for surface mount components.

**5.4.3 Datum Features** Datum features indicate the origin of a dimensional relationship between a toleranced feature and a designated feature or features on the printed board. Datum features are chosen to position the printed board in relation to a set of three mutually perpendicular planes (see Figure 5-5, A-E).

There are some cases where a single datum reference is sufficient, for example a printed board profile or a datum hole position.

Typically, printed board drawings are oriented with the primary (component) side or the designated Layer 1 facing up. This orientation establishes the backside of the printed board as the first (primary ("A")) of the three required datum planes.

The other two datum planes (secondary ("B") and tertiary ("C")) are typically established at minimum material conditions using holes and/or etched features on the printed board.

The choice of features to be used for datums depends on what design elements are intended to be controlled. Board edge or feature edge datums should not be used primarily because their use may not represent the function of the printed board. They also pose producibility problems to the fabricator. Coordinate zero should be located at the secondary datum feature. Datum features **shall** be specified on the master drawing by means of datum symbols per IPC-2615. The use of implied datums is not allowed. Datum features **shall** be functional features of the printed board, and should relate to mating parts such as mounting holes, connectors, or component leads or terminations. All datum features should be located on grid or establish the grid criterion, and they **shall** be located within the printed board profile.

To maximize the total available tolerance, a good practice is to separately locate and tolerance as patterns those printed board features that are produced in separate fabrication operations. Applicable patterns are as follows:

A. *Plated Through-Hole Patterns* The plated through-hole pattern (see Figure 5-5A) is generally the first drilling operation and is the first operation that defines the printed board. It is dimensioned as a basic grid with each hole toleranced to a basic grid intersection. The hole location tolerance is specified either in the hole list or by drawing note. A minimum of two holes on the grid **shall** be dimensioned and toleranced and **shall** establish the primary datum reference frame.

B. *Unplated Through Hole Patterns* Unplated through-hole patterns, especially tooling and mounting holes (see Figure 5-5B), are generally drilled in a separate drilling operation as one of the last fabrication operations. They **shall** be explicitly dimensioned and toleranced, even if they occur on grid. Two of these holes are typically established as secondary datum features because of their function, in spite of their place in the fabrication sequence.

C. *Conductor Patterns* The conductor pattern does not need a separate datum reference provided a minimum annular ring is specified. Minimum annular ring is a common way to tolerance the conductor pattern location with respect to the plated through-hole pattern. For some designs, particularly where automated assembly is used, this method may allow too much tolerance. In these cases, a feature location tolerance may be required and **shall** appear on the master drawing. Alternately, fiducials may be required to locate and tolerance the conductor pattern with respect to the assembly tooling holes (see Figure 5-5C).

The fiducial size, shape and quantity may depend on the type of equipment used in the assembly process and lead pitch and lead count. Figure 5-6 shows the Surface Mount Equipment Manufacturers Association (SMEMA) recommended fiducial design. Another method to locate and tolerance the conductor pattern is by dimensioning to the centerline of a conductor. A critical area is edge board connector contacts; these should be dimensional as shown in Figure 5-7. This figure establishes a second X datum from which the tang edge is established as well as any keying slot. Tolerances used for edgeboard and keying slots **shall** be such that keying slots do not cut into or damage the contact finger. Dimensioning to the edge of a conductor is not allowed.

Figure 5-5E shows how Figures 5-5A through 5-5D can be assembled into one drawing.

D. *Printed Board Profile* The printed board profile, including cutouts and notches (see Figures 5-5D and 5-7), requires a minimum of one datum reference. The use of three datum references and maximum material condition modifiers, as shown in Figure 5-5D, maximizes allowable tolerances and allows the use of hard tool gauging, which is particularly useful in high volume production situations.
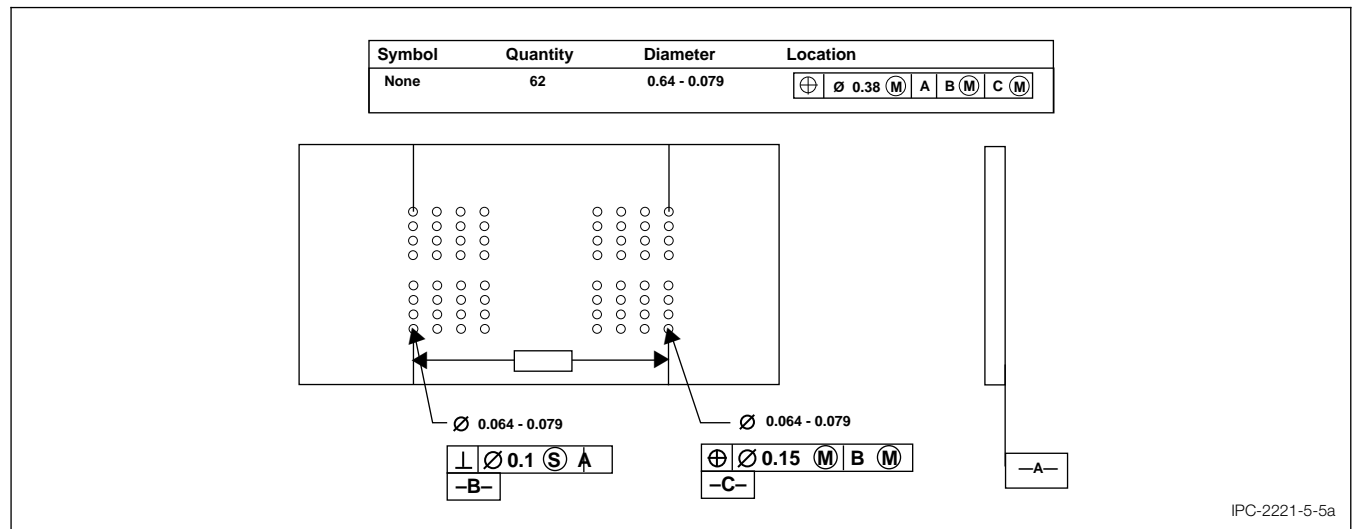
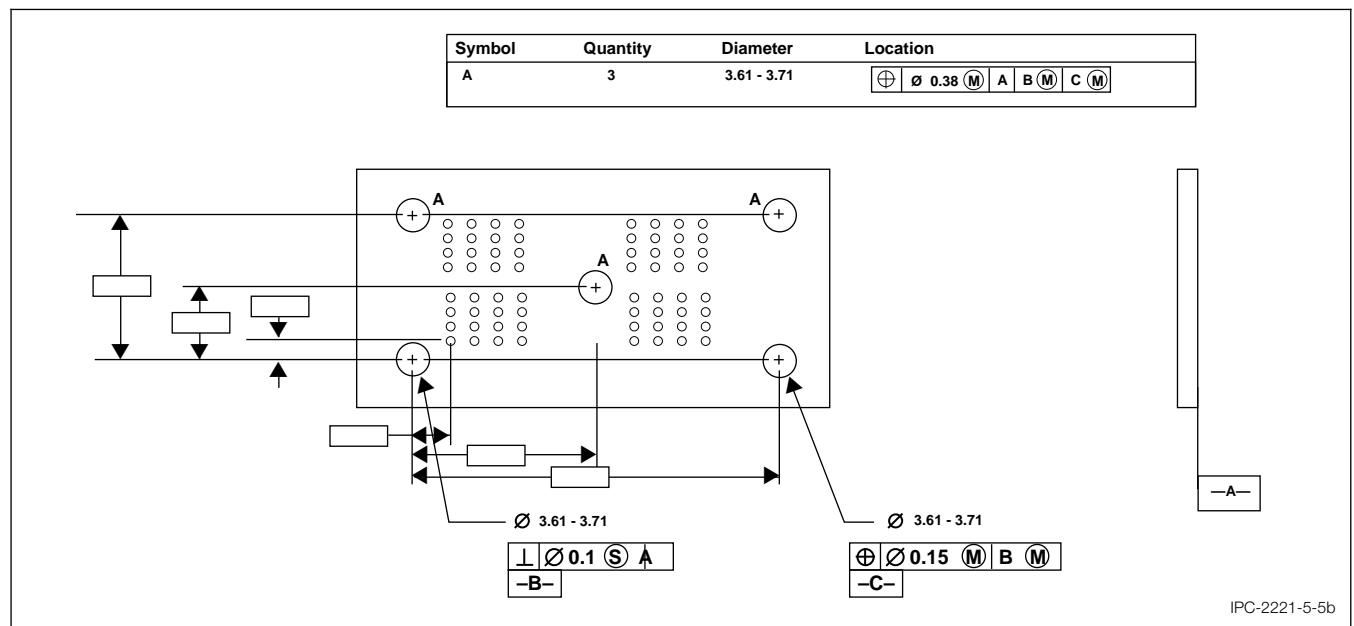**Figure 5-5A  Example of location of a pattern of plated-through holes, mm**



**Figure 5-5B   Example of a pattern of tooling/mounting holes, mm**

*E. Solder Resist Coatings*  The solder resist coating pattern may be located by specifying a minimum land clearance, or targets may be provided which serve the same function as fiducials for conductor patterns (see Figure 5-6). A minimum land clearance serves the same purpose as a minimum annular ring requirement in that it tolerances the solder resist pattern location with respect to the conductor pattern.

**5.4.3.1 Datum Feature for Palletization**  Palletization of parts is a standard process for both test and assembly. A datum system is required for the pallet, as well as each individual board in the pallet. To reduce tolerance buildup, it is important to relate each individual board datum to the panel datum. See Figure 5-7.

**6.0  ELECTRICAL PROPERTIES**

**6.1 Electrical Considerations**

**6.1.1 Electrical Performance**  When printed-board assemblies are to be conformal coated, they **shall** be constructed, adequately masked, or otherwise protected in such a manner that application of the conformal coating does not degrade the electrical performance of the assembly. High speed circuit designs should consider the recommendations of IPC-D-317.

**6.1.2 Power Distribution Considerations**  A predominately important factor that should be considered in the design of a printed board is power distribution. The grounding scheme can be used as a part of the distribution
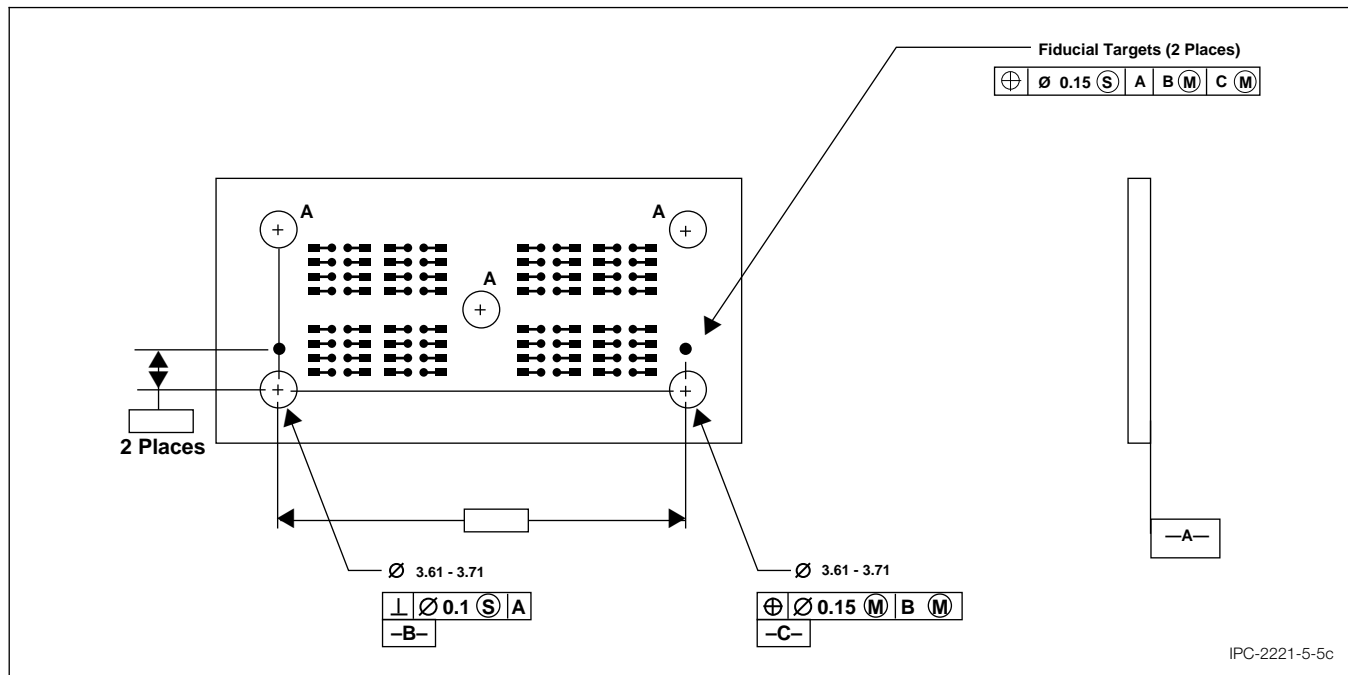
**Figure 5-5C   Example of location of a conductor pattern using fiducials, mm**
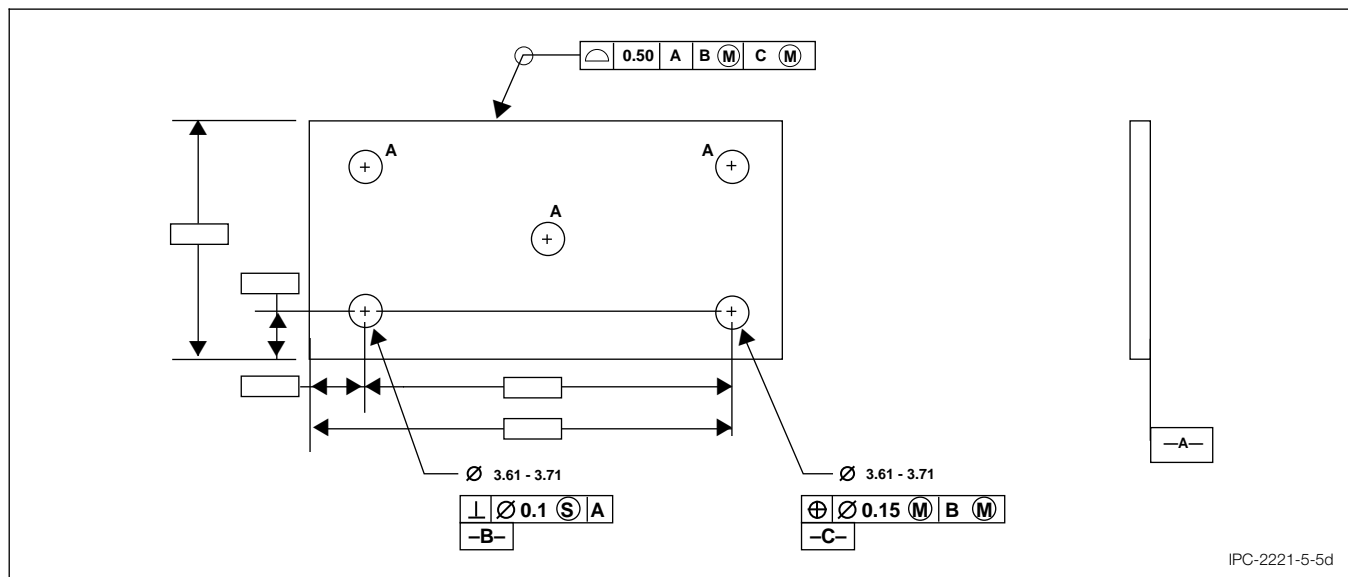


**Figure 5-5D   Example of printed board profile location and tolerance, mm**

system. It provides not only a DC power return, but also an AC reference plane for high-speed signals to be referenced. The following items should be taken into consideration.

Maintain a lower radio-frequency (RF) impedance throughout the DC power distribution. An improperly designed ground can result in RF emissions. This results from radiated field gradients developed across the uneven board impedance and its inability of decoupling capacitors to efficiently reduce the boards EMI.

Decouple the power distribution at the printed board connector using adequate decoupling capacitance. Distribute

adequate individual power/ground decoupling capacitors evenly throughout logic device board areas. Minimize the impedance and radiation loop of the coupling capacitor by keeping capacitor leads as short as possible, and locating them adjacent to the critical circuit.

In a multilayer printed board, planes should be used for power and ground distribution techniques. When utilizing planes for power and ground distribution, it is recommended that the incoming power and ground signals terminate at the input decoupling network, prior to connecting to the respective internal planes. If external power busses are
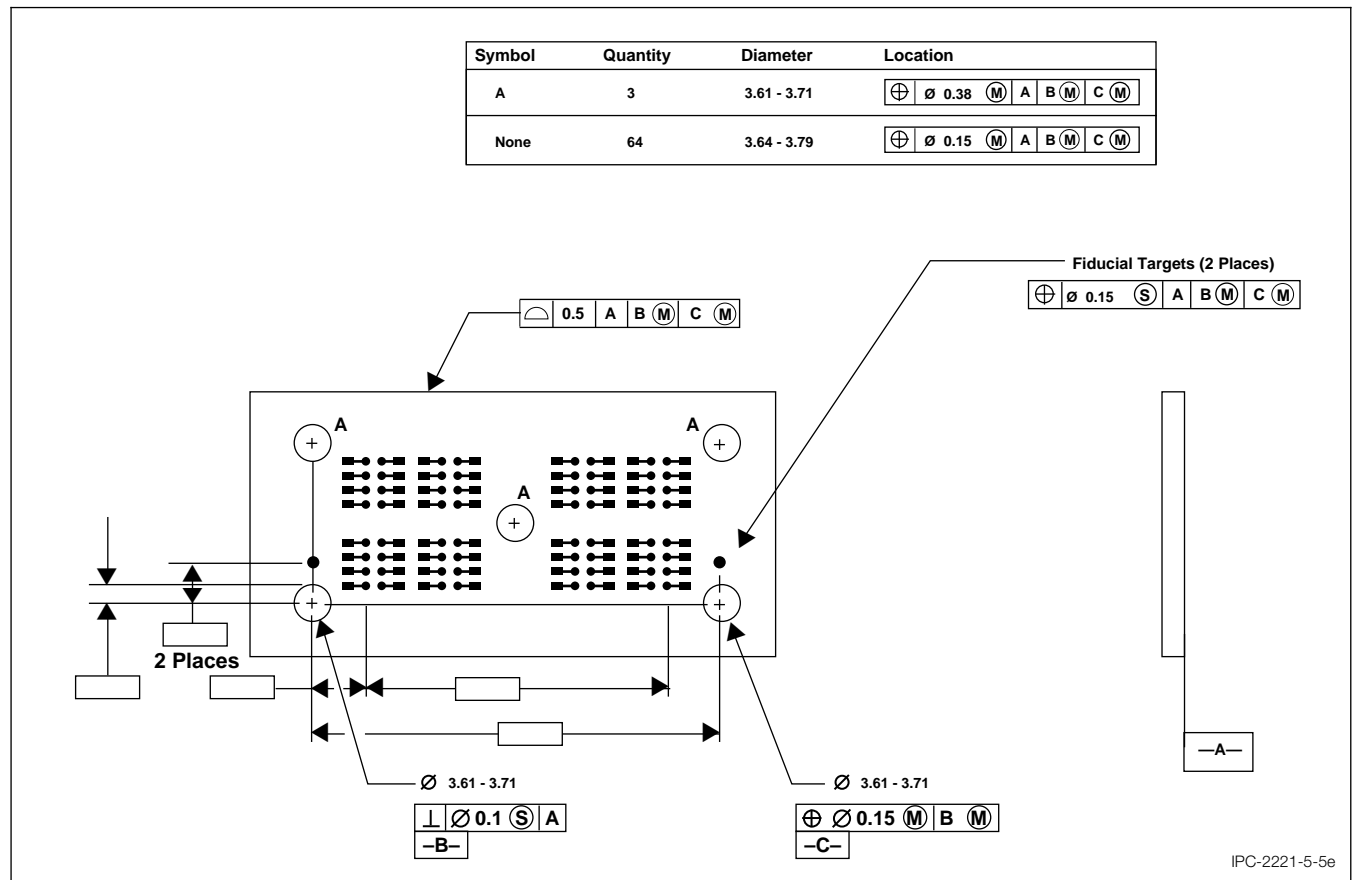
| Symbol | Quantity | Diameter | Location |
|--------|----------|----------|----------|
| A | 3 | 3.61 - 3.71 | ⊕ ⌀ 0.38 Ⓜ A B Ⓜ C Ⓜ |
| None | 64 | 3.64 - 3.79 | ⊕ ⌀ 0.15 Ⓜ A B Ⓜ C Ⓜ |

Fiducial Targets (2 Places)

⊕ ⌀ 0.15 Ⓢ A B Ⓜ C Ⓜ

▱ 0.5 A B Ⓜ C Ⓜ

2 Places

⌀ 3.61 - 3.71

⌀ 3.61 - 3.71

—A—

⊥ ⌀ 0.1 Ⓢ A
—B—

⊕ ⌀ 0.15 Ⓜ B Ⓜ
—C—

IPC-2221-5-5e

**Figure 5-5E    Example of a printed board drawing utilizing geometric dimensioning and tolerancing, mm**

**Clearance**    **Clearance**

R

2R

R
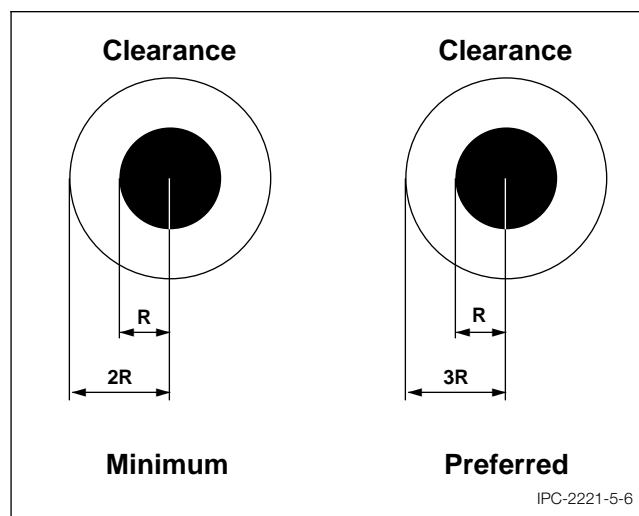
3R

**Minimum**    **Preferred**

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**Figure 5-6    Fiducial clearance requirements**

required, commercially available bussing schemes may be employed as defined in section 8.2.13. When using power conductors, as shown in Figure 6-1, power traces should be run as close as possible to ground traces. Both power and ground traces **shall** be maintained as wide as possible. The power and ground planes virtually become one plane at high frequencies, and should, therefore, be kept next to each other.

Figure 6-1A shows a poor layout, giving high inductance and few adjacent signal return paths; this leads to crosstalk.

Figure 6-1B is a better layout and reduces power distribution, logic-return impedances, conductor crosstalk and board radiation.

The best layout is shown in Figure 6-1C, which has further EMI problem reductions.

In digital power distribution schemes, the grounding and power should be designed first, not last, as is typically done with some analog circuits. All interfacing, including power, should be routed to a single reference edge, or area. Opposing end interconnections are to be avoided. When unavoidable, care should be taken to route the power and ground away from active circuits (see Figure 6-2). At the interconnection reference edge, all ground structures are to be made as heavy as possible.

The shortest possible conductor length should be used between devices. The printed board should be separated into areas for high, medium, and low frequency circuits (see Figure 6-3).

**6.1.3 Circuit Type Considerations**    The following guidelines should be considered when designing printed board assemblies:

PANEL TOOLING HOLE
(3 PLACES)

INDIVIDUAL BOARD TOOLING HOLES
(3 PLACES PER BOARD)

X.XXX

X.XXX

X.XXX

X.XX

DATUM

DATUM

X.XXX

X.XXX

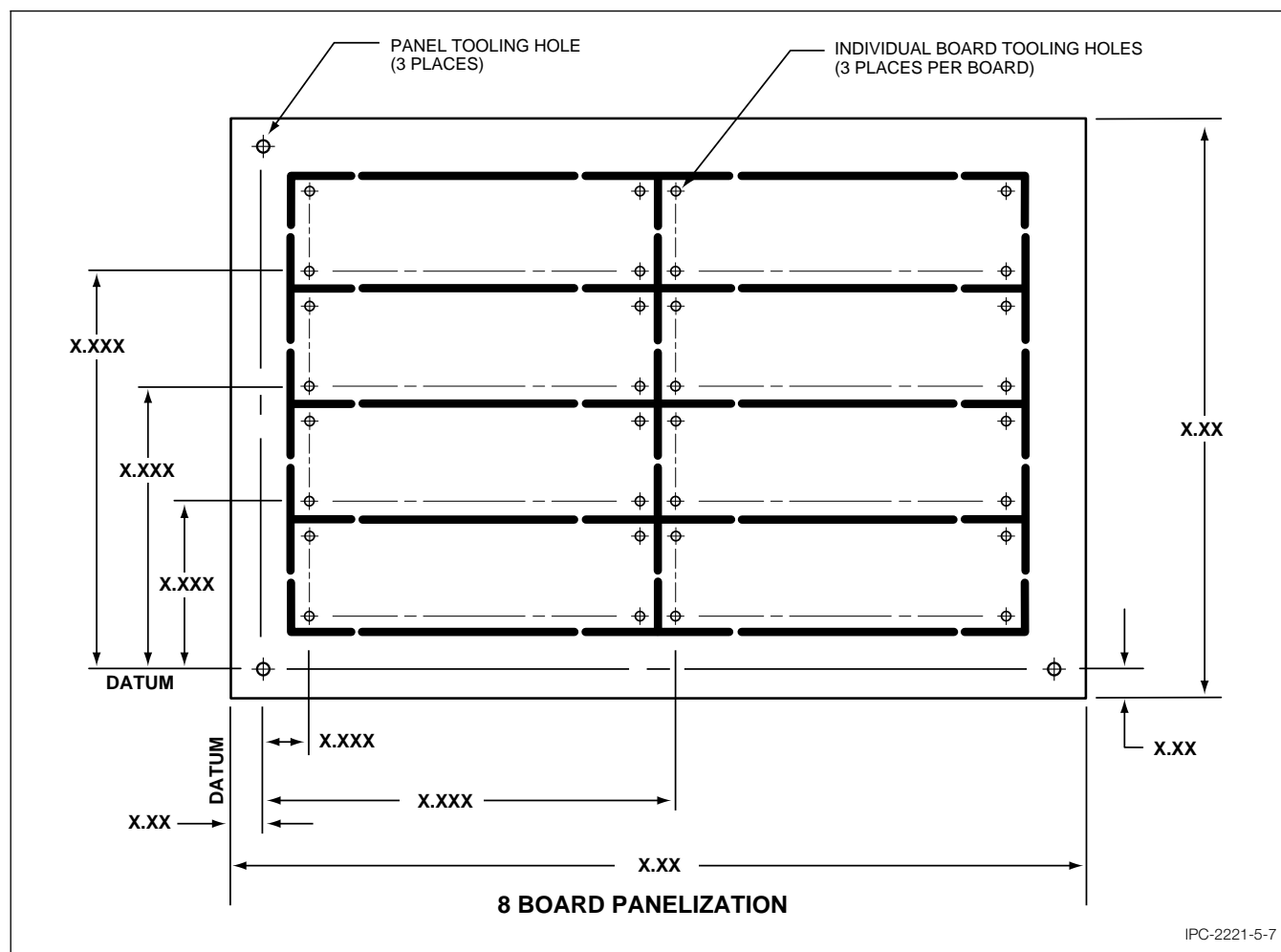X.XX

X.XX

**8 BOARD PANELIZATION**

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**Figure 5-7　Fiducials, mm**

- Always determine correct polarity of the component, where applicable.

- Transistor emitter/base and collector should be properly identified (ground transistor case where applicable).

- Keep lead length as short as possible, and determine capacitive coupling problems between certain components.

- If different grounds are used, keep grounding busses or planes as far away from each other as possible.

- As opposed to digital signals, analog design should have signal conductors considered first, and ground planes or ground conductor connections considered last.

- Keep heat-sensitive and heat-radiating components as far apart as possible (incorporate heatsinks whenever necessary).

**6.1.3.1 Digital Circuits** Digital circuits are composed of electronic components that can provide state information (1 or 0), as a function of the performance of the overall circuit. Normally, logic integrated circuits are used to perform this function; however, discrete components may also be used sometimes to provide digital responses.

Integrated circuit devices use a variety of logic families. Each family has its own parameters regarding the speed of the digital transmission, as well as the temperature rise characteristics necessary to provide the performance. In general, a single board usually uses the same logic family in order to facilitate a single set of design rules for conductor length for signal driving restrictions. Some of the more common logic families are:

TTL - Transistor Transistor Logic
MOS - Metal Oxide Semiconductor Logic
CMOS - Complimentary Metal Oxide Semiconductor
　　　　Logic
ECL - Emitter Coupled Logic
GaAs - Gallium Arsenide Logic

In certain high-speed applications, specific conductor routing rules may apply. A typical example is serial routing between signal source, loads and terminators. Rating branches (stubs) may also have specified criteria.

Digital signals can be roughly placed in four classes of criticality. These classes are:
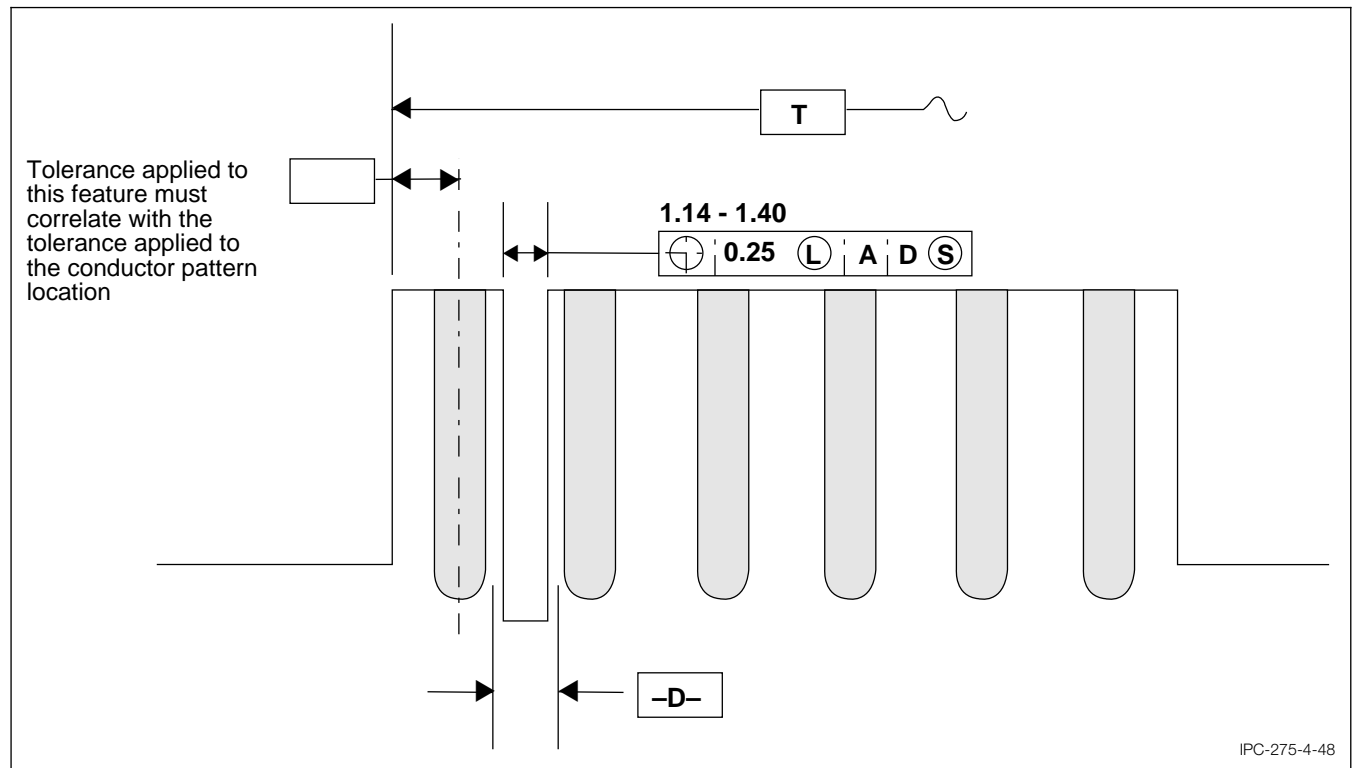
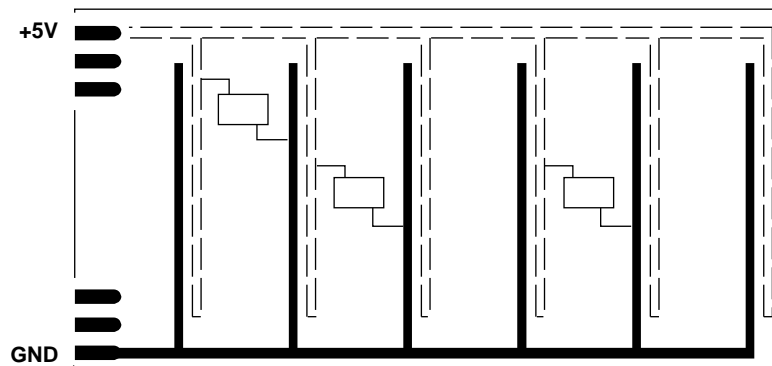**Figure 5-8   Example of connector key slot location and tolerance, mm**

1. *Non-Critical Signals* - are not sensitive to coupling between them. Examples are between the lines of a data bus or between the lines of an address bus where they are sampled long after they are settled.

2. *Semi-Critical Signals* - are those where coupling must be kept low enough to avoid false triggering, such as reset lines and level triggering strobe lines.

3. *Critical Signals* - have waveforms that must be monotonic through the voltage thresholds of the receiving device. These are normally clocking signals and any glitch while the wave form is in transition may cause a double clocking of the circuit. A non-critical signal has a waveform that need not be monotonous and may even make multiple transitions between the voltage thresholds before it settles. Obviously it must settle before the receiving device acts upon the data, e.g., the data input to a flip-flop may be a non-critical but the clock signal is most probably a critical signal. Asynchronous signals, although they may (or may not) be non-critical signals, should not be mixed with critical signals since there is a real possibility of the asynchronous signals inducing noise on the critical signals during the clock transitions. Clock signals that do not have a common master frequency should also not be routed together for similar reasons.

4. *Super-Critical Signals* - are those in applications such as clocks or strobes for A/D and D/A converters, signals in Phase Locked Loops, etc. In these types of applications phase lock jitters and crosstalk, causing errors, noise and timing jitters, will show up in the application's output performance. It is only a question of the amount of disturbance within the required performance specification. This class of signal is essentially the same as an analog coupling situation. In other words, it is completely linear (the total noise is the sum of the individual noise elements; no averaging of canceling out can be assumed).
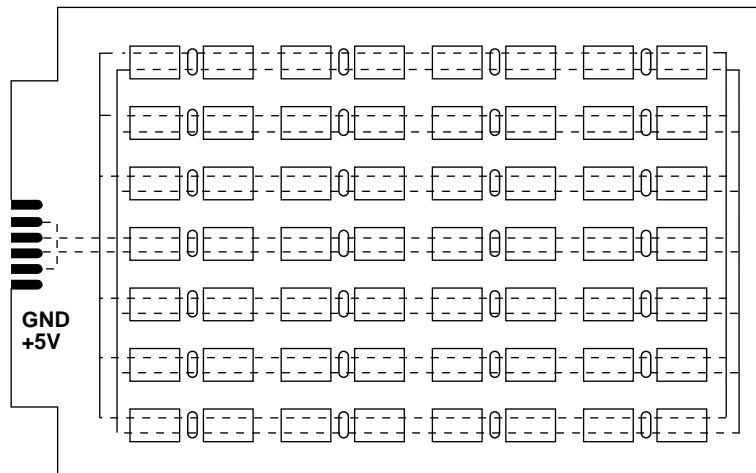
**6.1.3.2 Analog Circuits**   Analog circuits are usually made from integrated circuits and discrete devices.. Standard discrete components (resistors, capacitors, diodes, transistors, etc.), as well as power transformers, relays, coils and chokes, are usually the types of discrete devices used for analog circuits.

**6.2 Conductive Material Requirements**   The minimum width and thickness of conductors on the finished board **shall** be determined primarily on the basis of the current-carrying capacity required, and the maximum permissible conductor temperature rise. The minimum conductor width and thickness **shall** be in accordance with Figure 6-4 for conductors on external and internal layers of the printed board.

The conductor's permissible temperature rise is defined as the difference between the maximum safe operating temperature of the printed board laminate material and maximum temperature of the thermal environment to which the

**+5V**

**GND**

**A. Poor layout**

**B. Acceptable layout**

**GND +5V**

**GND +5VDC**
**GND +5VDC**
**GND +5VDC**
**GND +5VDC**
**GND +5VDC**
**GND +5VDC**
**GND +5VDC**
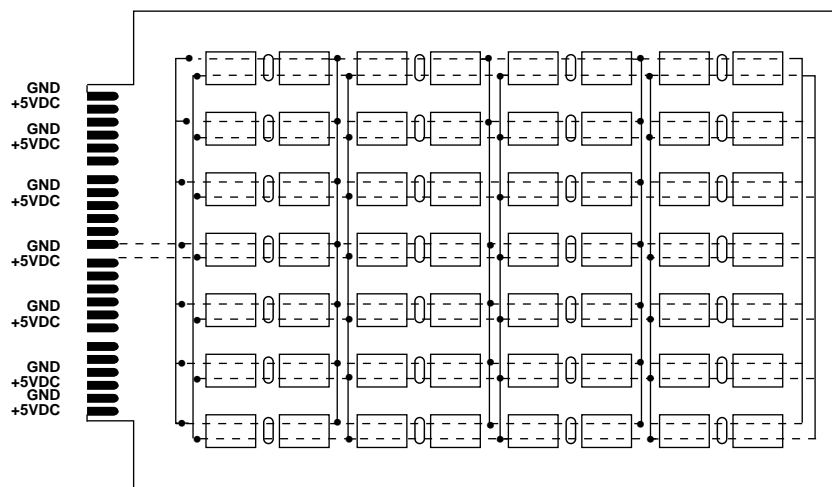
**C. Preferred layout**

☐ = Integrated Circuit

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**Figure 6-1  Voltage/ground distribution concepts**

**Figure 6-2   Single reference edge routing**



**Figure 6-3   Circuit distribution**

printed board will be subjected. For convection-cooled printed board assemblies, the thermal environment is the maximum ambient temperature where the printed board will be used. For conduction-cooled printed board assemblies in a convection environment, the temperature rise is c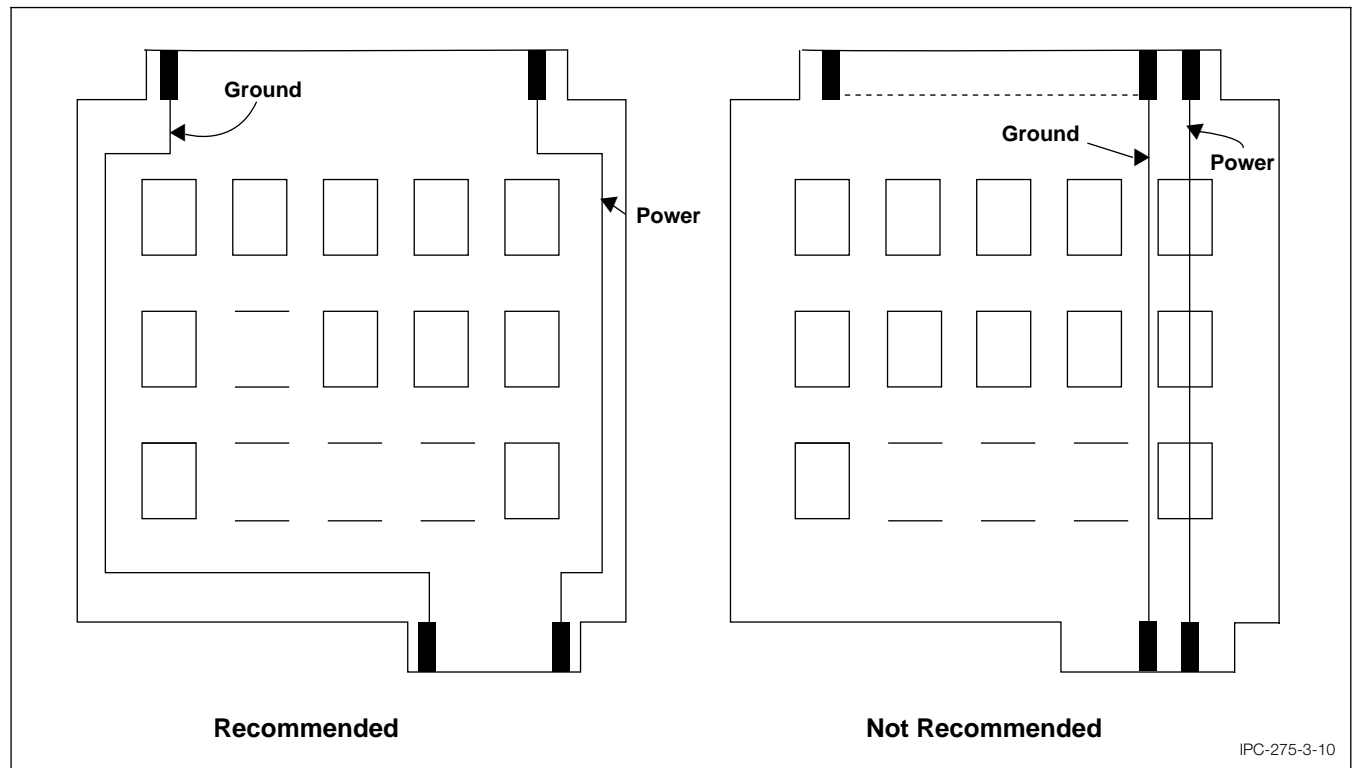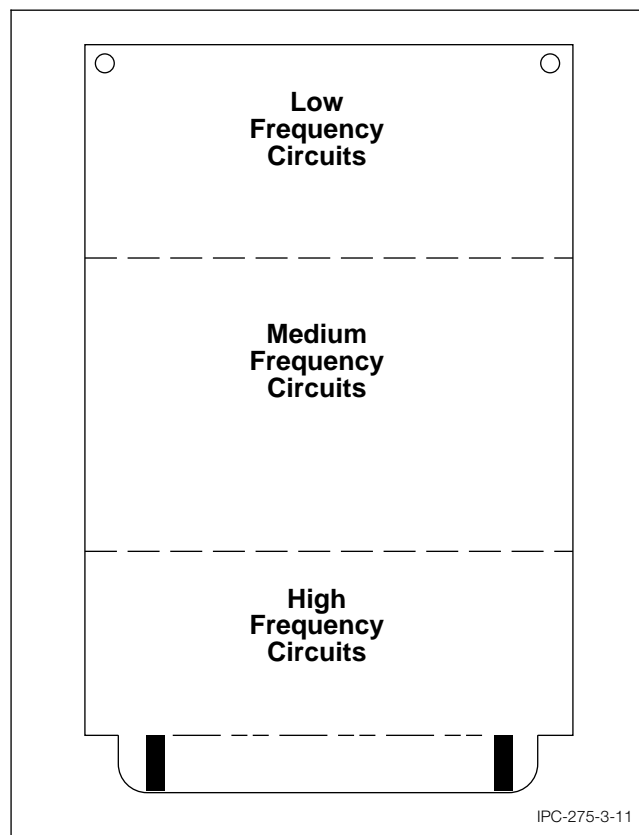aused by the dissipated power of the conduction-cooled parts and the temperature rise through the printed board and/or heatsink to the cold plate should also be considered. For conduction-cooled printed board assemblies in a vacuum environment, the thermal environment is the temperature rise caused by the dissipated power of the parts and the temperature rise through the printed board and/or heatsink to the cold plate. In a vacuum environment, the effects of radiation heat transfer between the parts, the printed board assembly and the cold plate should also be considered.

For internal layers, the conductor thickness is the copper foil thickness of the base laminate unless blind/buried vias are used in which case the copper foil thickness includes copper process plating. For external layers, the conductor thickness also includes the thickness of plated copper deposited during the plated-through hole process, but should not include the thickness of solder coating, tin-lead plating, or secondary platings. It should be noted that the foil thickness specified by the standard drawing noted for the preferred printed board materials are nominal thickness values which can generally vary by as much as ± 10%. For external layers, the total copper thickness will also vary
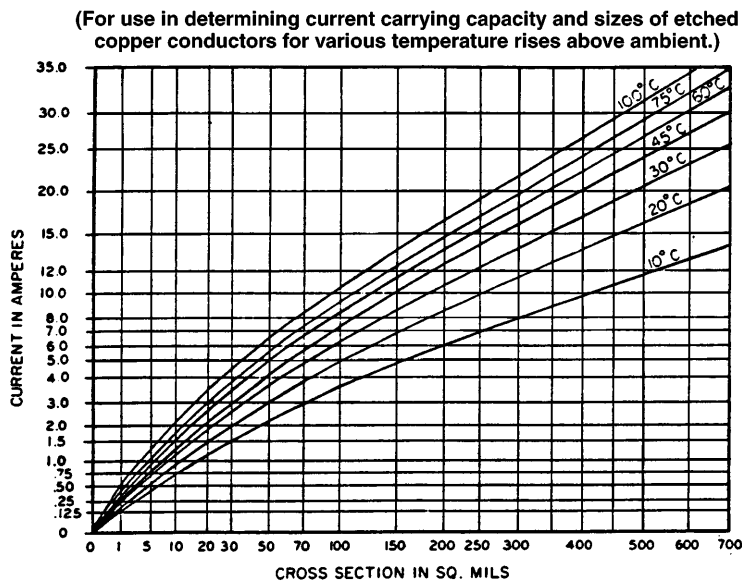
**(For use in determining current carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.)**



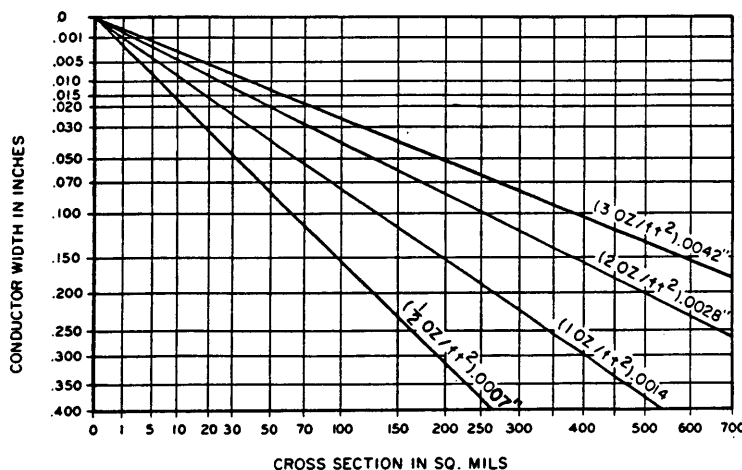**Figure A   External Conductors**



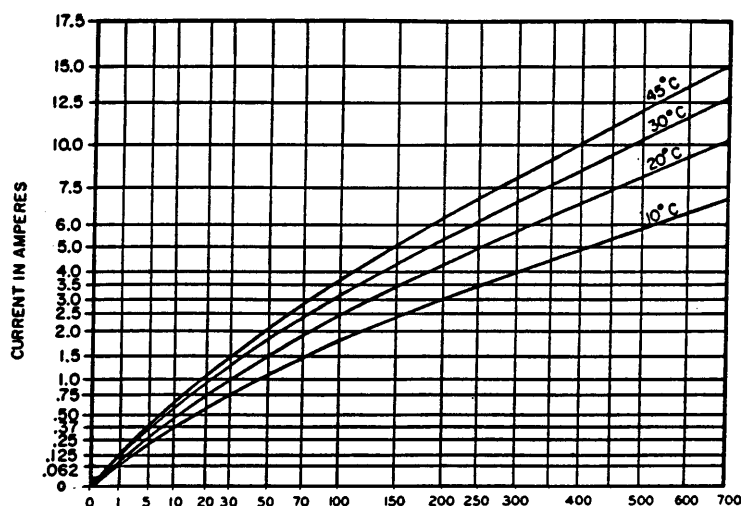**Figure B   Conductor width to cross-section relationship**



**Figure C   Internal Conductors**

Notes:

1. The design chart has been prepared as an aid in estimating temperature rises (above ambient) vs. current for various cross-sectional areas of etched copper conductors. It is assumed that, for normal design, conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves as presented include a nominal 10 percent derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.

2. Additional derating of 15 percent (current-wise) is suggested under the following conditions:

   (a) For panel thickness of 0.8 mm or less

   (b) For conductor thickness of 108 μm or thicker.

3. For general use the permissible temperature rise is defined as the difference between the ambient temperature and the maximum sustained operating temperature of the assembly.

4. For single conductor applications the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.

5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-section of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.

6. The effect of heating due to attachment of power dissipating parts is not included.

7. The conductor thicknesses in the design chart do not include conductor overplating with metals other than copper.

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**Figure 6-4   Conductor thickness and width for internal and external layers**

due to processing prior to plating which may reduce the thickness of base copper. Furthermore, since the thickness of plated copper is controlled by the requirement for the thickness of copper required in the barrel of the plated-through hole, the associated amount of copper on the external layers may not be the same thickness as the plating in the barrels of the plated-through holes (see 10.1.1). Therefore, if conductor thickness is critical, a minimum finished board conductor thickness should be specified on the master drawing.

For ease of manufacture and durability in usage, these parameters should be optimized while maintaining the minimum recommended spacing requirements. To maintain finished conductor widths, as on the master drawing, conductor widths on the production master may require compensation for process allowances as defined in Section 10.

**6.3 Electrical Clearance** Spacing between conductors on individual layers should be maximized whenever possible. The minimum spacing between conductors, between conductive patterns, layer to layer conductive spaces (z=axis), and between conductive materials (such as conductive markings or mounting hardware) and conductors **shall** be in accordance with Table 6-1, and defined on the master drawing. For additional information on process allowances effecting electrical clearance, see Section 10.

When mixed voltages appear on the same board and they require separate electrical testing, the specific areas **shall**

be identified on the master drawing or appropriate test specification. When employing high voltages and especially AC and pulsed voltages greater than 200 volts potential, the dielectric constant and capacitive division effect of the material must be considered in conjunction with the recommended spacing.

For voltages greater than 500V, the (per volt) table values must be added to the 500V values. For example, the electrical spacing for a Type B1 board with 600V is calculated as:

$$600V - 500V = 100V$$
$$0.25 \text{ mm} + (100V \times 0.0025 \text{ mm})$$
$$= 0.50 \text{ mm clearance}$$

When, due to the criticality of the design, the use of other conductor spacings is being considered, the conductor spacing on individual layers (same plane) **shall** be made larger than the minimum spacing required by Table 6-1 whenever possible. Board layout should be planned to allow for the maximum spacing between external layer conductive areas associated with high impedance or high voltage circuits. This will minimize electrical leakage problems resulting from condensed moisture or high humidity. Complete reliance on coatings to maintain high surface resistance between conductors **shall** be avoided.

**6.3.1 B1-Internal Conductors** Internal conductor-to-conductor, and conductor-to-plated-through hole electrical clearance requirements at any elevation. See Table 6-1.

Table 6-1 Electrical Conductor Spacing

| Voltage Between Conductors (DC or AC Peaks) | Minimum Spacing | | | | | | |
| | Bare Board | | | | Assembly | | |
| | B1 | B2 | B3 | B4 | A5 | A6 | A7 |
|---|---|---|---|---|---|---|---|
| 0-15 | 0.05 mm | 0.1 mm | 0.1 mm | 0.05 mm | 0.13 mm | 0.13 mm | 0.13 mm |
| 16-30 | 0.05 mm | 0.1 mm | 0.1 mm | 0.05 mm | 0.13 mm | 0.25 mm | 0.13 mm |
| 31-50 | 0.1 mm | 0.6 mm | 0.6 mm | 0.13 mm | 0.13 mm | 0.4 mm | 0.13 mm |
| 51-100 | 0.1 mm | 0.6 mm | 1.5 mm | 0.13 mm | 0.13 mm | 0.5 mm | 0.13 mm |
| 101-150 | 0.2 mm | 0.6 mm | 3.2 mm | 0.4 mm | 0.4 mm | 0.8 mm | 0.4 mm |
| 151-170 | 0.2 mm | 1.25 mm | 3.2 mm | 0.4 mm | 0.4 mm | 0.8 mm | 0.4 mm |
| 171-250 | 0.2 mm | 1.25 mm | 6.4 mm | 0.4 mm | 0.4 mm | 0.8 mm | 0.4 mm |
| 251-300 | 0.2 mm | 1.25 mm | 12.5 mm | 0.4 mm | 0.4 mm | 0.8 mm | 0.8 mm |
| 301-500 | 0.25 mm | 2.5 mm | 12.5 mm | 0.8 mm | 0.8 mm | 1.5 mm | 0.8 mm |
| > 500 See para. 6.3 for calc. | 0.0025 mm /volt | 0.005 mm /volt | 0.025 mm /volt | 0.00305 mm /volt | 0.00305 mm /volt | 0.00305 mm /volt | 0.00305 mm /volt |

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m
B3 - External Conductors, uncoated, over 3050 m
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated
A7 - External Component lead termination, with conformal coating (any elevation)

**6.3.2 B2-External Conductors, Uncoated, Sea Level to 3050 m**  Electrical clearance requirements for uncoated external conductors are significantly greater than for conductors that will be protected from external contaminants with conformal coating. If the assembled end product is not intended to be conformally coated, the bare board conductor spacing **shall** require the spacing specified in this category for applications from sea level to an elevation of 3050 m. See Table 6-1.

**6.3.3 B3-External Conductors, Uncoated, Over 3050 m**  External conductors on uncoated bare board applications over 3050 m require even greater electrical spacings than those identified in category B2. See Table 6-1.

**6.3.4 B4-External Conductors, with Permanent Polymer Coating (Any Elevation)**  When the final assembled board will not be conformally coated, a permanent polymer coating over the conductors on the bare board will allow for conductor spacings less than that of the uncoated boards defined by category B2 and B3. The assembly electrical clearances of lands and leads that are not conformally coated require the electrical clearance requirements stated in category A6 (see Table 6-1). This configuration is not applicable for any application requiring protection from harsh, humid, contaminated environments.

Typical applications are computers, office equipment, and communication equipment, bare boards operating in controlled environments in which the bare boards have a permanent polymer coating on both sides. After they are assembled and soldered the boards are not conformal coated, leaving the solder joint and soldered land uncoated.

Note: All conductors, except for soldering lands, must be completely coated in order to ensure the electrical clearance requirements in this category for coated conductors.

**6.3.5 A5-External Conductors, with Conformal Coating Over Assembly (Any Elevation)**  Externalconductors that are intended to be conformal coated in the final assembled configuration, for applications at any elevation, will require the electrical clearances specified in this category.

Typical applications are military products where the entire final assembly will be conformal coated. Permanent polymer coatings are not normally used, except for possible use as a solder resist. However, the compatibility of polymer coating and conformal coating must be considered, if used in combination.

**6.3.6 A6-External Component Lead/Termination, Uncoated**  External component leads and terminations, that are not conformal coated, require electrical clearances stated in this category.

Typical applications are as previously stated in category B4. The B4/A6 combination is most commonly used in commercial, non-harsh environment applications in order to obtain the benefit of high conductor density protected with permanent polymer coating (also solder resist), or where the accessibility to components for rework and repair is not required.

**6.3.7 A7-External Component Lead/Termination, with Conformal Coating (Any Elevation)**  As in exposed conductors versus coated conductors on bare board, the electrical clearances used on coated component leads and terminations are less than for uncoated leads and terminations.

**6.4 Impedance Controls**  Multilayer printed boards are ideally suited for providing interconnection wiring that is specifically designed to provide desired levels of impedance and capacitance control. Techniques commonly referred to as "stripline," or "embedded microstrip," are particularly suited for impedance and capacitance requirements. Figure 6-5 shows four of the basic types of transmission line constructions. These are:

A. *Microstrip:* A rectangular trace or conductor placed at the interface between two dissimilar dielectrics (usually air and usually FR-4) whose main current return path (usually a solid copper plane) is on the opposite side of the high-$\varepsilon r$ material. Three sides of the conductor contact the low-$\varepsilon r$ materials ($\varepsilon r = 1$), and one side of the conductor contacts the high-$\varepsilon r$ material ($\varepsilon r > 1$).

B. *Embedded Microstrip:* Similar to Microstrip except that the conductor is completely embedded in the higher-$\varepsilon r$ materials.

C. *Symmetric Stripline:* A rectangular trace or conductor surrounded completely by a homogeneous dielectric medium and located symmetrically between two reference planes.

D. *Dual (Asymmetric) Stripline:* Similar to Stripline except that one or more conductor layers are asymmetrically located between the two reference planes.

The design of such multilayer printed boards should take into consideration the guidelines of IPC-D-317 and IPC-D-330.

**6.4.1 Microstrip**  Flat conductors are the geometry normally found on a printed board as manufactured by the copper plating and etching processes (see Figure 6-5A). The capacitance is influenced most strongly by the region between the signal line and adjacent ground (or power) planes. Inductance is a function of the "loop" formed by the frequency of operation (i.e., skin effect) and the distance to the reference plane for microstrips and striplines, and the length of the conductor.

The following equations give the impedance ($Z_0$) propagation delay ($T_{pd}$), and intrinsic line capacitance ($C_0$) for microstrip circuitry.

$$Z_0 = \frac{87}{\sqrt{\mathcal{E}r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right] \quad \text{in ohms}$$

$$T_{pd} = \frac{\sqrt{\mathcal{E}r}}{c} \qquad \text{in psec/inch}$$

$$C_0 = \frac{T_{pd}}{Z_0} \qquad \text{in pF/inch}$$

$$\text{For } \frac{w}{h} < 1$$

where:

$c$ = Speed of light in vacuum (3.0x108 m/s)
$h$ = Dielectric thickness, inches
$w$ = Line width, inches
$t$ = Line thickness, inches
$\mathcal{E}r$ = Relative permittivity (dielectric constant) of substrate (see Table 6-2)

The radiated electromagnetic interference (EMI) signal from the lines will be a function of the line impedance, the length of the signal line and the incident waveform characteristics. This may be an important consideration in some high speed circuitry. In addition, crosstalk between adjacent circuits will depend directly upon circuit spacing, the distance to the reference planes, length of parallelism between conductors, and signal rise time. (see IPC-D-317).

**6.4.2 Embedded Microstrip** Embedded microstrip has the same conductor geometry as the uncoated microstrip discussed above. However, the effective dielectric constant is different because the conductor is fully enclosed by the dielectric material (see Figure 6-5B). The equations for embedded microstrip lines are the same as in the section on [uncoated] microstrip, with a modified effective dielectric constant. If the dielectric thickness above the conductor is 0.025 mm or more, then the effective dielectric constant can be determined using the criteria in IPC-D-317. For very thin dielectric coatings (less than 0.025 mm), the effective dielectric constant will be between that for air and the bulk dielectric constant (see Table 6-2).

**6.4.3 Stripline Properties** A stripline is a thin, narrow conductor embedded between two AC ground planes (Figure 6-5C). Since all electric and magnetic field lines are contained between the planes, the stripline configuration has the advantage that EMI will be suppressed except for lines near the edges of the printed board. Crosstalk between circuits will also be reduced (compared to the microstrip case) because of the closer electrical coupling of each circuit to ground. Because of the presence of ground planes on both sides of a stripline circuit, the capacitance of the line is increased and the impedance is decreased from the microstrip case.

Stripline impedance ($Z_0$) and intrinsic line capacitance ($C_0$) parameters are presented below for flat-conductor geom-

etries. The equations assume that the circuit layer is placed midway between the planes.

$$Z_0 = \frac{60 \ln\left[\frac{1.9(2H + T)}{(0.8W + T)}\right]}{\sqrt{\mathcal{E}r}} \quad \text{in ohms}$$

$$C_0 = \frac{1.41(\mathcal{E}r)}{\ln\left[\frac{3.81H}{(0.8W + T)}\right]} \qquad \text{in pF/in}$$

$$\text{For } \frac{W}{H} < 2$$

where:

$H$ = Distance between line and one ground plane
$T$ = Line thickness inches
$W$ = Line width inches
$\mathcal{E}r$ = Relative permittivity of substrate
pF = Picofarads

**6.4.4 Asymmetric Stripline Properties** When a layer of circuitry is placed between two ground (or power) layers, but is not centered between them, the stripline equations must be modified. This is to account for the increased coupling between the circuit and the nearest plane, since this is more significant than the weakened coupling to the distant plane. When the circuit is placed approximately in the middle third of the interplane region, the error caused by assuming the circuit to be centered will be quite small.

One example of an unbalanced stackup is the dual stripline configuration. A dual-strip transmission line closely approximates a stripline except that there are two signal planes between the power planes. The circuits on one layer are generally orthogonal to those on the other to keep parallelism and crosstalk between layers to a minimum.

Dual stripline impedance ($Z_0$) and intrinsic line capacitance ($C_0$) parameters are:

$$Z_0 = \frac{80 \ln\left[\frac{1.9(2H + T)}{(0.8W + T)}\right] \cdot \left[1 - \frac{H}{4(H + C + T)}\right]}{\sqrt{\mathcal{E}r}} \quad \text{in ohms}$$

$$C_0 = \frac{2.82(\mathcal{E}r)}{\left[\frac{2H - T}{(0.268W + 0.335T)}\right]} \qquad \text{in pF/in}$$

where:

$H$ = Height above power plane
$C$ = Signal plane separation
$T$ = Line thickness, inches
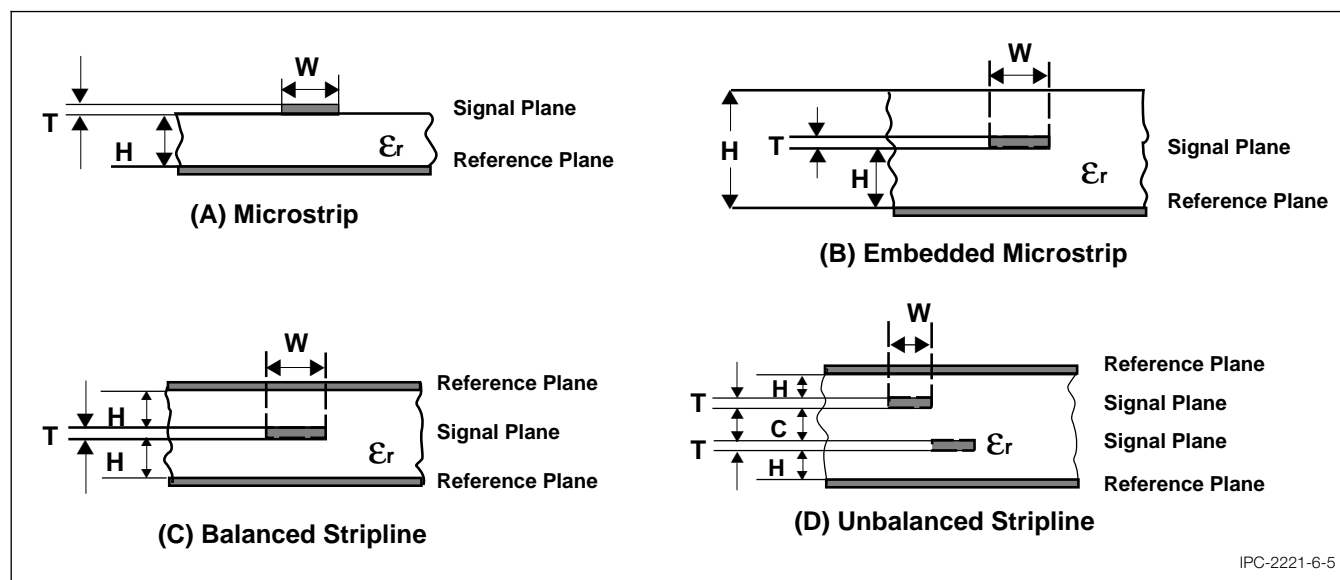$W$ = Line width, inches
pF = Picofarads

**Figure 6-5    Transmission line printed board construction**

**Table 6-2    Typical Relative Bulk Dielectric Constant of Board Materials**

| Designator | | Material Reinforcement/Resin | Dielectric Constant Er |
|---|---|---|---|
| **ANSI** | **MIL-S-13949** | | |
| FR-4 | GF | Woven Glass/Epoxy | 4.2-4.9 |
| FR-5 | GH | Woven Glass/Epoxy | 4.2-4.9 |
| | GP | Non-woven Glass/PTFE | 2.2-2.4 |
| | GR | Non-woven Glass/PTFE | 2.2-2.4 |
| | GT | Woven Glass/PTFE | 2.6-2.8 |
| | GX | Woven Glass/PTFE | 2.4-2.6 |
| GPY | GI | Woven Glass/Polyimide | 4.0-4.7 |
| | GY | Woven Glass/PTFE | 2.1-2.45 |
| | AF | Woven Aramid/Epoxy | 3.8-4.5 |
| | BF | Non-woven Aramid/Epoxy | 3.8-4.5 |
| | AI | Woven Aramid/Polyimide | 3.6-4.4 |
| | BI | Non-woven Aramid/Polyimide | 3.6-4.4 |
| | QI | Woven Quartz/Polyimide | 3.0-3.8 |
| | GFT or GIJ | Woven Glass/BT | 4.0-4.7 |
| | CF | Non-woven Polyester/Epoxy | 3.8-4.9 |
| | GC | Woven Glass/Cyanate Ester | 4.0-4.7 |
| | *P/*T/*R/*X/*Y | Non-supported PTFE | 2.2 |
| | *IN/*IL or *IJ | Non-supported Polyimide | 3.5 |

Values will vary approximately within the range given, depending on the reinforcement/resin ratio.
Generally thin laminates tend toward the lower values.

This stackup is shown in Figure 6-5D. As with stripline, EMI will be completely shielded except for signal lines near the edges of the printed board.

The above equations can be adapted to determine $Z_0$ or $C_0$ for asymmetric stripline circuits that are not dual stripline. Plane sequences for a four-layer board should be as described in Figure 6-5D. For boards with more than four layers, the sequence should be arranged so that the signal layers are symmetrical about the ground or voltage plane. This may be accomplished several ways provided that any adjacent signal layers, not separated by a ground or voltage plane should have their key axes running perpendicular to each other. For 6-layer board, the sequence might be:

| A | | B |
|---|---|---|
| Signal #1 | | Signal #1 |
| Plane #1 | | Signal #2 |
| Signal #2 | or | Plane #1 |
| Signal #3 | | Plane #2 |
| Plane #2 | | Signal #3 |
| Signal #4 | | Signal #4 |

"A" is the desired configuration since the impedance is well matched through the entire stack-up. "B" is a less desirable configuration since signals 1 and 4 will have a much higher impedance than signals 2 and 3.

Special attention is required in the design of specific circuit characteristics where attention must be given to total conductor lengths, both short and long conductor runs, as well as total interconnection routing.

DC power and ground planes also function as AC reference planes. Power and ground connector pins should be evenly distributed along the edge of the board for AC reference.

As a general rule, the reference planes of a multilayer printed board design should not be segmented. Limited plane segmentation, in which the segmented plane is supported by an elevated plane to an adjacent signal layer, and supported by plated-through holes on approximately 2.54 mm centers on both sides, may be used to "bury" a special high frequency signal within the planes to create a "coaxial type" line within the board. Spacing of the holes is dependent on frequency of the signal.

**6.4.5 Capacitance Considerations** Figures 6-6 and 6-7 show the intrinsic line capacitance/per unit length, of copper, for microstrip and stripline, respectively. These charts provide capacitance in pF/ft for 1 oz. copper conductors with various dielectric thicknesses to the ground or power reference plane. Figure 6-7 for stripline is based upon symmetry with the conductor centered between the reference ground and power planes.

The capacitance associated with single crossover (see Figure 6-8) is very small and is typically a fraction of a picofarad. As the number of crossovers per unit length increases, the intrinsic capacitance of the transmission line also increases. The crossover lumped capacitance adds to the intrinsic line capacitance. Crossover capacitance ($C_c$) may be approximated by:

$$C_c = X \varepsilon_r (l + 0.8h) \ \frac{(W + 0.8h)}{h} \ \text{in pF}$$

$$\text{provided that } l \geq 0.5h$$

$$W \geq 0.5h$$

where:

$X$ = 0.0089 if $h$, $l$ and $W$ are in mm, 0.225 if $h$, $l$ and $W$ are in inches
$\varepsilon_r$ = relative permittivity
$h$ = dielectric thickness between crossovers
$l$ = length
$W$ = Width

**6.4.6 Inductance Considerations** Inductance is the property of a conductor that allows it to store energy in a magnetic field induced by a current flowing through that conductor. When this current has high frequency components, the self-inductance of the leads and traces become significant, leading to transient or switching noise. These transients are related to the inductance of a power/ground loop and the circuit must be designed to reduce this inductance as much as possible.

A common technique to reduce this switching noise is the use of decoupling capacitors that serve to provide the current from a point closer to the IC gate than the power supply. Even when these capacitors are designed into the circuit, the positioning of the capacitor is important. If the capacitor leads are too long, the self inductance becomes too high leading to switching noise. Decoupling on the boards is normally achieved with discrete capacitors that can be closely positioned to the IC. In higher I/O packages, a trend has begun which places the decoupling capacitor inside of the package. This has the double advantage of not using real estate for the capacitor location and reducing the size of the capacitor interconnections.

Another consideration is the use of smaller diameter via holes and their associated pad sizes. A change from 0.5 mm vias to 0.3 mm vias will reduce parasitic inductance in the circuit. Smaller diameter vias will improve it even more.

Closely spaced adjacent power and ground planes are also being utilized to provide high frequency decoupling capacitance. This also decreases the real estate required for decoupling capacitors.
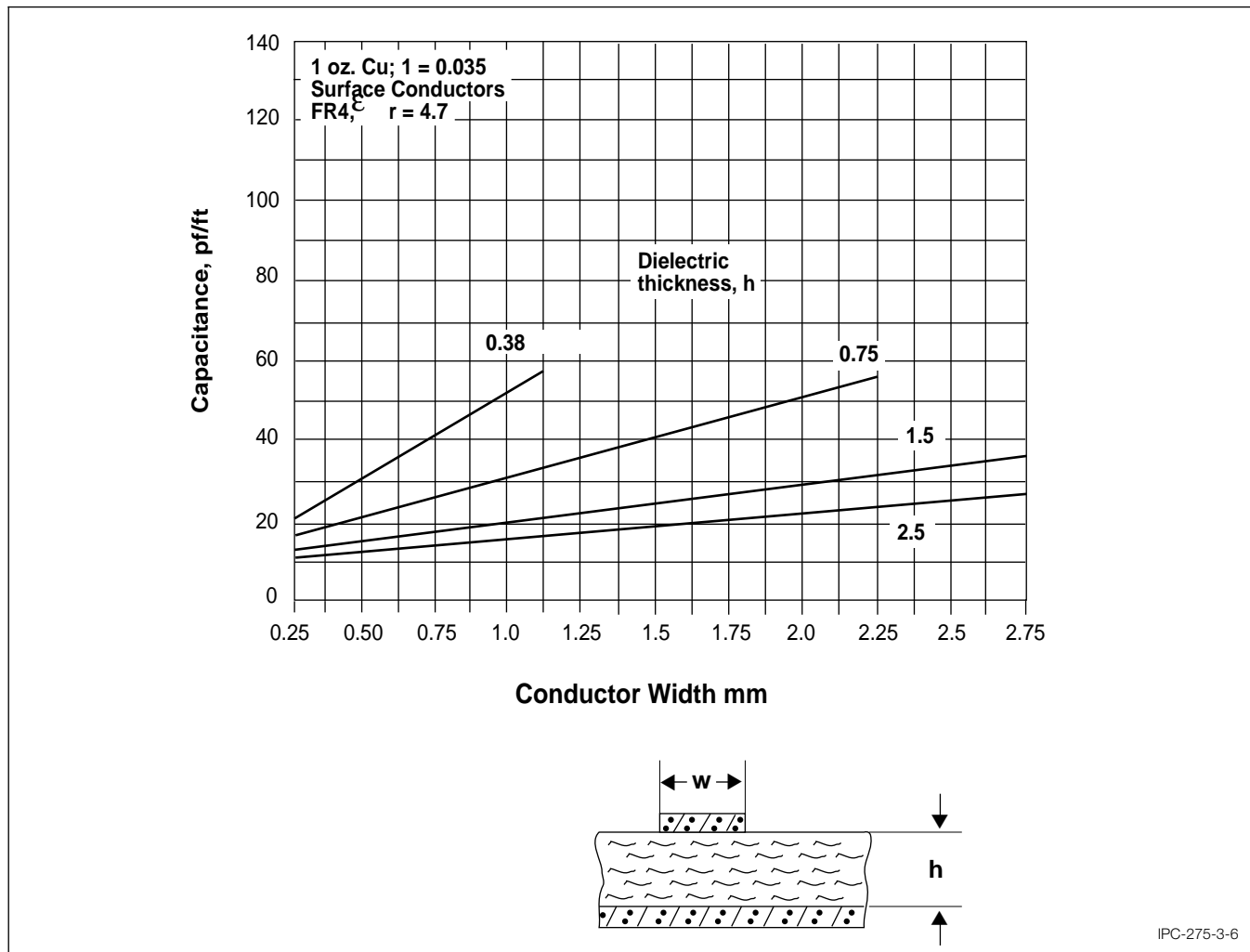
140

**1 oz. Cu; 1 = 0.035
Surface Conductors
FR4, ∊r = 4.7**

120

100

**Capacitance, pf/ft**

80

**Dielectric
thickness, h**

60

**0.38**          **0.75**

40          **1.5**

20          **2.5**

0

0.25  0.50  0.75  1.0  1.25  1.5  1.75  2.0  2.25  2.5  2.75

**Conductor Width mm**

← w →

h

IPC-275-3-6

**Figure 6-6   Capacitance vs. conductor width and dielectric thickness for microstrip lines, mm.**

## 7.0 THERMAL MANAGEMENT

This section is intended as an outline for temperature control and heat dissipation. This material, coupled with appropriate thermal analysis (see IPC-D-330), can result in greatly reduced thermal stresses and improved reliability of the components, solder attachment and the printed wiring board.

The primary objective of thermal management is to ensure that all circuit components, especially the integrated circuits, are maintained within both their functional and maximum allowable limits. The functional temperature limits provide the ambient, or component package (case) temperature range, within which the electronic circuits can be allowed to properly perform.

The cooling technique to be used in the printed board assembly application must be known in order to ensure the proper printed board assembly design. For commercial applications, direct-air cooling (i.e., where cooling air contacts the printed board assembly) may be used.

For rugged and hostile environment usage, indirect cooling must be used to cool the printed board assembly. In this application, the assembly is mounted to the structure, that is air or liquid cooled, and the components are cooled by conduction to a heat-exchange surface. These designs must use appropriate metal heatsinks on the printed board assembly. Appropriate component mounting and bonding may be required. To ensure adequate design, thermal dissipation maps must be provided to aid analysis and thermal design of the printed board assembly.

**7.1 Cooling Mechanisms**   The dissipation of the heat generated within electronic equipment results from the interaction of the three basic modes of heat transfer: conduction, radiation and convection. These heat transfer modes can, and often do, act simultaneously. Thus, any thermal management approach should attempt to maximize their natural interaction.

**7.1.1 Conduction**   The first mode of heat transfer to be encountered is conduction. Conduction takes place to a
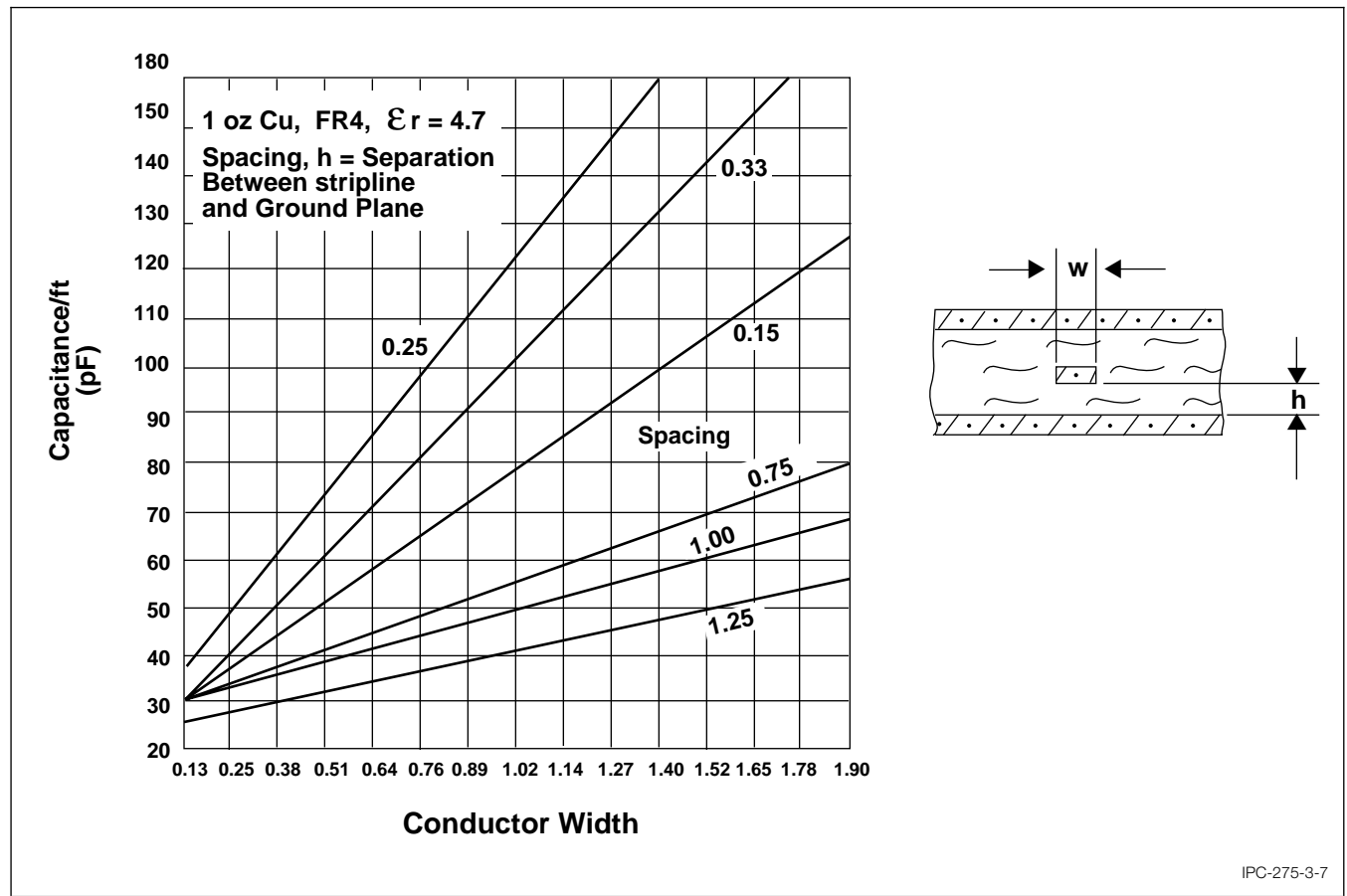
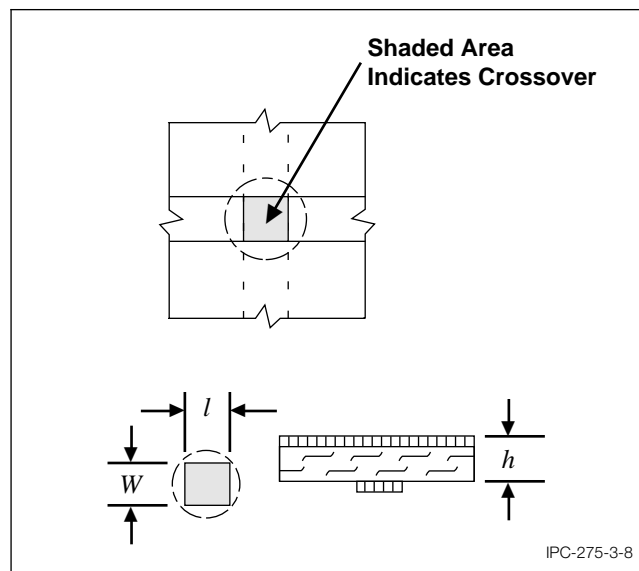**Figure 6-7   Capacitance vs. conductor width and spacing for striplines, mm.**



**Figure 6-8   Single conductor crossover**

varying degree through all materials. The conduction of heat through a material is directly proportional to the thermal conductivity constant (K) of the material, the cross sectional area of the conductive path and the temperature

difference across the material. Conduction is inversely proportional to the length of the path and the thickness of the material (see Table 7-1).

**7.1.2 Radiation**   Thermal radiation is the transfer of heat by electromagnetic radiation, primarily in the infrared (IR) wavelengths. It is the only means of heat transfer between bodies that are separated by a vacuum, as in space environments.

Heat transfer by radiation is a function of the surface of the ''hot'' body with respect to its emissivity, its effective surface area and the differential to the forth power of the absolute temperatures involved.

The emissivity is a derating factor for surfaces that are not ''black bodies,'' It is defined as the ratio of emissive power of a given body to that of a black body, for which emissivity is unity (1.0). The optical color of a body has little to do with it being a ''thermal black body.'' The emissivity of anodized aluminum is the same if it is black, red or blue. However, surface finish is important. A matte or dull surface will be more radiant than a bright or glossy surface (see Table 7-2).

**Table 7-1   Effects of Material Type on Conduction**

| Materials | Thermal Conductivity (K) | |
|---|---|---|
| | Watts/m °C | Gram-calorie/cm °C • s |
| Still Air | 0.0276 | 0.000066 |
| Epoxy | 0.200 | 0.00047 |
| Thermally Conductive Epoxy | 0.787 | 0.0019 |
| Aluminum Alloy 1100 | 222 | 0.530 |
| Aluminum Alloy 3003 | 192 | 0.459 |
| Aluminum Alloy 5052 | 139 | 0.331 |
| Aluminum Alloy 6061 | 172 | 0.410 |
| Aluminum Alloy 6063 | 192 | 0.459 |
| Copper | 194 | 0.464 |
| Steel Low Carbon | 46.9 | 0.112 |

**Table 7-2   Emissivity Ratings for Certain Materials**

| Material and Finish | Emissivity |
|---|---|
| Aluminum Sheet - Polished | 0.040 |
| Aluminum Sheet - Rough | 0.055 |
| Anodized Aluminum - any color | 0.80 |
| Brass - Commercial | 0.040 |
| Copper - Commercial | 0.030 |
| Copper - Machined | 0.072 |
| Steel - Rolled Sheet | 0.55 |
| Steel - Oxided | 0.667 |
| Nickel Plate - Dull Finish | 0.11 |
| Silver | 0.022 |
| Tin | 0.043 |
| Oil Paints - Any Color | 0.92-0.96 |
| Lacquer - Any Color | 0.80-0.95 |

Devices, components, etc. close to one another will absorb each others radiant energy. If radiation is to be the principle means of heat transfer, "hot" spots must be kept clear of each other.

**7.1.3  Convection**   The convection heat transfer mode is the most complex. It involves the transfer of heat by the mixing of fluids, usually air.

The rate of heat flow by convection from a body to a fluid is a function of the surface area of the body, the temperature differential, the velocity of the fluid and certain properties of the fluid.

The contact of any fluid with a hotter surface reduces the density of the fluid and causes it to rise. The circulation resulting from this phenomenon is known as "free" or "natural" convection. The air flow can be induced in this manner or by some external artificial device, such as a fan or blower. Heat transfer by forced convection can be as much as ten times more effective than natural convection.

**7.1.4  Altitude Effects**   Convection and radiation are the principle means by which heat is transferred to the ambient air. At sea level approximately 70% of the heat dissipated from electronic equipment might be through convection and 30% by radiation. As air becomes less dense, convective effects decrease. At 5200 m the heat dissipated by convection may be less than half that of radiation. This needs to be considered when designing for airborne applications.

**7.2 Heat Dissipation Considerations**   Design of multi-layer boards to remove heat from a high thermal radiating printed board assembly should consider the use of:

• Heatsinking external planes (usually copper or aluminum);

• Heatsinking internal planes;

• Special heatsink fixtures;

• Connection to frame techniques;

• Liquid coolants and heatsink formation;

• Heat pipes; and

• Heatsinking constraining substrates.

**7.2.1 Individual Component Heat Dissipation**   Heatsinking of individual components can use a variety of different techniques. 8.1.10 of this standard provides information on some of the heatsinking devices that come with individual components requiring specific heat dissipation. In addition, consideration should be given to:

• Heatsink mounting (hardware or soldering);

• Thermal transfer adhesives, paste, or other materials;

• Solder temperature requirements; and

• Cleaning requirements under heatsinks.

**7.2.2 Thermal Management Considerations for Board Heatsinks** The following factors must be addressed while the printed board components are being placed:

1. Method of heatsink mounting (i.e., adhesive bond, rivet, screw, etc.) to printed board

2. Thickness of heatsink and printed board assembly to allow adequate component lead protrusion

3. Automatic component insertion clearances (see Figure 7-1)

4. Heatsink material and material properties

5. Heatsink finish (i.e., anodize, chemical film, etc.)

6. Component mounting methods (i.e., spacers, screw, bonding, etc.)

7. Heat transfer path and rate of heat transfer

8. Producibility (i.e., method of assembly, method of cleaning, etc.)

9. Dielectric material required between the heatsink and any circuitry that may be designed on the heatsink mounting surface of the printed board

10. Edge clearance to any exposed circuitry (i.e., component pads and circuit runs) Tooling hole location and size

11. Heatsink shape as it relates to the structure of heatsink/printed board assembly

12. The heatsink should fully support the component. Do not allow the component the opportunity to tip during assembly or soldering.

Heatsinks **shall** be designed to avoid the occurrence of moisture traps and to allow access for post-soldering cleaning. This can be accomplished by providing accessible slots in the heatsink instead of round clearance holes under TO3, TO66, and similar packages with leads which extend through the heatsink and are soldered into the printed board.

Through hole printed board assembly heatsinks generally are of a ladder configuration when standard component package types (i.e., DIPs and axial-leaded components) can be used. The ladder heatsink type is preferred due to its relative simplicity in design and fabrication. Figure 7-1 provides standard clearances between heatsink and components that are necessary to facilitate automatic component insertion.

Certain printed board assemblies (e.g., power supplies and other analog designs in particular) utilize many different component types. The circuit function for these analog circuits may be very dependent upon component placement. For analog designs, heatsinks sometimes cannot be designed in a ladder type configuration, however they should be designed with producibility in mind. Minimizing

the number of unique cutout shapes required, and the number of areas where the heatsink thickness must change (requiring milling or lamination) will enhance heatsink producibility. When machined heatsinks are used efforts should be made to utilize as large a radius as possible in corners to enhance producibility (e.g., a 3.0 mm radius can cost substantially more to fabricate than a 6.0 mm radius). In all cases, analog heatsink designs that can't use ladders should be designed in parallel with the printed board (as opposed to after completion of artwork) and should be reviewed for producibility in both the metal fabrication and printed board assembly areas.

**7.2.3 Assembly of Heatsinks to Boards** Assembly of heatsinks to printed wiring boards may be accomplished as listed below (in order of manufacturing preference). If the board and the heatsink are purchased as an assembly, the manufacturer may have other preferences. Table 7-3 shows the preferences.

Details of these assembly methods are as follows:

1. *Mechanical Fasteners:* Riveting is the preferred fastening method, but care must be taken in rivet selection (solid or tubular), and rivet installation, to obviate laminate damage. Screws should be used if the unit is expected to be disassembled. Closer contact may be necessary to resist vibration or improve heat transfer. Use of adhesives along with mechanical fasteners can promote warpage but may help in a vibration environment. Dry film epoxy adhesives are preferred over liquids. Bonding temperatures should be as low as possible to minimize warpage.

2. *Film Type Adhesives:* Sheet adhesive is die or mechanically cut to fit the outline of the heatsink. The associated cure cycles and warpage of the heatsink/printed board assembly are problems that affect producibility. See 4.2.3 for film type adhesives.

3. *Liquid Adhesives:* Liquid adhesive is a producibility concern because of the difficulty in application associated cure cycle and warpage of the heatsink/printed board assembly. The recommended structural adhesives listed in 4.2.2 are well suited for the heatsink bonding application.

Specification of adhesive thickness involves a trade-off between contact area (bond line) and producibility. Bond line may be reduced by process variables (e.g., surface finish or cleanliness), material warpage, and surface protrusions (especially surface runs of 2 oz. copper). More adhesive may improve contact, but excess can flow from under the heatsink and contaminate lands and plated-through holes. In many cases, a 75% (of the heatsink) bond is sufficient, but care must be taken to avoid moisture or flux entrapment that cannot be cleaned. Adhesive bonding will
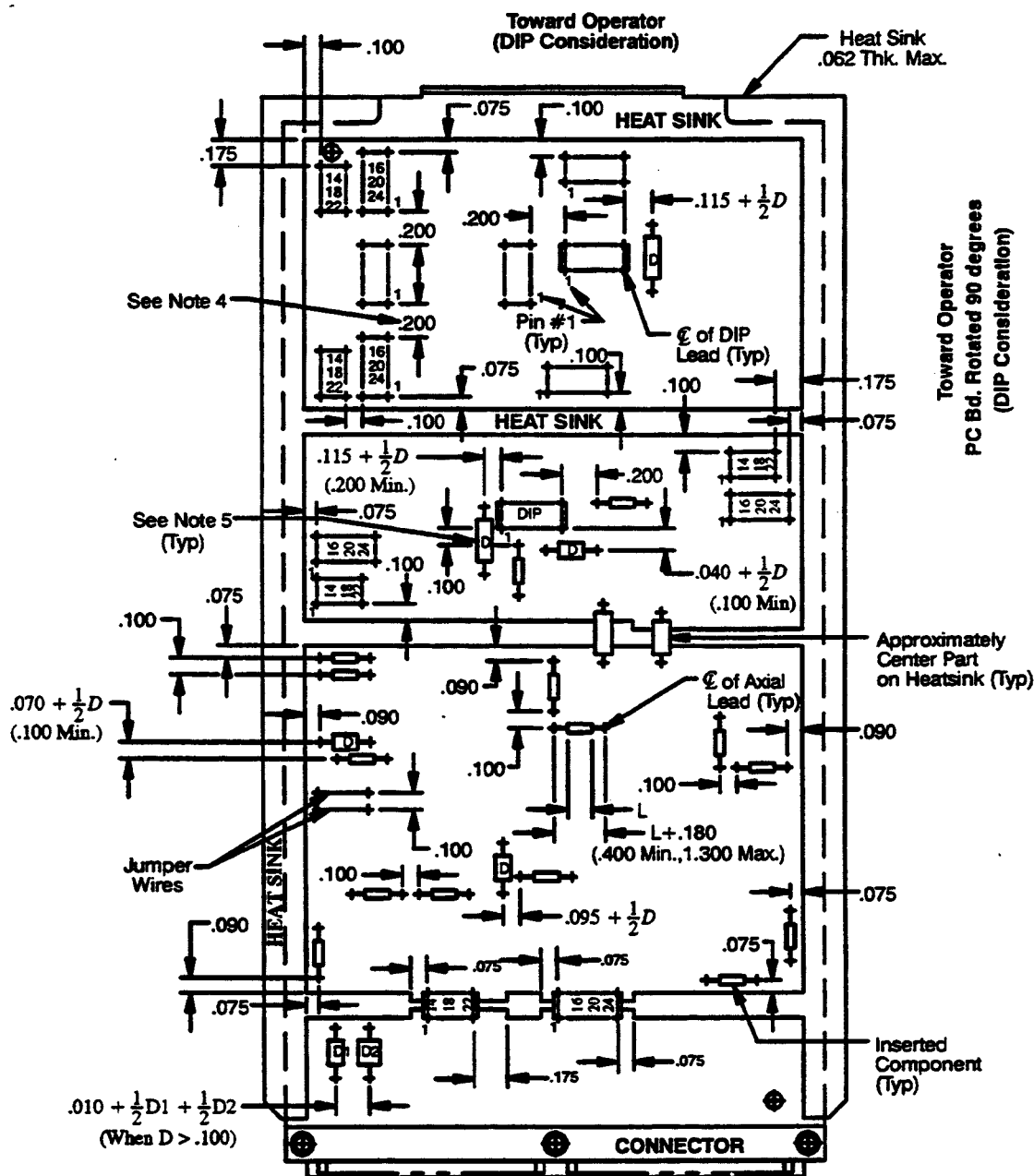
**Figure 7-1    Component clearance requirements for automatic component insertion on through hole technology printed board assemblies. (in.)**

**Table 7-3   Board Heatsink Assembly Preferences**

| Method | Major Advantages | Major Disadvantages | Considerations |
|---|---|---|---|
| Rivets | Fastest, no cure cycle or adhesive application | Board area and holes needed for rivets | Use standard rivet sizes |
| Screws | Allows disassembly | Requires washers and nuts, board area and holes | Use standard hardware |
| Film Adhesive | No wasted space, potentially improved heat transfer, higher vibration natural frequency. Increased insulation | Cure time and possible warpage | Low cure temperature will minimize warpage |
| Liquid Adhesive | No wasted space, potentially improved heat transfer, higher vibration natural frequency | Producibility concern as well as cure time and warpage concern | Low cure temperature will minimize warpage |

raise the vibration natural frequency of the printed board assembly above that which can be obtained by mechanical fasteners alone. Heat transfer may also be improved when adhesive bonding is used.

**7.2.4 Special Design Considerations for SMT Board Heatsinks**  Surface mount heatsinks can dramatically affect the coefficient of thermal expansion (CTE) of the surface mount assembly. The reliability of surface mount component solder joints may be compromised if a high CTE material is used, but depends upon the service environment of the surface mount assembly. Laboratory environments which do not subject the surface mount assembly to significant temperature changes may allow heatsink materials such as 1100 aluminum to be used. Most environments require the use of low CTE heatsink materials to provide long solder joint life.

Heatsinks used in surface mount applications are either built within the printed board (typically copper-Invar-copper layers laminated in the printed board) or are a solid plate that has a surface mount printed board bonded to one or both sides.

Bonding of the heatsink to two printed wiring boards requires a compliant sheet adhesive to decouple the difference in CTE of the heatsink and printed board and serve as a vibration damping and heat transfer material. A solid sheet adhesive provides an inspectable material that allows the assembler to check for pin holes that might allow electrical connection between the heatsink and the printed board.

Silicone sheet adhesives have been very effective in bonding printed boards to a solid heatsink. The bonding integrity of silicone sheet adhesives is dependent upon the proper application of a primer to the surfaces to be bonded. Care must be taken to prevent silicone contamination of surfaces which are to be soldered and/or conformal coated. See 4.2.2 for silicone sheet adhesives. To minimize warpage of the final bonded assembly, and thermal and mechanical stress on the assembled components during the adhesive cure process, a low temperature curing silicone

adhesive should be chosen. Components subject to damage should be so noted on the drawing and protection during assembly required. It may be necessary to assemble some components by hand after the bonding process is complete.

**7.3 Heat Transfer Techniques**

**7.3.1 Coefficient of Thermal Expansion (CTE) Characteristics**  For applications with surface mount components, the CTE of the interconnecting structure becomes an important consideration. Table 7-4 establishes calculated reliability figures of merit related to the differences in the X and Y expansion characteristics of the component and the substrates, the distance from the solder joint to the neutral point (zero strain point), and the solder joint height. This factor is related to the total strain per cycle of the solder joint. It is important to minimize the relative differences in the CTE of the component and printed board assembly. Typical ceramic substrates have a CTE from 5 to 7 ppm/°C. Figure 7-2 provides examples of the CTE for some materials used by themselves (polymide, glass or epoxy glass) and some constraining substrate materials used in conjunction with the printed board dielectric materials.

**7.3.2 Thermal Transfer**  Components, which for thermal reasons require extensive surface contact with the board or with a heatsink mounted on the board, **shall** be compatible with or protected from processing solutions at the conductive interface.

**7.3.3 Thermal Matching**  A primary thermal concern with through-hole mounted glass components and with ceramic surface-mounted components is the thermal expansion mismatch between the component and the printed board. This mismatch may result in fractured solder joint interconnections if the assembly is subjected to thermal shock, thermal cycling, power cycling and high operating temperatures.

The number of fatigue cycles before solder joint failure is dependent on, but not limited to, the thermal expansion

**Table 7-4   Comparative Reliability Matrix Component Lead/Termination Attachment**

| Cyclic Services Environment [°C] | Design Life [Years] | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 5 | | | 10 | | | 20 | | |
| | Cyclic Frequency [Cycles/Day] | | | | | | | | |
| | 0.1 | 1 | 10 | 0.1 | 1 | 10 | 0.1 | 1 | 10 |
| | Mean Cyclic Life Frequency [Cycles/Day] | | | | | | | | |
| | 183 | 1825 | 18,250 | 365 | 3650 | 36,500 | 730 | 7300 | 73,000 |
| | Relative Reliability Index, R [ppm/°C] | | | | | | | | |
| +20 to +40 | 2200 | 790 | 360 | 1600 | 580 | 270 | 1150 | 420 | 200 |
| +20 to +80 | 670 | 240 | 110 | 490 | 170 | 79 | 350 | 130 | 58 |
| -40 to +40[1] | 600 | 230 | 110 | 440 | 170 | 83 | 330 | 130 | 62 |
| -40 to 80[1] | 370 | 140 | 65 | 270 | 100 | 48 | 200 | 75 | 36 |

(1) These environments straddle the transition region from stress-driven (<20°C) to strain/creep-driven (>+20°C); for such environments it has been shown that fatigue occurs significantly earlier by a mechanism different from that underlying this reliability matrix and it should be assumed that the R-values for these environments are optimistic.

mismatch between the component and the printed board, the temperature excursion over which the assembly must operate, the solder joint size, the size of the component, and the power cycling that may cause an undesirable thermal expansion mismatch if a significant temperature difference exists between the component and the board.

**7.4 Thermal Design Reliability**   Design life can be verified through comparative testing intended to simulate the service environment. Table 7-4 represents an example of design verification of surface mounted devices for three service environments: 0.1 cycles per day, 1 cycle per day, and 10 cycles per day. The service environments shown represent four categories of different temperature ranges. The table establishes a relative reliability index (ppm/°C) for the design depending on a desired equipment life of 5, 10, or 20 years. This reliability index (R) is a factor that may be used in considering if the assembly will survive in the environment for the expected life.

The longer the life or the more severe the requirements, the lower the number in the matrix becomes. A reliability index roughly gives the maximum cyclic strain that will result in a mean fatigue life just equal to the expected design life. The matrix is primarily meant for leadless components; for leaded components, some underlying relationships are different which, while not changing the indicated trends, will change the matrix quantitatively. Only mean cyclic life is represented, indicating when half the components are expected to fail, not when the first component in a system fails. The statistical distribution of the solder joint fatigue failure has to be included in a reliability assessment.

In the case of through-hole mounted glass components, it is often sufficient to provide stress-relief bends in the component's leads (see section 8.1.14). With surface-mount components, the number of fatigue cycles can be increased by reducing the thermal expansion mismatch, reducing the temperature gradient, increasing the height of the solder joint, using the smallest physical size component wherever possible, and by optimizing the thermal path between the component and the board. For more detailed information, see IPC-D-279 and IPC-SM-785.

**8.0  COMPONENT AND ASSEMBLY ISSUES**

The mounting and attachment of components play an important role in the design of a printed board. In addition to their obvious effect on component density and conductor routing, these aspects of board design also impact fabrication, assembly, solder joint integrity, repairability and testing. Therefore, it is important that the design reflects appropriate tradeoffs that recognize these and other significant manufacturing considerations.

All components **shall** be selected so as to withstand the vibration, mechanical shock, humidity, temperature cycling, and other environmental conditions the design must endure when the components are installed. The following are requirements the designer should consider and detail on the assembly drawing in specific notes or illustrations.

As a minimum, component mounting and attachment should be based on the following considerations:

• Electrical performance and electrical clearance requirements of the circuit design.

• Environmental requirements.

• Selection of active and passive electronic components and associated hardware.

• Size and weight.

• Minimizing of heat generation and heat dissipation problems.

• Manufacturing, processing and handling requirements.

• Contractual requirements.

• Serviceability requirements.

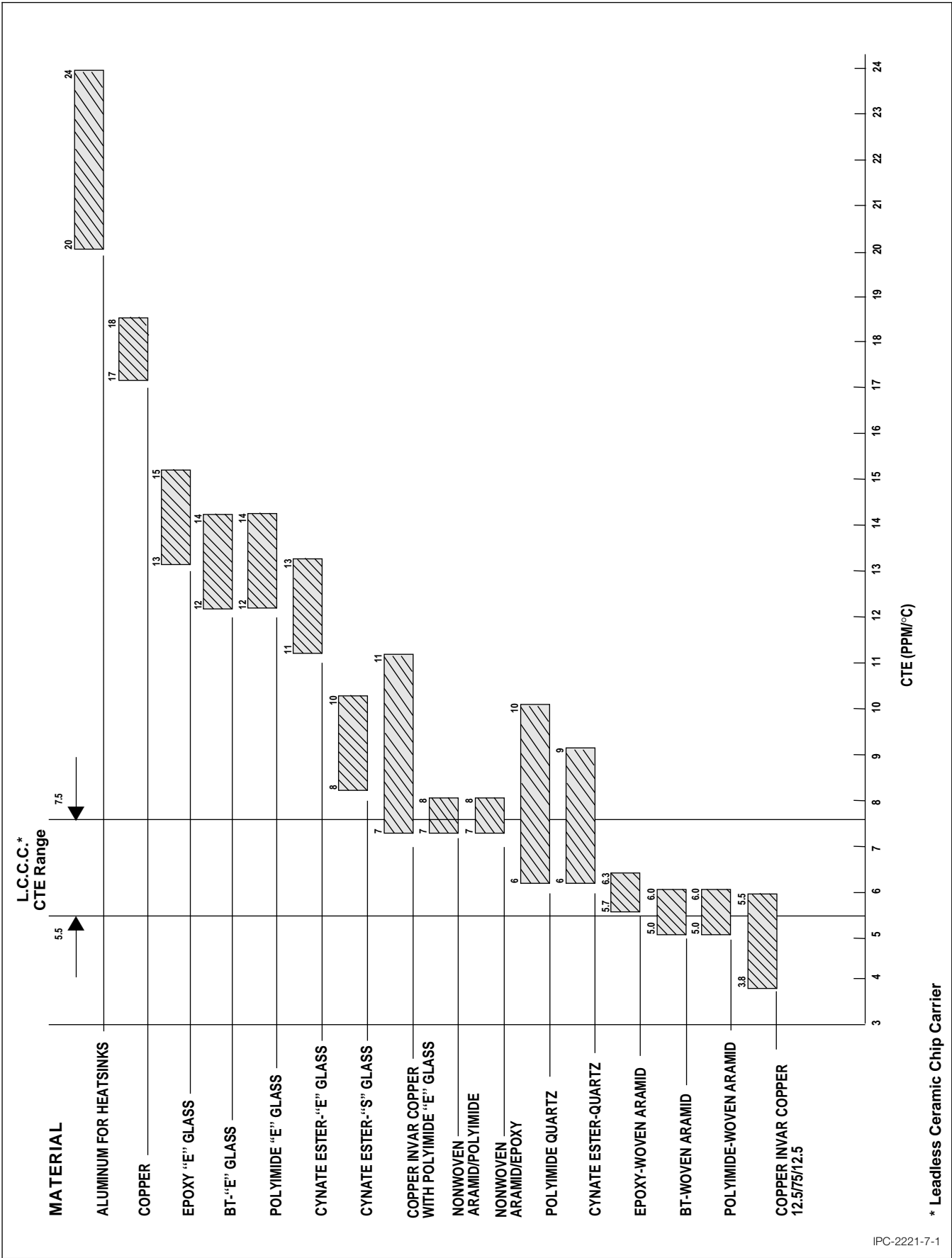• Equipment usage and useful life.

Figure 7-2   Relative coefficient of thermal expansion (CTE) comparison

• Automatic insertion and placement requirements, when these methods of assembly are to be used.

• Test methods to be employed before, during and after assembly.

• Field repair and maintenance considerations.

• Stress relief.

• Adhesive requirements.

## 8.1 General Placement Requirements

**8.1.1 Automatic Assembly** When automatic component insertion and attachment is employed, there are several printed board design parameters that must be taken into account that are not applicable when manual assembly techniques are used.

**8.1.1.1 Board Size** The size of the printed board to be automatically assembled can vary substantially. Therefore, manufacturers' equipment specifications should be evaluated with respect to the finished board requirements (see 5.3.3).

Standardization of automatic assembly operations can be achieved through standard fixtures that can accommodate a variety of board sizes or assembling boards in panel format. Using the panel assembly concept requires close cooperation with the printed board manufacturer in order to establish tooling concepts, tool hole location, board location, coupon and fiducial locations.

**8.1.1.2 Mixed Assemblies** Automatic processes used for both surface mounted and through-hole mounted components require special design considerations in order that the components assembled in the first phase of the assembly do not interfere with insertion heads during the second phase. Component placement should consider the stresses that are put on the board with insertion equipment, by isolating parts wherever possible to specific areas so that the second phase insertion/placement stresses do not impact previously soldered connections.

**8.1.1.3 Surface Mounting** Automatic assembly considerations for surface mounted components include pick-and-place machines used to place/position chip components, discrete chip carriers, small outline packages, and flat packs.

Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled surface mounted part. Techniques may include special symbols, or special land configurations to identify such characteristics as a lead of an integrated circuit package.

**8.1.2 Component Placement** Whenever possible, through-hole parts and components should be mounted on the side of the printed board opposite that which would be in contact with the solder, if the board is machine soldered.

Intermixing of through-hole and surface mount parts, or mounting parts on both sides of the board, requires complete understanding of the assembly and attachment processes (see IPC-CM-770 and IPC-SM-780).

Whenever possible, if their leads are dressed through the holes, axial and non-axial-leaded components should be mounted per IPC-CM-770 on only one side of the printed board assembly.

Unless a component or part is specifically designed to accept another part into its configuration, there **shall** be no stacking (piggybacking) of components or parts (see J-STD-001).

Component leads **shall** either be surface mounted, mounted in through-holes, or mounted to terminals. Lead and wire terminations **shall** be soldered or wire bonded.

The variations in the actual placement of the component's leads into plated-through holes or on the termination area in addition to the tolerances on the component's envelope (body and leads) will cause movement of the component body from the intended nominal mounting location. This misregistration **shall** be accounted for such that worst case placement of components **shall** not reduce their spacing to adjacent printed wiring or other conductive elements by more than the minimum required electrical spacing.

If a component is bonded to the surface of the printed board utilizing an adhesive (structural or thermally conductive), the placement of the component **shall** consider the area of adhesive coverage such that the adhesive may be applied without flowing onto or obscuring any of the terminal areas. Part attachment processes **shall** be specified which control the quantity and type of bonding material such that the parts are removable without damage to the printed board assembly. The adhesive used **shall** be compatible with both the printed board material, the component, and any other parts or materials in contact with the adhesive.

Thermal concerns, functional partitioning, electrical concerns, packing density, pick-and-place machine limitations, wave soldering holder concerns, vibration concerns, part interference concerns, ease of manufacture and test, etc., all affect the parts placement.

Parts should be placed on a 0.5 mm placement grid whenever possible. When a 0.5 mm grid is not adequate, a 0.05 mm placement grid should be used. Certain parts (such as some relays) have leads that are not on standard grids but otherwise the parts should be placed so that the through holes are on grid.

If equipment or other constraints do not allow for a metric grid, parts may be on 0.100 in. placement grid. When this is not adequate, a 0.050 in. grid may be used or even a 0.025 in. grid. The 0.100 in. placement grid facilitates not only parts insertion but also standard bed-of-nails testing of the board and of the assembly. If bed-of-nails testing is to be used (including in-circuit printed board assembly testing), the test fixturing becomes much more difficult when components are placed off grid.

Figure 7-1 illustrates the producibility design allowances for automatic component insertion. Through hole mount printed boards should observe component to edge of the board spacing constraints on two (2) opposite edges to allow direct insertion into wave solder fingers. Other designs will require fixturing.

Both component heatsink considerations and board heatsink requirements must be addressed in parts placement.

If the printed board assembly will not be tested with a bed-of-nails testing then the assembly grid will be limited only by the assembly machinery. If the printed board assembly is testable with a bed-of-nails scheme, a 0.100 in. grid for plated through hole spacing is preferred. A 0.075 in. grid allows greater design density and is not a concern with the assembly machinery but is a concern with bare board and completed assembly testing if a bed-of-nails testing approach is utilized. Bare board testing will normally be done at the printed board supplier and there presently is no cost penalty for off grid nor reduced grid printed board testing.

The designer should allow sufficient component to board edge separation for test and assembly processes. If this is not possible, the designer should consider adding a removable section of board (i.e., breakaway tab). The edge of the component is defined as the physical edge of the component on sides where no leads protrude from the component, and the edge of the surface land pattern for the leaded side of a component. Preferably, components should be a minimum of 1.5 mm from the edge of the board and board guide or mounting hardware to allow for component placement, soldering, and test fixturing.

Components should not be grouped in such a way that they shadow one another during soldering. Do not align rows of components perpendicular to the direction of travel; stagger them.

Component polarities should be oriented consistently (in the same direction) throughout a given design.

For wave soldered surface mount chip types, components should be bonded to the printed board prior to automated soldering with an adhesive specially formulated for the purpose.

Specific requirements for part mounting are functions of the type of component, the mounting technology selected for the printed board assembly, the lead bending requirements for the component, the lead stress relief method selected, and placement of the components (either mounted over surfaces without exposed circuitry, over protected surfaces, or over circuitry). Additional requirements are dependent upon the thermal requirements (the operating temperature environment, maximum junction temperature requirements, and the component's dissipated power), and the mechanical support requirements (based on the weight of the component).

Mounting methods for components of the printed board assembly **shall** be selected so that the final assembly meets applicable vibration, mechanical shock, humidity, and other environmental conditions. The components **shall** be mounted such that the operating temperature of the component does not reduce the component's life below required design limits. The selected component mounting technique **shall** ensure that the maximum allowable temperature of the board material is not exceeded under operating conditions.

**8.1.3 Orientation** Components should be mounted parallel to the edges of the printed board. They should also be mounted parallel or perpendicular to one another in order to present an orderly appearance. When appropriate, the component should be mounted in such a manner as to optimize the flow of cooling air.

Assemblies are usually flow soldered with the top edge of the board in the lead (perpendicular to the direction of travel through the wave), mounting flanges and hardware against the fixture or conveyor fingers, and edge connector last. Surface mount components should be placed to facilitate solder flow in the wave. Rectangular components (with solder caps at the ends) should be oriented with the long axis parallel to the leading edge of the board, perpendicular to the direction of travel. This avoids the "shadow" effect, where the body of the component would otherwise prevent free flow of solder to the trailing solder joint. See Figure 8-1.

**8.1.4 Accessibility** Electronic components **shall** be located and spaced so that the lands for each component are not obscured by any other component, or by any other permanently installed parts. Each component **shall** be capable of being removed from the assembly without having to remove any other component. These requirements do not apply to assemblies manufactured with no intent to repair (throw away assemblies) or as specified in 8.2.13.
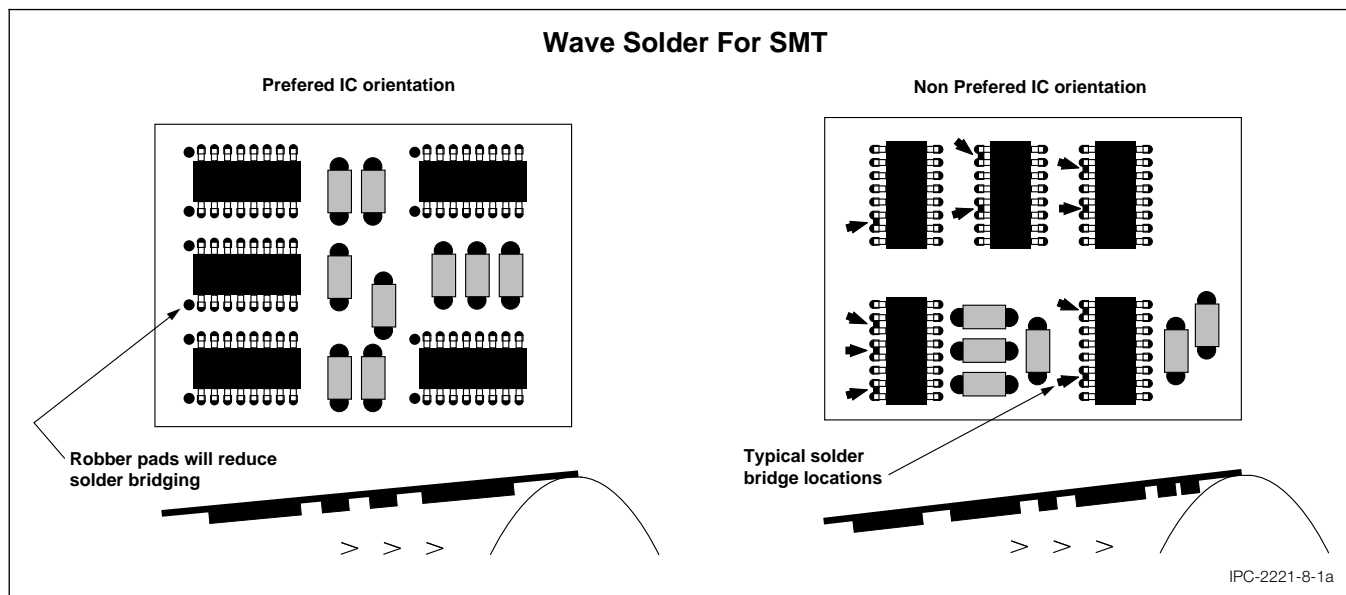
**Wave Solder For SMT**

Prefered IC orientation                                          Non Prefered IC orientation

**Robber pads will reduce
solder bridging**

**Typical solder
bridge locations**

> > >                                                            > > >

IPC-2221-8-1a

**Figure 8-1  Component orientation for boundaries and/or wave solder applications**

**8.1.5 Design Envelope**  The projection of the component, other than connectors on the board should not extend over the edge of the board or interfere with board mounting.

Unless otherwise detailed on the assembly drawing, the board edge is regarded as the extreme perimeter of the assembly, beyond which no portion of the component, other than connector, is allowed to extend. The designer **shall** prescribe the perimeter with due regard for maximum part body dimensions and the mounting provisions dictated by the board and assembly documentation.

**8.1.6 Component Body Centering**  Except as otherwise specified herein, the bodies (including end seals or welds) of horizontally mounted, axial leaded components should be approximately centered in the span between mounting holes, as shown in Figure 8-2.

**X is approximately equal to Y**

IPC-275-4-2
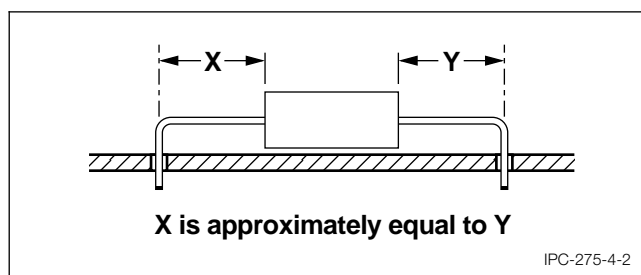
**Figure 8-2  Component body centering**

**8.1.7 Mounting Over Conductive Areas**  Metal-cased components **shall** be mounted insulated from adjacent electrically conductive elements. Insulation materials **shall** be compatible with the circuit and printed board material.

Conductive areas under the parts **shall** be protected against moisture entrapment by one of the following methods.

• Application of conformal coating using material in accordance with IPC-CC-830 (usually specified on the assembly drawing).

• Application of cured resin coating by using low flow prepreg material.

• Application of a permanent polymer coating (solder resist) using material in accordance with IPC-SM-840.

This requirement is applicable to components with or without sleeving (see Figure 8-3).

**Conformal Coating, Soldermask, etc.**

IPC-275-4-3
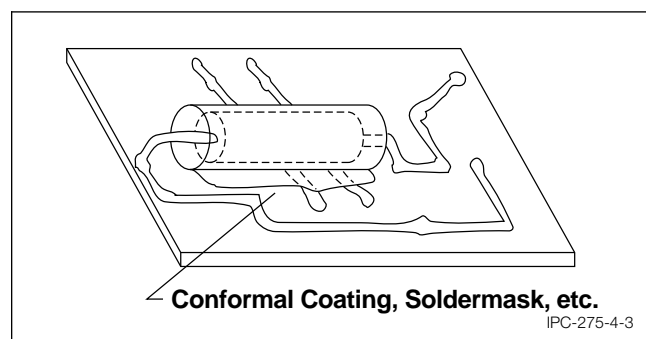
**Figure 8-3  Axial-leaded component mounted over conductors**

**8.1.8 Clearances**  The minimum clearance between component leads or components with metal cases and any other conductive path **shall** be a minimum of 0.13 mm. In general, uncoated conducting areas should provide for a clearance of approximately 0.75 mm as shown in Figure 8-4, but not less than the values shown in Table 6-1.

Parts and components **shall** be mounted such that they do not obstruct solder flow onto the topside termination areas of plated through-holes.

**8.1.9 Physical Support**   Dependent upon weight and heat generation characteristics, components weighing less than 5 grams per lead which dissipate less than 1 watt, and are not clamped or otherwise supported **shall** be mounted with the component body in intimate contact with the printed board as is practical, unless otherwise specified.

**8.1.9.1 Component Mounting Techniques for Shock and Vibration**   Axial-leaded components weighing less than 5 grams per lead **shall** be mounted with their bodies in intimate contact with the board. Dimensional criteria for lead bending and spacing **shall** be as specified in Figure 8-9. Axial-leaded components weighing 5 grams or more per lead should be secured to the board utilizing mounting clamps. If clamps are not practical due to density considerations, other techniques should be employed such that the solder connections are not the only means of mechanical support. These techniques are used for components weighing more than 5 grams when high vibration requirements must be met. (See 5.2.7 and Figures 8-5 and 8-6.)

When mounting chip components on edge, if the vertical dimension is greater than the thickness dimension, then chip components should not be used in assemblies subject to high vibration or shock loads. Vertical mounting **shall** be used for:

a)   Low and tall profile SMDs with reflow termination pads located in a single base surface;

b)   Non-axial-leaded devices with leads egressing from two or more sides of the device(s); and

c)   Non-axial-leaded devices with leads egressing from a single base surface.
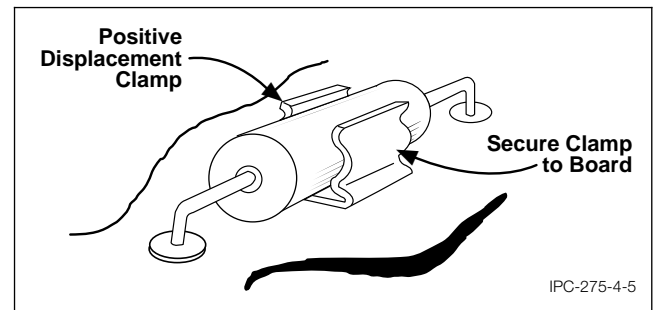


Figure 8-5   Clamp-mounted axial-leaded component
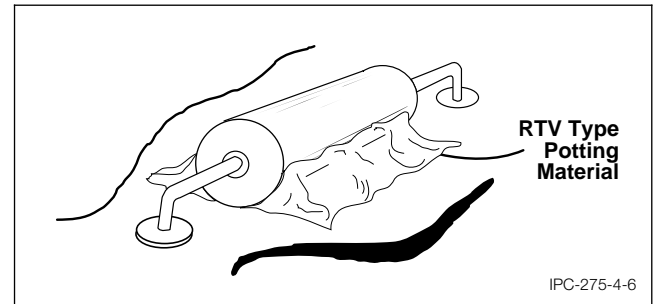


Figure 8-6   Adhesive-bonded axial-leaded component

For radial leaded components with three or more leads, such as transistors, that require the use of spacers between their base and the board surface for vertical mounting, special attention should be given to ensuring that there is no movement of the spacer during vibration that might cause damage to surface conductors.

**8.1.9.2 Class 3 High Reliability Applications**   Free standing components weighing more than 5.0 grams per lead **shall** be mounted with the base surface paralleling the surface of the board (see Figure 8-7). The component **shall** be supported on either:
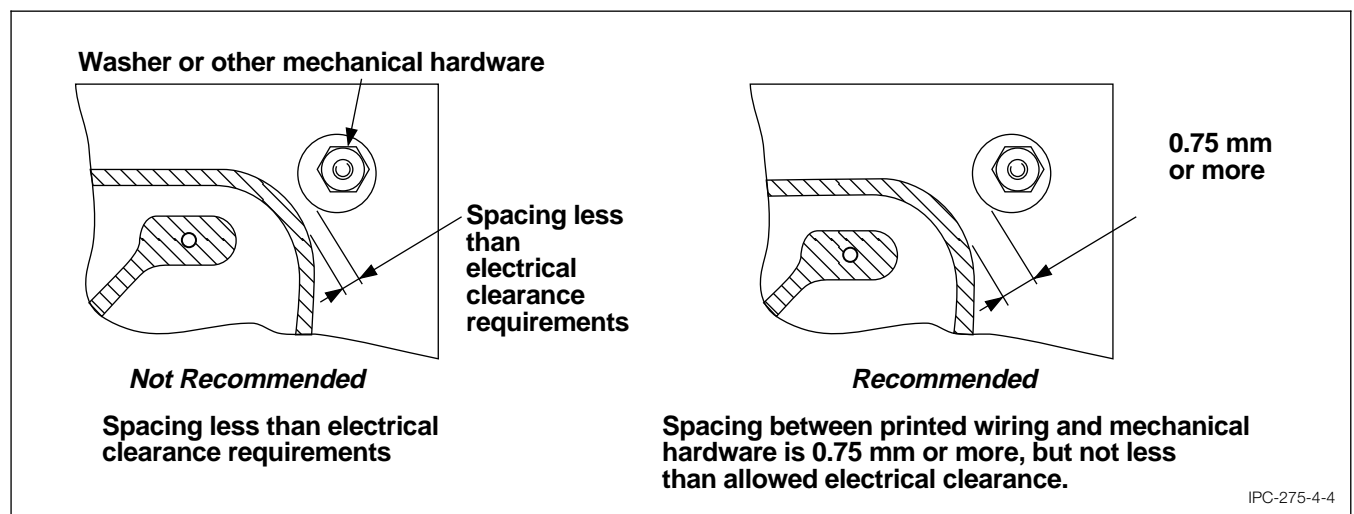


Figure 8-4   Uncoated board clearance

• Feet or standoffs integral to the component body (see Figure 8-7A and B);

• Specially configured non-resilient footed standoff devices (see Figure 8-7C); or

• Separate non-footed standoffs which do not block plated through-holes nor conceal connections on the component side of the board.

Standoffs, footed or non-footed, are intended to be mounted flush to the surface of the board. For this requirement, a button standoff as shown in Figure 8-7B is considered a foot. Footed standoffs, as illustrated in Figures 8-7C and 8-7D, **shall** have a minimum foot height of 0.25 mm.

When a separate footed standoff device or separate base non-footed standoff is utilized and the component is mounted with the base surface paralleling the board surface, mounting should be such that the component base is seated in contact with, and flat to, the footed or non-footed standoff. Mounting should also be such that the feet of the footed standoff maintain full contact with the board surface. No standoff **shall** be inverted, tilted, or canted, and should not be seated with any foot (or base surface) out of contact with the board or conductors thereon. Neither **shall** the component be tilted, canted nor separated from the mating surface of the resilient standoff device.

**8.1.10 Heat Dissipation**  Design for heat dissipation of components **shall** insure that the maximum allowable temperature of the board material and the component is not exceeded under operating conditions. Heat dissipation may be accomplished by requiring a gap between board and component, using a clamp or thermal mounting plate, or attaching a compatible thermally-conductive material working in conjunction with a thermal bus plane to the component. (See Figure 8-8 for examples.)

Any heat dissipation technique or device **shall** permit appropriate cleaning to remove contaminants from the assembly. Conductive materials used to transfer heat

between parts and heatsink **shall** be compatible with assembly and cleaning processes.

Components on Class 3 assemblies which for thermal reasons require extensive surface contact with the board or with a heatsink mounted on the board, **shall** be protected from processing solutions at the conductive interface. To prevent risk of entrapment, compatible materials and methods **shall** be specified to seal the interface from entry of corrosive or conductive contaminants.

*Note:* Even totally nonmetallic interfaces that are prone to entrap fluids can have adverse effects on the fabricator's ability to pass required cleanliness tests.

**8.1.11 Stress Relief**  Lands and terminals **shall** be located by design so that components can be mounted or provided with stress relief bends in such a manner that the leads cannot overstress the part lead interface when subjected to the anticipated environments of temperature, vibration, and shock. Where the lead bend radius cannot be in accordance with Figure 8-9 in order to achieve design goals, the bends **shall** be detailed on the assembly drawing.

The leads of components mounted horizontally with their bodies in direct contact with the printed board **shall** be mounted with a method that ensures that stress relief is not reduced or negated by solder fill in the lead bends. Leads **shall** not be formed at the body of the component or between the body of a component and any lead weld. The lead **shall** extend straight from the body seal or lead weld before starting the bend radius as shown in Figure 8-9.

The requirements shown in Figures 8-9 and 8-10 should be implemented to prevent possible component damage, particularly glass-bodied parts. Lead bending equipment capability should be considered when selecting a lead configuration. The use of spacers under components not mounted directly in contact with the board is recommended.

DIPs mounted directly to heatsink frames, as described in section 8.1.10, may have special stress relief provisions
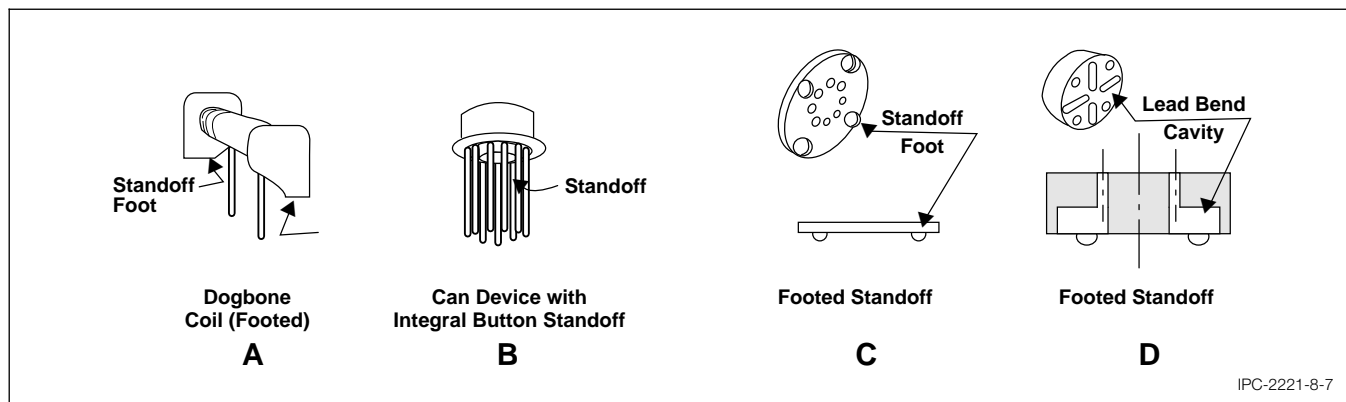


**Figure 8-7   Mounting with feet or standoffs**
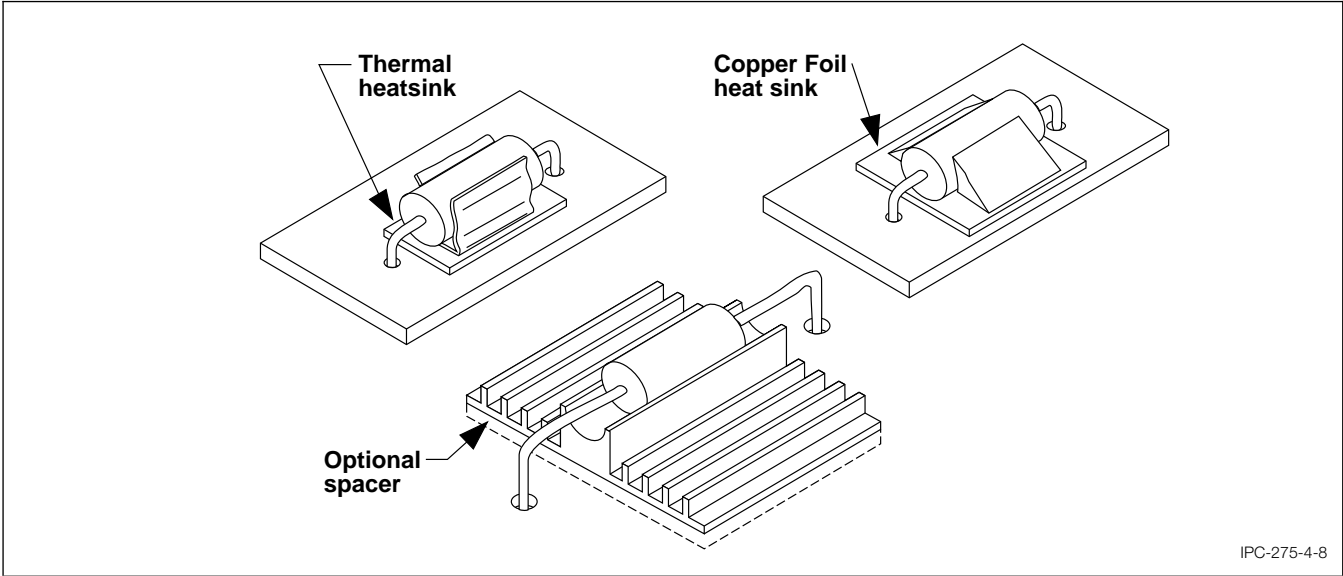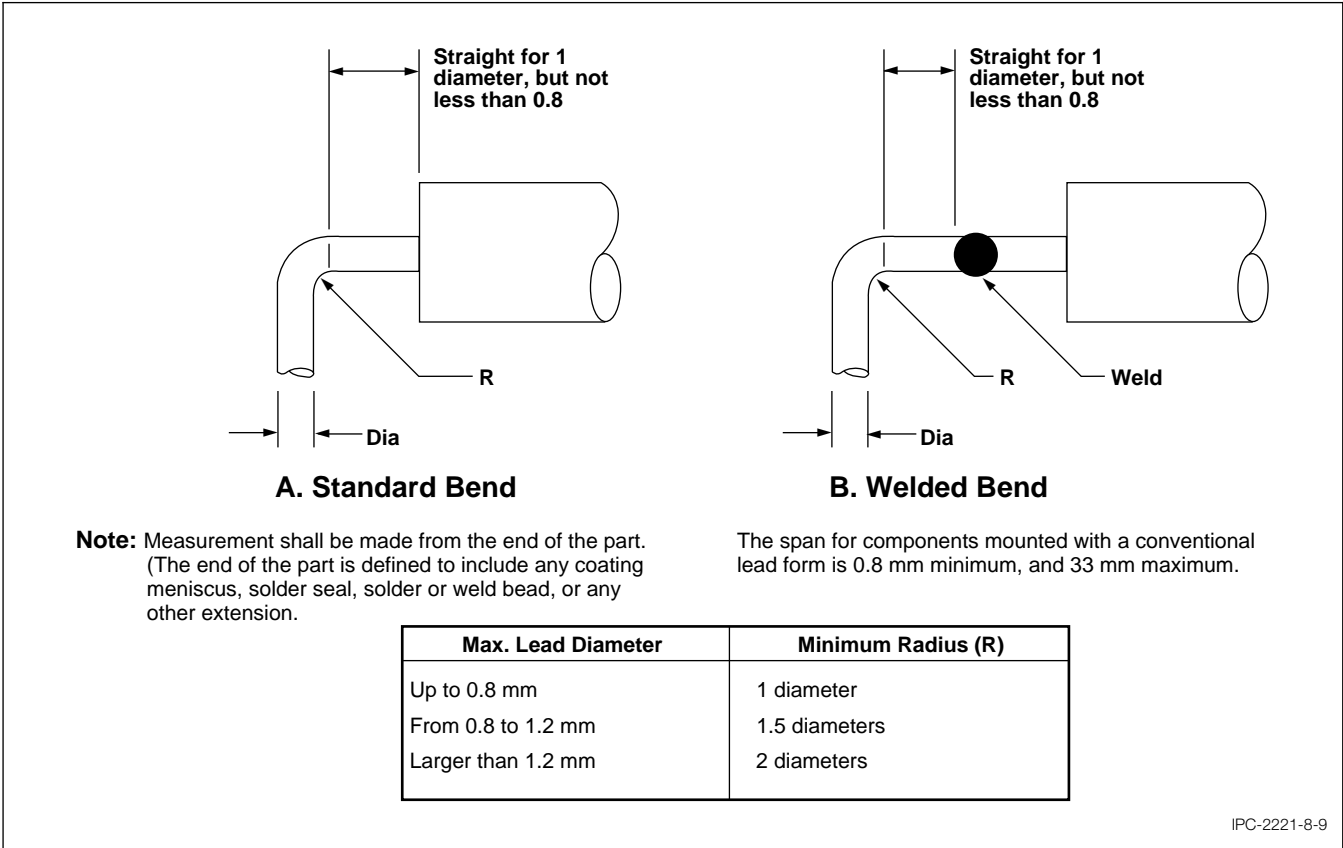
**Figure 8-8   Heat dissipation examples**



**Straight for 1 diameter, but not less than 0.8**

**Straight for 1 diameter, but not less than 0.8**

**R**

**R**          **Weld**

**Dia**

**Dia**

**A. Standard Bend**

**B. Welded Bend**

**Note:** Measurement shall be made from the end of the part. (The end of the part is defined to include any coating meniscus, solder seal, solder or weld bead, or any other extension.)

The span for components mounted with a conventional lead form is 0.8 mm minimum, and 33 mm maximum.

| Max. Lead Diameter | Minimum Radius (R) |
| --- | --- |
| Up to 0.8 mm | 1 diameter |
| From 0.8 to 1.2 mm | 1.5 diameters |
| Larger than 1.2 mm | 2 diameters |

IPC-2221-8-9

**Figure 8-9   Lead bends**

included. The inclusion of a pliable spacer material between the heatsink frame and the printed wiring board is an acceptable method for ensuring stress relief provided the resilient added material is of sufficient thickness (0.2 mm typical) to compensate for forces imposed during temperature change. Many of the pliable spacer materials tend to have low $T_g$ and high CTE characteristics, imparting more stress than no spacer at all.
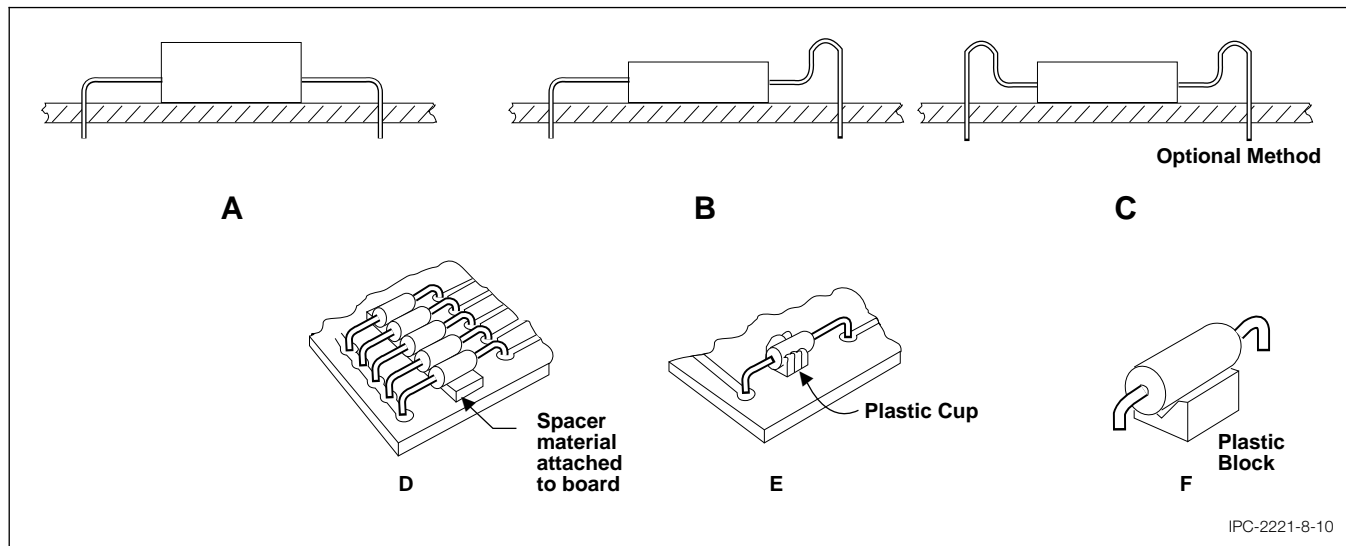
**Figure 8-10   Typical Lead configurations**

## 8.2   General Attachment Requirements

**8.2.1 Through-Hole**   For automatic assembly of boards with through-hole components, specific consideration should be given to providing the allowable clearances for the insertion and clinching of leads of the components. See Figure 7-1, 8.3.1 and IPC-CM-770 for specific details.

**8.2.2 Surface Mounting**   Design restrictions **shall** maintain appropriate clearances for the automatic pick-and-place equipment to position the parts in their proper orientation and allow sufficient clearances for the placement heads (see IPC-SM-780). Clearances should be provided to allow for inspection of solder joints wherever possible (see IPC-SM-782).

**8.2.3 Mixed Assemblies**   Automatic processes used for both surface mounted and through-the-board mounted components require special design considerations in order that the components assembled in the first phase of the assembly do not interfere with insertion heads during the second phase.

Component placement **shall** consider the stresses that are put on the board with insertion equipment, by isolating parts wherever possible to specific areas so that the second phase insertion/ placement stresses do not impact previously soldered connections.

**8.2.4 Soldering Considerations**   Components used **shall** be capable of withstanding soldering temperatures used in the assembly process. Although the components are exposed to these temperatures for relatively short periods of time, due to the thermal capacity of the printed board assembly, component case temperatures remain near these temperatures for longer periods of time. Therefore avoid

through hole mounted components not capable of withstanding the following examples:

1. The wave soldering environment (260°C for one minute)

2. Surface mounted components in vapor phase environments (profile 216°C for four minutes)

3. Surface mounted components in other processes (profile 216°C for up to one minute)

When design restrictions mandate mounting components incapable of withstanding soldering temperatures, such components **shall** be mounted and hand-soldered to the assembly as a separate operation or **shall** be processed using an approved localized reflow technology.

Surface mounted components mounted to the bottom surface of assemblies intended to be wave soldered must be capable of resisting immersion in 260°C molten solder for 5 seconds. In addition, preheat is limited due to sensitivity of the underlying board substrate, so up to 120°C of thermal shock can be expected when components enter the solder wave.

**8.2.5 Connectors and Interconnects**   One of the major advantages of using printed board assemblies, as opposed to other types of component mounting and interconnection methods, is their ability to provide ease of maintainability. Devices (connectors) have been developed to provide the desired mechanical/electrical interface between the printed board assemblies, or between a printed board assembly and discrete interconnection wiring.

Board size and weight are important factors in choosing connector mounting hardware, and in deciding whether the board will be mounted horizontally or vertically. It is common practice to mount a connector either to a mother board

or to board racks or frames, and then insert the component board into the connector using appropriate guiding and support mechanisms. In general, if the assembly is to encounter a great deal of vibration, the board should be attached to a connector or supported by mechanical means other than relying on contact friction to provide the mechanical interface.

Connectors may be mounted to the printed board by soldering, welding, crimping, press fitting or other means. Leads may be extended through holes or contact maybe made to lands provided on the board. Holes may be plated through or simply drilled. The exact method will depend on the connector design.

**8.2.5.1 One-Part Connectors** One part connectors provide the female receptacle for communication between the printed board with an edge-board connector and its environment.

If low signal levels, or frequent mating, or adverse environmental conditions are anticipated, the contacts should be gold plated. Whenever it is possible to install a connector on the printed board two different ways, or install a connector on the wrong board, a key **shall** be provided in the contact field (see Figure 8-13).

**8.2.5.2 Dual In-line Connectors** In-line printed wiring board connectors may be mounted in full contact with the printed wiring board. Connectors mounted in full contact with the printed board **shall** be designed so that there are both stress relief provisions internal to the connector body and cavities (either visible or hidden) which preclude blocking of plated through-holes.

**8.2.5.3 Edge-Board Connectors** Edge-board connectors use one edge of the printed board as the plug dielectric with printed/plated conductors as the male contacts.

The width of the printed board edge (tang) that mates with the one-part connector ("T" of Figure 8-11), **shall** be dimensioned in such a manner that when T reaches its maximum dimension (MMC), the size of the tang will be no greater than the minimum throat of the one-part connector. (See 5.4.3 for establishing connector circuit pattern.) In addition, it will be necessary to provide for special processing of the board tang to accommodate the mating of the board's edge contacts with the one-part connector in order to permit ease of mating and prevent undue wear or damage of the board. This consists of beveling (chamfering) the leading edge and corners of the board tang (see Figure 8-12). The uneven tang configurations shown in Figure 8-12 enable some connections to be made, or broken, before others. As an example, applying power before making signal connections.

Whenever it is possible to install a connector on the printed board two different ways, or install a connector on the wrong board, keying slots **shall** be cut into the board to be used with keying devices in the connector to ensure proper installation (see Figure 8-13).

If low signal levels, or frequent mating, or adverse environmental conditions are anticipated, the contacts should be gold-plated.

**8.2.5.4 Two-Part Multiple Connectors** Two-part multiple connectors consist of self-contained multiple contact plug and receptacle assemblies. Usually, although not always, the receptacle is an unmoveable connector assembly which mounts to an interconnection-wiring backplane (motherboard) or chassis (see Figure 8-14). Each connector half may have either male or female contacts. For safety, the receptacle usually contains female power contacts.

**8.2.5.5 Two-Part Discrete-Contact Connectors** Two-part discrete-contact connectors that consist of individual plug (male), and receptacle (female) contacts are mounted directly to the printed board, usually without being part of molded dielectric assemblies.

**8.2.5.6 Edge-Board Adapter Connectors** Edge-board adapter connectors may be used in lieu of printed/plated conductors as the male contacts (see Figure 8-15). These connectors eliminate many of the problems associated with the edge-board connectors, such as varying board thicknesses and board warping problems. Use of these connectors does not require special printed board processing, e.g., gold plating of contacts or tang chamfer on the printed board.

It is important to be sure that the method of mounting is sufficiently strong to withstand the forces of mating and withdrawal.

When one part of the connector is mounted to a printed board backplane using press-fit technology, the backplane should be designed in accordance with the guidelines of IPC-D-422.

**8.2.6 Fastening Hardware** The installed location and installation orientation for fastening hardware **shall** be prescribed on the assembly drawing for such devices as rivets, machine screws, washers, inserts, nuts and bracketry. Specifications and precautions of tightening torques **shall** be provided wherever general assembly practice might be inadequate or detrimental to the assembly's structure or functioning. The use of such hardware should be in accordance with the clearance requirements of this section.
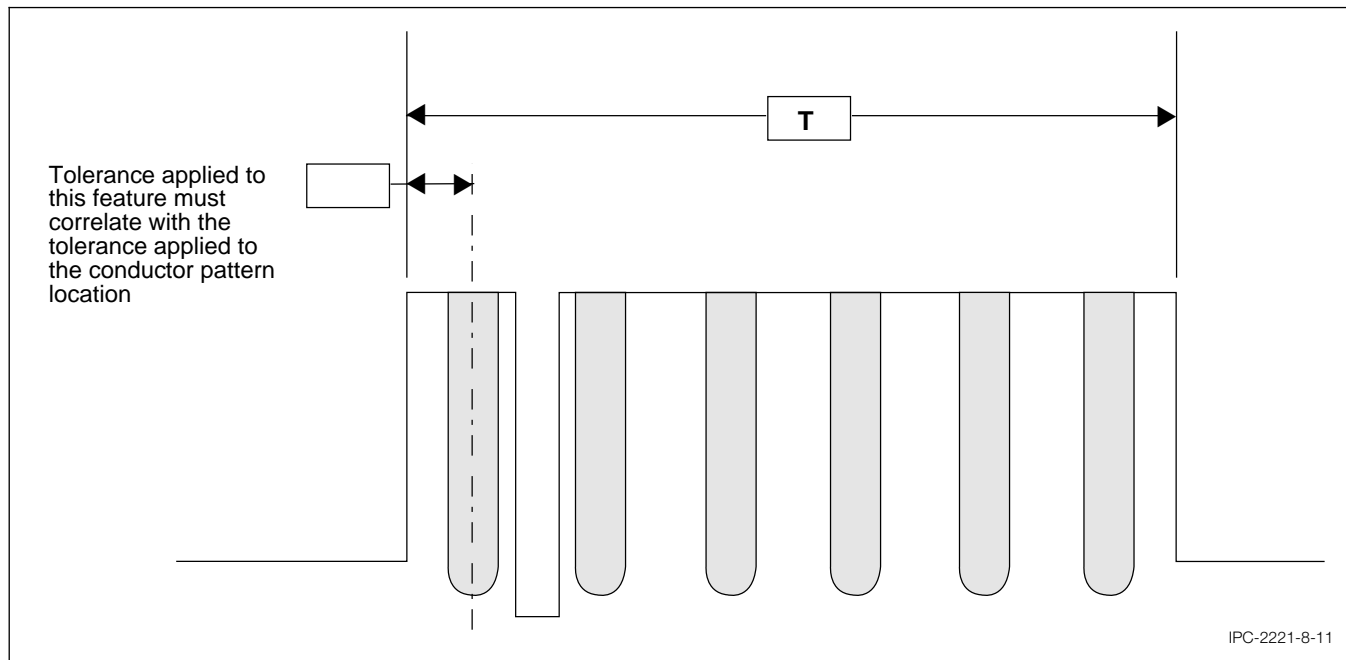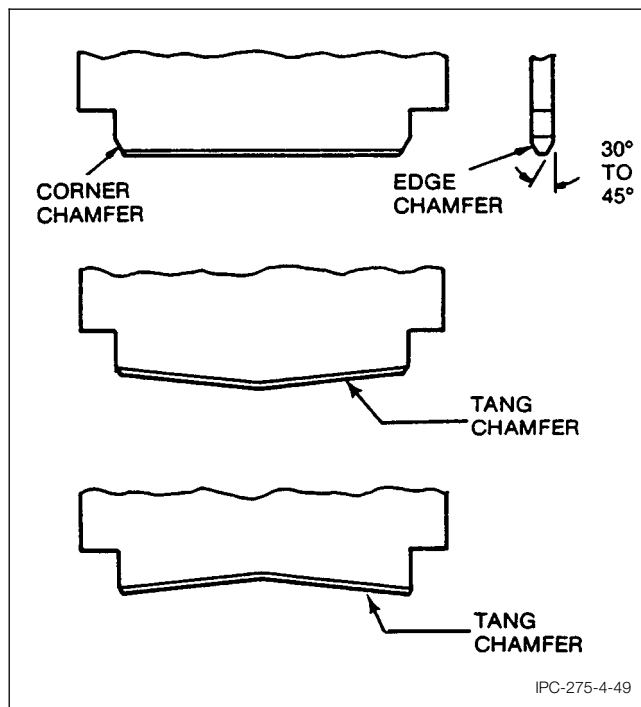
**Figure 8-11    Board edge tolerancing**

Tolerance applied to this feature must correlate with the tolerance applied to the conductor pattern location



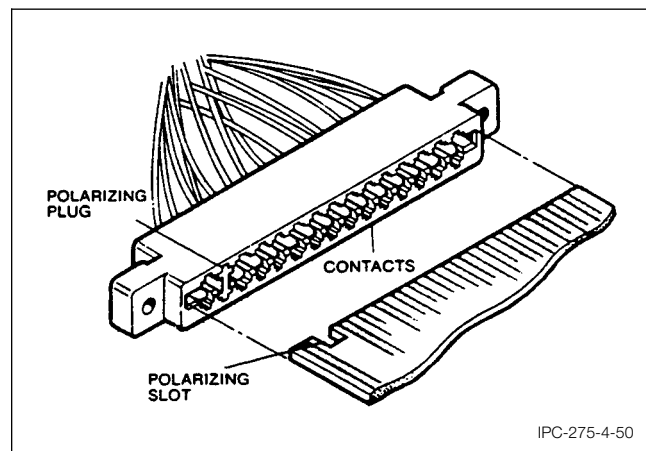**Figure 8-12    Lead-in chamfer configuration**



**Figure 8-13    Typical keying arrangement**

is soldered using flow solder process, the board typically must be held flat by flow solder fixtures.

Adequate physical and electrical clearance must be provided between stiffeners, conductors, and components. Fiber or plastic insulators should be incorporated where adequate clearance from circuitry cannot be provided.

During the fabrication process of large printed boards, a physical bow and/or twist of the board occasionally occurs. The magnitude of these phenomena can normally be controlled by balancing the metal planes in multilayer printed boards, and adhering to proven fabrication processes. However, cases have been experienced whereby large unsupported printed boards may warrant special stiffening to reduce the degree of bow particularly during flow solder assembly process.

**8.2.7 Stiffeners**  Stiffeners are designed into the board to provide rigidity to the assembly and prevent flexing of the circuitry which could cause solder and copper foil cracking during mechanical stress.

Stiffeners may be fabricated from aluminum, steel having an adequate protective finish, plastic or fiber reinforced material. Stiffeners may be attached to the board with solder or by fasteners (rivets, nuts and bolts). If the stiffener

**Figure 8-14   Two-part connector**
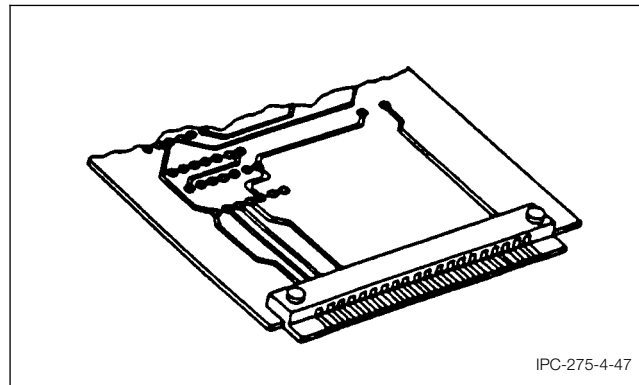


**Figure 8-15   Edge-board adapter connector**

The following is to be used as a general design guide for establishing the mechanical characteristics of the subject stiffening member(s).

$$E = \frac{E^1 h^3}{I} \frac{W_o\,(a + 5)}{300Z}$$

$E$ = Young's modulus of stiffener material (lb./inch$^2$)

$I$ = Moment of inertia (lb. inch$^2$)

$E^I$ = Flexural modulus of elasticity of the printed board base material (lb./inch$^2$)

$h$ = Thickness of the printed board (inch)

$W_o$ = Initial offset of the printed board, due to bow (inch)

$a$ = Dimension of the printed board, in the direction of bow (inch)

$Z$ = Allowable offset of the printed board after the stiffening member is added (inch)

Provision for the addition of stiffening member(s) should be provided to otherwise unsupported printed boards (typically larger than 230 mm as measured along the printed board connector side). To allow for proper engagement of the printed board connector, the stiffener should be adjacent to the printed board connector(s).

**8.2.8 Lands for Flattened Round Leads**   Flattened round (coined) leads **shall** have a land which will provide the seating so that the heel and the terminal relationship is in accordance with Figure 8-16. Lead and land size should be designed so that a minimum side overhang may occur. (Class 3 product allows for a manufacturing process allowance of up to 1/4 of the lead diameter to overhang.)

A manufacturing allowance for toe overhang is acceptable provided it does not violate the minimum designed conductor spacing. If flattened leads are used, the flattened thickness **shall** not be less than 40% of the original diameter (see J-STD-001).

**8.2.9 Solder Terminals**   Single-/double-ended, or single-/multi-sectioned turret solder terminals may be used to facilitate the installation of components, jumper wires, input/output wiring, etc. The wires or leads of components **shall** be soldered to the posts of the solder terminals.

Eyelets and solder terminals are to be considered components and specified on the assembly drawing or a subassembly drawing for board fabrication.

**8.2.9.1 Terminal Mounting-Mechanical**   Solder terminals that are not connected to conductive patterns or copper planes **shall** be of the rolled flange configuration (see Figure 8-17A).

**8.2.9.2 Terminal Mounting-Electrical**   For printed boards or printed board assemblies, solder terminals **shall** be of the flange configuration shown in Figure 8-17B. The terminal **shall** be approximately perpendicular to the board surface and may be free to rotate.

Flat body flanges **shall** be seated to the base material of the printed board and not on ground planes or lands. Flared flanges **shall** be formed to an included angle between 35 and 120 degrees and **shall** extend between 0.4 mm and 1.5 mm beyond the surface of the land provided minimal electrical spacing requirements are maintained (see Figure 8-17B) and the flare diameter does not exceed the diameter of the land.

Terminals should only be mounted in unsupported holes or in plated-through holes in Type 2 boards with a nonfunctional land on the component side (see Figure 8-17B). If it is essential that a terminal be utilized for interfacial connection, on Type 3 through Type 6 (inclusive) boards, a
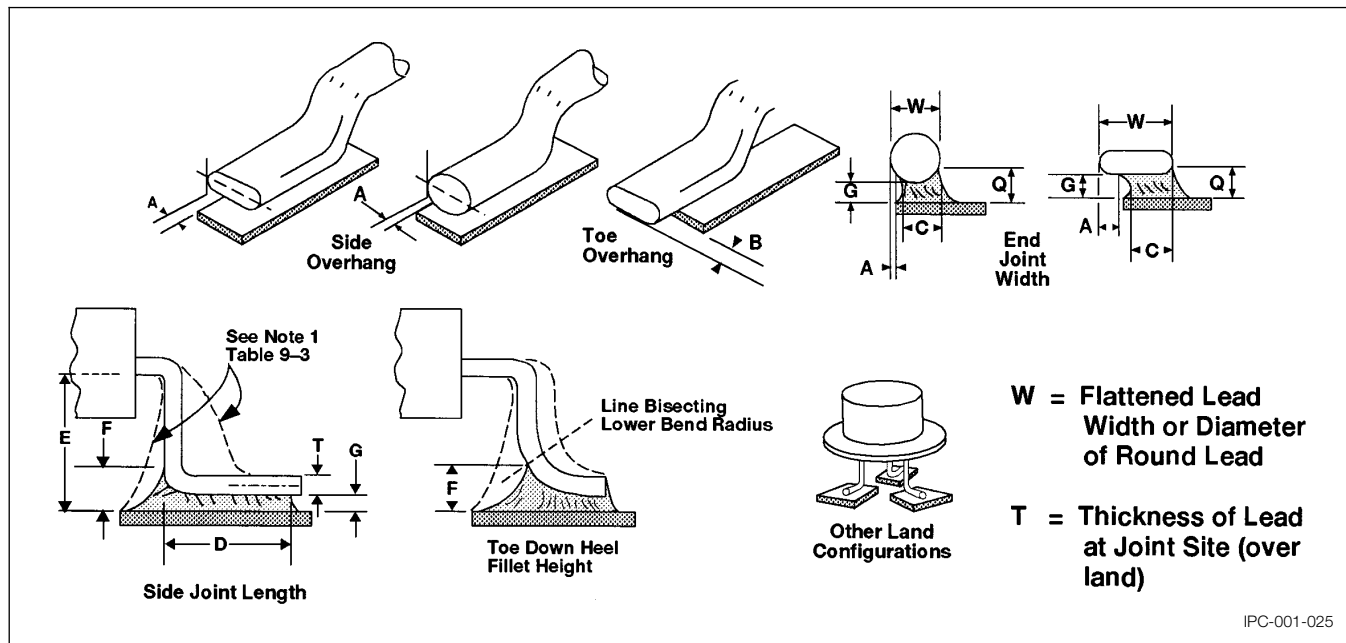
**Figure 8-16   Round or flattened (coined) lead joint description**
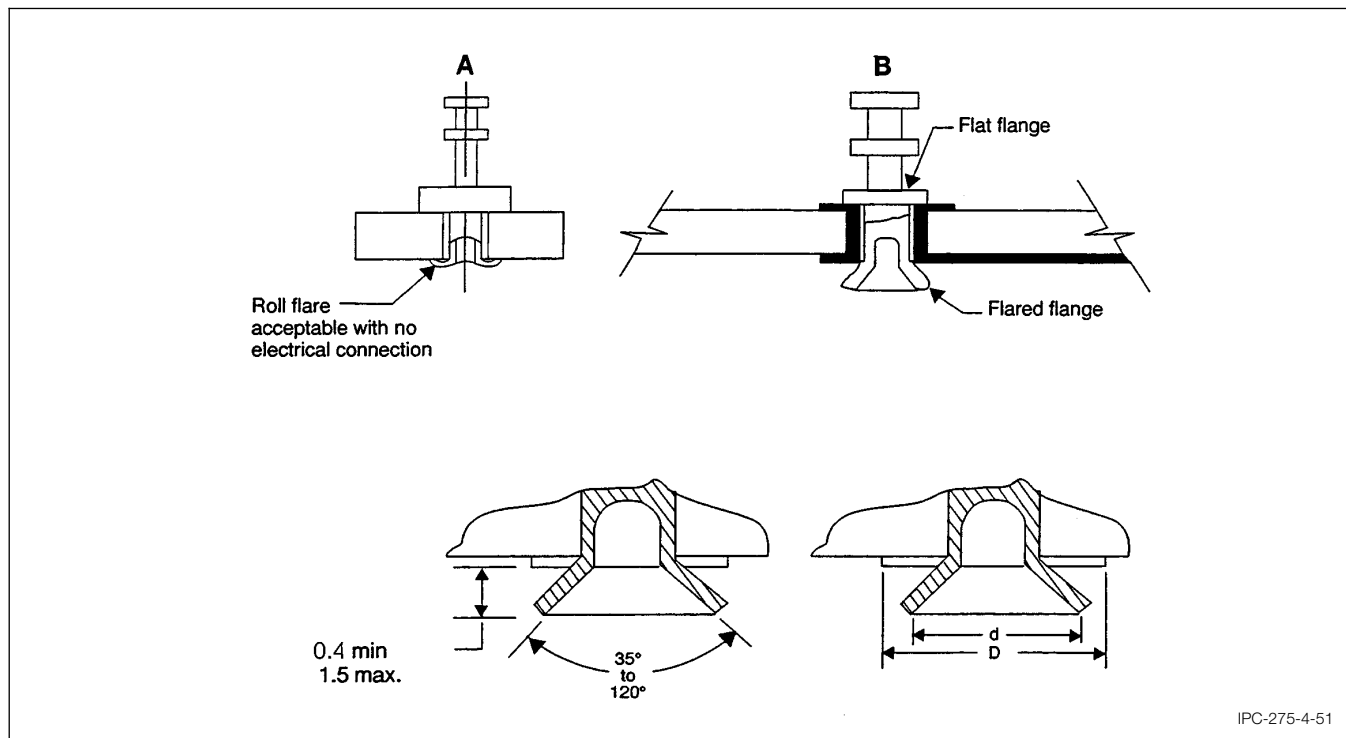


**Figure 8-17   Standoff terminal mounting, mm**

dual hole configuration incorporating a supported plated-through hole **shall** be combined with the terminal hole interconnected by a land on the solder side of the printed board (see Figure 8-18).

**8.2.9.3 Attachment of Wires/Leads to Terminals**  In cases in which more than one wire is attached to a termi-

nal, the largest diameter wire should be mounted to the bottom-most post for ease of rework and repair. No more than three attachments should be made to each section of a turret of bifurcated terminal. As an exception, bus bar terminals (see sectional standards for more information) may hold more than three wires or leads per section when specifically designed to hold more.
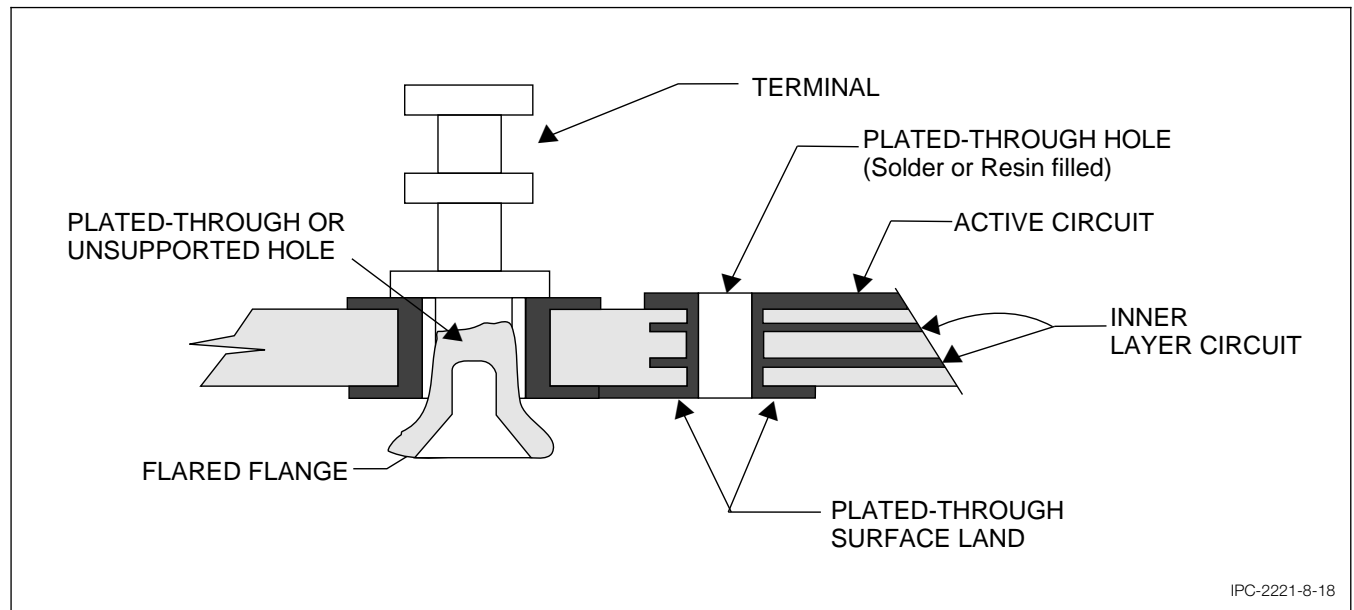
**Figure 8-18    Dual hole configuration for interfacial and interlayer terminal mountings**

**8.2.10  Eyelets**  The requirements for the use of eyelets on printed boards are similar to those for solder terminals. The criteria for their use should be provided by the assembly drawing.

Interfacial connections **shall** not be made with eyelets. Eyelets installed at an electrically functional land **shall** be required to be of the funnel flange type.

**8.2.11  Special Wiring**

**8.2.11.1  Jumper Wires**  It may be necessary to include point-to-point wiring to a printed board as a part of the original design. Such wiring **shall** not be considered as being part of the printed board, but as part of the board assembly process, and considered as components. Therefore, their use **shall** be documented on the printed board assembly drawing.

Jumper wires **shall** be terminated in holes, on lands or standoffs. Jumper wires **shall** not be applied over or under other replaceable components (including uninsulated jumper wires).

Jumper wires **shall** be permanently fixed to the printed board at intervals not to exceed 25 mm. Jumper wires less than 25 mm length whose path does not pass over conductive areas and does not violate the spacing requirements may be uninsulated. Insulation, when required on jumper wires, **shall** be compatible with the use of any conformal coatings. When using non-sealed wire insulation, consider the assembly cleaning process.

**8.2.11.2  Types**  Point-to-point (jumper) wires are usually of the following types:

- Bare bus wire that consists of a single strand of wire that is of sufficient cross-section to be compatible with the electrical requirements of the circuit without the use of sleeving or other insulation.

- Sleeved bus wire that consists of a single-strand of bare buswire (see above) that is covered by insulation tubing.

- Insulated bus wire that consists of a single-strand wire purchased with its own insulation, such as varnish coating.

- Insulated stranded wire that consists of multiple strands of wire purchased with an insulating material, such as a polymer coating.

**8.2.11.3  Application**  The use of jumper wires **shall** adhere to the following rules:

- Bare bus wires should not be longer than 25 mm.

- Bare bus wires **shall** not cross over board conductors.

- Bend radii for jumper wires should conform to that of normal component bend requirements (see 8.1.11).

- The shortest X-Y path of jumper routing should be used unless board design considerations dictate otherwise.

Sleeving **shall** be of sufficient length to ensure that its slippage at either end of the jumper wire will not result in a gap between the insulation and solder connection or wire bend that violates minimum electrical clearance distances. Also, the sleeving chosen **shall** be able to withstand the jumper wire or printed board soldering operations.

**8.2.12  Heat Shrinkable Devices**  Heat shrink soldering devices are typically used to terminate shields on cables. The devices are composed of a solder ring enclosed in a

solder sleeve insulator. The device is placed over the terminations to be soldered and heated with a hot air device. The heat melts the solder to form a joint and simultaneously encases the connection in insulation. Heat shrinkable devices may be self-sealing and may encapsulate the entire solder connection.

Solder sleeves compose a unique category because they form a portion of the design, yet are not integral to the printed wiring board.

**8.2.13 Bus Bar**  Bus bars are usually in the form of pre-formed components that are part of the printed board assembly and serve the function of providing most, if not all, of the power and ground distribution over the board surface. Their use is primarily to minimize the use of board circuitry for power and ground distribution and/or to provide a degree of power and ground distribution not cost-effectively provided by the printed board.

The number of conductor levels in the bus bar, the type and number of their terminals, the size and finish of their conductors, and the dielectric strength of their insulation depends on the application. However, these parameters should be clearly defined on the procurement document for these parts. Whenever possible, their interface with the printed board should be at plated-through holes, while conforming to conventional lead size-to-hole and lead bending requirements (see 8.1.11). Also, for optimum board design efficiency, the bus bar terminals should interface with the board on a uniform termination pattern, may share the same holes as an integrated circuit and may be placed under an integrated circuit.

**8.2.14 Flexible Cable**  When flexible cable becomes part of a printed board, the terminations **shall** be accomplished in a manner that imposes no undue stress on the cable/printed board interconnection.

Sometimes this interconnection uses pins, where a pin passes through the board and the flexible cable to provide the proper interconnection. At other times, the flexible cable may be surface soldered directly to land patterns on the printed board or may be integral to the printed board as in rigid-flex applications. Proper mechanical support, using tie-down bars, or adhesives, **shall** be used to prevent stresses on the solder joints.

**8.3 Through-Hole Requirements**  For automatic assembly of boards with components whose leads pass through the board, specific consideration should be given to providing the allowable clearances for the insertion and clinching of leads of the components. See 8.3.1 through 8.3.1.5 and IPC-CM-770 for specific details.

**8.3.1 Leads Mounted in Through-Holes**  Part attachment **shall** be described on the assembly drawing following the methods specified herein. Requirements for lead-to-hole relationships are detailed in s 9.2.3 through 9.3 of the related design sectional. Component leads, jumper wires and other leads **shall** be mounted such that there is only one lead in any one hole except as specified in 8.2.13. Component leads in unsupported holes **shall** be required to extend a minimum of 0.5 mm and a maximum of 1.5 mm from the surface of the plating or foil. As a minimum the lead **shall** be discernible in the completed solder connection. The lead should not extend more than 1.5 mm (measured vertically) from the printed board surface, and the lead must not violate minimum electrical spacing requirements.

**8.3.1.1 Straight Through-Hole Mounted Leads**  The straight-through leads on connectors or other devices with tempered leads may extend from 0.25 mm to 2.0 mm, provided there is no electrical or mechanical interference.

**8.3.1.2 Unclinched Leads**  Unclinched leads, straight or partially bent for retention **shall** be soldered in component holes or eyelets in accordance with J-STD-001 as applicable. (See IPC-CM-770.)

**8.3.1.3 Clinched Leads**  When maximum mechanical retention of a lead or terminal is required by design, the lead or terminal **shall** be clinched. Component holes may be plated-through holes, unsupported holes, or eyeletted holes. Clinching requirements **shall** be defined on the assembly drawing. The lead end **shall** not extend beyond the edge of its land, or its electrically connected conductor pattern, if it violates the minimum spacing requirements. Partial clinching of leads for part retention **shall** be considered under the requirements of 8.3.1.4 (see Figure 8-19).
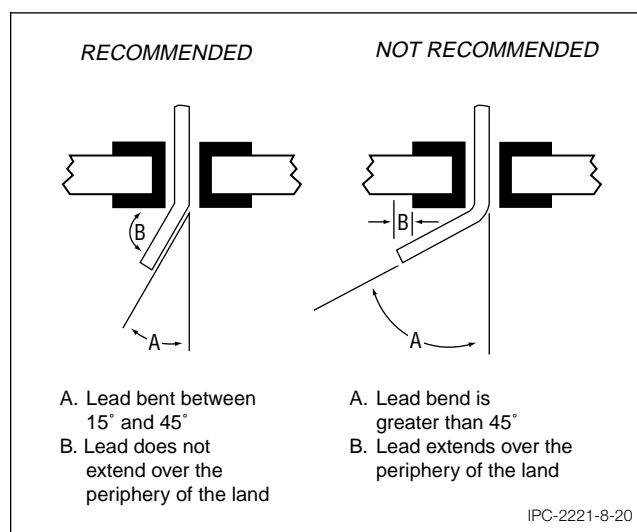


**Figure 8-19   Partially clinched through-hole leads**

Clinched leads are not applicable for tempered pins or for leads over 1.3 mm in diameter.

**8.3.1.4 Partially Clinched** Partially clinched leads are typically bent between 15 degrees to 45 degrees as measured from a vertical line perpendicular to the board. Partially clinched lead terminations **shall** not be used for manually inserted components except on diagonally opposite corner pins of dual in-line packages (DIPs) (see Figure 8-19).

**8.3.1.5 Dual In-line Packages** Leads on DIPs may be clinched in either direction for part retention. Clinch angle should be limited to 30 degrees from the lead's original centerline. The clinch may be limted to two leads per side (four leads per part). See Figure 8-20.

Dual in-line packages may be surface mounted provided the leads are intended for surface mount applications. For applications in which severe thermal stress is evident and the board provides the thermal management function, butt mounted packages **shall** not be used.

**8.3.1.6 Axial Leaded Components** Axial leaded components **shall** be mounted as defined in 8.1.14. Lead bends **shall** be stress relieved as identified in that general paragraph. See Figure 8-2 for component body centering and Figure 8-9 for lead bend extensions.

The leads of components mounted horizontally with bodies in direct contact with the printed board **shall** be formed to ensure that excess solder is not present in the formed bends of the component leads (see Figure 8-21). Solder may be present in the formed bends of axial-leaded components provided that it is a result of normal lead interface wetting action and that the topside bend radius is discernible. Solder **shall** not extend so that it contacts the component body (see J-STD-001).

**8.3.1.7 Radial-Lead Components**

A. *Radial-Lead Components (2 Leads)* - Radial-leaded components vary in lead spacing. The design lead spacing is generally a function of the spacing at which the leads exit the body of the component (see Figure 8-22) and the nearest grid intersection.

Dual-lead components of configurations A through E of Figure 8-22 should be mounted freestanding with the larger sides perpendicular to the board surface within 15 degrees as shown in Figure 8-23 when:
- Angularity is required for clearance in the next higher assembly; or
- That edge of the body nearest the surface of the board parallels the board surface within 10 degrees and is no less than 1.0 mm and no more than 2.3 mm from the surface. Components of configurations F through J of Figure 8-22 are not included under the angularity exception.

Radial-leaded components with coating meniscus on one or more leads should be mounted such that there is visible clearance between the meniscus and the solder fillet. Trimming of the meniscus is prohibited (see Figure 8-24).

B. *Radial-Leaded Components (3 or more Leads)* - Radial-leaded components with three or more leads vary in lead spacing. The design lead spacing is generally a function of the spacing at which the leads exit from the body of the component (see Figure 8-25) and the nearest pattern of grid intersections that provides for suitable conductor routing.

C. *Class 3 High Reliability Requirements* - For Class 3 high reliability applications, components **shall** be mounted freestanding (i.e., with the base surface separated from the surface of the board with no support other than the component leads) only if the weight of



**Axis of Hole**
**30° Max.**

IPC-2221-8-20a
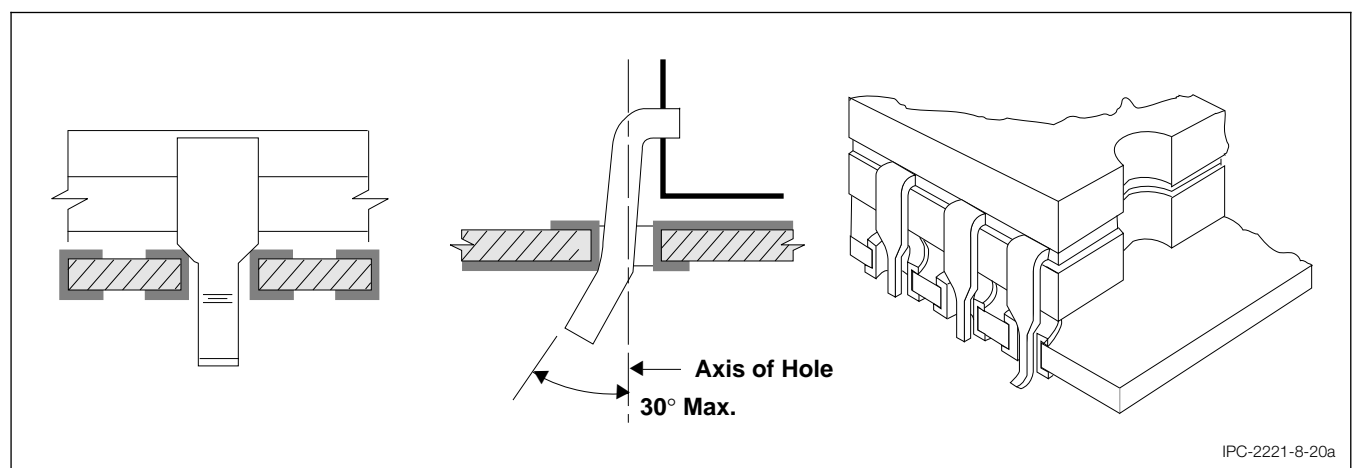
**Figure 8-20   Dual in-line package (DIP) lead bends**
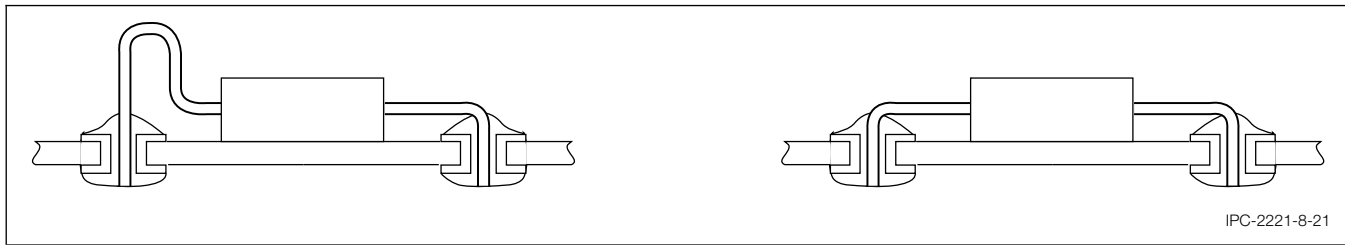
**Figure 8-21   Solder in the lead bend radius**
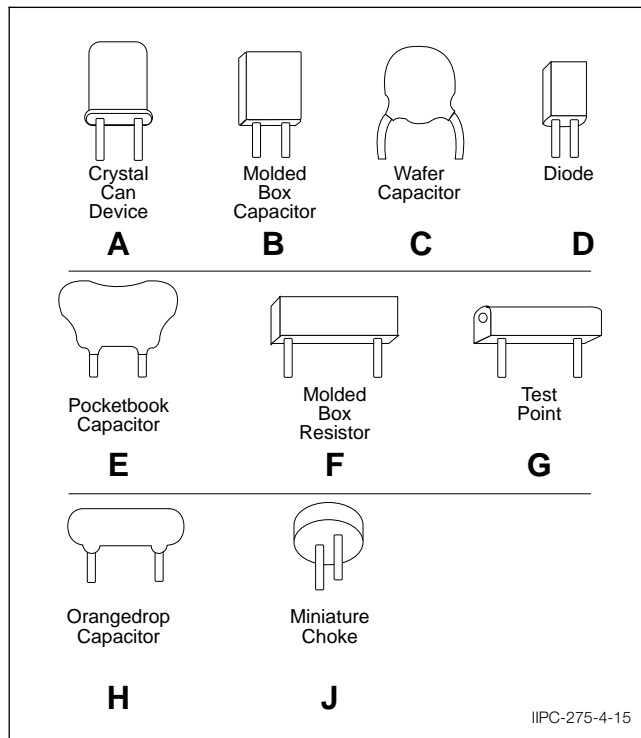


**Figure 8-22   Two-lead radial-leaded components**
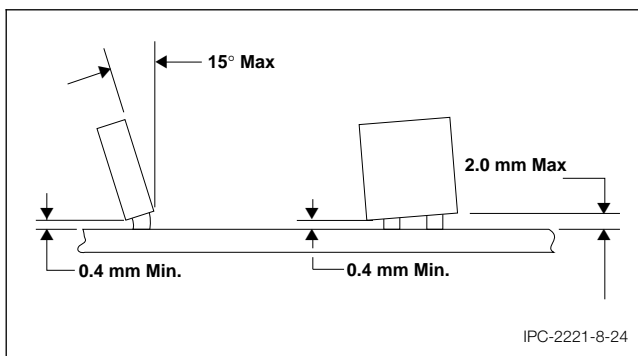


**Figure 8-23   Radial two-lead component mounting, mm**



**Figure 8-24   Meniscus clearance, mm**
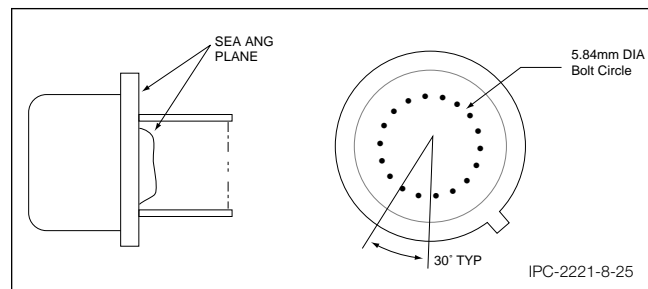


**Figure 8-25   "TO" can radial-leaded component, mm**

the component is 3.5 gm per lead or less. When components have an integral seating plane, the seating plane may be in contact with the board. When components are mounted freestanding, the spacing between the surface of the component and the surface of the board **shall** be a minimum of 0.25 mm and a maximum of 2.5 mm.

In no instance **shall** non-parallelism result in nonconformance with the minimum or maximum spacing limit.

**8.3.1.8  Perpendicular (Vertical) Mounting**  Axial-leaded components weighing less than 14 grams may be mounted on the assembly using vertical mounting criteria that have the major axis of the component body perpendicular to the board surface. The space between the end of the component body (or lead weld) and the board **shall** be a minimum of 0.25 mm. Height restriction for general component mounting normally pertains to axial-leaded components mounted vertically. In general, the profile of components should be kept as low as possible to the surface of the board. A maximum allowable vertical height from the board mounting surface should be 15 mm, see Figure 8-26.

**8.3.1.9  Flat-Packs**  Flat-pack components normally have flat ribbon leads that exit from the component body on 1.27 mm lead centers (see Figure 8-27). Forming of the leads
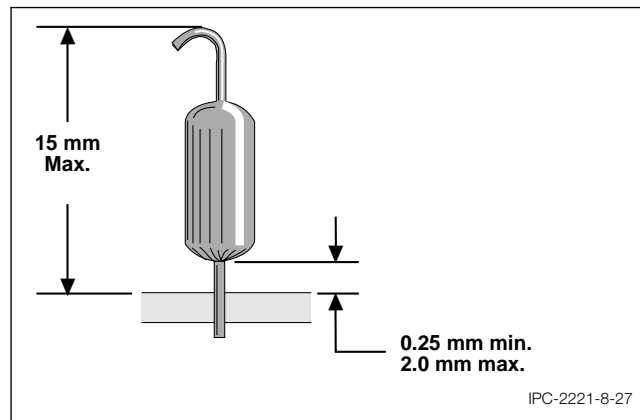
**Figure 8-26   Perpendicular part mounting, mm**

may be required to prevent stressing the lead exit at the component body, especially for through-hole mounted applications (see Figure 8-28). An off-board clearance of 0.25 mm minimum is required for cleaning purposes.
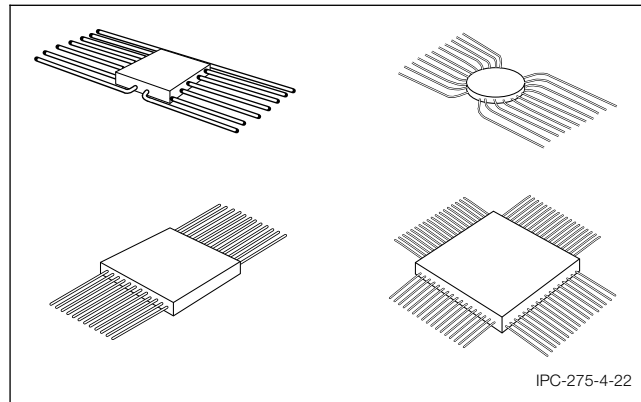


**Figure 8-27 Flat-packs and Quad Flat-packs**
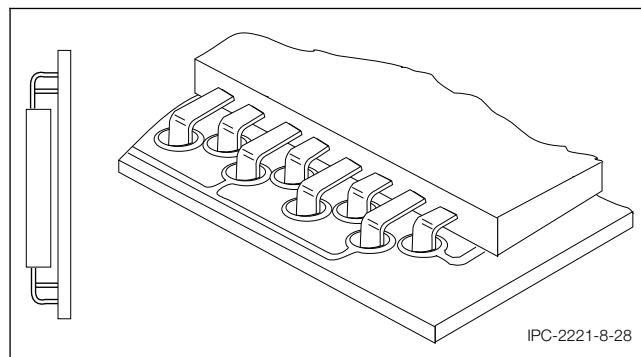


**Figure 8-28   Examples of configuration of ribbon leads for through-hole mounted flat-packs**

The body of the component **shall** not be in contact with any vias unless the vias are coated per 8.1.10 Leads **shall** extend from the body of the part a minimum of one lead diameter or thickness but not less than 0.8mm from the body or weld before the start of the bend radius (see Figure 8-9 and J-STD-001).

**8.3.1.10 Metal Power Packages** Metal power package configurations (TO-3 to TO-66, etc.) **shall** not be mounted free standing. Stiffeners, heatsinks, frames and spacers may be utilized to provide needed support.

Metal power packages with leads that are neither tempered nor greater than 1.25 mm (compliant leads) may be terminated in plated-through holes or with through-the-board terminations. With through-the-board terminations the leads **shall** be provided with stress relief (see Figure 8-29).
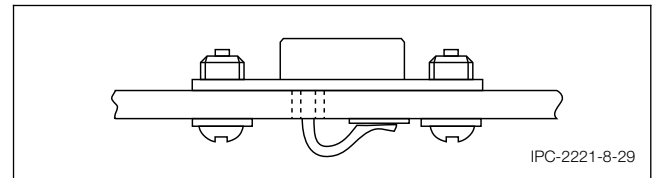


**Figure 8-29   Metal power packages with compliant leads**

With plated-through hole terminations the package **shall** be mounted off the board and spacers used to provide stress relief for the leads (see Figure 8-30). Side mounting may also be employed.
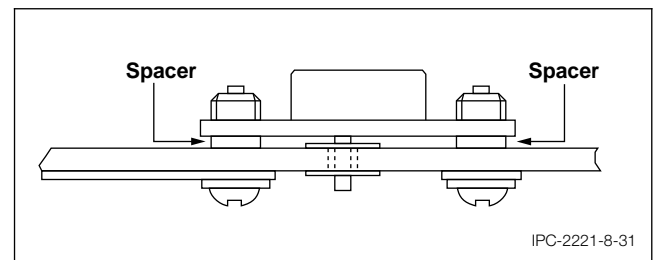


**Figure 8-30   Metal power package with resilient spacers**

Metal power packages with noncompliant leads may also be mounted with the leads terminated in plated-through holes or with through hole termination. The requirements for plated-through hole terminations **shall** be the same as those for packages with compliant leads (see Figure 8-30). For through-the-board terminations, the leads **shall** be terminated to the board by jumper connections (see Figure 8-31). The termination of the jumper to the board **shall** be made either to a plated-through hole or to a land.
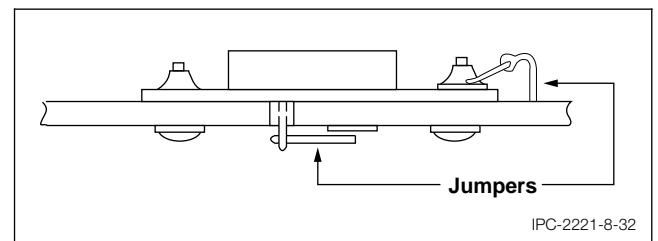


**Figure 8-31   Metal power package with non-compliant leads**

Care must be exercised when the mounting utilizes spacers to ensure that any electrical connection between the component case and the board circuitry remains constant under all operating conditions.

Whenever the terminations are made in plated-through holes, the mounting **shall** ensure that the connections can be cleaned between the component and the board. Metal power packages, the standoffs, heatsink frames, and resilient spacers on which metal power packages are mounted **shall** be of configurations which do not block plated through-holes, preclude excessive stresses (provide stress relief), and facilitate cleaning.

**8.4 Standard Surface Mount Requirements** Automatic assembly considerations for surface mounted components are driven by pick-and-place machines used to place/position chip components, discrete chip carriers, small outline packages, and flat packs. Printed board designs **shall** maintain appropriate clearances for the automatic pick-and-place equipment to position the parts in their proper orientation and allow sufficient clearances for the placement heads. (See IPC-SM-780).

Typically, fine pitch devices could be between 250 and 775 $mm^2$ case size for automatic placement without vision. Generally, the largest component that can be placed with vision alignment is 1300 $mm^2$, measured to the outside of the leads. Large packages exaggerate the effects of the thermal mismatch between the component and substrate. Normally, the minimum size leadless component that can be placed with automatic equipment is 1.5 mm nominal length by 0.75 mm nominal width. Smaller components require high placement accuracy. Vacuum pickup with standard equipment is also difficult.

Avoid extremely small passive components. Leadless passive components should have an aspect ratio greater than one and less than three. High aspect ratio parts tend to fracture during soldering. Square devices (aspect ratio = 1) are difficult to orient.

Smaller components are easier to solder, but footprints must be large enough to permit reliable placement of adhesive without smearing onto the conductor. Avoid components which require mounting land spacings (on the same component) closer than 0.75 mm, due to process limitations on applying (chip bonding or thermal adhesive). High profile SMT components (higher than 2.5 mm) interfere with wave solder flow to adjacent components, and should be avoided.

Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled surface mounted part. Techniques may include special symbols, or special land configurations to identify such characteristics as pin 1 of an integrated circuit package.

**8.4.1 Surface-Mounted Leaded Components** The requirements and consideration of 8.1.14 apply to the surface-mounting of leaded components. Lead forming is a major design consideration. Custom lead forms should be described on the assembly drawing to provide for lead stress relief to ensure fit to the land pattern to allow under-body clearance for cleaning, and to provide any designed-in provisions for thermal transfer (see Figure 8-32). (See IPC-SM-782.)

Axial leaded components may be surface mounted provided the leads are coined (see Figure 8-33). However, they may never be surface mounted in a perpendicular orientation (see Figure 8-26).

**8.4.2 Flat-pack Components** Flat-pack components normally have flat ribbon leads that exit from the component body on 1.27 mm lead centers (see Figure 8-34). Although they generally have from 14 to 16 leads, flat-packs with up to 50 leads are available.

When planar mounted flat-packs require lead forming, the leads **shall** be configured as shown in Figure 8-34. Non-insulated parts mounted over exposed circuitry **shall** have their leads formed to provide a minimum of 0.25 mm between the bottom of the component body and the exposed circuitry. The maximum clearance between the bottom of the leaded component body and the printed wiring surface should be 2.0 mm. Parts insulated from circuitry or over surfaces without exposed circuitry may be mounted flush. If the component requires thermal transfer to the board, special consideration for cleaning should be given.

**8.4.3 Ribbon Lead Termination** Flat-wire ribbon leads may be attached to lands on the printed board (see Figure 8-35). Connections **shall** be made by soldering or wire bonding only.

**8.4.4 Round Lead Termination** In some instances, components with round leads may be attached to the surface lands without first passing through a hole. The land **shall** be designed with the proper shape and spacing to comply with proper soldering techniques. Components with axial leads of round cross-section may be coined or flattened to provide positive mounting (see Figure 8-33).

**8.4.5 Component Lead Sockets** Component lead sockets may be allowed for Class 3 high reliability requirements when engineering analysis proves acceptable. Care should be taken in specifying the use of non-noble platings or finishes on either sockets or the component leads because of the possibility of producing inherent heat or open circuits due to fret corrosion during vibration or temperature cycling.
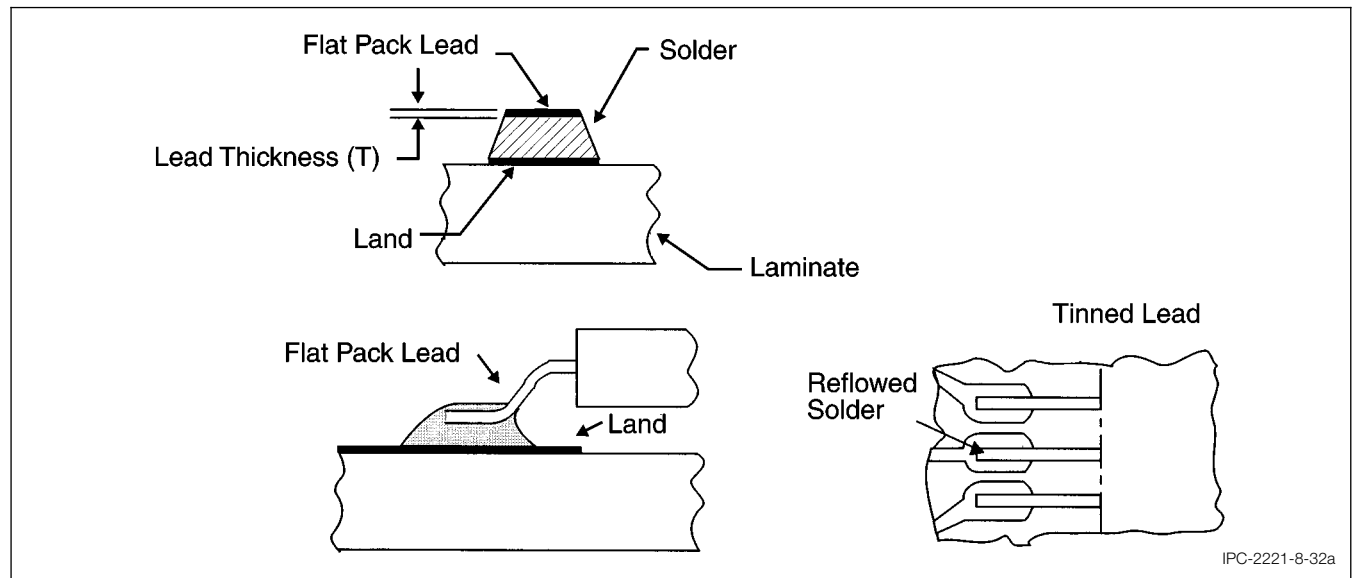
## 9.0 HOLES/INTERCONNECTIONS

**9.1 General Requirements for Lands with Holes**  Lands **shall** be provided for each point of attachment of a part lead or other electrical connection to the printed board. Circular lands are most common, but it should be noted that other land shapes may be used to improve producibility. If breakout is allowed, modified land shapes **shall** be used. These may include, for example, filleting to create additional land area at the conductor junction, corner entry on rectangular lands or ''keyholing'' to create additional land area along the axis of the incoming lead (see Figure 9-1). The modified land shape **shall** provide for the current carrying capacity of the circuit design.

**9.1.1 Land Requirements**  All lands and annular rings **shall** be maximized wherever feasible, consistent with good design practice and electrical clearance requirements. To meet the annular ring requirements specified in section 9.1.2, the minimum land surrounding a supported, or unsupported, hole **shall** be determined by the following. The worst-case land-to-hole relationship is established by the equation:

Land size, minimum = a + 2b + c

where:

a = Maximum diameter of the finished hole.
b = Minimum annular ring requirements (see section 9.1.2).
c = A standard fabrication allowance, detailed in Table 9-1, which considers production master tooling and process variations required to fabricate boards.

*Etchback, when required will reduce the insulation area that supports the internal land. The minimum annular ring considered in the design **shall** not be less than the maximum etchback allowed.

**Table 9-1   Minimum Standard Fabrication Allowance for Interconnection Lands**

| Level A | Level B | Level C |
|---------|---------|---------|
| 0.4 mm | 0.25 mm | 0.2 mm |

1. For copper weights greater than 1oz/sq.ft., add 0.05 mm minimum to the fabrication allowance for each additional oz/sq. ft. of copper used.
2. For more than 8 layers add 0.05 mm.
3. See 1.6.3 for definition of Levels A, B and C.

**9.1.2 Annular Ring Requirements**  An annular ring **shall** be required for all plated-through holes in Class 3 designs. The performance specifications for Class 1 and Class 2 products may allow partial hole breakouts. The design for these products should take into consideration that breakout is undesirable and the design should require adequate hole and land size so that breakout does not appear in the finished product. Landless holes or holes with partial circumscribing lands **shall** only be used when approved by the acquiring activity prior to the start of the design process and require conformance specimen that reflect the approach being used.

The minimum annular ring on external layers is the minimum amount of copper (at the narrowest point) between the edge of the hole and the edge of the land after plating of the finished hole (see Figure 9-2). The minimum annular ring on internal layers is the minimum amount of copper (at the narrowest point) between the edge of the drilled hole and the edge of the land after drilling the hole (see Figure 9-3).

A. *External Annular Ring*—The minimum annular ring for unsupported and supported holes **shall** be in accordance with Table 9-2 and Figure 9-2.
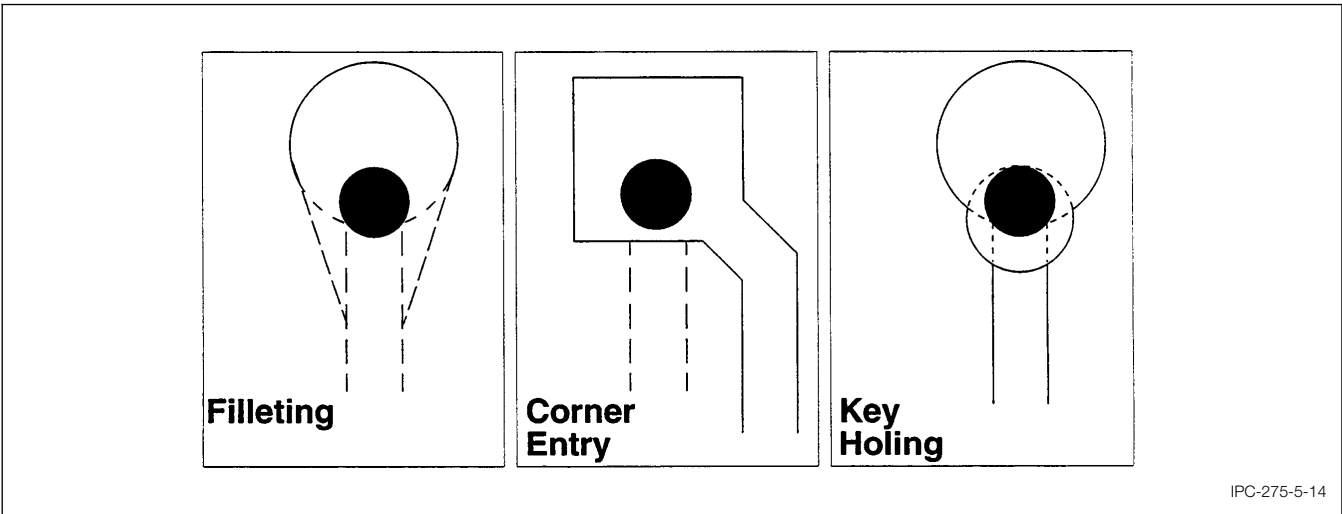


**Figure 9-1   Examples of modified land shapes**
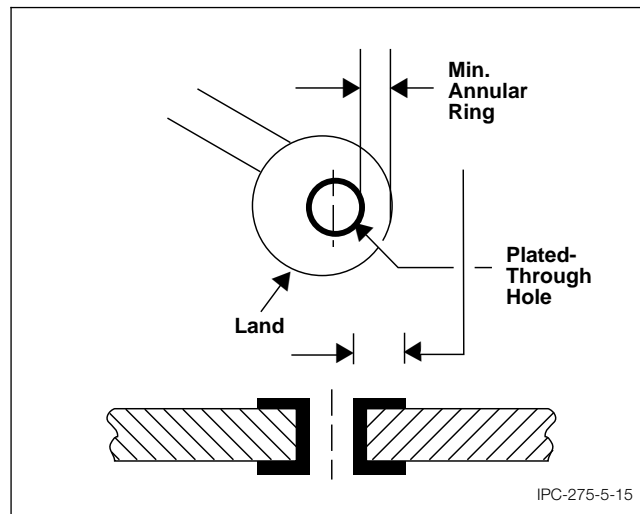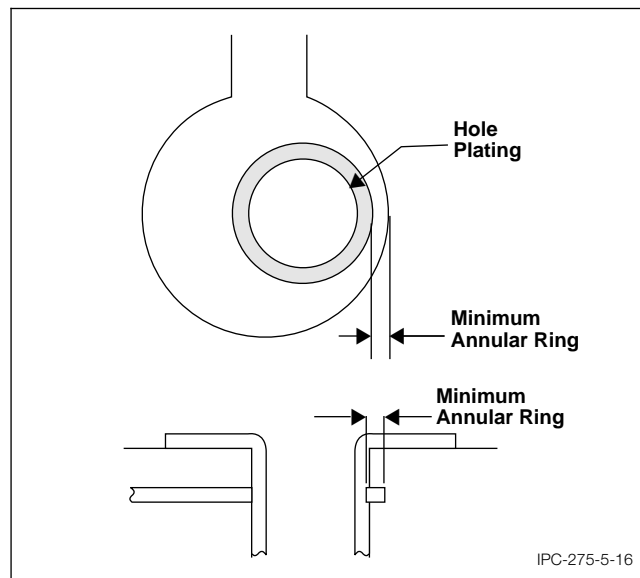
**Figure 9-2   External annular ring**



**Figure 9-3   Internal annular ring**

B. *Internal Annular Ring—*The minimum annular ring for internal lands on multilayer and metal core boards **shall** be in accordance with Table 9-2 and Figure 9-3. Etchback, when required, will reduce the insulation supporting the annular ring of internal lands. The minimum annular ring considered in the design **shall** be not less than the maximum etchback allowed.

**Table 9-2   Annular Rings (Minimum)**

| Annular Ring | Class 1, 2, and 3 |
|---|---|
| Internal Supported | 0.03 mm |
| External Supported | 0.05 mm |
| External Unsupported | 0.15 mm |

**9.1.3 Thermal Relief in Conductor Planes**   Thermal relief is only required for holes that are subject to soldering in large conductor areas (ground planes, voltage planes, thermal planes, etc.). Relief is required to reduce soldering dwell time by providing thermal resistance during the soldering process.

These type connections **shall** be relieved in a manner similar to that shown in Figure 9-4. The relationship between the hole size, land and web area is critical. See the sectional standards for more detailed information.

**9.1.4 Lands for Flattened Round Leads**   Flattened round (coined) leads **shall** have a land which will provide the seating so that the heel and the terminal relationship is in accordance with Figure 8-33.

Lead and land size should be designed to minimize side overhang. (Class 3 product allows up to 1/4 of the lead diameter to overhang.) Toe overhang is acceptable provided it does not violate the minimum designed conductor spacing. If flattened leads are used, the flattened thickness **shall** not be less than 40% of the original diameter (see J-STD-001).

**9.2 Holes**

**9.2.1 Location**   All holes and profiles **shall** be dimensioned in accordance with 5.4.

Note: The lead patterns of the majority of the components to be mounted on a printed board should be the major influence on choice of measurement system (metric vs. inches).

**9.2.2 Hole Location Tolerances**   Table 9-3, based on glass/epoxy materials, shows the values for hole location tolerances that are to be applied to the basic hole position. All tolerances are expressed as diameter about true position. These tolerances only take into account drill positioning and drill drift. The basic hole position may be further affected by material thickness, type and the copper density. The effect is usually a reduction (shrinkage) between basic hole positions.

**9.2.3 Quantity**   A separate component hole **shall** be provided for each lead, terminal of a part, or end of a jumper wire that is to be through-hole mounted, except as specified in 8.2.11.

**9.2.4 Spacing of Adjacent Holes**   The spacing of unsupported or plated-through holes (or both) **shall** be such that the lands surrounding the holes meet spacing requirements of the 6.3. Consideration should be given to the printed board material structural requirements, with the residual laminate material being no less than 0.5 mm.
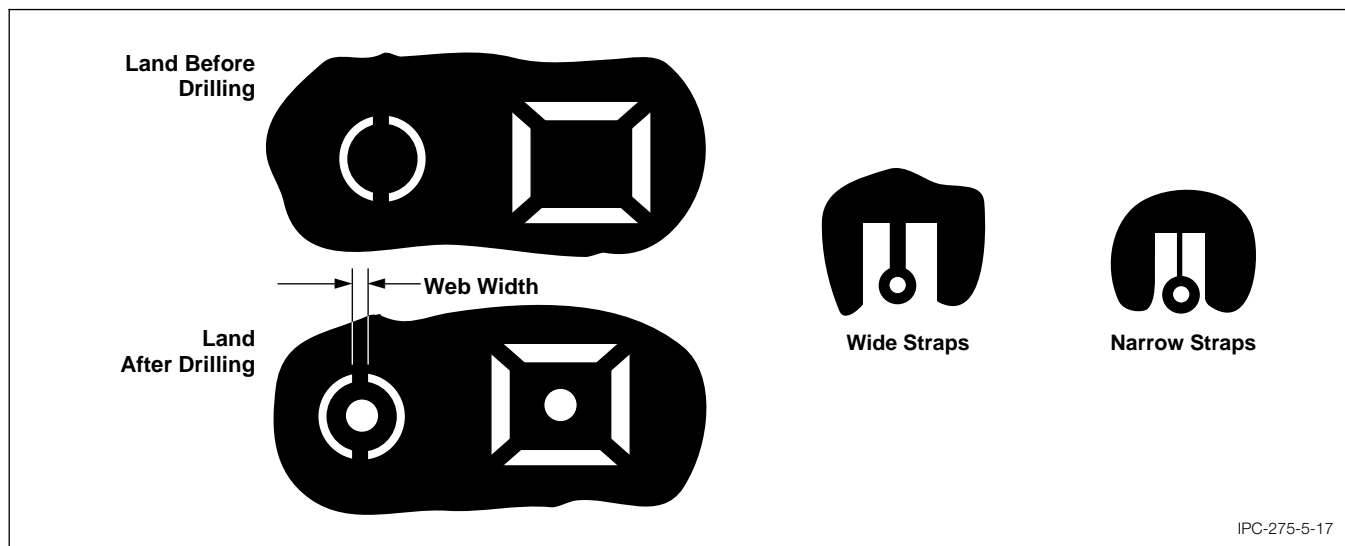
**Figure 9-4   Typical thermal relief in planes**

**Table 9-3   Minimum Hole Location Tolerance, dtp**

| Level A | Level B | Level C |
|---------|---------|---------|
| 0.25 mm | 0.2 mm | 0.15 mm |

**9.2.5 Hole Pattern Variation** When a modular grid increment is selected, see 5.4.2, parts whose leads emanate in a pattern that varies from the grid intersections of the modular dimensioning system of the printed board, **shall** be mounted on the printed board with one of the following hole patterns.

A hole pattern where the hole, for at least one part lead, is located at a grid intersection of the modular dimensioning system, and the other holes of the pattern are dimensioned from that grid location.

A hole pattern where the center of the pattern is located at a grid intersection of the modular dimensioning system, and all holes of the pattern are dimensioned from that grid location.

**9.2.6 Aspect Ratio** The aspect ratio of plated-through holes plays an important part in the ability of the manufacturer to provide sufficient plating within the plated-through hole.

**9.2.6.1 Plated-Through Hole Tolerances** When using the basic dimensioning system, plated-through holes used to attach component leads or pins to the printed board should be expressed in terms of MMC and LMC limits.

**9.2.7 Blind and Buried Vias** Plated-through holes connecting two or more conductive layers of multilayer printed board, but not extending fully through all layers of the base material comprising the board, are called blind and buried vias.

**9.2.7.1 Blind Vias** Blind via plated-through holes extend from the surface and connect the surface layer with one or more internal layers. The blind via can be produced by two methods: (1) After multilayer lamination by drilling a hole from the surface to the internal layers desired and electrically interconnecting them by plating the blind via holes during the plating process; (2) Before multilayer lamination by drilling the blind via holes from the surface layers to the first or last buried layers and plating them through, imaging and etching the internal sides, and then laminating them in the multilayer bonding process. For the second process if an interconnection is desired between the surface layer and more than one internal layer, sequential etching, laminating, drilling and plating-through of these layers together before final multilayer lamination is required. Blind via holes should be filled or plugged with a polymer or solder resist to prevent solder form entering them as solder in the small holes decreases reliability.

**9.2.7.2 Buried Vias** Buried via plated-through holes do not extend to the surface but interconnect only internal layers. Most commonly the interconnection is between two adjacent internal layers. These are produced by drilling the thin laminate material, plating the holes through and then etching the internal layer pattern on the layers prior to multilayer lamination. Buried vias between non-adjacent layers requires sequential etching of inside layers, laminating them together, drilling the laminated panel, plating the holes through, etching external sides and laminating this panel into the final multilayer panel.

**9.2.7.3 Hole Size of Blind and Buried Vias** Small holes are usually used for either blind or buried vias and may be produced mechanically, by laser or by plasma techniques. The minimum drilled hole size for buried vias is shown in

Table 9-4 and the minimum drilled hole size for blind vias is shown in Table 9-5. In either case plating aspect ratios must be considered; small deep blind vias are very difficult to plate because of decreased throwing-power and limited plating solution exchange in the holes. Blind and buried via holes may be plated shut; thus, the master drawing call out should be similar to that used for through-holes vias. See sectional standards for more information.

**Table 9-4   Minimum Drilled Hole Size for Buried Vias**

| Layer Thickness | Class 1 | Class 2 | Class 3 |
|---|---|---|---|
| <0.25 mm | 0.10 mm | 0.10 mm | 0.15 mm |
| 0.25 - 0.5 mm | 0.15 mm | 0.15 mm | 0.20 mm |
| 0.5 mm | 0.15 mm | 0.20 mm | 0.25 mm |

**Table 9-5   Minimum Drilled Hole Size for Blind Vias**

| Layer Thickness | Class 1 | Class 2 | Class 3 |
|---|---|---|---|
| <0.10 mm | 0.10 mm | 0.10 mm | 0.2 mm |
| 0.10 - 0.25 mm | 0.15 mm | 0.20 mm | 0.3 mm |
| 0.25 mm | 0.20 mm | 0.30 mm | 0.4 mm |

## 10.0 GENERAL CIRCUIT FEATURE REQUIREMENTS

**10.1 Conductor Characteristics**  Conductors on the printed board may take a variety of shapes. They may be in the form of single conductor traces, or conductor planes.

Critical pattern features which may affect circuit performance such as distributed inductance, capacitance, etc., **shall** be identified, unless the procurement contract requires the delivery of a stable master produced within the tolerance required for circuit performance.

**10.1.1 Conductor Width and Thickness**  The width and thickness of conductors on the finished printed board **shall** be determined on the basis of the signal characteristics, current carrying capacity required and the maximum allowable temperature rise. These **shall** be determined using Figure 6-4. The designer should recognize that processing may vary the thickness of copper on circuit layers. See Tables 10-1 and 10-2

The minimum finished conductor width used on the finished board **shall** not be less than 0.1 mm and, when the Underwriters Laboratories (UL) requirements are imposed, within the limits approved by UL for the printed board manufacturer (see UL 746E).

For ease of manufacturing and durability in usage, conductor width and spacing requirements should be maximized while maintaining the minimum desired spacing requirements. The minimum or nominal finished conductor width **shall** be shown on the master drawing.

When bilateral tolerances are required on the conductor, the nominal finished conductor width and the tolerances

**Table 10-1   Internal Layer Foil Thickness After Processing**

| Copper Foil | Minimum |
|---|---|
| 1/8 oz | 3.5 μm |
| 1/4 oz | 6.0 μm |
| 3/8 oz | 8.0 μm |
| 1/2 oz | 12.0 μm |
| 1 oz | 25.0 μm |
| 2 oz | 56.0 μm |
| 3 oz | 91.0 μm |
| 4 oz | 122.0 μm |
| Above 4 oz | 13 μm below minimum thickness listed for that foil thickness in IPC-MF-150 |

Note: Additional platings that may be required for internal layer conductors **shall** be separately designated as a plating thickness requirement.

**Table 10-2   External Conductor Thickness After Plating**

| Base Copper Foil | Minimum |
|---|---|
| 1/8 oz | 20 μm |
| 1/4 oz | 20 μm |
| 3/8 oz | 25 μm |
| 1/2 oz | 33 μm |
| 1 oz | 46 μm |
| 2 oz | 76 μm |
| 3 oz | 107 μm |
| 4 oz | 137 μm |
| For each succeeding ounce of copper foil, increase minimum conductor thickness by 30.0 μm | |

shown in Table 10-3, which are typical for 46 μm copper, **shall** be shown on the master drawing. This dimension need only be shown on the master drawing for a typical conductor of that nominal width.

**Table 10-3   Conductor Width Tolerances for 46 μm Copper**

| Feature | Level A | Level B | Level C |
|---|---|---|---|
| Without plating | ±0.06 mm | ±0.04 mm | ±0.015 mm |
| With plating | ±0.10 mm | ±0.08 mm | ±0.05 mm |

If the tolerances in Table 10-3 are too broad, tighter tolerances than Table 10-3 can be agreed to between the user and supplier and **shall** be stated on the master drawing and considered Level C. Table 10-3 values are bilateral tolerances for finished conductors.

The width of the conductor should be as uniform as possible over its length; however, it may be necessary because of design restraints to "neck down" a conductor to allow it to be routed between restricted areas, e.g., between two plated-through holes. The use of "necking down" such as that shown in Figure 10-1, can also be viewed as "beefing up." Single width, having a thin conductor throughout the

board, as opposed to the thin/thick approach is less desirable from a manufacturing point of view as the larger width conductor is less rejectable due to edge defects rated as a percentage of the total width.

In any event, if the conductor width change is used, the basic design requirements defined herein **shall** not be violated at the necking down location.
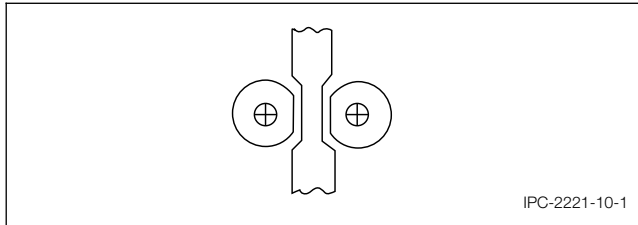


**Figure 10-1   Example of conductor beef-up or neck-down**

**10.1.2 Electrical Clearance** Clearances are applicable for all levels of design complexity (A, B, C) and performance classes (1, 2, 3). Conductive markings may touch a conductor on one side, but minimum spacing between the character marking and adjacent conductors **shall** be maintained (see Table 6-1).

To maintain the conductor spacing shown on the master drawing, space widths on the production master may require compensation for process allowances as defined in 10.1.1. Plated-through holes passing through internal foil planes (ground and voltage) and thermal planes **shall** meet the same minimum clearance between the plated-through hole and foil or ground planes as required for spacing between internal conductors (see 10.1.4). See 6.3 for more information on electrical clearance.

**10.1.3 Conductor Routing** The length of a conductor between any two lands should be held to a minimum. However, conductors which are straight lines and run in X, Y, or 45 degree directions are preferred to aid computerized documentation for mechanized or automated layouts. All conductors that change direction, where the included angle is less than 90 degrees, should have their internal and external corners rounded or chamfered.

In certain high speed applications, specific routing rules may apply. A typical example is serial routing between signal source, loads and terminators. Routing branches (stubs) may also have specified criteria.

**10.1.4 Conductor Spacing** Minimum spacing between conductors, between conductive patterns, and between conductive materials (such as conductive markings, see 10.1.2, or mounting hardware) and conductors **shall** be defined on the master drawing. Spacings between conductors should be maximized and optimized whenever possible (see Figure 10-2). To maintain the conductor spacing shown on the

master drawing, conductor widths and spaces on the production master should be compensated for process allowances.

**10.1.5 Plating Thieves** Plating thieves are added metallic areas which are nonfunctional. When located within the finished board profile, they allow uniform plating density, giving uniform plating thickness over the board surface. They **shall** neither adversely impact the minimum conductor spacing nor violate the required electrical parameters.

**10.2 Land Characteristics**

**10.2.1 Manufacturing Allowances** The design of all land patterns **shall** consider the manufacturing allowances, specifically those relating to conductor width and spacing.

Processing allowances similar to the characteristics shown in Figure 10-3 **shall** be built into the design to allow the manufacturer to produce a part that will meet the end-item requirements detailed on the master drawing. See IPC-D-310, and IPC-D-325.

**10.2.2 Lands for Surface Mounting** When surface attachment is required, the requirements of 10.1 **shall** be considered in the design of the printed board. The selection of the design and positioning of the land geometry, in relation to the part, may significantly impact the solder joint. The possibility of heat thieving is reduced by "necking down" the conductor near the soldering area. The designer must understand the capabilities and limitations of the manufacturing and assembly operations (see IPC-SM-782).

The various soldering processes associated with surface mounting have specific land pattern requirements. It is desirable that the land pattern design be transparent to the soldering process to be used in manufacturing. This will be less confusing for the designer and reduce the number of land sizes.

**10.2.3 Test Points** When required by the design, test points for probing **shall** be provided as part of the conductor pattern, and **shall** be identified on the assembly drawing. Vias, wide conductors, or component mounting lands may be considered as probe points, provided that sufficient area is available for probing, and maintaining the integrity of the via, conductor, or component solder connection. Test points **shall** be free of coating material. After test has been completed, test points may be coated.

**10.2.4 Orientation Symbols** Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled part. Techniques may include special symbols, or special land configurations to identify such characteristics as pin 1 of an integrated circuit package. Care should be taken to avoid adversely effecting the soldering process.
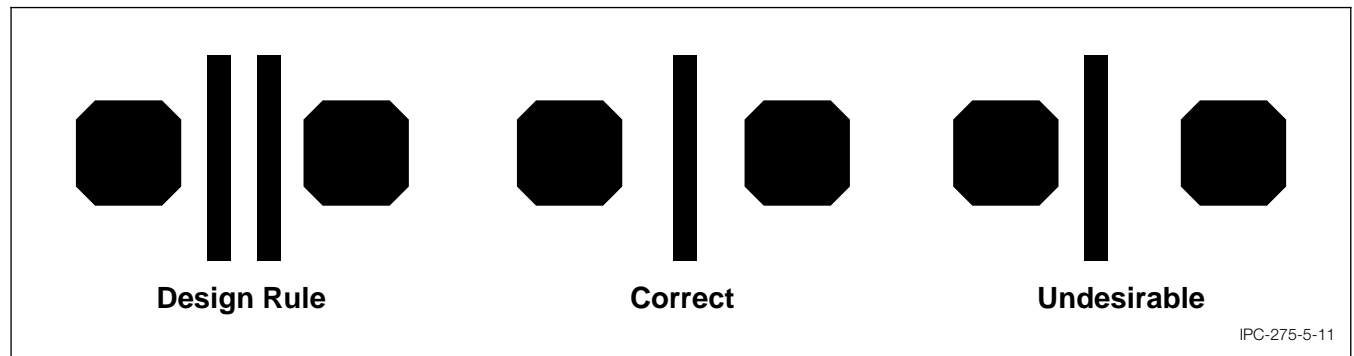
**Figure 10-2   Conductor optimization between lands**

**10.3 Large Conductive Areas**   Large conductive areas are related to specific products and are addressed in sectional design standards.

**11.0 DOCUMENTATION**

The printed board documentation package usually consists of the master drawing, master pattern drawing or copies of the artwork masters (film or paper), printed board assembly drawing, parts lists, and schematic/logic diagram..

The documentation package may be provided in either hard copy or electronic data. All electronic data **shall** meet the requirements of IPC-2510 series of standards.

Other documentation may include numerical control data for drilling, routing, libraries, test, artwork, and special tooling. There are design and documentation features/requirements that apply to the basic layout, the production master (artwork), the printed board itself, and the end-item printed board assembly; all must be taken into consideration during the design of the board. Therefore it is important to understand the relationships they have with one another as shown in Figure 11-1.

The printed board documentation **shall** meet the requirements of IPC-D-325. In order to provide the best documentation package possible, it is important to review IPC-D-325 and identify all the criteria that are effected by the design process, such as:

• parts information

• nonstandard parts information

• master drawing

• artwork masters production

• master pattern drawing

**11.1 Special Tooling**   During the formal design review prior to layout, special tooling that can be generated by the design area in the form of artwork or numerical control data **shall** be considered. This tooling may be needed by fabrication, assembly, or testing. Examples of such tooling are:

• Plots of numerical data to be used as check film.

• Buried or blind via land masters to assist in determining the location of the vias during layer fabrication for composite printed boards.

• Via land masters for composite printed boards to assist in distinguishing between vias that are to be drilled before lamination and vias that will be drilled after lamination.

• Artwork overlays to provide aids such as drill origin, spotter lands for nonplated through-holes without lands on the artwork, printed board coordinate zero, printed board profile, coupon profile, or profile of internal routed areas.

• Artwork for solder resist stripping which is used in some processes for solder mask over bare copper. The artwork should be designed to allow a solder resist overlap onto the solder at the copper/solder interface.

• Artwork overlays that can be used in assembly to assist with component insertion.

• Numerical data for auto-insert equipment at assembly.

• Solder paste stencil data

**11.2 Layout**

**11.2.1 Viewing**   The layout should always be drawn as viewed from the primary side of the board. For phototool generation purposes, the viewing requirements **shall** be identical to the layout. (See IPC-D-310.)

The definition of layers of the board **shall** be as viewed in Figure 11-2. Distinguishing characteristics **shall** be used to differentiate between conductors on different layers of the board.

**11.2.2 Accuracy and Scale**   The accuracy and scale of the layout must be sufficient to eliminate inaccuracies when the layout is being interpreted during the artwork generation process. This requirement can be minimized by strictly adhering to a grid system which defines all features on the printed board.
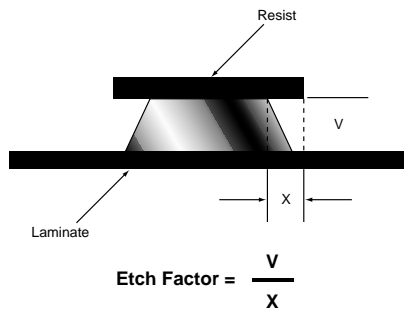
"A" POINT OF NARROWEST CONDUCTOR WIDTH: This is not "Minimum Conductor Width" noted on master drawings or performance specifications.

"B" CONDUCTOR BASE WIDTH: The width that is measured when "Minimum Conductor Width" is noted on the master drawing or performance specification.

"C" PRODUCTION MASTER WIDTH: The width usually determines the width of the metal or organic resist on the etched conductor.

Design width of the conductor is specified on the master drawing and is most often measured at the conductor base "B" for compliance to "minimum conductor width" requirements.

$$\text{Etch Factor} = \frac{V}{X}$$

The following two configurations show that conductor width may be greater at the surface than at the base.
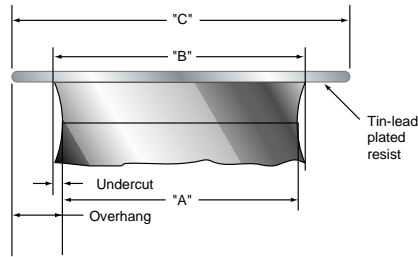
Pattern plating (dry film resist)
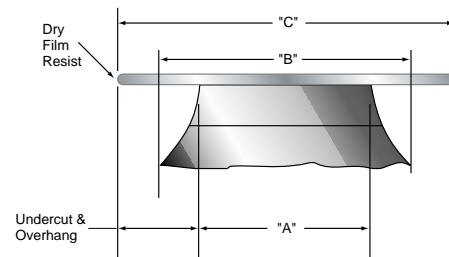
Panel plating (dry film resist)
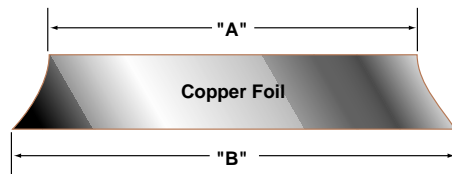
Internal layer after etch
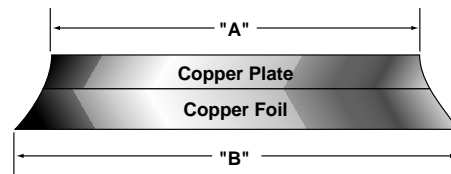
Internal plated layer as used for buried vias
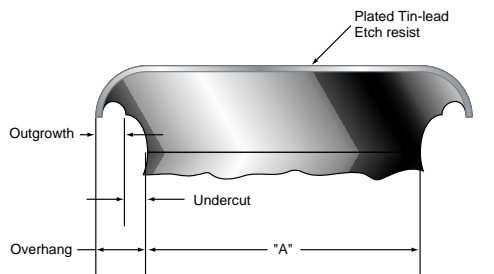
Pattern plating (dry film resist) with outgrowth
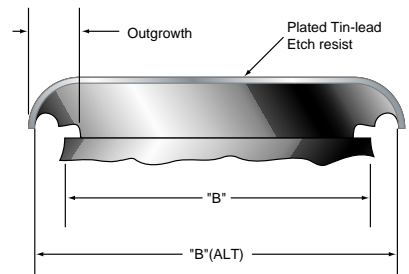
Pattern plating (liquid resist) with outgrowth

**Note:** The extent of outgrowth, if present, is related to the dry film resist thickness. Outgrowth occurs when the platting thickness exceeds the resist thickness.

"B" (ALT) would be used to determine compliance with "Minimum Conductor Width" for this etch configuration.
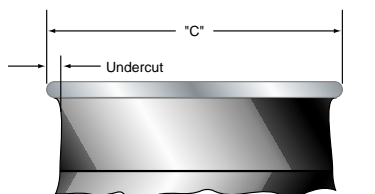
Thin clad & pattern plating (etch resist)
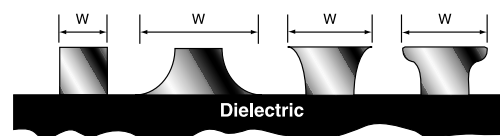
The effective width of a conductor may vary from the conductor width from surface obstructions (W).

**Note:** The different etch configurations may not meet intended design requirements.                    IPC-2221-10-3

**Figure 10-3   Etched Conductor Characteristics**

**Circuit Design**

PARTS LIST

SCHEMATIC DIAGRAM
LOGIC DIAGRAM

END PRODUCT
PERFORMANCE & TEST
REQUIREMENTS

**Packaging Design**

STANDARDS

PRINTED BOARD
LAYOUT

MANUFACTURING
CAPABILITIES

**Documentation**

MASTER
DRAWING

TEST/
PERFORMANCE
SPECIFICATION

PRINTED BOARD
ASSEMBLY
DRAWING

ARTWORK
(See note.)

**Manufacturing**

FABRICATION
PROCESS
SPECIFICATION

ARTWORK
MASTER
(See note.)

PRODUCTION
MASTER
(See note.)

MULTIPLE IMAGE
PRODUCTION MASTER
(See note.)

HOLES &
PROCESS
DATA

PANEL OR
PRINTED BOARD
(RIGID OR FLEXIBLE)

ASSEMBLY
SEQUENCE/
PROCESS DATA

**Assembly**

PRINTED
BOARD
ASSEMBLY

**Test**

IPC-2221-11-1

Note: The term "original" may be used to preface any of the drafting and photographic tooling terms used in the figure. The "original" is not usually used in manufacturing processes. In the event a "copy" is made, the copy **shall** be of sufficient accuracy to meet its intended purpose if it is to take on the name of any one of the tems used in this figure. Other adjectives may also be used to help describe the kind of copy, i.e.: "nonstable," "first generation," "record," etc.

**Figure 11-1   Flow Chart of Printed Board Design/Fabrication Sequence**
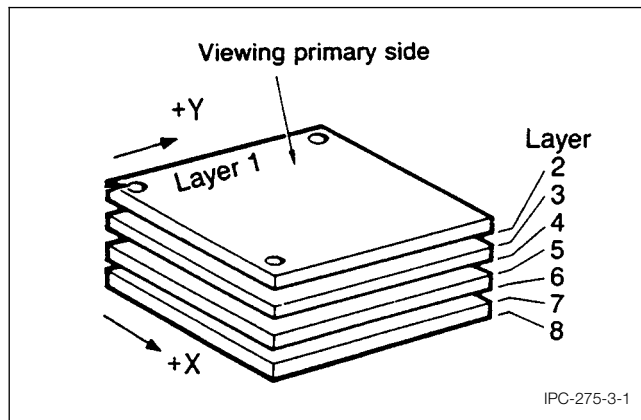
Figure 11-2   Multilayer Board Viewing

**11.2.3 Layout Notes** The layout should be completed with the addition of appropriate notations, marking requirements, and revision/status-level definition. This information should be structured to assure complete understanding by all who view the layout. Notes are especially important for the engineering review cycle, the digitizing effort, and when the document is used by someone other than the originator.

**11.2.4 Automated-Layout Techniques** All the information listed in 11.2.1 through 11.2.3 is applicable to both manual and automated layout generation. However, when automated layout techniques are used, they must also match the design system being employed. This may include the use of computer-aided drafting assistance that primarily helps in the defining of components and conductors, or may be as sophisticated as to add the placement of digital circuit gates, the placement of components, and the routing of conductors.

When automated systems must communicate with each other, it is recommended that standard files be used for this technique. IPC-D-350, IPC-D-356 and the IPC-2510 series of documents have been developed to serve as the standard format to facilitate the interchange of information between automated systems. Archiving of data should be in accordance with those documents. Delivery of computer-generated data as a part of a documentation package should meet these requirements.

With automated techniques, the data base should detail all the information that will be needed to produce the printed board. This includes all notes, plating requirements, board thickness, etc. A check plot should be employed to verify that the data base matches the requirements.

**11.3 Deviation Requirements** Any deviation from this standard or drawing **shall** have been recorded on the master drawing or a customer-approved deviations list.

**11.4 Phototool Considerations** The same land pattern configuration and nominal dimensions may be used for preparing the phototool for the stencil or screen used for solder paste application.

Solder resist coating phototools may be prepared in two ways. The first method is to provide a special land pattern for each component using larger shapes to establish the solder resist clearance around the conductive pattern (see Figure 11-3).
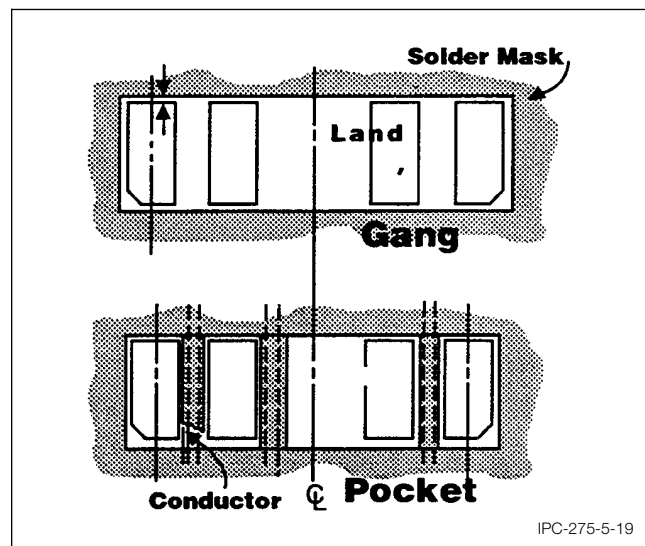


Figure 11-3   Solder resist windows

The second method is to provide the same land pattern shapes for solder resist windows as used to establish the conductive pattern. In this method, the manufacturer of the printed board photographically expands the solder resist pattern to provide the necessary clearances. Thus, the same phototool may be used to establish the conductive pattern, the solder resist openings, and the solder paste deposition tool. The ability to use the same phototool for the three processing steps enhances registration capabilities of the three image-dependent procedures and also keeps computer library symbol (land pattern) types to a manageable limit when computer aided design (CAD) systems are used. When utilizing this option, maximum clearance values must be specified on the master drawing.

## 12.0  QUALITY ASSURANCE

Quality assurance concepts should be considered in all aspects of printed board design. Quality assurance evaluations relating to design should consist of the following:

• Material

• Conformance inspection

• Process control evaluations

This section defines the various specimen that should be considered during the design process. Also included is the rationale and purpose for the use of each specimen.

**12.1 Conformance Test Specimen** Conformance test specimen, when required, **shall** be in accordance with this section. Quality assurance provisions often require the use of specific test procedures or evaluations to determine if a particular product meets the requirements of the customer or specifications. Some of the evaluations are done visually, others are done through destructive and nondestructive testing.

Some quality evaluations are performed on test specimen because the test is destructive or the nature of the test requires a specific design which may not exist on the printed board. Test specimen are used in these types of tests as representatives of the printed boards fabricated on the same panel.

A test specimen is a suitable sample for destructive testing since it has been subjected to the same processes as the printed boards on the same panel; however, the design and location of the test specimen are critical in order to ensure that the specimen are truly representative of the printed boards. A production board may be used for destructive tests. Tests requiring specific circuit configuration (e.g., insulation resistance) may also be performed on production boards if appropriate circuitry is included in the design.

**12.2 Material Quality Assurance** Material inspections normally consist of certification by the manufacturer supported by verifying data based on statistical sampling that all materials which become a part of the finished product is in accordance with the master drawing, material specifications, and/or procurement documentation.

Conformance specimen are defined in the detailed specifications for the base material. As an example, copper foil is tested for tensile strength, ductility, elongation, fatigue ductility, peel strength, and carrier release strength. In most instances, the conformance test specimen for metal foil consist of a specific length and width.

Laminate specifications, however, require conformance specimen that relate more to performance of the end product board. Not only are peel strength, dielectric breakdown, and water absorption tested, the methods of examination require that specific specimen geometries be prepared in order to make the test as meaningful as possible. When a design requires verification of the base material at the end product board level, conformance specimen are used to establish that evaluation is identical or similar to those defined in existing base material specifications. Some users may require more than one ply of reinforcement and greater than 0.05 mm dielectric thickness. Example: Some military specifications require two ply reinforcement and greater than 0.09 mm dielectric thickness.

Each design sectional allows for a minimum dielectric thickness between layers of a multilayer printed board, when agreed upon between user and supplier. When this requirement is agreed upon, conformance test specimen must be provided as a part of the design to verify the specific resin and resin content, glass style, dielectric withstanding voltage between claddings and moisture resistance verification.

**12.3 Conformance Evaluations** Conformance evaluations are performed on production boards and/or conformance specimen. If a production board is selected for conformance evaluation, it should be capable of meeting the requirements of Table 12-1. Specimen required for conformance evaluation **shall** be as defined herein. Additional conformance specimen may be added by the manufacturer. Conformance specimen **shall** be traceable to the production panel.

**12.3.1 Specimen Quantity and Location** The conformance test circuitry comprised of the specimen described in 12.4 **shall** be a part of every panel used to produce printed boards when required by the performance specification.

All required configurations of the specimen **shall** be defined on the master artwork and master drawing. The location of the specimen on the production master **shall** be positioned within 6.4 mm and 12.7 mm of the printed board image. The minimum number specimen and their requirement for location on the production master **shall** be in accordance with Table 12-1. Figure 12-1 shows an example of specimen location concepts. When feasible, specimen should also be located in the center of each panel to reflect plating characteristics. Other specimen may be positioned by the fabricator to optimize material utilization and tooling provided the 6.4 mm and 12.7 mm requirement is maintained. At least one hole in each specimen should be located on the same grid as the printed board features.

**12.3.2 Specimen Identification** Conformance test circuitry **shall** provide space for:

- Board part number and revision letter
- Traceability identification
- Lot date code
- Manufacturer's identification, e.g., Commercial and Government Entity (CAGE), logo, etc.

Special coding systems may be used provided they are identified on the master drawing.

**Table 12-1  Specimen Frequency Requirements[1]**

| Specimen Purpose | I.D.[2] | Class 1 | Class 2 | Class 3 |
|---|---|---|---|---|
| **Conformance Testing** | | | | |
| Hole Solderability | A | Not Required | Twice per panel | Twice per panel |
| Solderability | S | Optional | Optional | Optional |
| Solder Resist Tenting (if used) | T | Not required | Once per panel with solder resist, location optional | Once per panel with solder resist, location optional |
| Thermal Stress, Plating Thickness, and Bond Strength Type 1 | B | Twice per panel opposite corners | Twice per panel opposite corners | Twice per panel opposite corners |
| Plating Adhesion and Surface Solderability | C | Not Required | Once per panel, location optional, pattern defined by artwork | Once per panel location optional, pattern defined by artwork |
| Solder Resist (if used) | G | Once per panel with solder resist, location optional | Once per panel with solder resist, location optional | Once per panel with solder resist, location optional |
| Surface Mount Solderability (Optional for SMT) | M | Not required | Once per panel, location optional, pattern defined by artwork | Once per panel, location optional, pattern defined by artwork |
| **Reliability Assurance Inspection** | | | | |
| Surface Mount Bond Strength (Optional for SMT) | N | Not Required | Once per panel, location optional, pattern defined by artwork | Once per panel, location optional, pattern defined by artwork |
| Surface Insulation Resistance | H | Once per panel, location optional | Twice per panel opposite corners | Twice per panel opposite corners |
| Moisture and Insulation Resistance | E | Once per panel, location optional | Twice per panel, opposite corners | Twice per panel opposite corners |
| **Optional or Process Control** | | | | |
| Registration (Option 1 or 2) | F | Not required | Four per panel, opposite sides defined by artwork | Four per panel, opposite sides defined by artwork |
| Registration (Optional) | R | Not required | Four per panel, opposite sides defined by artwork | Four per panel, opposite sides defined by artwork |
| Interconnect Resistance (Optional 1 or 2) | D | Not required | Once per panel, location optional, pattern defined by artwork | Once per panel, location optional, pattern defined by artwork |

[1] If additional coupons for impedance testing are required, follow guidelines of IPC-D-317 and IPC-D-330.
[2] Where possible, coupon identification letters have been chosen to conform to those currently being used for conformance evaluations.
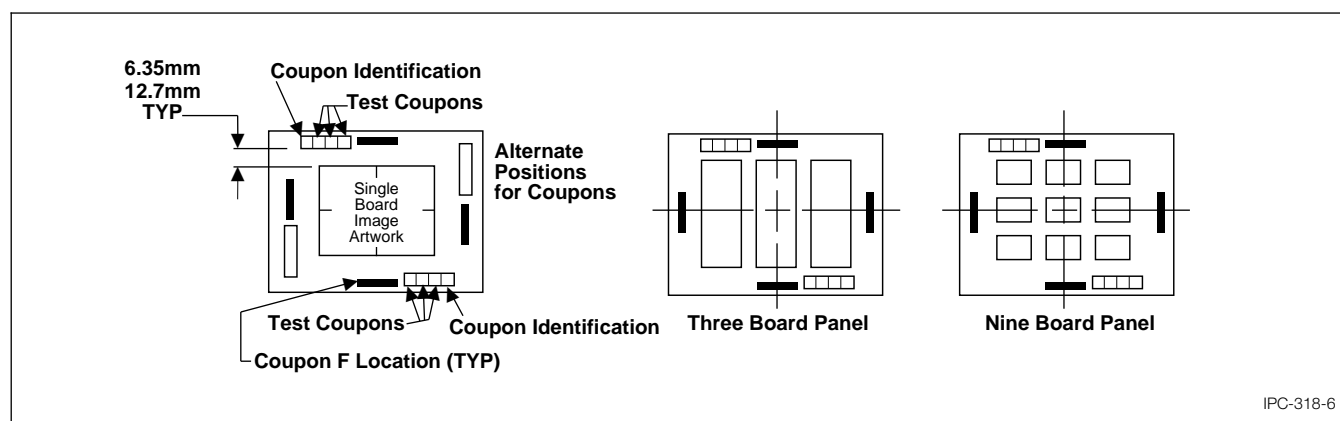


**Figure 12-1   Location of test circuitry**

**12.3.3 General Specimen Requirements**  Test specimen should reflect the specific board characteristics. This information consists of meeting the requirements for holes, conductors, spaces, etc. When specimen are used to establish process control parameters, they **shall** consistently use a single hole size or land configuration which reflects the process. Process characteristics and general board characteristics should be matched (i.e., threshold technology, leading edge technology, etc.).

**12.3.3.1 Tolerances** Tolerances for the fabrication of test specimen **shall** be the same as those for the printed board.

**12.3.3.2 Etched Letters** Etched letters shown on specimen are for reference only.

**12.3.3.3 Interlayer Connection Holes** Whenever a multilayer design incorporates interlayer connection holes in the form of blind or buried vias, specimen A, B, and D **shall** be designed so as to incorporate these types of holes connecting the appropriate layers. The individual specimen description contains information on how these holes are to be incorporated. The specific number of holes for evaluation should be a minimum of three in each individual test specimen with a minimum of two test specimen required on each individual panel.

**12.3.3.4 Metal Cores** Whenever a multilayer design uses metal cores, the same core(s) **shall** be incorporated into the design of the specimen.

If the metal core(s) has interlayer connection holes that pass through the core without contact, the design of the specimen **shall** be representative of that characteristic. If the hole contacts the core, that characteristic **shall** also be represented in the specimen. The minimum number of holes for this evaluation are three per specimen with a minimum of two specimen on each individual panel. Additional A and B specimen may be required for horizontal microsections.

Composite printed boards **shall** have separate specimen for the top side board, the bottom side board, and the composite board. The specimen for the composite printed board **shall** include the core material.

**12.4 Individual Specimen Design** Individual test specimen are designed to evaluate specific individual characteristics of the printed boards they represent (see also IPC-A-22). Variations in specified coupon design must meet the intent of the original design and be representative of the board.

**12.4.1 Specimen A and B (Plated Hole Evaluation)** Test specimen A and B are used to evaluate plated hole characteristics.

Figure 12-2 shows the general configuration of the specimen. The nominal hole size for solderability testing **shall** be the diameter of the smallest solder-coated hole on the board and the nominal land size **shall** be the diameter of the land used for that hole. For thermal stress, the nominal hole size **shall** be the diameter of the smallest hole and the nominal land size **shall** be the diameter of the land used for that hole. The land shape **shall** be the same as that used on the printed board for these lands and holes. Plated layers

**shall** represent printed board design, e.g., ground ties on specific layers, deleted non-functional lands, etc. Spacing between holes **shall** be representative of the printed board. Conductors **shall** be included in between the holes on each signal layer. The direction of the conductor **shall** alternate from layer to layer on the x and y-axis as shown in Figure 12-3. The conductor width **shall** be representative of the smallest line width in the design.

For internal layer connection holes (blind and buried vias) a minimum of one additional A or B specimen **shall** be added for each interconnection plating operation required by the design.
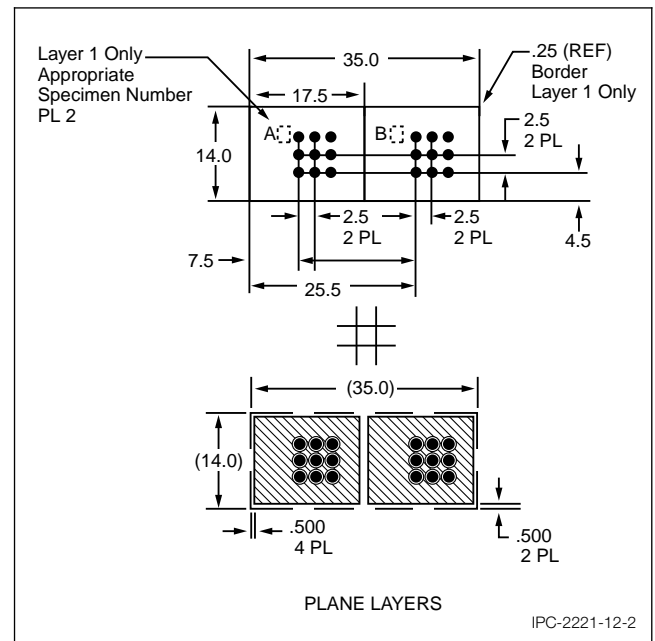


**Figure 12-2   Test Specimen A and B, mm**

**12.4.2 Specimen C (Plating Adhesion and Surface Solderability)** This specimen is used to evaluate plating adhesion and surface solderability to J-STD-003 requirements. The design of this specimen is shown in Figure 12-4.

**12.4.3 Specimen D (Interconnection Resistance and Continuity)** Test specimen D is used to evaluate interconnection resistance, continuity, correct lay-up, and other performance criteria. See Figure 12-5 for an example of specimen D. Figure 12-6 shows the modification to be made to specimen D for buried vias.

**12.4.3.1 Conformance Testing** For conformance testing, the number of layers, lay-up, layer configuration, and use of nonfunctional lands **shall** be modified to reflect the board design. The land size **shall** be representative of the board and the hole diameter **shall** be the smallest in the associated board with the exception of A1, A2, B1, and B2
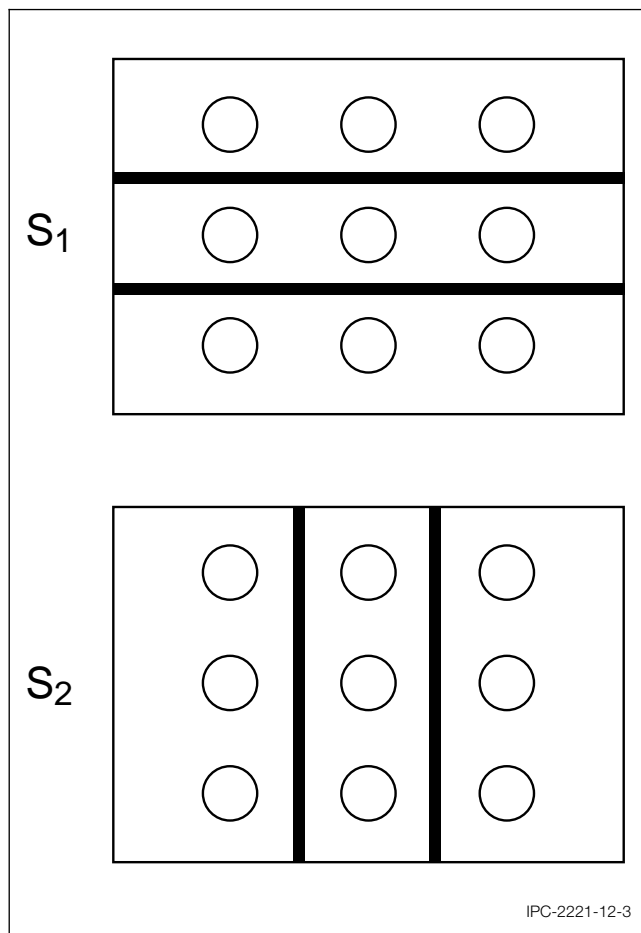
**Figure 12-3   Test Specimen A and B (conductor detail)**
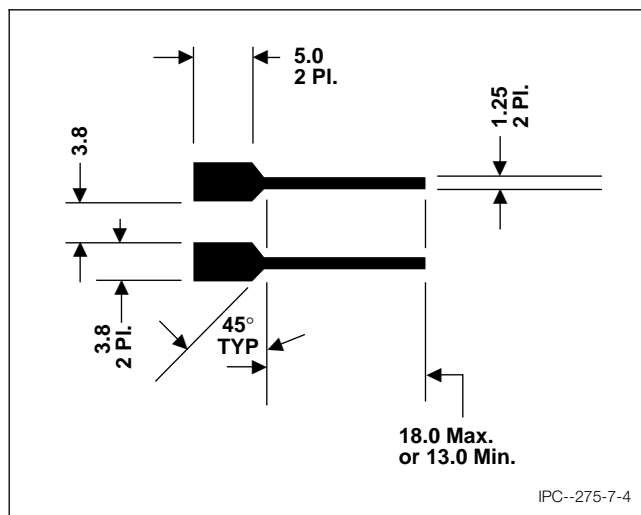


**Figure 12-4   Specimen C, external layers only, mm**

which **shall** be a minimum of 0.75 mm. Since the smallest hole represents the most difficulty in meeting plating requirements, this will ensure that the evaluation of the D specimen parallel the characteristic with the most variability. The length of the specimen will vary with the number of layers.

A typical example of a ten-layer, specimen D modified to include blind and buried vias is shown in Figure 12-5 and Figure 12-6. In general, the conductor **shall** be continuous from holes A1/A2 to holes B1/B2 and **shall** be arranged symmetrically around the centerline of the specimen.

The conductors **shall** not be routed stepwise through the specimen, but rather arranged so that the interconnects in a specific hole are separated to the greatest extent possible. The maximum number of holes in the specimen are not restricted; however, the minimum number of holes **shall** be two times the number of layers plus four (for holes A1, A2, B1, and B2).

Except for plane layers, there **shall** be a minimum of two conductor paths for each layer of the printed board design, one on each side of the centerline. If there are no conductors on the external layers, the connections **shall** be moved to layer 2 and layer n-1 respectively.

The conductor width on each layer **shall** be the minimum used on that layer of the printed board design. Constraining cores and plated layers **shall** represent printed board design, e.g., ground ties on specific layers, deleted non-functional lands, etc. Blind and buried vias **shall** be included in the specimen design.

**12.4.3.2 Process Control**   See Figure 12-7 as an example of a process control specimen.

**12.4.4 Specimen E and H (Insulation Resistance)**   These specimen are used for evaluating insulation resistance, bulk resistance and cleanliness of the material after exposure to an elevated cyclic temperature and humidity under an applied voltage. The specimen can also be used for evaluating dielectric withstanding voltage.

The design of the specimen **shall** be in accordance with Figure 12-8 or Figure 12-9 except as noted below. The minimum land hole diameter **shall** be any convenient size. A pair of holes and a pair of conductors **shall** be provided for all layers of the specimen.

When using surface mount patterns, alternate specimen may be used to evaluate both insulation resistance and cleanliness of the bare board before and after solder resist. The ''Y'' pattern of specimen E can provide a useful tool for cleanliness and insulation resistance property evaluations. As in most instances, the specimen under large surface mount devices should be a comb pattern. Figure 12-10 shows several comb pattern combinations to evaluate land patterns used for surface mounting. These specimen and concepts may be incorporated directly on the board in a spare position for a component, or may be incorporated as conformance specimen on the panel for evaluation when assembling surface mount component in panel format. If a ''Y'' pattern is assigned to a chip component, the position
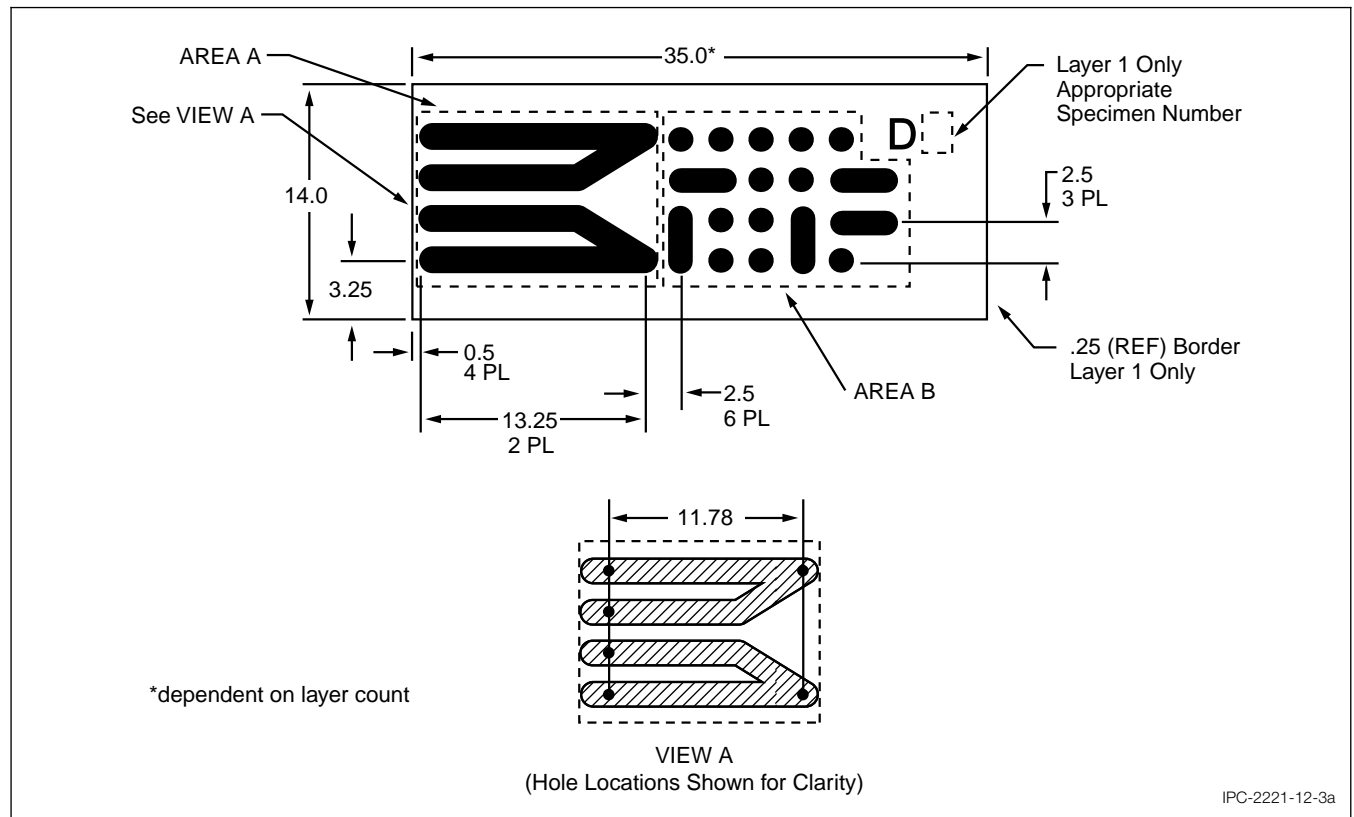
**Figure 12-5   Test Specimen D, mm**

can be left empty or can be filled to reflect cleanliness/ insulation resistance properties of the bare board, or cleanliness/insulation resistance properties of the assembly (see Figure 12-11).

**12.4.4.1 Specimen E**   Specimen E is used for general testing purposes. It is less sensitive to dirt and ionic contaminants. The general design of the specimen is shown in Figure 12-8.

**12.4.4.2 Specimen H**   Specimen H is used for higher level insulation testing, such as telecommunications. See Figure 12-9 for typical design. The comb pattern requires more intensive cleaning process. This specimen is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

**12.4.5 Registration Specimen**   The purpose of the registration specimen is to evaluate the internal annular ring. Although specimen A and B may be used for registration evaluation, the techniques require multiple microsections. Specimen F and specimen R represent various alternatives using electrical, x-ray, or visual inspection.

Figure 12-12 and Figure 12-13 dimensions apply to qualification testing only.

Specimen F is used to evaluate layer-to-layer registration and annular ring without microsection.

The advantages of specimen R are that it can be evaluated for annular ring by x-ray after drilling, it provides a quick electrical check to determine if the correct annular ring is present, and provides a digital measurement of the annular ring which makes it an effective method of process control. The disadvantages are that the etch factor must be known for each layer, the x-ray must have a resolution of less than 0.025 mm, a separate land must be present for each layer, and the specimen cannot be evaluated electrically until after the holes are plated.

Either F or R, or a combination, may be used to evaluate misregistration of the layers. The specimen **shall** be placed close to the board at the edge of the panel, near the center of the horizontal or vertical edge since that is where the most material movement occurs (see Figure 12-1).

**12.4.5.1 Specimen F, Conformance Testing (Option 1)** The design of the specimen **shall** be in accordance with Figure 12-12 with the hole diameter at the option of the manufacturer. The land size for this option includes an annular ring. Constraining cores and plated layers **shall** represent printed board design. The advantages to this option are that the specimen may be evaluated immediately

D SPECIMEN TEST LAYERS



6. Internal Plane Layer – No nonfunctional lands

7. Internal Plane Layer – No nonfunctional lands

8. Internal Layer – With nonfunctional lands

9. Internal Layer – No nonfunctional lands

10. Internal Layer – Lands at all hole locations

1. External Layer – Lands at all hole locations

2. Internal Layer – No nonfunctional lands

3. Internal Plane Layer – With nonfunctional lands

4. Internal Layer – No nonfunctional lands

5. Internal Layer – With nonfunctional lands

IPC-2221-12-3b

**Figure 12-5 cont.   10 Layer Example**

**TEST LAYERS.**

IPC-I-002036

**Wiring Schematic**

IPC-I-002133

**Representative Layer Diagram**

Conductive Layers
Core Layers
B-Stage Layers

IPC-I-002133

IPC-2221-12-4
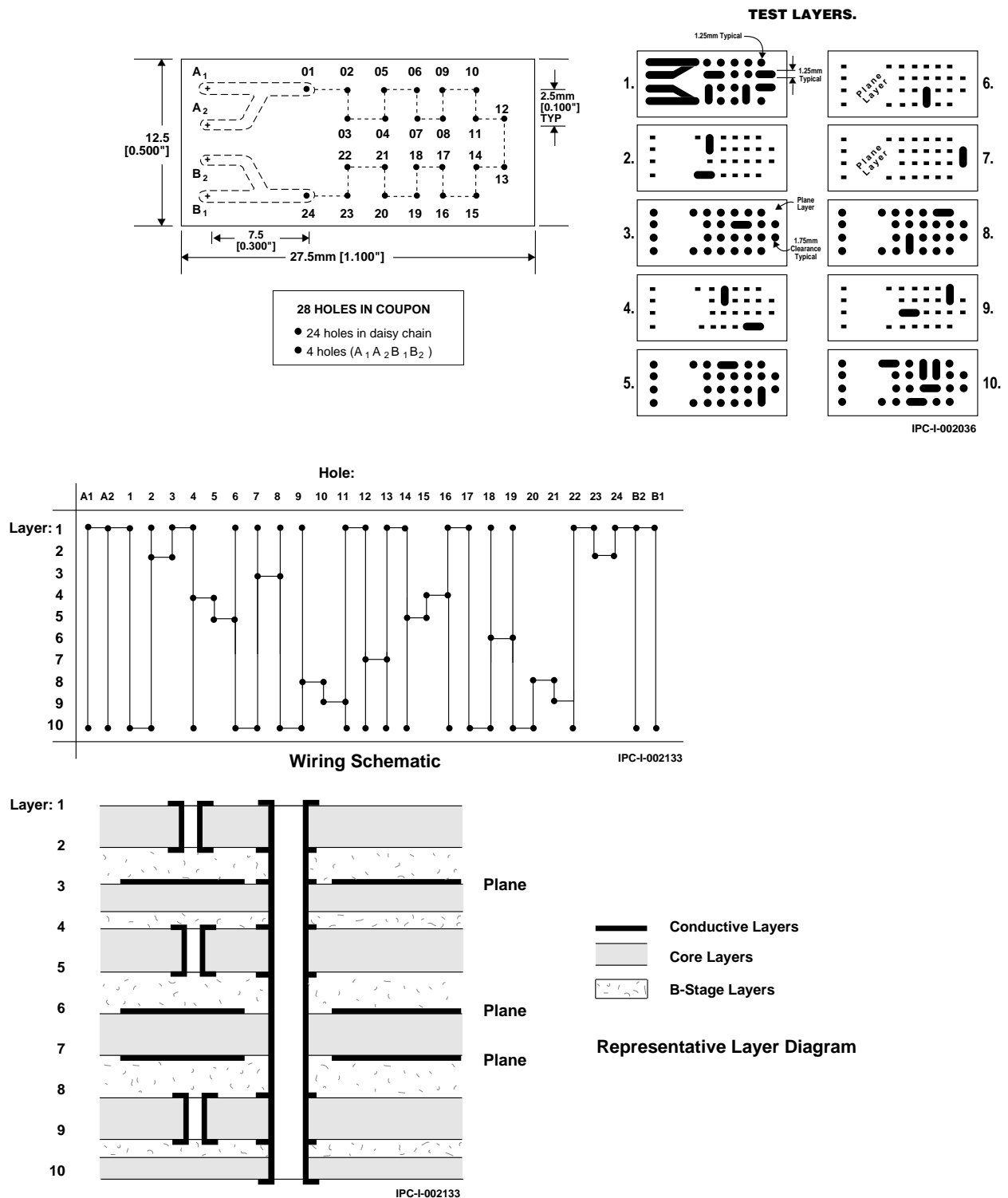
**Figure 12-6   Example of a 10 layer specimen D, modified to include blind and buried vias**
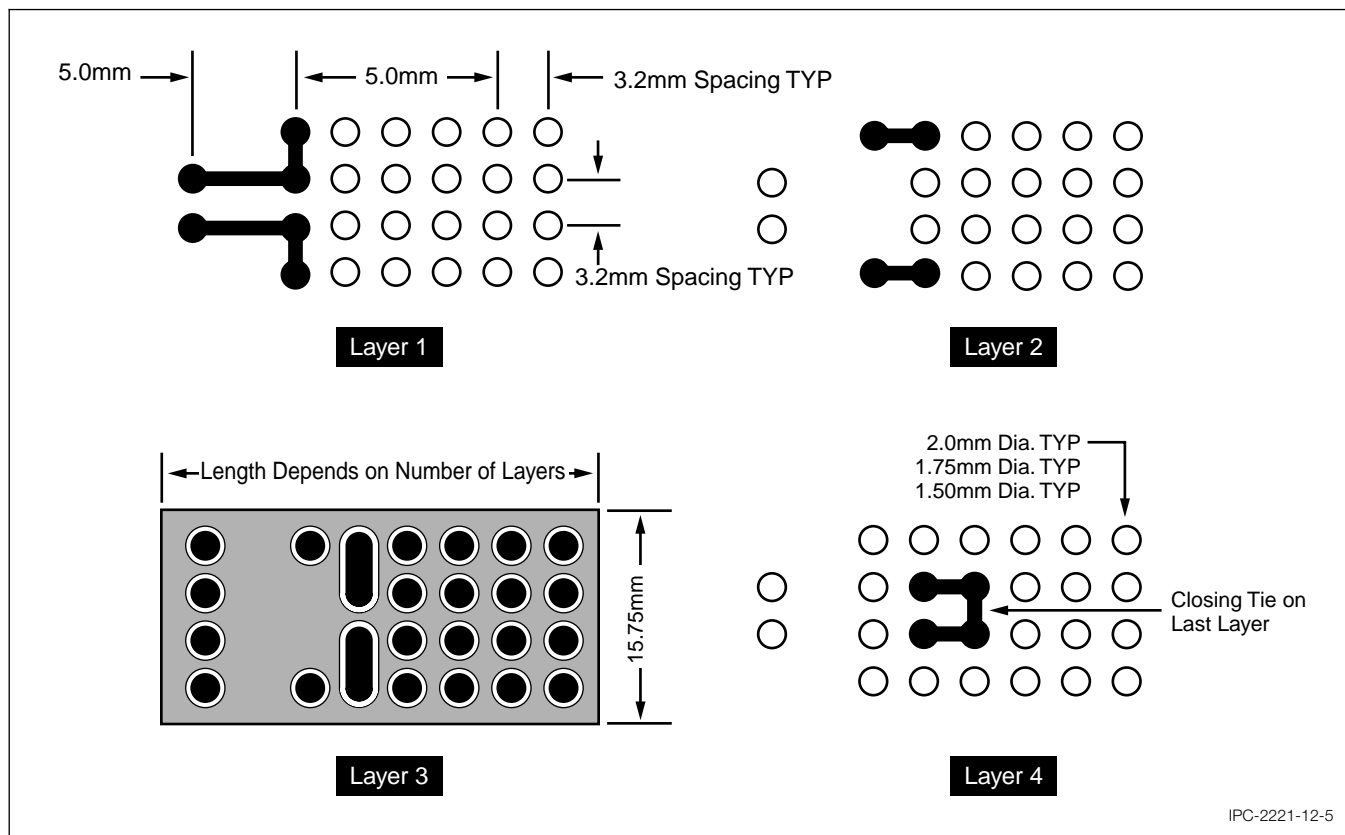
**Figure 12-7   Test Specimen D for process control of 4 layer boards**
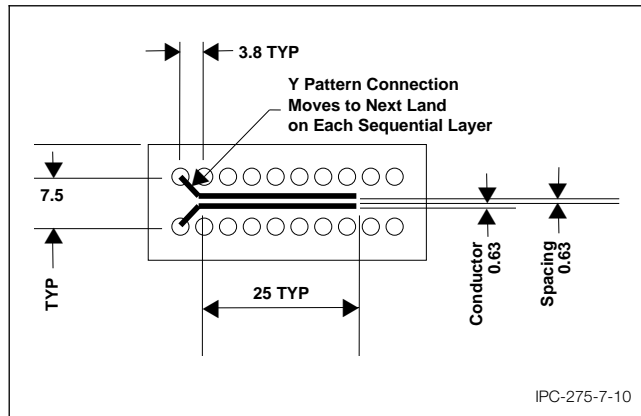


**Figure 12-8   Specimen E, mm**

after drilling, and the etch factor does not need to be considered. The disadvantage is that it requires an x-ray with a resolution of less than 0.025 mm to measure the annular ring.

This concept places a land on every layer. If the manufacturer wishes to use another hole diameter, the land size **shall** be calculated for each internal layer separately using the formula in 9.1.1. The specimen are evaluated after drilling by measuring the annular ring using x-ray.

**12.4.5.2 Specimen F, Conformance Testing (Option 2)** The design of the specimen **shall** be in accordance with

Figure 12-12 with the hole diameter at the option of the manufacturer. The land size for this option does not include an annular ring. Constraining cores and plated layers **shall** represent printed board design. This is the preferred specimen. The advantages to this option are that the specimen may be evaluated after drilling by x-ray for breakout, evaluation may be after etchback or hole clean using a visual inspection, and the etch factor need not be considered.

This concept places a land on every layer. If the manufacturer wishes to use another hole diameter, the land size **shall** be calculated for each internal layer separately using the formula in 9.1.1.

The specimen can be evaluated after drilling by inspecting for breakout using x-ray, or the specimen can be inspected after hole clean or etchback for a continuous ring in the drilled hole using a back-lit table.

**12.4.5.3 Specimen R, Conformance Testing** A typical specimen design is shown in Figure 12-13. The hole size and external lands are at the option of the fabricator. On internal layers, the specimen uses a ten hole pattern on 2.5 mm centers through a copper plane with circular clearance areas around nine of the holes. The clearance diameters are stepped in 0.05 mm increments for the first nine holes. There is no clearance area for the tenth hole so that the
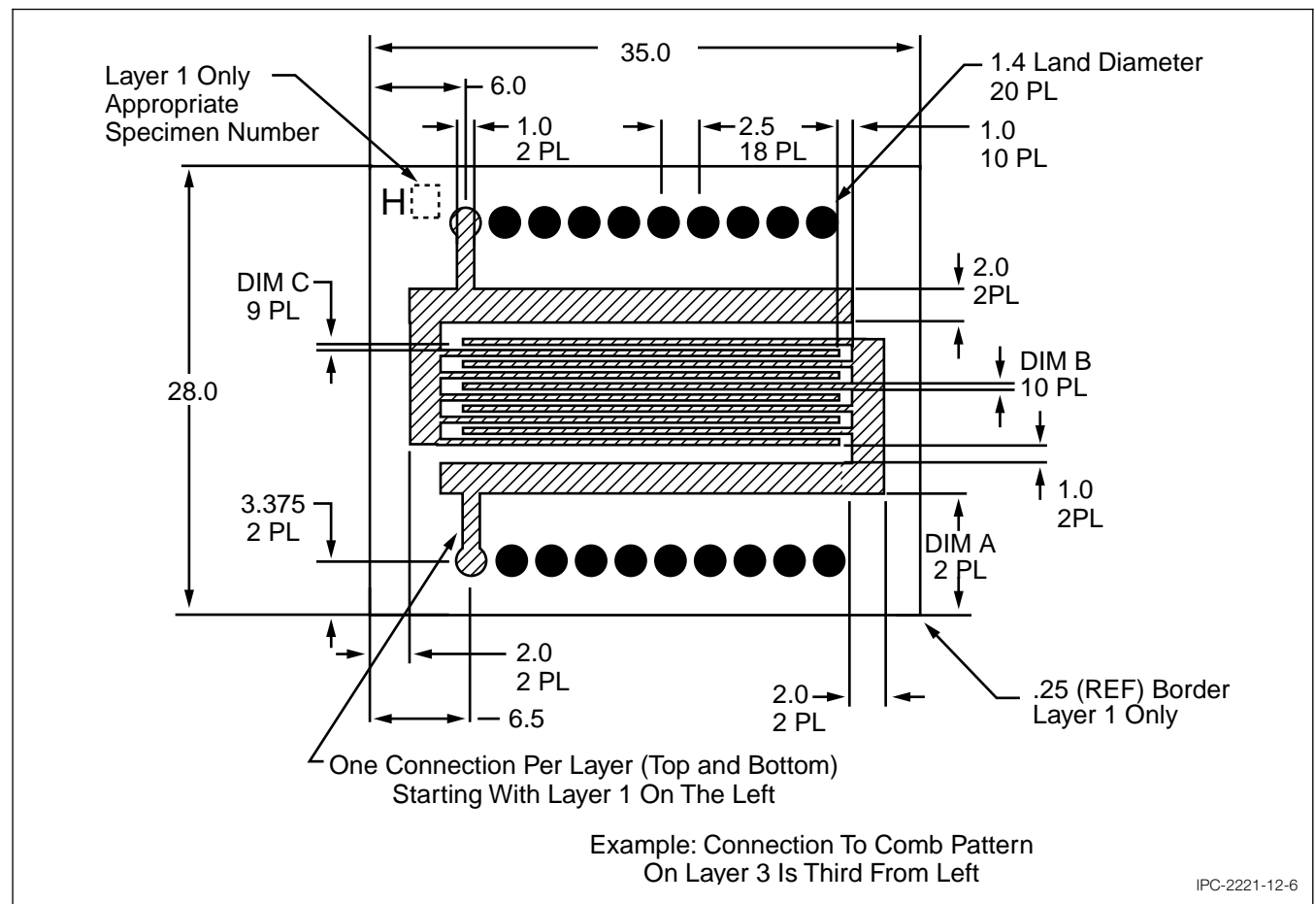
**Figure 12-9   Optional Specimen H, mm**
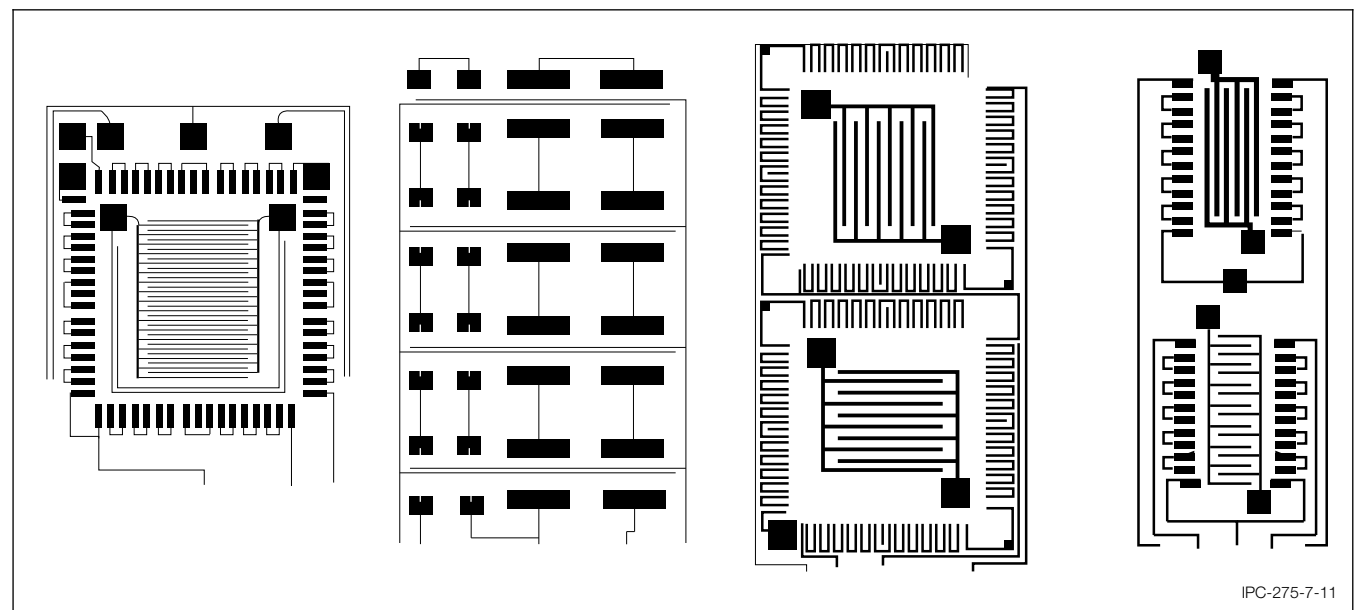


**Figure 12-10   Comb pattern examples**

IPC-275-7-12
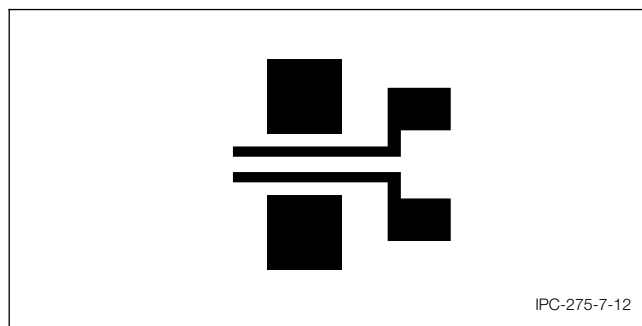
**Figure 12-11 "Y" pattern for chip component cleanliness test pattern**

hole will make contact with the plane. The center clearance area **shall** be designed for the worst case hole-to-pad diameter difference for the layer. Since the manufacturing allowance may vary from layer-to-layer, see Figure 12-14, the diameter of the artwork center clearance area **shall** be calculated for each internal layer separately as follows:

Clearance diameter = nominal drilled hole diameter + manufacturing allowance

Manufacturing allowance = smallest difference between any functional plated hole and land on that layer - 2X annular ring.

Evaluation of the specimen can only take place after determining the etch factor for each layer. The etch factor **shall** be determined before lamination as follows:

Etch loss = the diameter of the center clearance area after etch - the diameter of the center clearance on the artwork

The reference hole for annular ring evaluation will be to the left or the right of the center clearance area based on the etch factor. For example: If the etch factor is +0.1 mm, the reference hole **shall** be two holes to the right of the center clearance area. If the etch factor is -0.05 mm, the reference hole **shall** be one hole to the left of the center clearance area.

The specimen can be evaluated after drilling by measuring the annular ring using x-ray. To accept the specimen using x-ray, the reference hole **shall** not touch the plane.

The specimen are designed to measure annular ring after the holes are plated. The specimen are acceptable if there is no electrical connection between the reference hole and the tenth hole. The dimension of the annular ring can be determined by finding the first hole which makes electrical connection to the tenth hole and noting its position in relation to the reference hole. Each hole to the left or right of the reference hole represents a + 0.025 mm or -0.025 mm respectively to the reference annular ring. This specimen is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

**12.4.6 Specimen G (Solder Resist Adhesion)** The test specimen for evaluating solder resist adhesion **shall** be as shown in Figure 12-15. The artwork **shall** provide for solder resist to cover the entire specimen.

**12.4.7 Specimen M (Optional)** The specimen **shall** be as shown in Figure 12-16. This specimen may be used to evaluate solderability of surface mount lands This specimen is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

**12.4.8 Specimen N (Optional)** Specimen **shall** be as shown in Figure 12-17. This specimen may be used to evaluate the bond strength and peel strength of surface mount lands. This specimen is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

**12.4.9 Specimen S** This specimen is used to evaluate plated-through hole solderability when a larger population of holes is required. The general design of the coupon is shown in Figure 12-18. The hole diameter **shall** be 0.8 mm ± 0.13 mm required to be solder filled. This specimen is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

**12.4.10 Specimen T** This specimen **shall** be used to validate tenting characteristics when solder resists are used to tent plated-through holes (see 4.5.1). Specimen T is the same as shown in Figure 12-18 (specimen S) except that the entire specimen **shall** be covered with solder resist on both sides.

The hole diameter **shall** be the largest plated hole which will be tented with solder resist. This specimen is not referenced in IPC-6012. If it is used, the test method and performance criteria **shall** be specified in the procurement documentation.

**12.4.11 Process Control Test Specimen** Process control test specimen are used at strategic points in the process flow to evaluate a specific process or set of processes. The designs of the process control test specimen are at the option of the printed board fabricator. Each design is specific to the processes for which the fabricator intends to evaluate.

Process control evaluations are established through a systematic path for implementing statistical process control. This includes those items shown in Figure 12-19.

If the contract permits the use of process control specimen in lieu of conformance specimen, the design of the specimen **shall** be agreed to between the user and manufacturer.

.25 (ref) Border
layer 1 only

8.0

3.5
7 PL

F

Layer 1 only
appropriate
specimen number

6.5

4.0

35.0

Specimen placement point
intersection of border centerlines
(see chart)

Hole
1  2  3  4  5  6  7  8

Layer 1
2
3
4
5
6
7
8
9
10

**Option 1**

**Land Size** includes
an annular ring

**Option 2**

**Land Size** does not
include an annular ring

## Accept/Reject Criteria

MIN.
ANNULAR
RING

REDUCED
ANNULAR RING
OR BREAKOUT

**Option 1**

ACCEPT

REJECT

TANGENT

BREAKOUT

**Option 2**

ACCEPT

REJECT

IPC-2221-12-11

**Figure 12-12   Test Specimen F, mm**

The design of existing test specimen can serve as a guide for the design of process control test specimen. In general, the design of the specimen is consistent with the process to be evaluated rather than an attempt to represent a printed board design. Finished conductor width **shall** be 0.5 ± 0.07 mm and finished land size **shall** be 1.8 ± 0.13 mm. Hole size **shall** be consistent with process(es) being evaluated. The location of test specimen on the panel and hole diameters **shall** remain constant. The design dimensions may require compensation for process allowances.
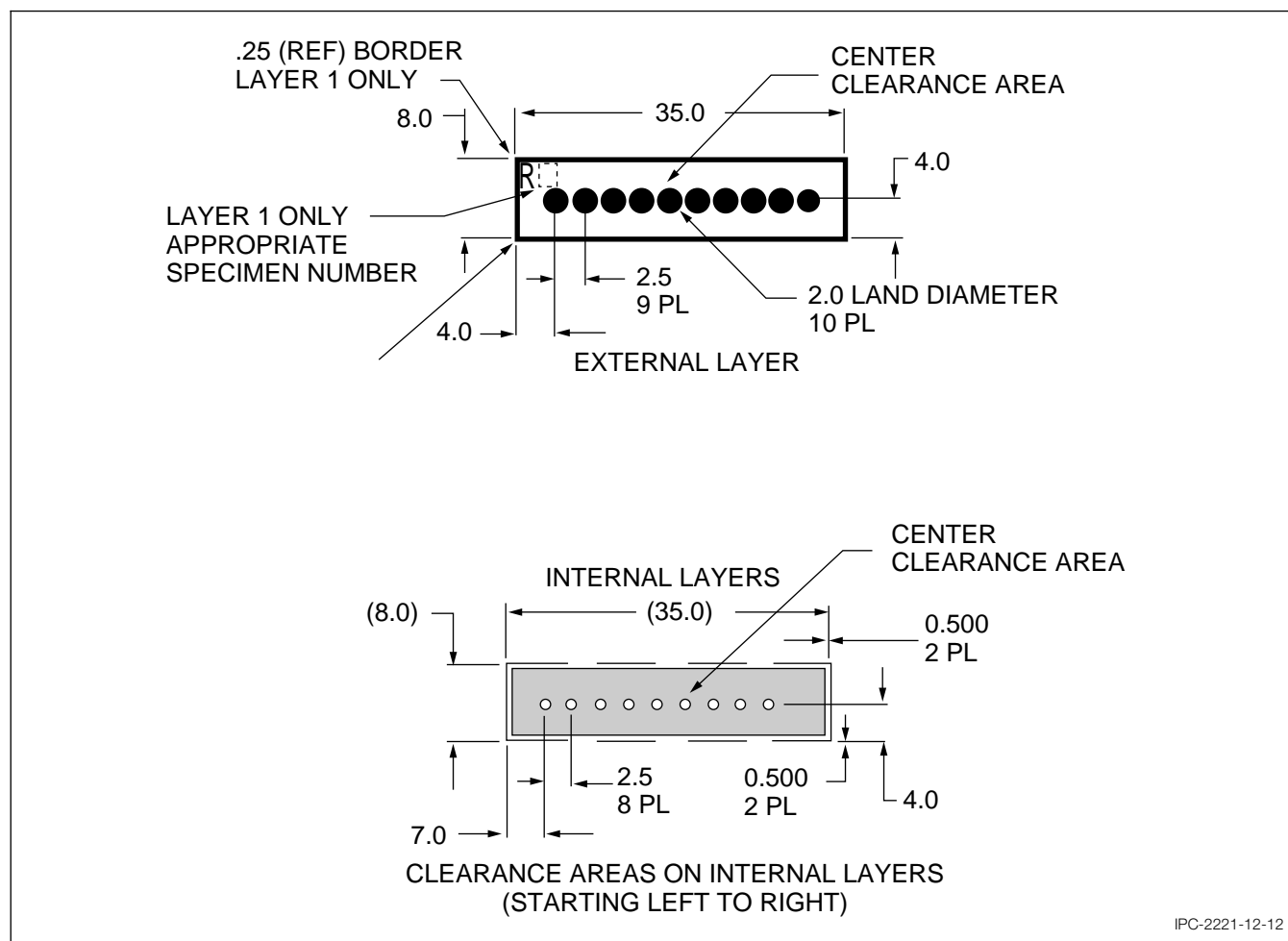
**Figure 12-13   Test Specimen R, mm**
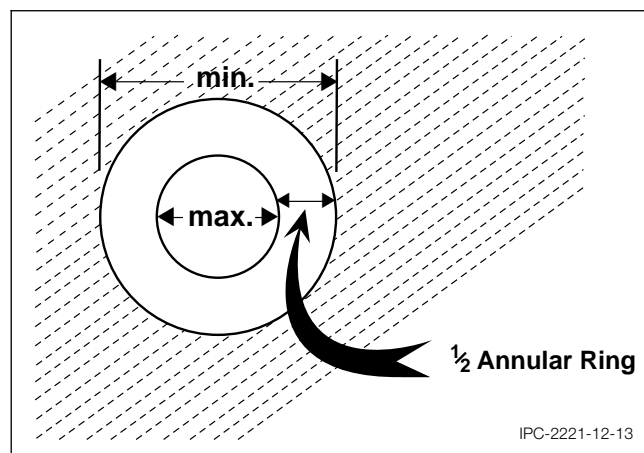


**Figure 12-14   Worst-case hole/land relationship**
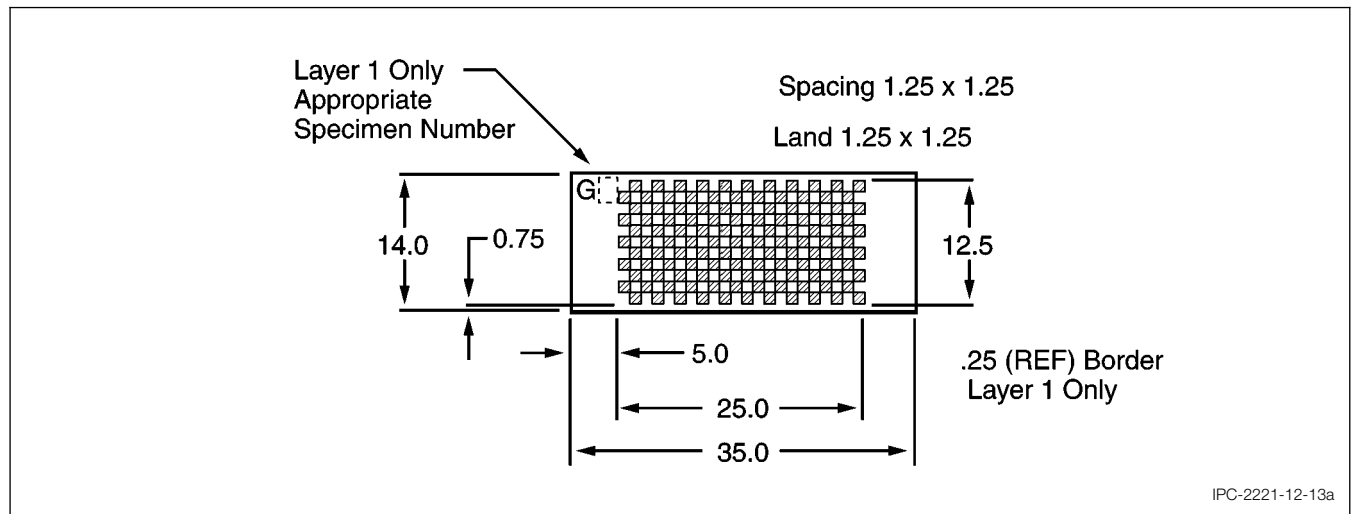
Figure 12-15   Test Specimen G, mm
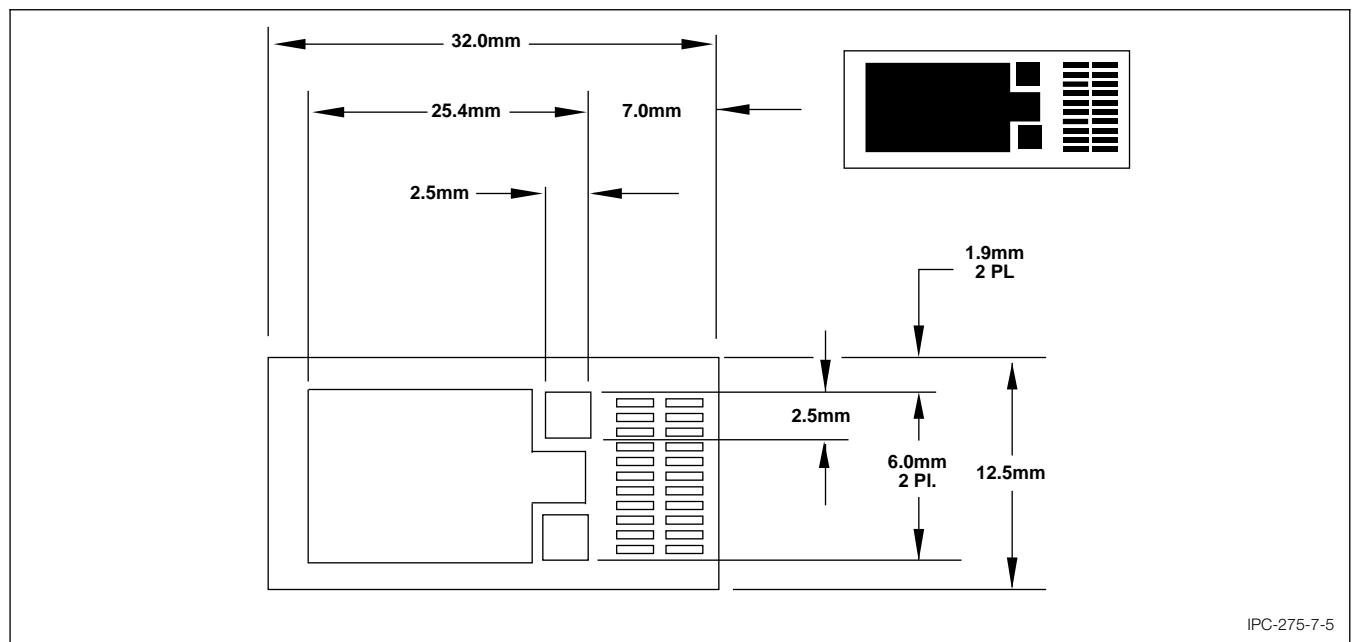


Figure 12-16   Test Specimen M, surface mounting solderability testing, mm
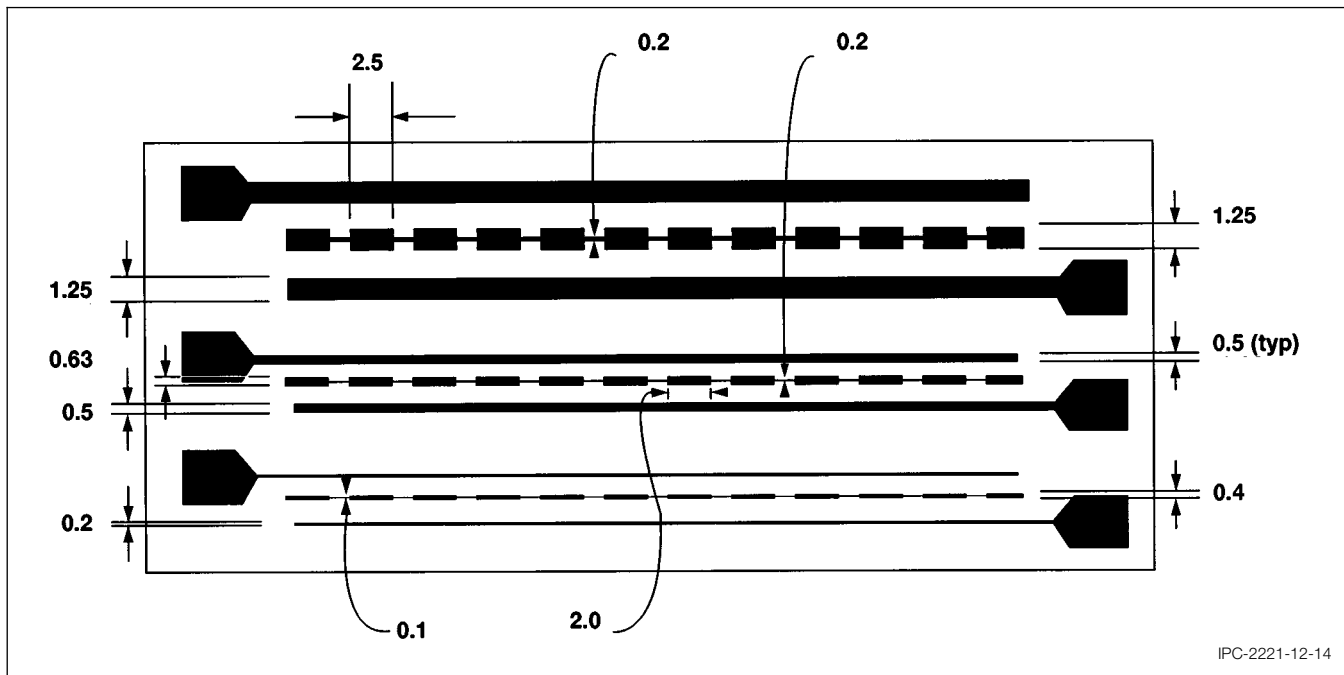
**Figure 12-17    Test Specimen N, surface mounting bond strength and peel strength, mm**
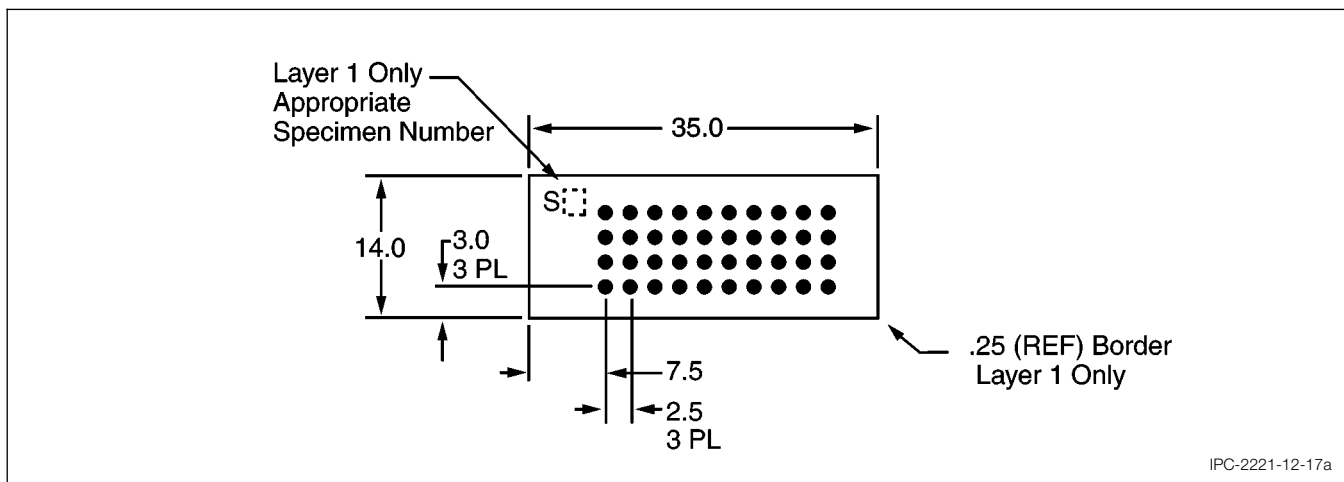


**Figure 12-18    Test Specimen S, mm**
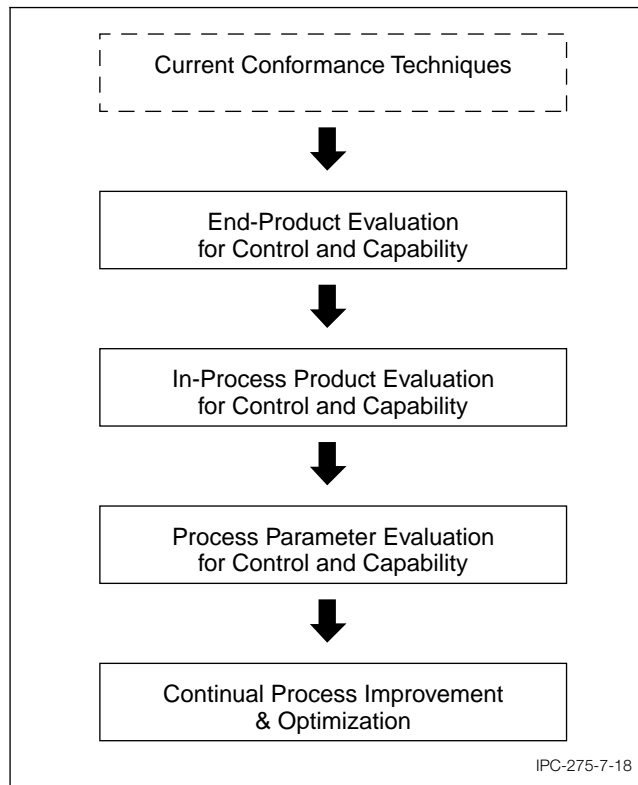
**Figure 12-19   Systematic path for implementation of statistical process control (SPC)**

# Appendix A
# Example of a Testability Design Checklist

- Route test/control points edge connector to enable monitoring and driving of internal board functions and to assist in fault diagnosis.

- Divide complex logic functions into smaller, combinational logic sections.

- Avoid one-shots; if used, route their signals to the edge connector.

- Avoid potentiometers and ''select-on-test'' components.

- Use a single, large-edge connector to provide input/output pins and test/control points.

- Make printed board input/output signal logic-compatible to keep test equipment interface costs low and give flexibility.

- Provide adequate decoupling at the board edge and locally at each integrated circuit.

- Provide signals leaving the board with maximum fan-out drive, or buffer them.

- Buffer edge-sensitive components from the edge connector - such as clock lines and flip-flop outputs.

- Do not tie signal outputs together.

- Never exceed the logic rated fan-out; in fact, keep it to a minimum.

- Do not use high fan-out logic devices. do use multiple fan-out devices, and keep their outputs separate.

- Keep logic depth on any board to a low level by using edge terminated test/control points.

- Single-load each signal entering the board whenever possible.

- Terminate unused logic pins with a resistive pull-up to minimize noise pick-up.

- Do not terminate logic outputs directly into transistor bases. do use a series current-limiting resistor.

- Buffer flip-flop output signals before they leave the board.

- Use open-collector devices with pull-up resistors to enable external override control.

- Avoid using redundant logic to minimize undetectable faults.

- Bring outputs of cascaded counters to higher- order counters so that they can be tested without large counts.

- Construct trees to check the parity of selected groups of eight bits or fewer.

- Avoid ''wired'OR'' and ''wired'AND'' connections.

- If you cannot, use gates from the same integrated circuit package.

- Provide some way to bypass level-changing diodes in series with logic out-puts.

- Break paths when a logic element fans out to several places that converge later.

- Use elements in the same integrated circuit package when designing a series of inverters or inverters following a gate function.

- Standardize power-on and ground pins to avoid test-harness multiplicity.

- Bring out test points as near to digital-to-analog conversion as possible.

- Provide a means of disabling on-board clocks so that the tester clock may be substituted.

- Provide mounted switches and resistor-capacitor networks with override lines to the edge-board connector.

- Route logic drivers of lamps and displays to the edge connector so that the tester can check for correct operation.

- Divide large printed boards into subsections whenever possible, preferably by function.

- Separate analog circuits from digital logic, except for timing circuits.

- Uniformly mount integrated circuits and clearly identify them to make it easier to locate them.

- Provide sufficient clearance around integrated circuit sockets and direct-soldered integrated circuits so that clips can be attached whenever necessary.

- Add top-hat connector pins or mount extra integrated circuit sockets when there are not enough edge-board connector pins for test/control points.

- Use sockets with complex integrated circuits and long, dynamic shift registers.

- Wire feedback lines and other complex circuit lines to an

- Use jumpers that can be cut during debugging. The jumpers can be located near the edge-board connector.

- Fix locations of power and ground lines for uniformity among several board types.

- Make the ground conductor large enough to avoid noise problems.

- Group together signal lines of particular families.

- Clearly label all parts, pins and connectors.

# INDEX

The following is an index of key subjects related to specific paragraph numbers in this standard. The index is organized alphabetically.

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2215 Sanders Road • Northbrook, IL 60062-6135

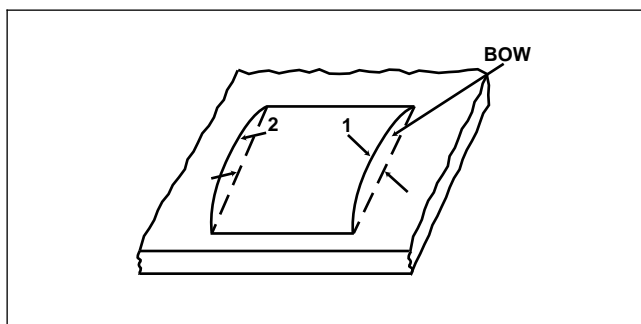| Number | |
|---|---|
| **2.4.22** | |
| Subject | |
| **Bow And Twist** | |
| Date | Revision |
| **12/87** | **B** |
| Originating Task Group | |
| **Printed Board Test Methods (7-11d)** | |

# IPC-TM-650
# TEST METHODS MANUAL



**Figure 1**

**1.0 Scope**   Four procedures are presented to determine the bow and twist of either cut to size panels or finished rigid printed circuit boards including single and double sided, multilayer and the rigid segments of rigid flex printed circuits.

**1.1 Definitions**

**1.1.1**   Bow is defined in IPC-T–50 as ''The deviation from flatness of a board characterized by a roughly cylindrical or spherical curvature such that if the board is rectangular its four corners are in the same plane (see Figure 1).''

**1.1.2**   Twist is defined in IPC-T–50 as ''The deformation of a board parallel to a diagonal of a rectangular sheet such that one of the corners is not in the plane containing the other three corners (see Figure 2).''

**2.0 Applicable Documents**

**IPC–T–50**   Terms and Definitions

**3.0 Test Specimen**

**3.1 Specimens**

**3.1.1**   Cut-to-size panels

**3.1.2**   Finished boards (single side, double sided, multilayer, rigid/flex finished board or coupons)

**4.0 Apparatus**

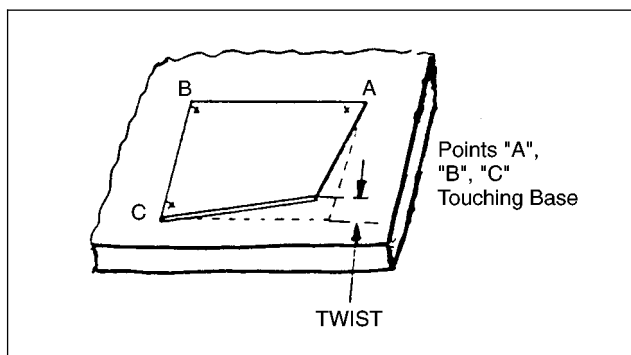**4.1**   Precision surface plate



**Figure 2**

**4.2**   Standard metrology height dial indicator gauge

**4.3**   Thickness measurement feeler gauges

**4.4**   Standard pin gauges

**4.5**   Leveling jacks

**4.6**   Gauge blocks

**4.7**   Shims of suitable thickness

**4.8**   Linear measuring devices of suitable accuracy

**4.9**   One inch micrometer

**5.0 Procedures**

**5.1**   Procedure No. 1 (Bow) (As illustrated in Figure 1)

**5.1.1**   Place the sample to be measured on the datum surface with the convex of the sample facing upwards. For each edge, apply sufficient pressure on both corners of the sample to insure contact with the surface. Take a reading with the dial indicator at the maximum vertical displacement of this edge denoted as R1 in Figure 3.

Repeat this procedure until all four edges of the sample have been measured. It may be necessary to turn the sample over to accomplish this. Identify the edge with the greatest deviation from the datum. This is the edge to be measured per paragraph 5.1.2 and 5.1.3.
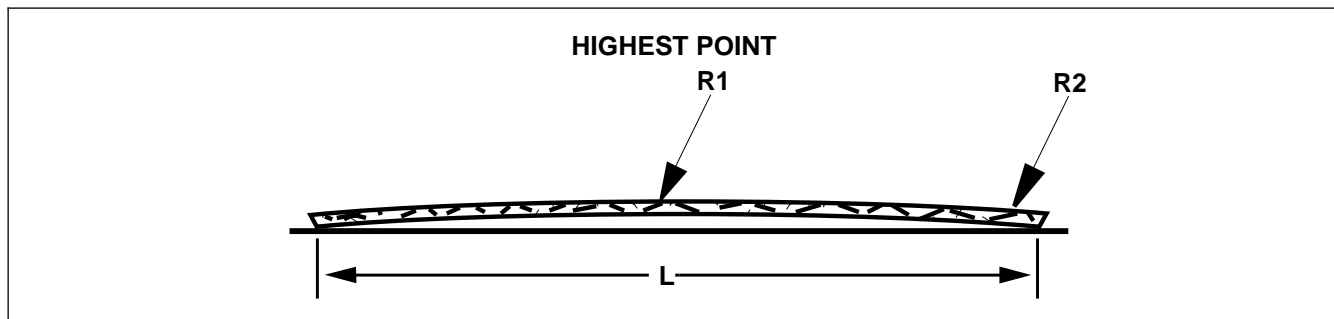
**HIGHEST POINT**

**R1**　　　　**R2**

**L**

**Figure 3**

**5.1.2**  Take a reading with the dial indicator at the corner of the sample contacting the datum surface, or determine R2 by measuring the thickness of the sample with a micrometer (denoted R2 in Figure 3).

**5.1.3**  Apply sufficient pressure so that the entire edge contacts the datum surface. Measure the length of the edge and denote as ''L''.

**5.1.4**  Calculate bow for this edge as follows:

$$\text{Percent Bow} = \frac{R1 - R2}{L} \text{ X } 100$$

The result of this calculation is the % of bow.

Repeat the procedure for the other three edges and record the largest value % of bow for the sample.

**5.2  Procedure No. 2 (Twist)**

**5.2.1**  Place the sample to be measured on the datum surface with any three corners of the sample touching the surface. Apply sufficient pressure to insure that three corners are in contact with the datum surface. Take a measurement from the datum surface to the lifted corner and record the reading.

Repeat this procedure until all four corners of the sample have been measured. It may be necessary to turn the sample over to accomplish this. Identify the corner with the greatest deviation from the datum. This is the corner to be measured per paragraph 5.2.2 and 5.2.3.

**5.2.2**  Place the sample to be measured on the datum surface with three corners touching the surface, insert suitable shims under the raised corner so that it is just supported.

When the correct shim thickness is used the three corners will be in contact with the datum surface without applying pressure to any corner.

**5.2.3**  Without exerting any undue pressure on the sample, take a reading with the dial indicator at the maximum vertical displacement (denoted R1 in Figure 4) and record the reading.

Without disturbing the sample, take a reading with the dial indicator on the topic surface of the sample at the edge contacting the datum surface or determine R2 by measuring the thickness of the sample with a micrometer.

*Note:* For fabricated boards, both readings must be made on base material.

**5.2.4**  Measure the diagonal of the sample (for rectangular boards) and record the reading. For nonrectangular boards measure from the corners exhibiting displacement diagonally to the point on the opposite end of the board.

**5.2.5  Calculation**

**5.2.5.1**  Deduct R2 reading from R1 reading (this value is divided by 2 in the formula defined in 5.2.5.2 because of the method of measurement) doubles the vertical defection.

**5.2.5.2**  Divide the measured deviation (para. 5.2.5.2) by the recorded length and multiply by 100. The result of this calculation is the % of twist.

$$\text{Percent Twist} = \frac{R1 - R2}{(2)\ (\text{Length})} \text{ X } 100$$
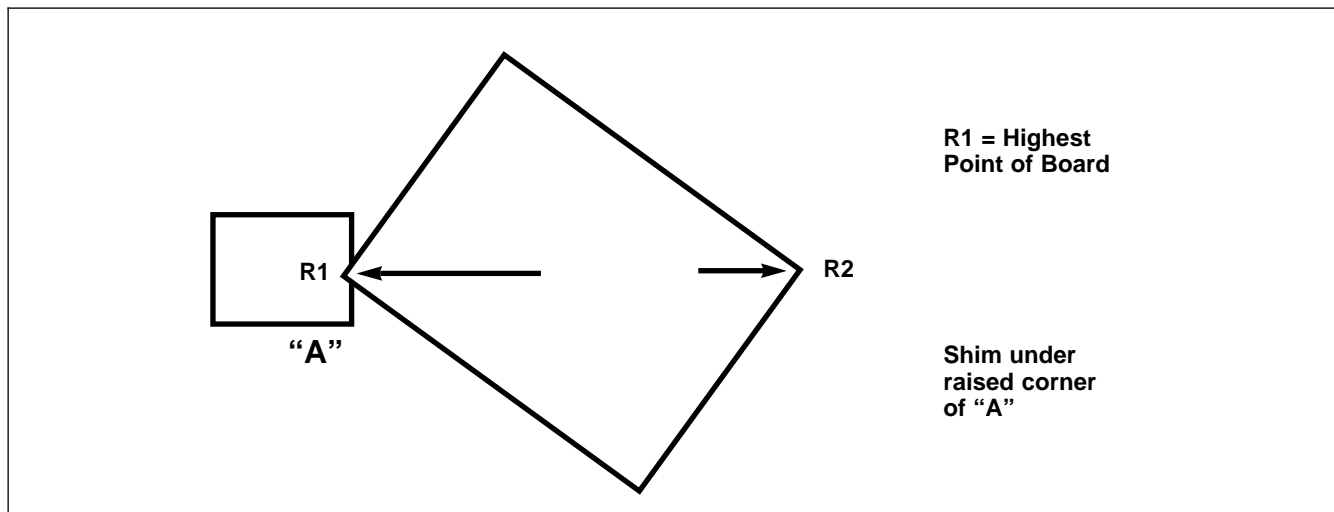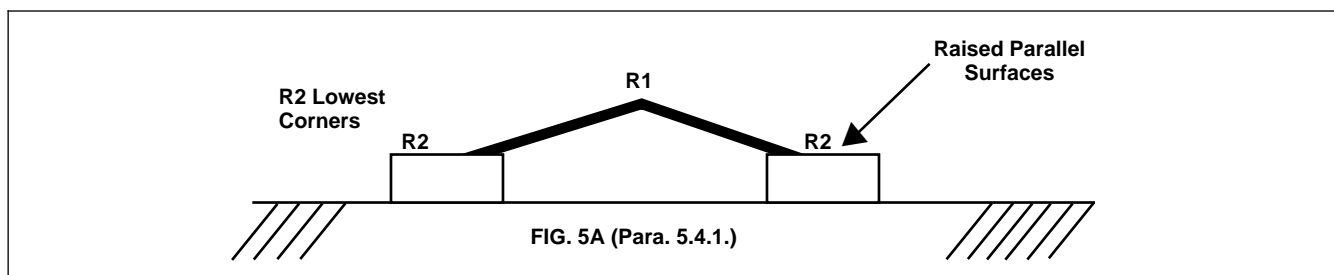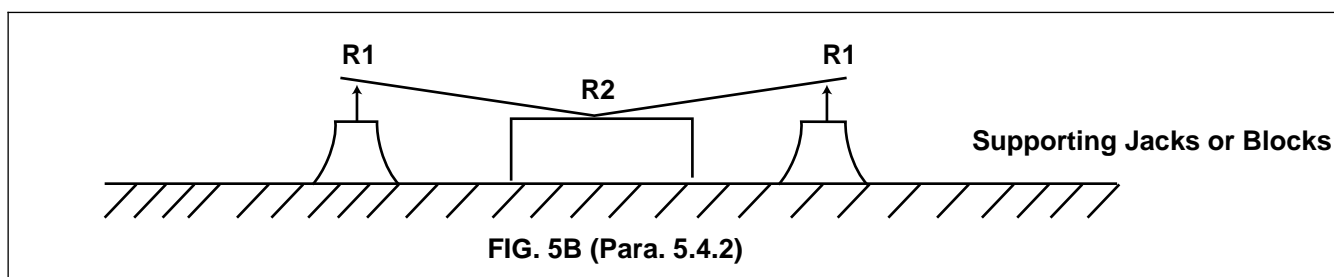
**Figure 4**



**Figure 5a**



**Figure 5b**

**5.3  Procedure No. 3 Twist Referee Test**

**5.3.1**  Place the sample to be measured on the datum surface with the two lower opposite corners touching the datum surface or on raised parallel surfaces of equal height from the datum surface (Figure 5A).

**5.3.2**  Support the other two corners with leveling jacks or other appropriate devices ensuring that the two raised corners are of equal height from the datum surface. This may be checked by using the dial indicator (Figure 5B).

**Figure 5c**



**Figure 6**



**Figure 7**

**5.3.3** With the dial indicator, measure the highest raised portion on the board and record the reading as R1 (Figure 5C).

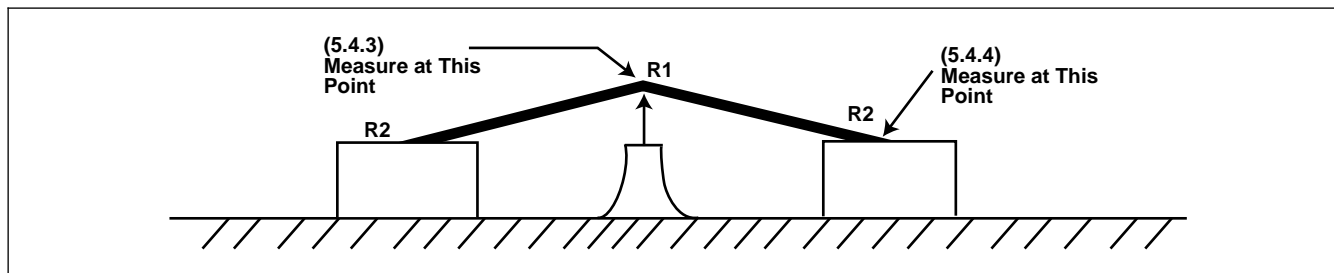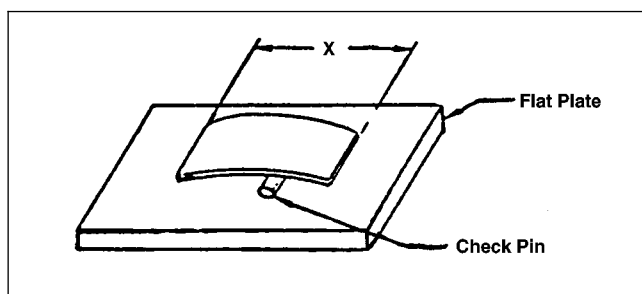**5.3.4** Without disturbing the sample, take a reading with the dial indicator on one of the corners contacting the surface (R2) and record the reading (Figure 5C).

**5.3.5** Measure the diagonal of the sample (for rectangular boards) and record the reading. For nonrectangular boards measure from the corner exhibiting maximum displacement diagonally to the point on the opposite end of the board.

**5.3.6 Calculation**

**5.3.6.1** Deduct the measurement R2 from the measurement R1. This difference is denoted as twist.

**5.3.6.2** Divide the measured deviation (para. 5.3.6.1) by the recorded length and multiply by 100. The result of this calculation is the % of twist.

$$\text{Percent Twist} = \frac{R1 - R2}{L} \times 100$$
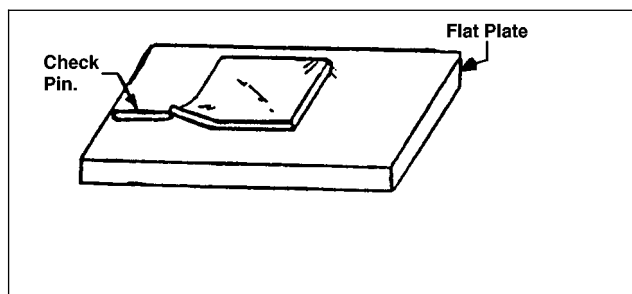
**5.4 Procedure 4, Production Testing** (Bow and Twist)

Having previously determined the maximum allowable deviation of a board from a flat plane, the following GO-NO GO procedures may be used.

**5.4.1** With both corners of an edge touching the datum surface and using a suitable known dimensional standard such as a pin gauge or feeler gauge, conforming to the maximum allowable deviation (5.4), attempt to insert the gauge between the raised portion of the board and the datum surface (Figure 6).

**5.4.2** Attempt to insert gauge conforming to the allowable surface dimension between the raised edge of the board and the datum (Figure 7).

**5.4.3** If the gauge does not enter the gap, the board will have met the bow/twist criteria.

**5.5 Notes**

**5.5.1** Forms of distortion other than as defined in this test method (such as multiple convolutions) cannot be evaluated accurately by these test methods and therefore should receive special attention.

# IPC

## Standard Improvement Form

**IPC-2221**

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:
IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax 847 509.9798

1. I recommend changes to the following:

    ___ Requirement, paragraph number _____

    ___ Test Method number _____ , paragraph number _____

    The referenced paragraph number has proven to be:

    ___ Unclear    ___ Too Rigid    ___ In Error

    ___ Other _____

2. Recommendations for correction:

    _____

    _____

    _____

    _____

3. Other suggestions for document improvement:

    _____

    _____

    _____

    _____

Submitted by:

Name _____    Telephone _____

Company _____    E-mail _____

Address _____

City/State/Zip _____    Date _____

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# ANSI/IPC-T-50 Terms and Definitions
# for Interconnecting and Packaging Electronic Circuits
# Definition Submission/Approval Sheet

**IPC**

*THE INSTITUTE FOR*

*INTERCONNECTING*

*AND PACKAGING*

*ELECTRONIC CIRCUITS*

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax: 847-509-9798

SUBMITTOR INFORMATION:

Name: _____

Company: _____

City: _____

State/Zip: _____

Telephone: _____

Date: _____

❑ This is a **NEW** term and definition being submitted.
❑ This is an **ADDITION** to an existing term and definition(s).
❑ This is a **CHANGE** to an existing definition.

| Term | Definition |
|------|------------|
|      |            |
|      |            |
|      |            |
|      |            |
|      |            |

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ❑ Not Applicable  ❑ Required  ❑ To be supplied
❑ Included: Electronic File Name: _____

Document(s) to which this term applies: _____
_____
_____

Committees affected by this term: _____
_____
_____

---

**Office Use**

| IPC Office | Committee 2-30 |
|------------|----------------|
| Date Received: _____ | Date of Initial Review: _____ |
| Comments Collated: _____ | Comment Resolution: _____ |
| Returned for Action: _____ | Committee Action:  ❑ Accepted  ❑ Rejected |
| Revision Inclusion: _____ | ❑ Accept Modify |

**IEC Classification**

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:

Committee 2-30 has approved the above term for release in the next revision.

Name: _____  Committee: ___IPC 2-30___  Date: _____

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## Technical Questions

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

tel 847/509-9700            fax 847/509-9798
http://www.ipc.org         e-mail: answers@ipc.org

## IPC Technical Forums

IPC technical forums are opportunities to network on the Internet. It's the best way to get the help you need today! Over 2,500 people are already taking advantage of the excellent peer networking available through e-mail forums provided by IPC. Members use them to get timely, relevant answers to their technical questions.

### TechNet@ipc.org

TechNet forum is for discussion of technical help, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

### ChipNet@ipc.org

ChipNet forum is for discussion of flip chip and related chip scale semiconductor packaging technologies. It is cosponsored by the National Electronics Manufacturing Initiative (NEMI).

### ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

### DesignerCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comment, and feedback on current design issues,local chapter meetings, new chapters forming, and other design topics.

### Roadmap@ipc.org

The IPC Roadmap forum is the communication vehicle used by members of the Technical Working Groups (TWGs) who develop the IPC National Technology Roadmap for Electronic Interconnections.

### IPCsm840@ipc.org

This peer networking forum is specific to solder mask qualification and use.

### ADMINISTERING YOUR SUBSCRIPTION STATUS:

All commands (such as subscribe and signoff) must be sent to listserv@ipc.org. Please DO NOT send any command to the mail list address, (i.e.<mail list> @ipc.org), as it would be distributed to all the subscribers.

| Example for subscribing: | Example for signing off: |
| --- | --- |
| To: LISTSERV@IPC.ORG | To: LISTSERV@IPC.ORG |
| Subject: | Subject: |
| Message: subscribe TechNet Joseph H. Smith | Message: sign off DesignerCouncil |

Please note you must send messages to the mail list address ONLY from the e-mail address to which you want to apply changes. In other words,if you want to sign off the mail list, you must send the signoff command from the address that you want removed from the mail list. Many participants find it helpful to signoff a list when travelling or on vacation and to resubscribe when back in the office.

### How to post to a forum:

To send a message to all the people currently subscribed to the list, just send to <mail list>@ipc.org Please note, use the mail list address that you want to reach in place of the <mail list> string in the above instructions.

Example:
To: TechNet@IPC.ORG
Subject: <your subject>
Message: <your message>

The associated e-mail message text will be distributed to everyone on the list, including the sender. Further information on how to access previous messages sent to the forums will be provided upon subscribing.

For more information, contact Dmitriy Sklyar
tel 847/509-9700 x311        fax 847/509-9798
e-mail: sklydm@ipc.org       http://www.ipc.org/html/forum.htm

BENEFITS OF IPC MEMBERSHIP

# IPC World Wide Web Page  http://www.ipc.org

Our home page provides access to information about upcoming events, publications and videos, membership, and industry activities and services.  Visit soon and often.

## Education and Training

IPC conducts local educational workshops and national conferences to help you better understand emerging technologies.  National conferences have covered Ball Grid Array and Flip Chip/Chip Scale Packaging.  Some workshop topics include:

| | |
|---|---|
| Printed Wiring Board Fundamentals | High Speed Design |
| Troubleshooting the PWB Manufacturing Process | Design for Manufacturability |
| Choosing the Right Base Material Laminate | Design for Assembly |
| Acceptability of Printed Boards | Designers Certification Preparation |
| New Design Standards | |

IPC video tapes and CD-ROMs can increase your industry know-how and on the job effectiveness.

For more information on programs, contact John Riley
tel 847/509-9700 ext. 308        fax 847/509-9798
e-mail:  rilejo@ipc.org                http://www.ipc.org

For more information on IPC Video/CD Training, contact Mark Pritchard
tel 505/758-7937 ext. 202        fax 505/758-7938
e-mail:  markp@taos.newmex.com
http://www.ipc.org

## Training and Certification
### IPC-A-610 Training and Certification Program

"The Acceptability of Electronic Assemblies" (ANSI/IPC-A-610) is the most widely used specification for the PWB assembly industry.  An industry consensus Training and Certification program based on the IPC-A-610 is available to your company.
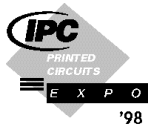
For more information, contact John Riley
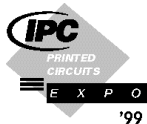tel 847/509-9700 ext. 308        fax 847/509-9798
e-mail:  rilejo@ipc.org                http://www.ipc.org/html/610.htm

## IPC Printed Circuits Expo

IPC Printed Circuits Expo is the largest trade exhibition in North America devoted to the PWB industry.  Over 90 technical presentations make up this superior technical conference.

April 28-30, 1998
Long Beach, California
'98

March 16-18, 1999
Long Beach, California
'99

For more information, contact Kim Behr
tel 847/509-9700 ext. 319        fax 847/509-9798
e-mail:  behrki@ipc.org              http://www.ipc.org

## How to Get Involved

The first step is to join IPC. An application for membership can be found on page 74.
Once you become a member, the opportunities to enhance your competitiveness are vast.  Join a technical committee and
learn from our industry's best while you help develop the standards for our industry.  Participate in market research programs which forecast the future of our industry.  Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support.  Pick from a wide variety of educational opportunities:  workshops, tutorials, and conferences.  More up-to-date details on IPC opportunities can be found on our web page: http:/www.ipc.org.

For information on how to get involved, contact:
Jeanette Ferdman, Membership Manager
tel 847/509-9700 ext. 309        fax 847/509-9798
e-mail:  JeanetteFerdman@ipc.org        http://www.ipc.org

# A P P L I C A T I O N   F O R   S I T E   M E M B E R S H I P

**IPC**

Thank you for your decision to join IPC members on the "Intelligent Path to Competitiveness"! IPC Membership is **site specific,** which means that IPC member benefits are available to all individuals employed at the site designated on the other side of this application.

To help IPC serve your member site in the most efficient manner possible, please tell us what your facility does by choosing the most appropriate member category.

**PLEASE CHECK APPROPRIATE CATEGORY**

---

■ **INDEPENDENT PRINTED BOARD MANUFACTURERS**

Our facility manufactures and sells to other companies, printed wiring boards or other electronic interconnection products on the merchant market.

WHAT PRODUCTS DO YOU MAKE FOR SALE?

☐ One-sided and two-sided rigid printed boards
☐ Multilayer printed boards

☐ Flexible printed boards
☐ Flat cable
☐ Hybrid circuits

☐ Discrete wiring devices
☐ Other interconnections

Name of Chief Executive Officer/President_____

---

■ **INDEPENDENT PRINTED BOARD ASSEMBLERS EMSI COMPANIES**

Our facility assembles printed wiring boards on a contract basis and/or offers other electronic interconnection products for sale.

☐ Turnkey
☐ SMT
☐ Chip Scale Technology

☐ Through-hole
☐ Mixed Technology

☐ Consignment
☐ BGA

Name of Chief Executive Officer/President_____

---

■ **OEM – MANUFACTURERS OF ANY END PRODUCT USING PCB/PCAS OR CAPTIVE MANUFACTURERS OF PCBS/PCAS**

Our facility purchases, uses and/or manufactures printed wiring boards or other electronic interconnection products for our own use in a final product. Also known as original equipment manufacturers (OEM).

IS YOUR INTEREST IN:
☐ purchasing/manufacture of printed circuit boards
☐ purchasing/manufacturing printed circuit assemblies

What is your company's main product line? _____

---

■ **INDUSTRY SUPPLIERS**

Our facility supplies raw materials, machinery, equipment or services used in the manufacture or assembly of electronic interconnection products.
What products do you supply?_____

---

■ **GOVERNMENT AGENCIES/ ACADEMIC TECHNICAL LIAISONS**

We are representatives of a government agency, university, college, technical institute who are directly concerned with design, research, and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)

---

**Please be sure both sides of this application are correctly completed**

# IPC  APPLICATION FOR SITE MEMBERSHIP

**Site Information:**

Company Name

Street Address

City                    State          Zip            Country

Main Phone No.                    Fax

Primary Contact Name

Title                    Mail Stop

Phone                    Fax                    e-mail

Alternate Contact Name

Title                    Mail Stop

Phone                    Fax                    e-mail

---

**Please check one:**

❏  $1,000.00    Annual dues for Primary Site Membership (Twelve months of IPC membership begins from the time the application and payment are received)

❏  $800.00    Annual dues for Additional Facility Membership: Additional membership for a site within an organization where another site is considered to be the primary IPC member.

❏  $600.00**    Annual dues for an independent PCB/PWA fabricator or independent EMSI provider with annual sales of less than $1,000,000.00. **Please provide proof of annual sales.

❏  $250.00    Annual dues for Government Agency/University/not-for-profit organization

**TMRC Membership** ❏ Please send me information on Membership in the Technology Marketing Research Council (TMRC)

**AMRC Membership** ❏ Please send me information for Membership in the Assembly Marketing Research Council (AMRC)

---

**Payment Information**

Enclosed is our check for $_____

Please bill my credit card: (circle one)  MC   AMEX  VISA   DINERS

Card No. _____    Exp date _____

Authorized Signature _____

---

**Mail application with check or money order to:**

IPC
Dept. 77-3491
Chicago, IL 60678-3491

**Fax/Mail application with credit card payment to:**

IPC
2215 Sanders Road
Northbrook, IL  60062-6135
Tel:  847 509.9700
Fax: 847 509.9798

**PLEASE ATTACH BUSINESS CARD OF OFFICIAL REPRESENTATIVE HERE**