Single Phase Compact DC-AC Power Converter for Medium and High-Power Applications

B.TECH. PROJECT

by

ACHINTYA PRATAP

SHEKHAR SINGH

ABHISHEK BHARDWAJ

AHSAN WASEEM

Under the Supervision of

Dr. M SAAD BIN ARIF

(Assistant Professor)

Z.H.C.E.T, A.M.U

DEPARTMENT OF ELECTRICAL ENGINEERING

Z.H.C.E.T., ALIGARH MUSLIM UNIVERSITY

ALIGARH – 202002 (INDIA)

MAY, 2024

CANDIDATE'S DECLARATION

We hereby certify that the work which is being presented in the project entitled "**SINGLE PHASE COMPACT DC-AC POWER CONVERTER FOR MEDIUM AND HIGH-POWER APPLICATIONS**" in partial fulfilment of the requirements for the award of the Degree of Bachelor of Technology and submitted in the Department of Electrical Engineering, Zakir Hussain College of Engineering and Technology of the Aligarh Muslim University, Aligarh is an authentic record of our work carried out during a period from August, 2023 to May, 2024 under the supervision of Dr M Saad Bin Arif, Assistant Professor, Department of Electrical Engineering, Z.H.C.E.T, Aligarh Muslim University, Aligarh, India.

The matter presented in this project has not been submitted by us for the award of any other degree of this or any other Institute.

ACHINTYA PRATAP	SHEKHAR SINGH	ABHISHEK BHARDWAJ	AHSAN WASEEM
20EEB227	20EEB232	20EEB233	20EEB262
GL9736	GL9681	GJ8535	GJ2773

This is to certify that the above statement made by the candidates is correct to the best of my knowledge.

(SUPERVISIOR)

ABSTRACT

DC-AC converters, play a crucial role in modern society by facilitating the conversion of DC power from sources like batteries, solar panels, and fuel cells into AC power usable by a wide range of devices and systems. This conversion is essential for various applications, including residential and commercial electricity supply, renewable energy integration, motor drives, and grid-tied systems. Multilevel inverters (MLIs) have gained attraction in various industries due to their ability to efficiently manage medium-voltage power applications. Moreover, advancements in MLI technology hold potential for further innovations in electric vehicles, and industrial automation, driving the transition towards a cleaner and more sustainable energy future. However, their widespread adoption faces hurdles such as high device count, size, cost, and control complexities. Traditional two-level inverters face limitations in voltage levels and device stress, leading to increased power losses and reduced reliability. To overcome these challenges, multilevel inverters (MLIs) have emerged as promising alternatives. MLIs utilize stacked power semiconductor devices to achieve higher voltage levels, reducing stress on individual components and improving system reliability. This study explores different MLI topologies, including conventional and recently proposed topologies assessing their performance and applicability across various scenarios. This work proposed an improved asymmetrical single-phase multilevel inverter (MLI) topology designed to reduce the number of DC sources, switch count, and overall cost. The proposed topology achieves 19 voltage levels at the output using only 12 power switches and 3 DC sources. MATLAB/Simulink simulations validate the circuit's performance, while PLECS software is employed for loss analysis and efficiency calculation. Cost factor and reliability analysis are also conducted to evaluate the economic feasibility of the converter. Comparative analysis with existing topologies demonstrates the effectiveness of the proposed circuit.

ACKNOWLEDGEMENT

We would like to thank our supervisor for his guidance to the work described in this report entitled "**SINGLE PHASE COMPACT DC-AC POWER CONVERTER FOR MEDIUM AND HIGH-POWER APPLICATION**". Our foremost thanks go to our academic supervisor, **Dr. M.Saad Bin Arif** (Assistant Professor), for accepting us into his group. During our course, he contributed a great experience by giving us intellectual freedom in our work, engaging us in new ideas, and demanding a high quality of work in all our endeavours. He has been actively interested in our work and has always been available to advise us. We are very grateful for his patience, motivation, enthusiasm, and immense knowledge in Electrical Engineering that, taken together, make him a great mentor.

We are deeply grateful to the Chairman, Department of Electrical Engineering, Z.H.C.E.T., Aligarh Muslim University for providing the required facilities throughout the project work. We are also grateful to entire Faculty and staff members of Electrical Engineering Department, Aligarh Muslim University, Aligarh-202002, India.

Achintya Pratap
Shekhar Singh
Abhishek Bhardwaj
Ahsan Waseem

CONTENTS

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Introduction

The big issue with two-level square wave and PWM inverters is that, for medium and high power systems, they require devices of high power rating which is not easy to find and hence to serve the purpose many devices need to be connected in series/parallel strings to obtain the required voltage/current capacity. Multilevel inverters (MLIs) are an advanced version of a two-level inverter suitable for medium and high-power applications. Multilevel converters consist of a network of power semiconductors and capacitive voltage sources. When these components are appropriately interconnected and regulated, the converter can produce a stepped voltage waveform closer to sinusoidal[1]. Various energy sources, such as batteries, capacitors, fuel cells, and solar panels, can be combined to power a system. Power switches are controlled using specific algorithms to merge these energy sources, resulting in a high output voltage. Additionally, the voltage blocking of each switch depends on the combined DC sources connected to it at any given time, reducing the voltage stress on individual switches compared to their operating voltage. Increasing the number of voltage levels in the output requires more power electronic switches, DC sources, driver circuits, heat sinks, and protection circuits. This leads to higher costs, more complex control, and decreased reliability of the inverter. An efficient and cost-effective power converter is necessary for modern power needs. Multilevel inverters (MLIs) have become popular for medium-voltage applications because of advanced switching devices. However, despite their potential in industry, MLIs are held back by their high number of parts, large size, cost, and complex controls, limiting their use. Researchers are continously working to overcome these disadvantages of MLIs and to develop an efficient topology. Multilevel converters find applications in diverse fields such as industrial drives, Flexible AC Transmission Systems (FACTS), High-Voltage Direct Current (HVDC) transmission, marine propulsions, electric vehicles and active filters.

1.2 Features and Importance of MLIs

Some of the important features of the MLI are as follows:

- Use of several levels of DC-voltage enables MLI to achieve better quality output voltages with extremely low distortions and lower dv/dt. Hence, associated problems are substantially reduced.
- Reduced voltage stress is offered on switching devices.
- They require more device count, but they are modular in configuration and compact as they require reduced size output filter.
- Less Electromagnetic interference can be achieved in MLI.
- They can operate with a lower switching frequency while giving same output waveform quality as compared to two-level inverter.

The growing emphasis on renewable energy sources including solar photovoltaic (SPV) generation, wind energy generation system has motivated researchers to explore innovative technologies that can integrate with renewable energy systems.

This heightened interest is driven by the numerous advantages that these technologies offer over conventional two-level converters such as generation of higher power quality waveforms which lead to reduce harmonic content, lower electromagnetic compatibility concerns as they can produce near sinusoidal voltage waveform with lower dv/dt stress, and a modular structure making them highly attractive for various applications. Modular structure of a MLI leads to a more economical life cycle as these designs allow easier maintenance and can be scaled more easily and also have a better fault tolerant ability.

1.3 Conventional Multilevel Inverter

The three conventional topologies of the multilevel inverter are Diode Clamped or Neutral Point Clamped, Flying Capacitor and Cascaded H-bridge multilevel converter. These conventional topologies can be classified as Seperate DC source and Common DC source. Cascaded converters come under separate DC source topology while Diode Clamped Converter and Flying Capacitor converters are in Common DC source topology[2]. These conventional topologies are facing the disadvantages of having large number of devices. As the number of output voltage levels increases, the number of required components also increases accordingly. The consequence of this exponential increment in the number of power switches is that the complexity and size of the MLI increases substantially with the number of levels. This can lead to higher costs, increased losses, and more challenging control and thermal management. However, it is important to note that the benefit of having more levels lies in the ability to synthesize a smoother output voltage waveform, which can help to eliminate or reduce the size of output filter.

1.4 Objective

1. Study of different multi-level inverter topologies and switching techniques.
2. To develop reduced switch count MLI topology.
3. To analyse the performance of developed topology operating under different loading conditions

1.5 Organization of the Report

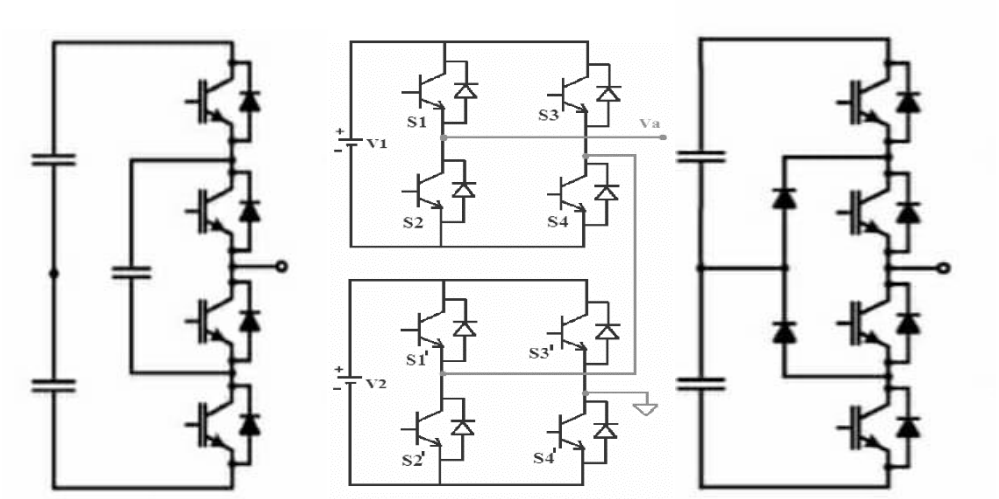
This study focuses on reducing the component count of multilevel inverters. The proposed topology can be easily cascaded to increase the number of voltage levels. The report is organized into four chapters. Chapter 2 presents Literature Review of different MLIs topologies, Chapter 3 presents the circuit description, including the switching table, modulation scheme, switch ratings, generalized structure of the topology, cost analysis and reliability of the converter. In Chapter 4, detailed simulations are discussed for static and dynamic loads both, validating the circuit's performance additionally conducts power loss analysis, with results presented graphically and compares the proposed topology with similar ones. Finally, the report concludes with a discussion of its findings.

Chapter 2

Literature Review

2.1 Introduction

In the literature, there exists a variety of multilevel inverter (MLI) topologies, broadly categorized into conventional and advanced designs. Three common topologies include diode-clamped, flying capacitor, and cascaded H-bridge inverters. Each of the conventional topology has its own advantages and disadavantages which are discussed in detail.



(a) Flying capacitor (b) Cascaded H-Bridge (c) Diode-Clamped

Figure 1: Conventional MLI topologies

2.2 Cascaded H-Bridge Multilevel Inverter Topology:

The Cascaded H-Bridge Multilevel Inverter Topology consists of multiple H-bridge cells connected in series. Each H-bridge cell has its own DC voltage source and can generate multiple voltage levels. By cascading multiple H-bridge cells, the topology can produce a staircase waveform output with reduced harmonic distortion. Cascaded H-Bridge inverters are highly modular and scalable, making them suitable for a wide range of applications.

Benefits:

- To decrease switching losses, a soft switching approach can be employed.
- Filters are not required to decrease harmonics.
- THD (total harmonic distortion) is extremely low.
- A lower number of components is used in this MLI.

Drawbacks:

- For power conversions, it requires independent dc sources.

2.3 Diode-Clamped Inverter (Neutral-Point Clamped Inverter)Topology:

The Diode Clamped or Neutral Point Clamped (NPC) Multilevel Inverter Topology utilizes diodes to clamp the switch voltage to the mid-point DC link voltage or across a DC link capacitor. The topology offers multiple voltage levels and provides a staircase waveform output.

Benefits:

- The real and reactive power flow can be controlled.
- Filters are not required to decrease harmonics.
- The voltage of the switch is just half of the voltage of the dc-link.
- The efficiency is high at the fundamental frequency.

Drawbacks:

- Clamping diodes are increased when each level is raised.
- Individual converter real power flow management is challenging.

2.4 Flying capacitor multilevel Inverter Topology:

The fundamental principle underlying this inverter revolves around the utilization of capacitors. It comprises a series arrangement of capacitor-clamped switching cells interconnected in sequence. Electrical apparatuses receive a constrained voltage supply from these capacitors. The switching configurations of this inverter mirror those of a diode-clamped counterpart. Notably, this form of multilevel inverter operates without necessitating clamping diodes. The resultant output voltage is restricted to half of the input DC voltage. Nonetheless, a deficiency is observed in the multilayer inverter employing flying capacitors. To mitigate this imbalance in flying capacitors, the design incorporates redundancy in switching within each phase. Moreover, it possesses the capacity to regulate both active and reactive power transmission. However, the operation at high frequencies entails switching losses.

Benefits:

- Get rid of the clamping diode problems.
- Filters are not required to decrease harmonics.
- Reduces the amount of stress on the semiconductor switches.
- It provides the correct switching combination for balancing various voltage levels.

Drawbacks:

- Controlling the voltage across all of the capacitors is hard to achieve.
- A decrease in switching efficiency
- Higher cost because of using more capacitors

2.5 Comparative Analysis of Conventional MLIs

Comparative analysis of the conventional MLIs topologies is carried out based on various parameter and the study is summarized in Table below.

Table 1 : Comparison of Conventional topologies

Parameter	Diode Clamped	Flying Capacitor	Cascaded H-Bridge
Switch Count	2(N-1)	2(N-1)	2(N-1)
No. of DC Sources	1	1	(N-1)/2
No. of Diodes	(N-1)*(N-2)	0	0
No. of Capacitors	(N-1)	N(N-1)/2	0

Note: Where N = Level of MLI

2.6 Overview of some recently proposed RSC topologies:

The large increase in device counts has drawn a focus of researchers to propose a topology having fewer dc source , gate driver and switch requirement under the name of reduced switch count (RSC) MLIs[3]. The authors of [4] provide a comprehensive review and categorization of RSC-MLI topologies, considering their structure, features, limitations and suitability for particular application. According to [4] RSC-MLIs can be categorised as Generalized RSC-MLIs, stacked topologies, Unit-based MLIs, switched capacitor(SC) RSC-MLIs, Transformer based RSC-MLIs, Three phase topologies. Generalized RSC-MLIs include topologies having separate level and polarity generator, there is a backend H-bridge converter which limit their applications in high voltage applications. Some of the topologies without backend H-bridge converter are Envelope (E-type) type, Square T-type (ST-type), K-type, Packed U Cell(PUC) type and Switched dc-sources(SDS) . E-type, ST-type and K-type topologies come under unit-based topologies these cannot be extended directly to generate higher levels. The possible way to extend is to cascade the suitable modules. ST-type was derived from E-type and there is a reduction in switch count in ST-type as compared to E-type. K-type topology utilizes capacitors in order to reduce the dc sources.

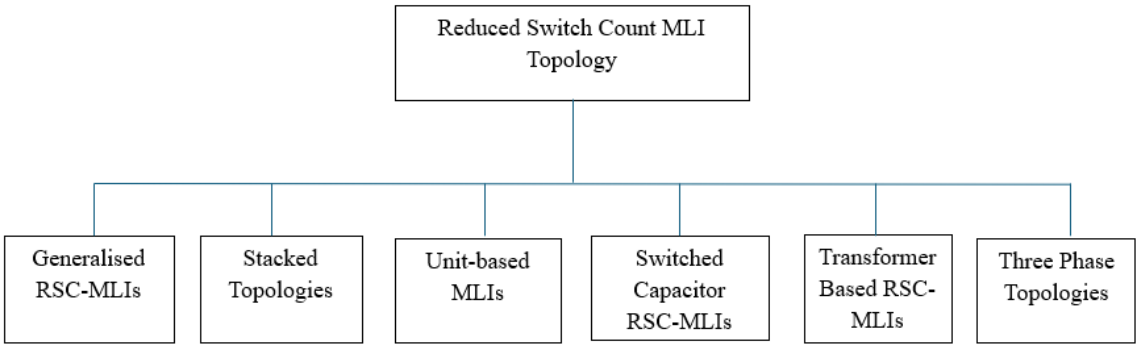


Figure 2: Categorization of RSC MLI topologies

ST-type topology of [5] utilizing 4 dc sources in which 2 are of same variety and 12 power switches to produce 17 levels at the output. The topology of [6] is a K-type (Kite Type) using 2 asymmetrical dc sources and 2 capacitors but 14 power switches to generate 13 voltage levels. PUC and SDS are the topologies having ladder-based structure comes under Generalized RSC-MLI. The PUC topology of [7] and SDS topology of [8] are same except the polarity of dc sources. In PUC there is a consecutive addition and subtraction of dc sources in the conduction path. The limitation of PUC toplogy is that it always operates in buck mode which means that output voltage will always be lesser than the sum of dc sources[4]. SDS overcomes the disadvantages of PUC due to opposite polarity of dc sources. There is another class of MLI topology, known as Stacked inverters which generates higher number of voltage levels by stacking MLIs, finding applications in three phase and six phase IM drives[9]. The authors of [9] are producing 49 levels by using three 17-level inverters which involves casading a Flying capacitor inverter with 3 cascaded H-bridges and stacking them using selector switches.In recent years, there has been significant attention in the research domain towards switched capacitor topologies due to their remarkable characteristics. These include capability of voltage boosting, enabling the replacement of multiple DC voltage sources with capacitors, mostly possessing an inherent self-balancing property and having modular structure. These attributes have led to reductions in weight, size, and costs associated with such systems[10]. The authors of [11] have categorized SC MLIs on the basis of (i) number of levels in the output voltages, (ii) backend H-bridge (with or without H-bridge), (iii) dc supply(single/multiple dc supply) and (iv) capacitor balancing(Inherent capacitor voltage balancing or by using some switching techniques).

According to [12] MLIs can also be classified into two main groups, transformerless and transformer based MLI. Transformer based reduced component MLI is reported in [12] producing 9 level by using eight switches, one transformer and a single dc source. This topology consists two H-bridge converter and a transformer is shared between them. Using transformer in MLI enhances fault tolerance and reducing the need of dc sources but it also increases the weight and losses of the inverter[4].There is another way to categorize MLIs topologies on the basis of voltage ratio which is symmetrical MLI topology and asymmetrical MLI topology. Symmetric MLIs have the equal magnitude of dc voltage sources. The

topologies which involve unequal ratio of dc voltage source are referred to as assymetrical and these are preferred to increase the output levels without increasing the device count.

In symmetric configuration, Cascaded H bridge converter requires 16 power switches and 4 dc sources to generate 9 level at the output whereas in the asymmetric mode it produces 17 levels by same number of switches and dc sources. In order to reduce the device counts researchers are continuously proposing the circuits. The topology of [13] is generating 9 levels in symmetric operation and 17 levels in asymmetric mode by utilizing 10 power switches and 4 dc sources. The topoloy reported in [14] operating in both symmetrical and asymmetrical mode and producing 7 levels and 13 level repectively by using 10 switches and 3 dc sources. This topology is using backend H-bridge inverter as a polarity generator. The stress on the switches of polarity generator is higher as compared to the level generator. Topologies of [15] and [16] are using capacitors in order to reduce the isolated dc voltage sources. The authors of [15] are generating 17 levels by using 4 capacitors, 2 dc sources and 18 power switches while topology of [16] is using only 12 switches keeping the number of dc sources and capacitors same as of [15] and also having lesser value of per unit total standing voltage.

Chapter 3

Proposed Topology

3.1 Introduction

There are numerous topologies of multilevel inverter are reported in literature. The drawbacks of conventional topologies are have been discussed in the introduction section of the report, prompting researchers to continuously strive to propose the new topologies to reduce component count. This section presents a new MLI topology aimed at achieving the goal of minimizing components in the circuit, thereby reducing costs and enhancing reliability of the converter. This chapter focuses into various aspects of propsed topology, starting with a brief description of the circuit and its look-up table. The look-up table outlines the conduction path necessary to achieve a desired voltage level. Subsequently, TSVpu is calculated, providing insight into the voltage stress across the switches; lower stress necessitates lower-rated switches, reducing converter costs. Furthermore, an extended generalized structure is discussed, which increases the number of voltage levels by cascading various basic units. Following this, a detailed discussion on modulation schemes is conducted. Finally, the chapter presents a cost analysis and reliability assessment of the proposed topology, crucial aspects for practical applications of a converter.

3.2 Brief description of circuit

The circuit configuration of the proposed topology of a multilevel inverter is shown in figure 3. It consists of twelve unidirectional switches and three dc sources (V_1,V_2,V_3). The switches are unipolar which means that they are capable to block the voltage in one direction. The proposed topology consists separate level and polarity generator. Level generator consistsing of switches (S1,S2…S8) is generating nine level before an H-bridge and nineteen levels are generated at the output of an H-bridge. There are nineteen different modes of operation. For different modes of operation, Table 2 provides all the switching combination to get the desired voltage levels in terms of dc voltage sources where 1 indicates ‘’ON’’ and 0 indicated ‘’OFF’’ of a particular switch. The dc voltage sources ratio of proposed topology is V_1:V_2:V_3 = 1:2:6.

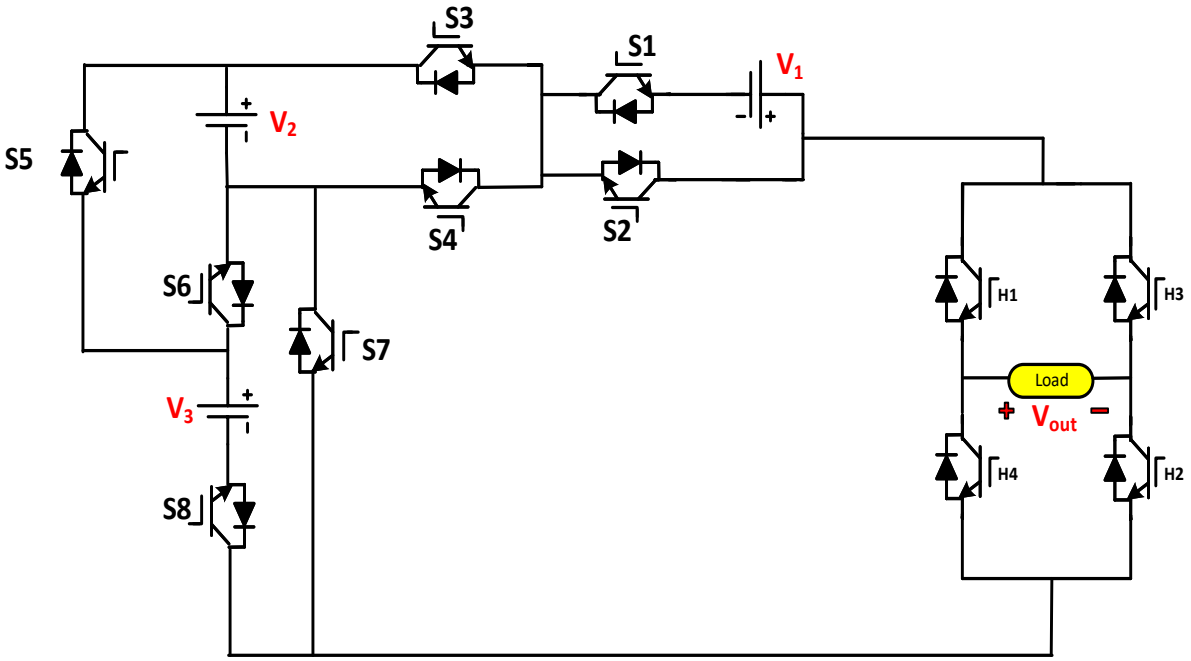


Figure 3: Proposed Multilevel Topology

Table 2: Switching states of switches of proposed topology

V_{OUT}	Switches States											
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	H_1	H_2	H_3	H_4
0V	0	1	0	1	0	0	1	0	1	0	0	1
+1V	1	0	0	1	0	0	1	0	1	0	0	1
+2V	0	1	1	0	0	0	1	0	1	0	0	1
+3V	1	0	1	0	0	0	1	0	1	0	0	1
+4V	0	1	0	1	1	0	0	1	1	0	0	1
+5V	1	0	0	1	1	0	0	1	1	0	0	1
+6V	0	1	0	1	0	1	0	1	1	0	0	1
+7V	1	0	1	0	1	0	0	1	1	0	0	1
+8V	0	1	1	0	0	1	0	1	1	0	0	1
+9V	1	0	1	0	0	1	0	1	1	0	0	1
-1V	1	0	0	1	0	0	1	0	0	1	1	0
-2V	0	1	1	0	0	0	1	0	0	1	1	0
-3V	1	0	1	0	0	0	1	0	0	1	1	0
-4V	0	1	0	1	1	0	0	1	0	1	1	0
-5V	1	0	0	1	1	0	0	1	0	1	1	0
-6V	0	1	0	1	0	1	0	1	0	1	1	0
-7V	1	0	1	0	1	0	0	1	0	1	1	0
-8V	0	1	1	0	0	1	0	1	0	1	1	0
-9V	1	0	1	0	0	1	0	1	0	1	1	0

From the table it can be observed that operation of three pairs of switches (S1, S2), (S3, S4), (S7, S8) are complementary.

3.3 Modulation strategy

Modulation techniques are used to control the output voltage waveform, reduce harmonics, improve efficiency, and achieve better output quality. These techniques can be categorized into two types: Space vector-based algorithms and Voltage-based algorithms [17]. In this work, Nearest Level Control (NLC) has been used as a modulation technique, which is one of the low or fundamental frequency switching techniques and falls under voltage-based algorithms. The switching losses associated with high-frequency techniques are higher because the switching signals are generated at high frequency. On the other hand, these losses are reduced, and hence the cooling requirement is also reduced in low frequency switching techniques. Low switching frequency modulation techniques such as Nearest Level Control and Selective Harmonic Elimination (SHE) are often preferred in high-power applications. SHE involves solving a set of nonlinear equations to determine the switching angles that will eliminate lower-order harmonics. This calculation can become complex and time-consuming, especially for converters with a large number of levels. NLC eliminates the drawback of selective harmonic elimination. However, Total Harmonic Distortion (THD) in the output voltage increases in the case of NLC for a low number of levels. Figure 7, as reported in [18], explains the implementation of NLC, indicating that there is a sinusoidal reference wave Nmsin(ωt) where N is the number of positive voltage levels and m is termed as the modulation index. The comparison is made between the reference wave and a predefined constant value, and when the reference wave crosses the constant level, the switching state of the converter changes, and hence the output voltage level changes. The change in output voltage levels is shown in Figure 8 [19].

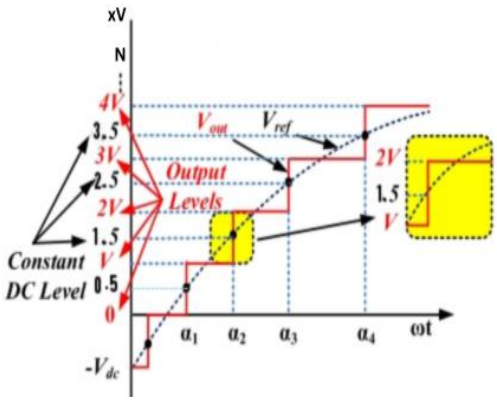


Figure 4: Method to generate levels from NLC

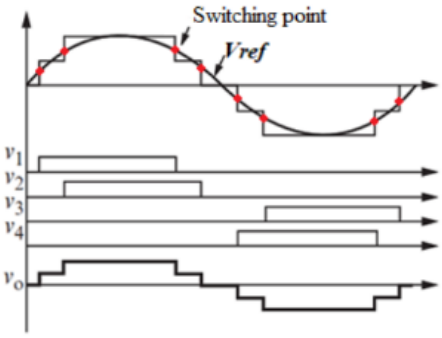


Figure 5: Staircase sinusoidal output from NLC

3.4 Voltage rating of switches

The voltage rating of switch determines the maximum voltage stress they can handle in OFF state. For the selection of switches having appropriate voltage ratings analysis of Total Standing Voltage (TSV) is required. It is the cumulative value of the highest voltage stress appearing across each switch. TSV is a significant factor in determining the cost of a converter. Higher TSV values require switches with higher voltage rating, which can be costlier. Regarding the Fig.1 the value of the TSV for the proposed topoloy can be calculated as follows:

$$TSV = (V_{S1} + V_{S2} + \ldots + V_{S8}) + (V_{H1} + \ldots + V_{H4})$$

For the proposed topology the maximum voltage stress across each switch is given as:

$V_{S1} = V_{S2} = V_1$
$V_{S3} = V_{S4} = V_2$
$V_{S5} = V_{S6} = V_2$
$V_{S7} = V_3$
$V_{S8} = (V_3 - V_2)$
$V_{H1} = V_{H2} = V_{H3} = V_{H4} = (V_1 + V_2 + V_3)$

In case of proposed 19-level topology. The value of TSV will be:

$$TSV = 2 \times (V_1) + 4 \times (V_2) + V_3 + (V_3 - V_2) + 4 \times (V_1 + V_2 + V_3) = 56V_1$$

The back-end H bridge inverter contributes to an increase in the TSV value as the switches experience higher voltage stress due to the cumulative effect of generating multiple voltage levels.

TSV in per unit offers a convenient and effective way to analyze and compare the impact of voltage stresses which is a ratio of TSV to the maximum output voltage.

$$TSV_{p.u.} = \frac{56V_1}{9V_1} = 6.22$$

Another important term is maximum blocking voltage per unit (MBV_{pu}) which is the ratio of peak stress across switch to the peak output voltage.

$$MBV_{pu} = \frac{9V_1}{9V_1} = 1$$

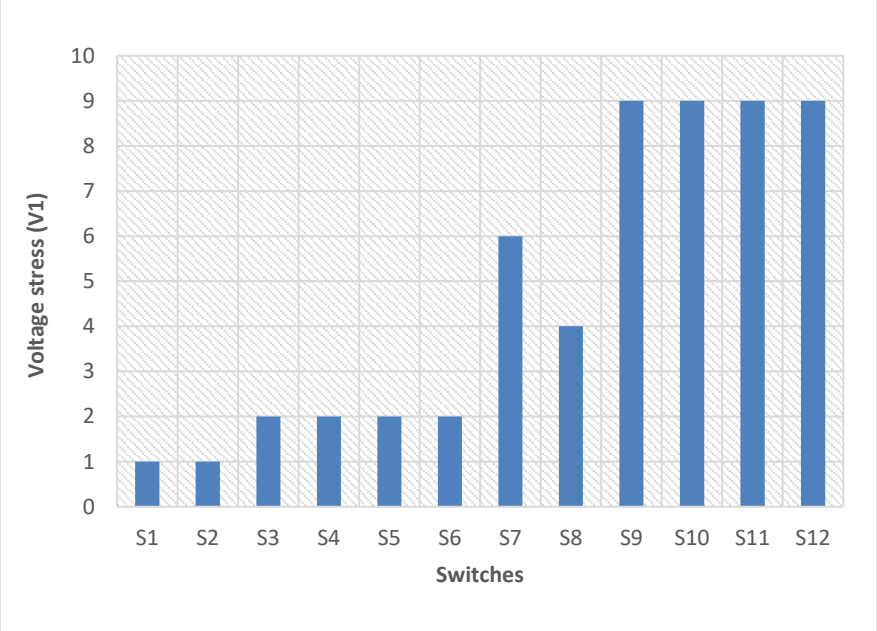
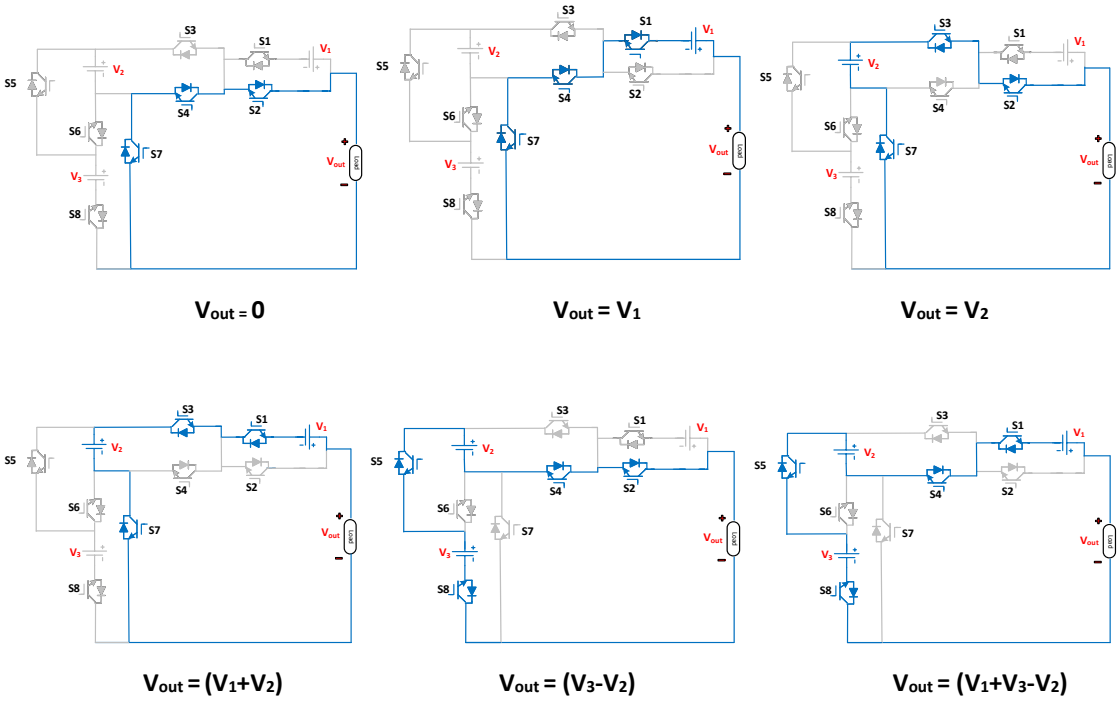


Figure 6: Maximum voltage stress of switches



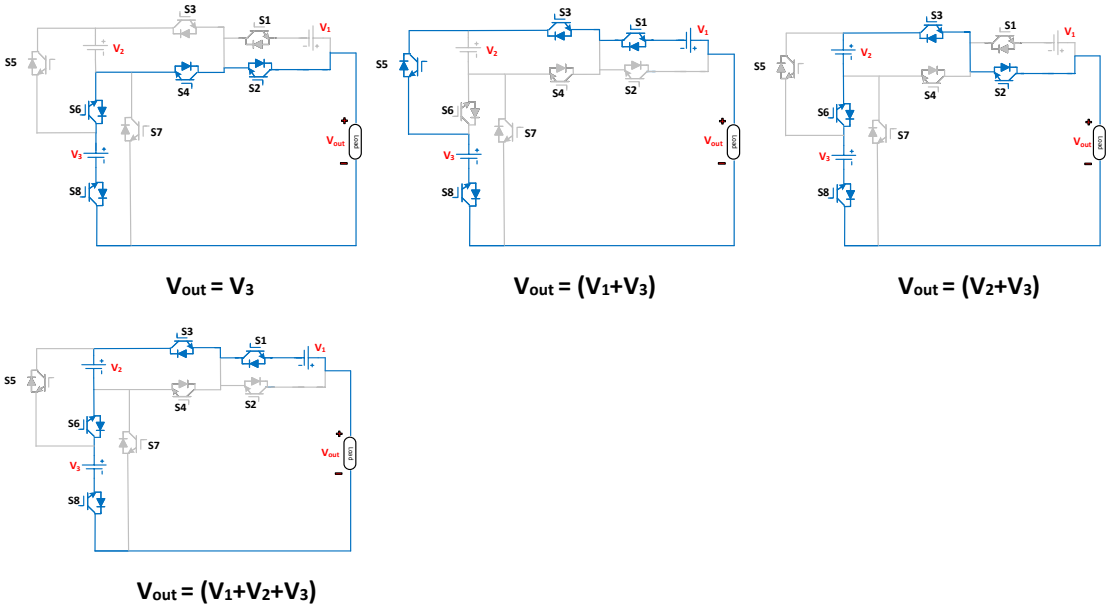


Figure 7: Conduction state of switches before H-bridge inverter

3.5 Extended generalized structure

As previously discussed, the proposed topology consists separate level generator (basic unit) and polarity generator which means it only generate positive voltage and requires an H-bridge inverter to change the polarity of output voltage. In order to increase the number of levels it is possible to connect n number of basic units in series before the H-bridge. In the genralized structure each basic unit is capable to generate nine different voltage levels and zero level. If $V_{out,1}$, $V_{out,2}$ …$V_{out,n}$ represents the output voltage of each basic unit then the total output voltage of the structure, which is the sum of the voltages of all the basic units, can be written as:

$$V_{\text{Total output}} = V_{out,1} + V_{out,2} + \ldots\ldots\ldots + V_{out,n}$$

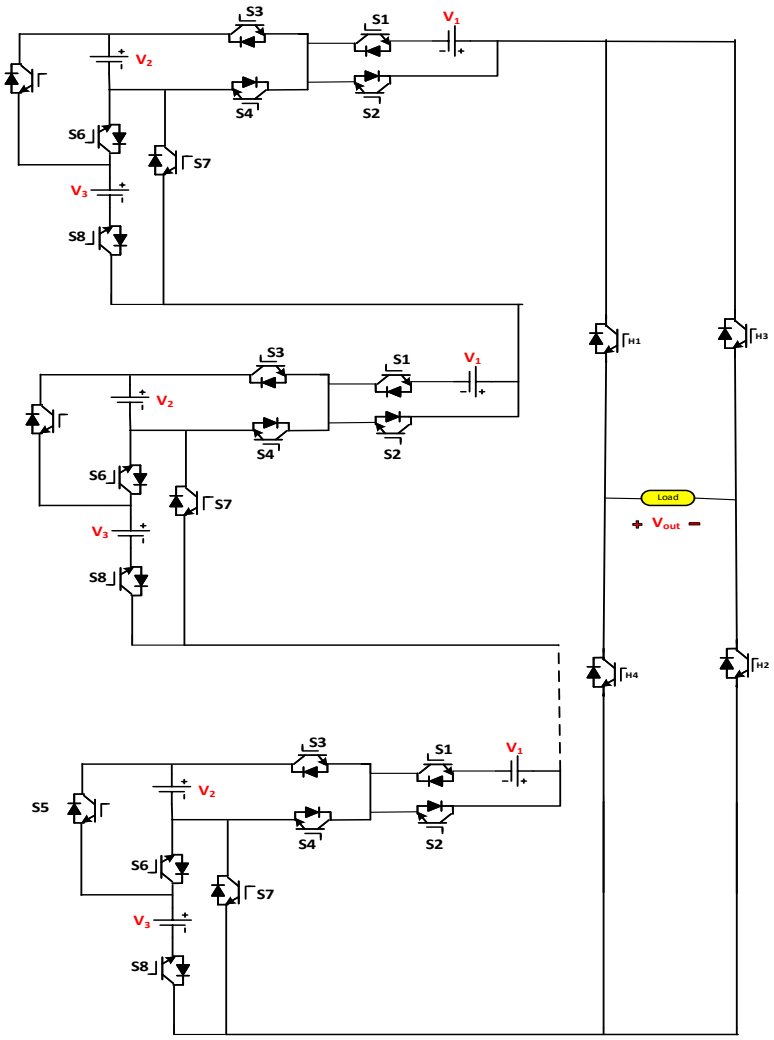


Figure 8: Generalized structure of a proposed topology

The relations for the generalized structure of the proposed topology for *n* number of basic units are given as:

Number of power switches = 8n+4
Number of gate drivers = 8n+4
Number of dc sources = 3n

3.6 Cost analysis

The cost factor is a crucial aspect in determining the most suitable multilevel inverter (MLI) with optimal affordability. Reducing the number of IGBTs(N_{IGBT}), driver circuits(N_{gd}), capacitors(N_C), diodes(N_d), dc sources(N_{dc}) and TSV per unit significantly decreases the overall cost and complexity of the circuit. CF is formulated as reported in[20]:

$$\text{Cost Factor (CF)} = N_{IGBT} + N_{gd} + N_C + N_d + N_{dc} + \alpha\, TSV_{p.u.}$$

where α is known as weighting factor it determines the emphasis placed on the rating of switches. CF value is calculated for α = 0.5 and α = 1.5 for the proposed topology.

CF (α = 0.5) = 30.11, CF(α = 0.5)/No. of levels = 30.11/19 = 1.58

CF (α = 1.5) = 36.33, CF(α = 1.5)/No. of levels = 36.33/19 = 1.91

3.7 Reliability

Reliability refers to the ability of power electronic converters and systems to consistently perform their intended functions over a specified period and under various operating conditions. As the number of devices is higher in an MLI compared to a 2-level inverter, the likelihood of faults occurring in the converter also increases. According to an industry-based survey, capacitors and power electronic switches are identified as the components most susceptible to faults[21]. A fault tolerant MLI with a high device count is expected to be less reliable compared to one with fewer devices. The following terms are used by the researchers in order to determine the reliability of converters: Failure rate (λ), mean time to failure (MTTF) and mean time to repair (MTTR)[22]. Failure rate is a reliability index that represents the rate at which the converter fails. It helps to determine the probability of failure over a specified time period. The MTTF refers to the average expected time until the occurrence of a first failure in the converter. MTTF has an inverse relation with failure rate. The next term is MTTR which tells about the time required to repair a faulty device. There are two methods to estimate the reliability called parts count and parts stress[23]. The exact method uses the part stress method scheme which consider different factors of operating conditions. In this method, failure rate of different components are calculated then summing them to determine the failure rate of a complete circuit.

Since the proposed topology consists only switches, the failure rate of switch (λ_s) can be calculated by the given equation[23]:

$$\lambda_s = \lambda_b \pi_T \pi_A \pi_R \pi_S \pi_Q \pi_E \quad \text{Failures}/10^6 \text{ hours}$$

Here, λ_b is a base failure rate whose value is taken from [MIL] as 0.00074, π_T is a temperature factor expressed as

$$\pi_T = e^{-2114(\frac{1}{T_j + 273} - \frac{1}{298})}$$

where T_j is the junction temperature and can be calculated as

$$T_j = T_c + \theta_{ji} P_l$$

Where T_c is known as ambient temperature and θ_{ji} indicates the sum of junction to case and case to ambient thermal resistance which can be obtained from datasheet. π_A is a application factor, π_Q is termed as quality factor, π_E is a envirnonmental factor , π_R is a power rating factor which has relation with power rating (P_r) of the switch and can be calculated using expression,

$$\pi_R = (P_r)^{0.37}$$

Finally, the last term is π_S known as voltage stress factor of switch, it depends on V_s which is the ratio of applied collector to emitter voltage to the collector to emitter voltage in OFF state of the switch. π_S is given by the expresion,

$$\pi_S = 0.0045 e^{3.1 V_s}$$

For the proposed topoloy, the failure rate is calculated as λ_t = 0.06216 Failures/hour which is same as the failure rate of switches. MTTF can be calculated as:

$$MTTF = 1/\lambda_t = 16.08 \ (10^6 \text{ hours/failure})$$

Chapter 4

Modelling and Performance Analysis

4.1 Introduction

This chapter covers all the analyses conducted for a proposed topology in the Plecs environment. The proposed topology undergoes simulation in the software utilizing NLC to deliver pulses to the switches. The circuit is evaluated under both static and dynamic loading conditions. Conduction and switching losses predominantly occur in the circuit due to the non-ideal nature of switches. After calculating both the losses, efficiency is assessed to understand the topology's performance. In the subsequent section, analyses under different loading conditions, which include fixed and varying R & RL loads, varying modulation index of the switching scheme, losses, and the circuit's efficiency, are presented. Additionally, the temperature profile of switches utilized in the topology is also presented, which is helpful in the appropriate selection of switches and determining the cooling requirement of the converter. Table 3 presents the parameters used for the simulation.

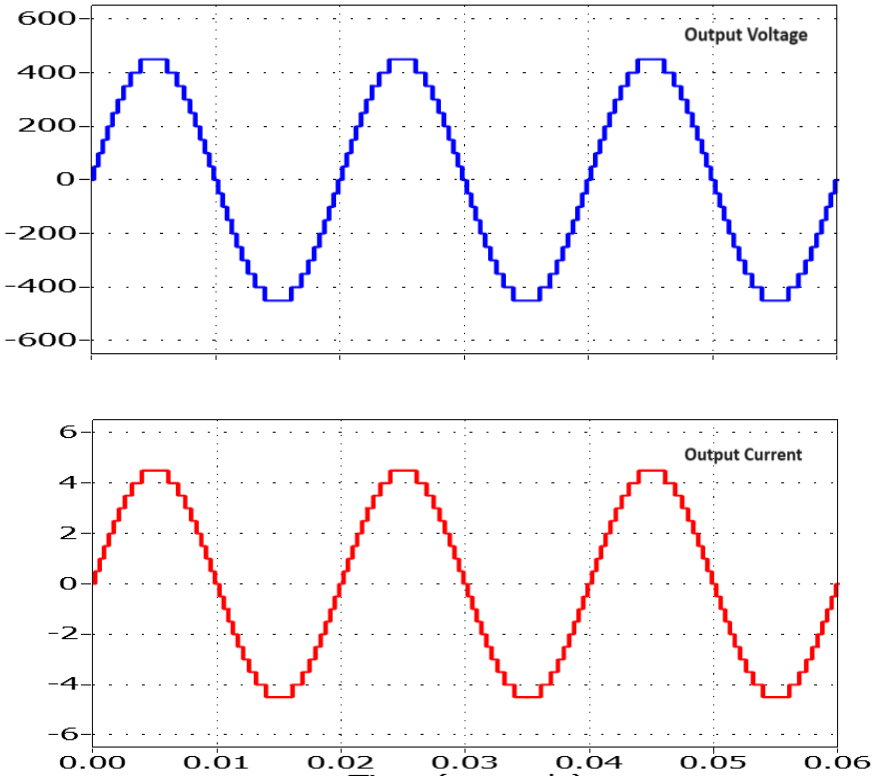
Table 3 : Simulation Parameters

Simulation Parameters	Values
Voltages	V_1 = 50 V, V_2 = 100 V, V_3 = 300 V
Power frequency	50 Hz
Switches	IGBT (IKW75N65EL5)
R load	50 Ω, 100 Ω
RL load	50 Ω + 40 mH, 100 Ω + 80 mH

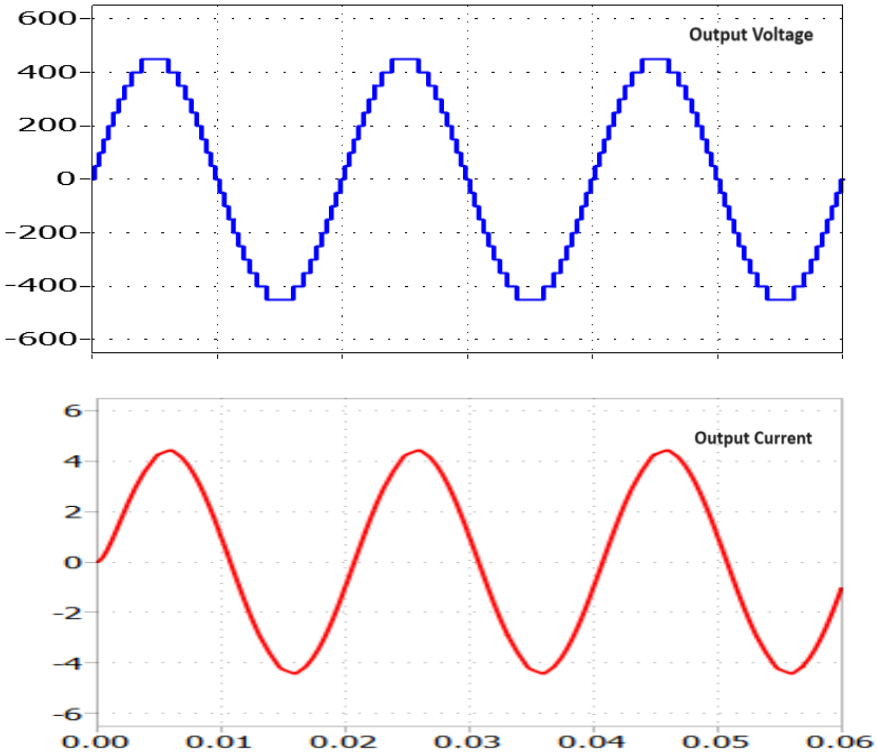
4.2 Performance Analysis

(A) Fixed loading conditions

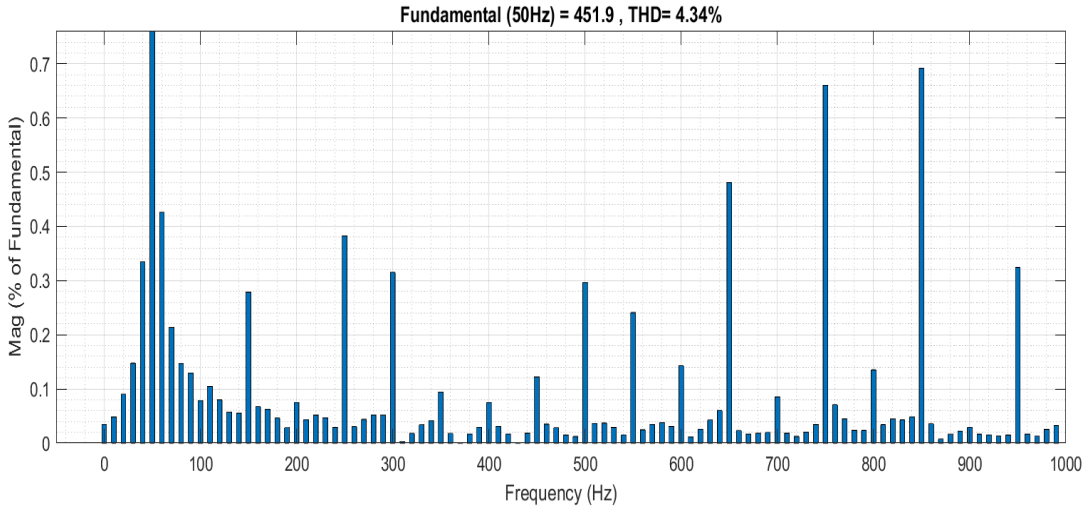
Under fixed loading conditions, simulations are done for both constant resistance (R) and resistive-inductive (RL) loads. Such loads resemble those found in household appliances like heating elements, which exhibit constant or varying resistance and inductance. When subjected to a fixed resistive load of R = 100Ω, the resulting output voltage and current waveforms are depicted in Figure 9(a). Similarly, when a constant RL load of Z = 100Ω+80mH is applied, the resulting output voltage and current waveforms are shown in Figure 9(b). Through FFT analysis, the Total Harmonic Distortion (THD) of the output voltage is determined to be 4.83% shown in Figure 9(c).



(a) Output Voltage and Current waveform for constant R load



(b) Output Voltage and Current waveform for constant RL load

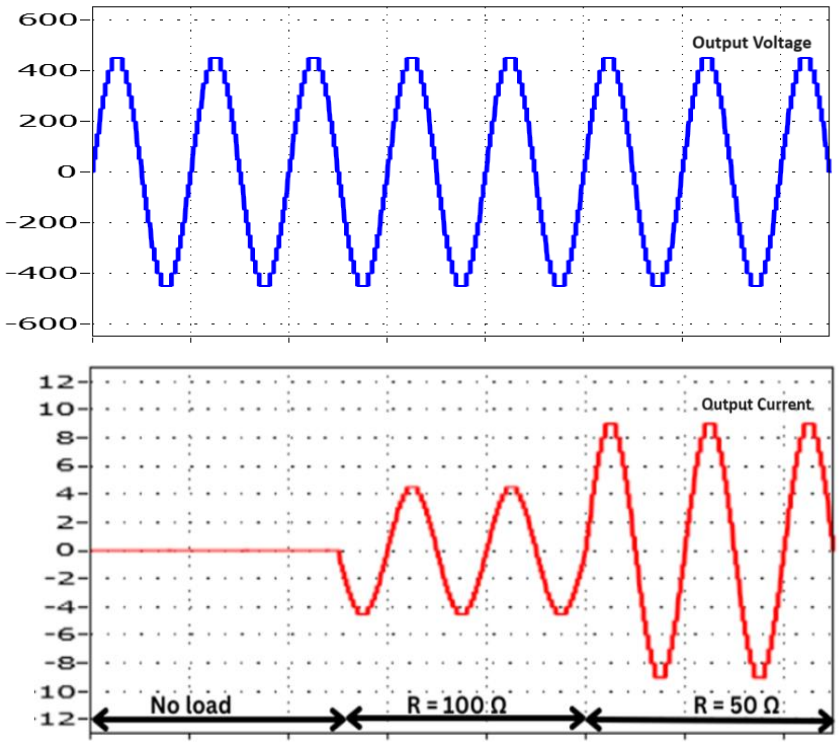


(c) FFT analysis and THD in output voltage

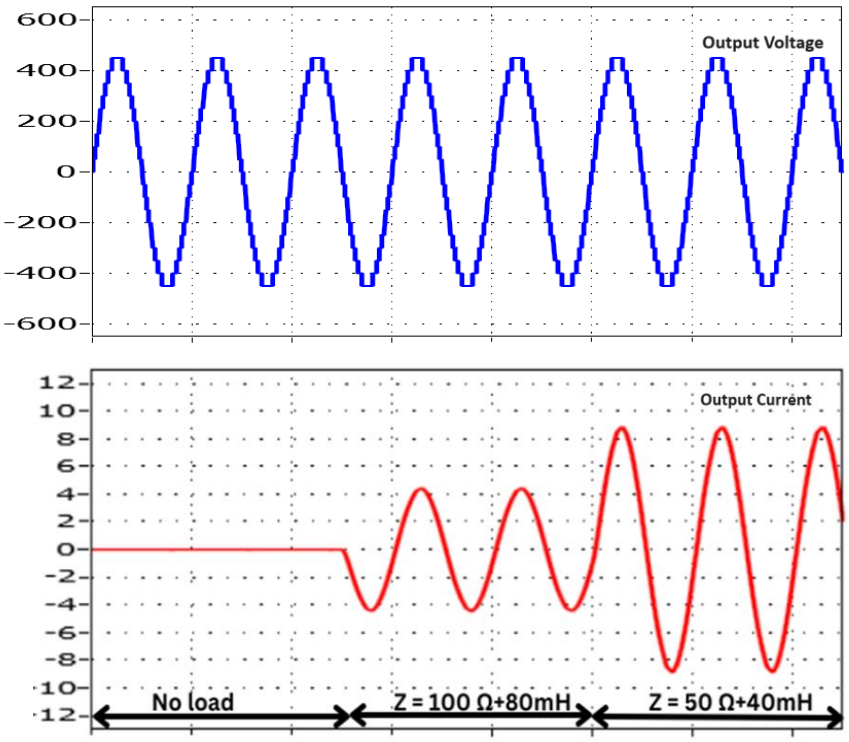
Figure 9: Simulation results obtained for the proposed topology with constant R and RL load

(B) Varying loading conditions

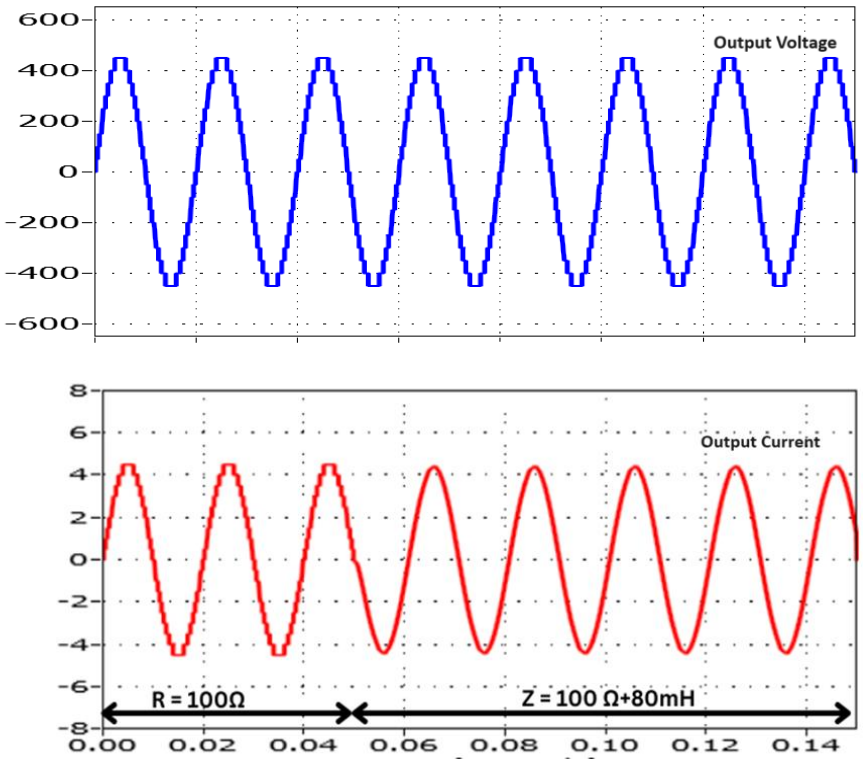
In real-world scenarios, load conditions often vary dynamically, due to various applications, such as industrial machinery operations, renewable energy systems, household applications and electric vehicles etc. By simulating load transitions, the inverter's ability to maintain stable operation under abrupt changes was assessed, ensuring its reliability across diverse applications. The waveforms for variable R and RL loads are depicted in Figure 10(a) and Figure 10(b) respectively. In both scenario, intially there was no current as no load was connected to the inverter. Subsequently, when the load is applied, it results in an output current. The waveforms for variable power factor are shown in Figure 10(c) in which initially the load was of R type and then changed to RL load.



(a) Voltage and current waveform for varying R load



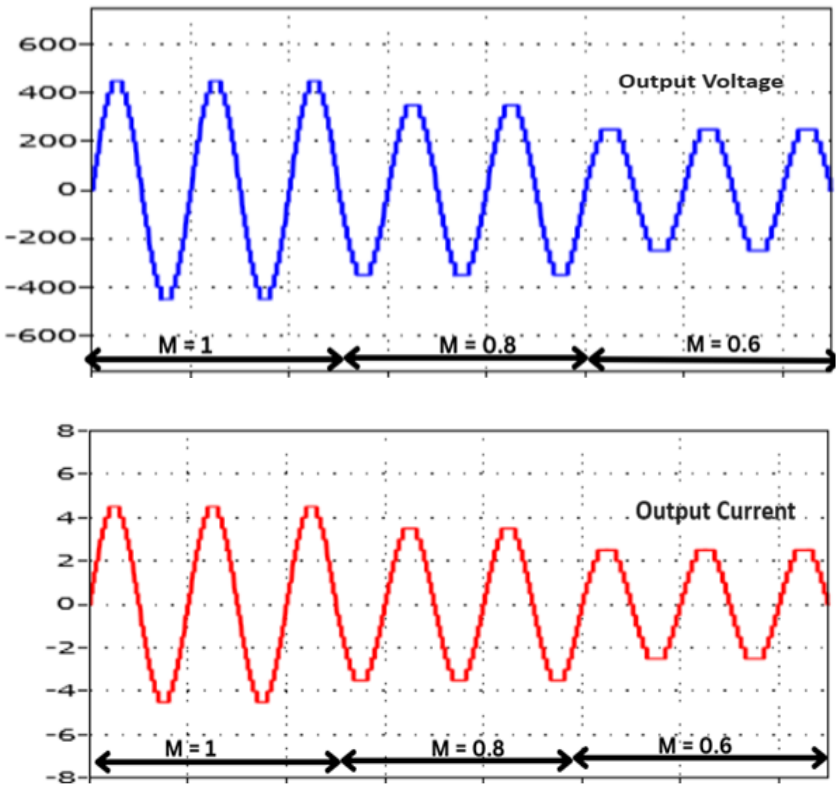
(b) Voltage and current waveform for varying RL load



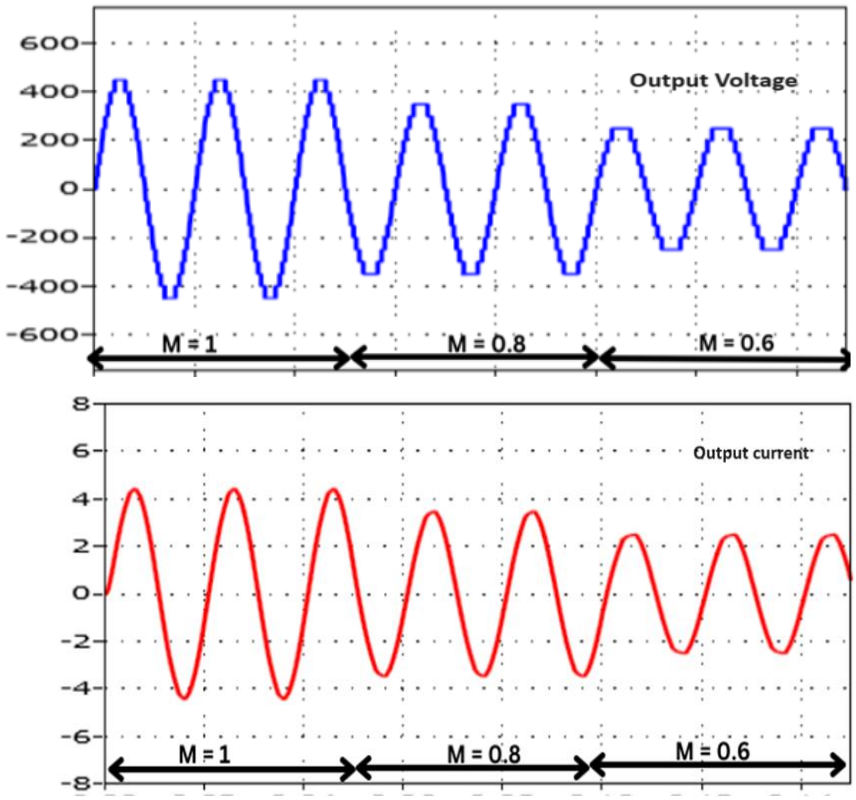
(c) Voltage and current waveform on changing power factor of a load

(C) Varying modulation index

In certain cases, the modulation index of the converter could change due to faults or control system errors. To assess the dynamic stability of the converter, simulations were conducted for different modulation indices ranging from 1 to 0.8, and subsequently to 0.6. Upon transitioning from a modulation index of 1 to 0.8, the voltage levels decreased from 19 to 15. Further reducing the modulation index from 0.8 to 0.6 led to a subsequent decrease in voltage levels from 15 to 11. The voltage and current waveforms for varying modulation index are shown in Figure 10(d) and 10(e) respectively.



(d) Voltage and current waveform with change in modulation index for R load



(e) Voltage and current waveform with chane in modulation index for RL load

Figure 10: Simulation results obtained for proposed topoloy for changing R and RL load with change in modulation index

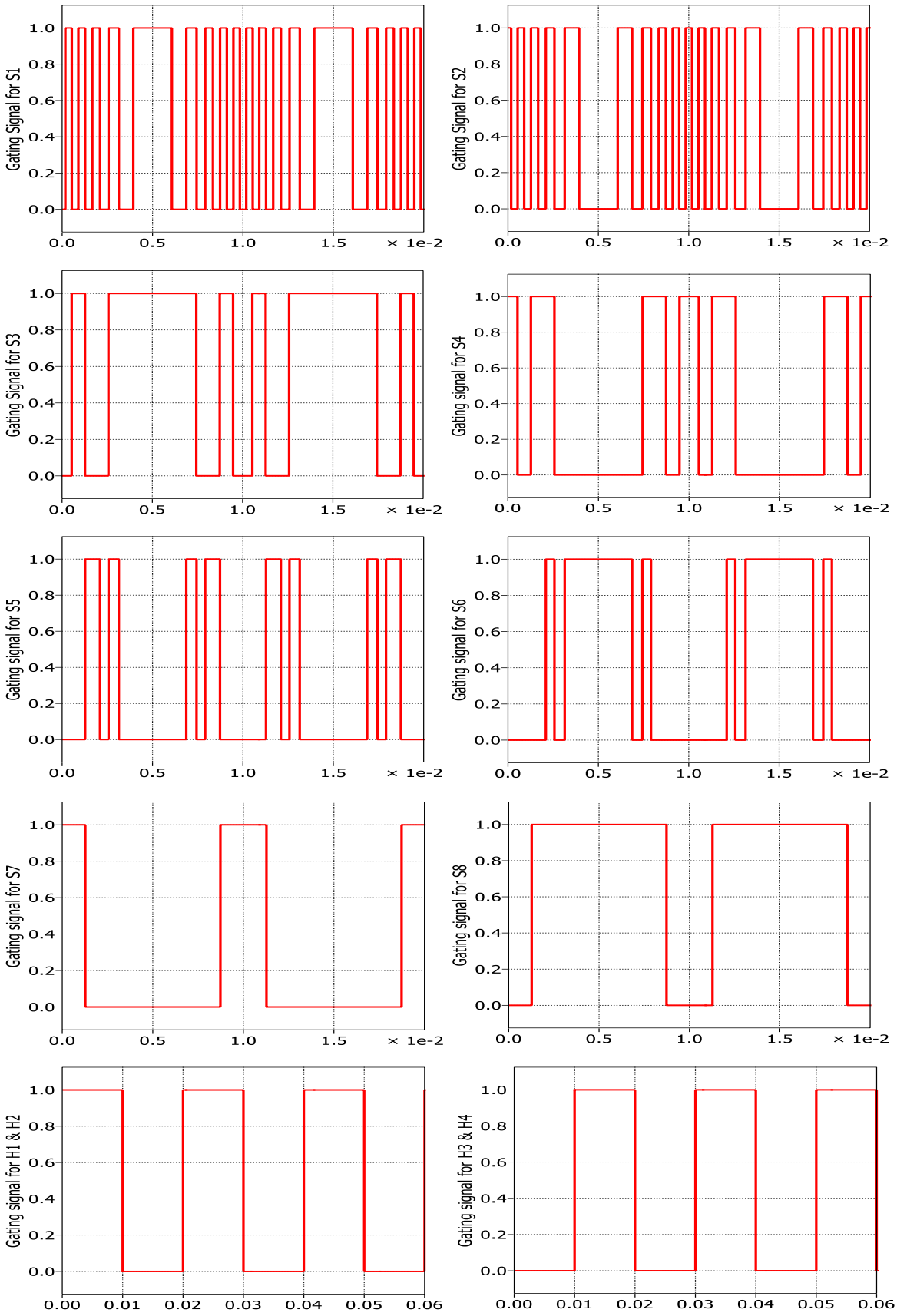


Figure 11: Gating signals for switches

4.3 Power loss and efficiency

The analysis of power losses is crucial during the design of any topology as they directly impact the efficiency of a converter. Power losses lead to the generation of heat within the components. Excessive heat can cause component degradation, reduce lifespan, and even lead to failure. A power electronic switch operates in three modes: blocking mode, conduction mode, and switching mode. However, there are negligible losses in blocking mode. Therefore, losses mainly occur during switching mode and conduction mode. Switching losses occur during the transitions of the semiconductor devices in the converter, including Turn-On and Turn-Off losses. Conduction losses occur when current flows through the ON-state semiconductor devices. These losses of IGBTs with antiparallel diodes are due to on state voltage drop and turn-on resistance. These losses increase with the number of switches in the conduction state. Conduction losses are more pronounced at low switching frequencies. The following equations can be used for the estimation of losses.

$$P_{cond,IGBT} = V_{ON,IGBT}\, i(t) + R_{IGBT} i^{\beta}(t)$$

$$P_{cond,d} = V_{ON,d} i(t) + R_d i^2(t)$$

Here, $V_{ON,IGBT}$ and $V_{ON,d}$ represent the ON-state voltage drops of the IGBT and antiparallel diode, respectively. R_{IGBT} and R_d denote the equivalent resistances of IGBT and diode, and i(t) is the conduction current. The term β is a constant determined by the datasheet of the switch. The total conduction losses of a switch can be determined by adding both of the above equations.

$$P_{cond} = \sum_{j=1}^{N_{IGBT}} \frac{1}{2\pi} \int_0^{2\pi} (V_{ON,IGBT}\, i(t) + R_{sw} i^{\beta}(t))dt + \sum_{k=1}^{N_d} \frac{1}{2\pi} \int_0^{2\pi} (V_{ON,d}\, i(t) + R_d i^2(t))dt$$

Switching losses arise due to the time delay during the transition of switches. Ideally, the switch should instantaneously change its state, but practically it takes a small duration to chane its state, causing energy dissipation in the form of heat. These losses are higher at high switching frequencies. Assuming the variation in voltage and current to be linear during transition, the switching loss P_{sw} for the fundamental frequency, f can be determined by the given equation:

$$P_{sw} = [\sum_{j=1}^{Nsw} (E_{ON,k} T_{ON,k} + E_{OFF,k} T_{OFF,k})] \times f$$

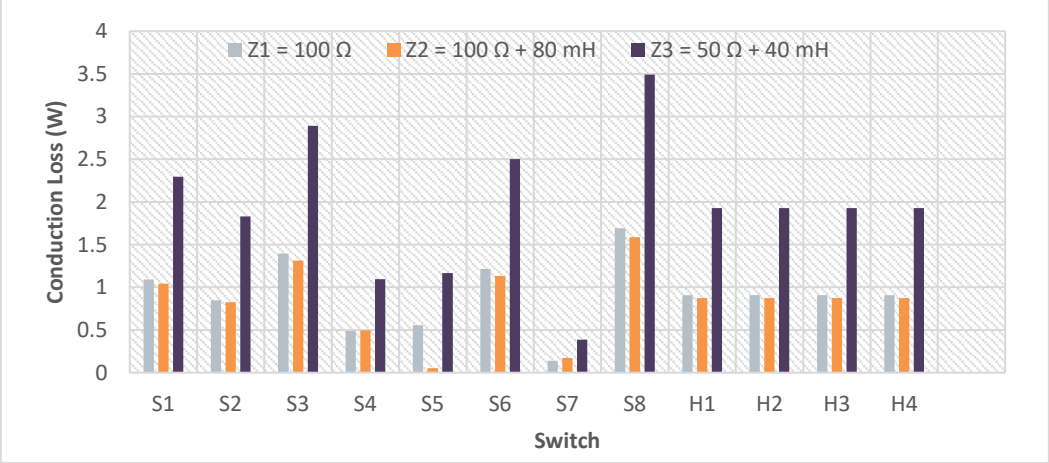
Here, $E_{ON,k}$ and $E_{OFF,k}$ represnt the energy loss during turn-ON and turn-OFF in one cycle for the k^{th} IGBT and diode respectively. $T_{ON,k}$ and $T_{OFF,k}$ indicate the number of turn-ON and turn-OFF cycles for the k^{th} IGBT and diode respectively. Now, total losses $P_{T,L}$ are given by:

$$P_{T,L} = P_{cond} + P_{sw}$$

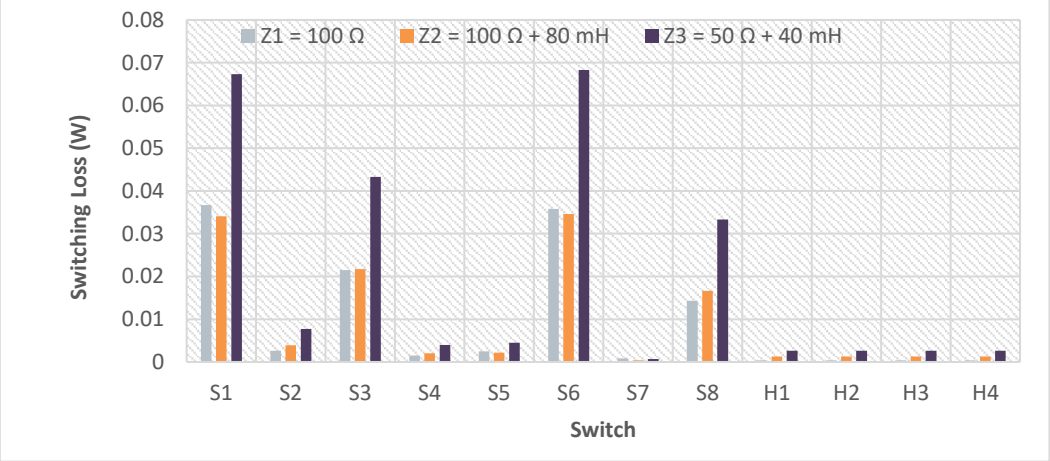
After calculating losses next step is to obtain the efficiency of the converter which gives the idea about its performance and can be calculated using equation:

$$\eta = \frac{P_{out}}{P_{out+}\, P_{T,L}} \times 100\ \%$$

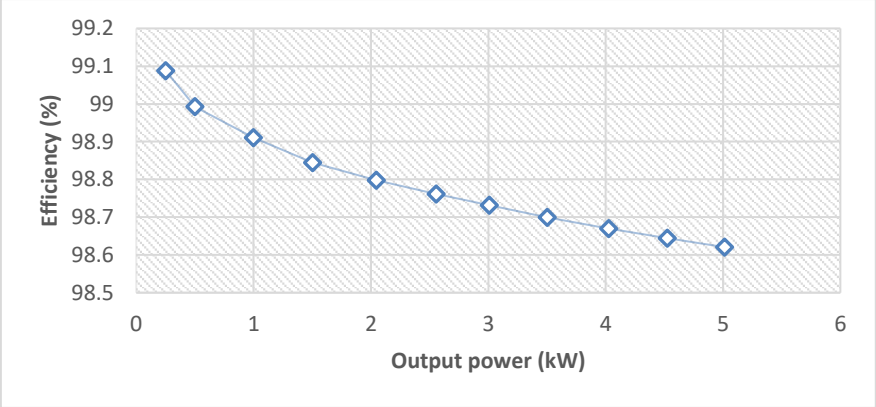
Thermal modelling of the proposed topology was performed using PLECS software. The model of IGBT/diode used for the loss analysis is provided in Table 2. Conduction and switching losses were evaluated for three different loading conditions, as shown in Figure 12(a) and 12(b). The results indicate that switching losses are smaller than conduction losses since the circuit was implemented using low switching frequency. Figure 12(c) shows the variation of efficiency with output power. The temperature profile of the switches, obtained through thermal analysis of the converter, is depicted in Figure 13. This profile is obtained while the converter is supplying a 1 kW load. It serves as a crucial parameter aiding in the selection of switches



(a) Conduction losses across switches



(b) Switching losses across switches



(c) Efficiency vs output power

Figure 12: Power losses and efficiency calculation for different loading conditions

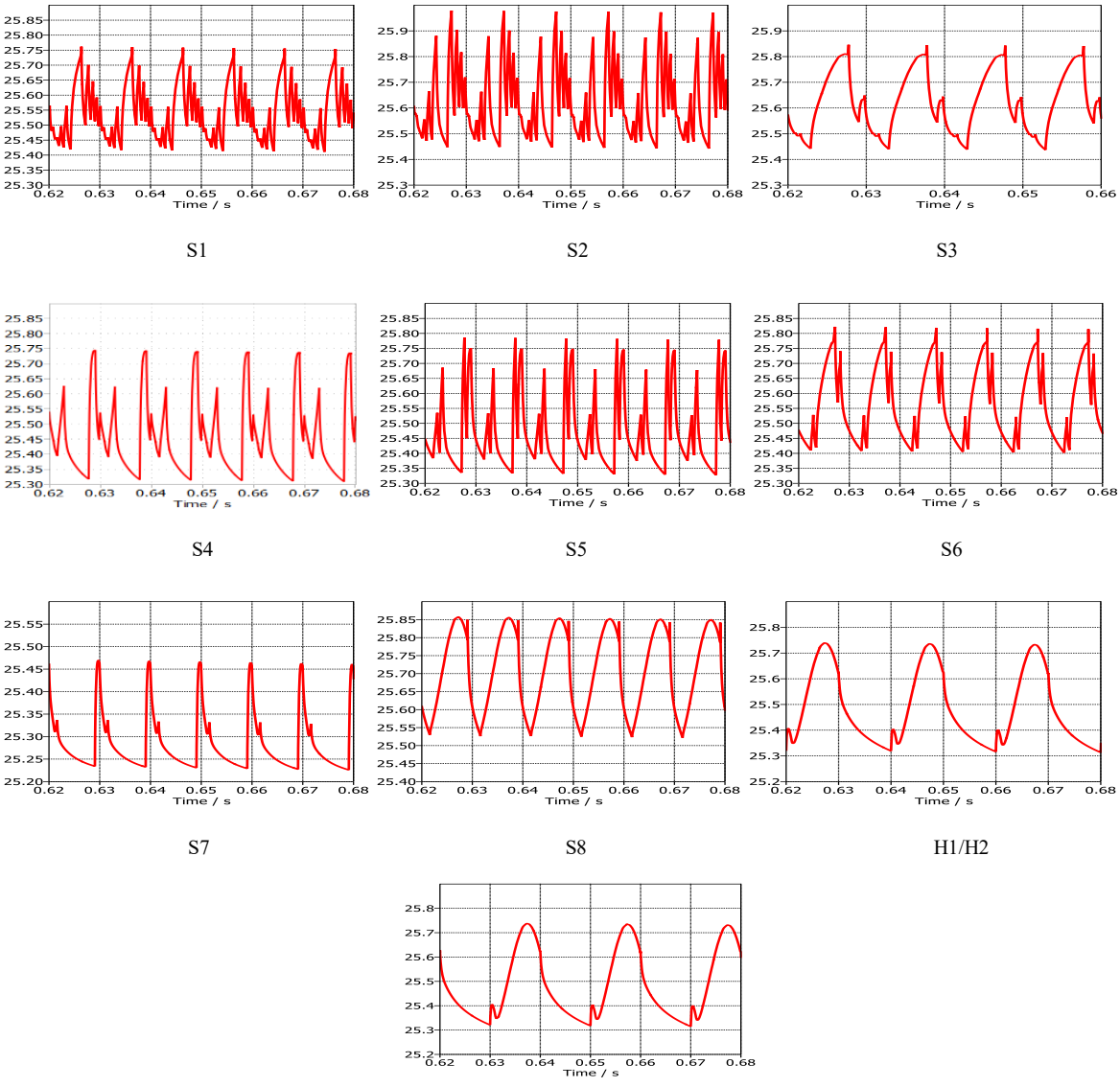


Figure 13 : Temperature Profile of Switches

4.4 Comparison of the proposed topology

This section is about the comparison of proposed topology with other multiple DC source topologies. The parameters considered for comparison include the number of levels (N_L), number of IGBTs (N_{IGBT}), number of gate drivers (N_{gd}), number of capacitors (N_C), number of dc sources (N_{dc}), TSV_{pu}, cost factor per level for $\alpha = 0.5$ and $\alpha = 1.5$ and as the topologies have different levels that is 17, 19 and 21. The value of TSV_{pu} is a crucial factor for determining the ratings of switches in the topology. The other parameter is the cost factor per level which helps to understand the economic validity of the proposed topology. Table 3 provides a comparison of the proposed topology with other similar topologies. The topology presented in [24-28] are generating 17 levels at the output [24], [25] and [28] are using 12 IGBTs to produce output levels, [24] and [28] have same number of gate drivers but [28] has lesser TSV_{pu} than [24] which decreases its cost factor per level. [25] is utilizing capacitors and also have high TSV_{pu}. The circuit of [26] has higher number of device count to generate same number of levels.[26] and [27] have same value of TSV_{pu} but [27] is using more number of components. [29P2] and 30 both are generating 21 levels, [30] is using lesser number of devices having N_{IGBT}/N_L of only 0.47 which is smallest also the value of TSV_{pu} is least on comparing with other topologies presented in table but using 6 dc sources. [31,32,33] are producing 19 levels, [31] and [32] both are using 18 IGBTs and [31] is using capacitors in order to reduce the number of dc sources which is more in [32]. [33] is using only 11 IGBTs but this topology is using 5 dc sources. On comparing with similar topologies, proposed topology is using lesser number of components and having least cost factor per level except [4].

Table 4: Comparative analysis

Topology	N_l	N_{IGBT}	N_{IGBT}/N_L	N_{gd}	N_{dc}	$TSV_{p.u.}$	N_C	CF/N_{level}, α=0.5	CF/N_{level}, α=1.5
24	17	12	0.70	10	4	6	0	1.7	2.05
25	17	12	0.70	12	2	6.6	3	1.9	2.28
26	17	16	0.94	14	4	6.5	4	2.42	2.8
27	17	18	1.05	18	8	6.5	0	2.77	3.16
28	17	12	0.70	10	4	5.5	0	1.69	2.01
29P2	21	16	0.76	16	7	6.7	0	2.01	2.33
30	21	10	0.47	10	6	4	0	1.33	1.52
31	19	18	0.94	18	2	4.9	4	2.33	2.59
32P2	19	18	0.94	18	6	4	0	2.31	2.52
33	19	11	0.57	10	5	6.25	0	1.53	1.86
Proposed	**19**	**12**	**0.63**	**12**	**3**	**6.22**	**0**	**1.58**	**1.91**

Conclusion and Future Work

This report presents a comprehensive study of various multilevel inverter (MLI) topologies, focusing on both conventional and advanced designs. It includes a detailed analysis of the Reduced Switch Count (RSC) topology and the implementation of the Nearest Level Control (NLC) technique for providing gating pulses to switches. A novel single-phase asymmetrical MLI topology capable of generating 19 output voltage levels is introduced, employing 12 switches and 3 DC sources using NLC, a low switching frequency technique to provide switching signal to switches that reduces switching losses compared to high-frequency switching techniques. Furthermore, an extended generalized structure of the topology is presented in which basic units are cascaded in order to increase the levels, the equations governing the generalized structure are also presented. The topology's performance is assessed using Plecs software under both static and dynamic loading conditions, demonstrating stable operation without waveform notches or spikes. Moreover, the Total Harmonic Distortion (THD) of the output voltage, measured at 4.34%, aligns with harmonic standards (IEEE-519). However, a drawback of the proposed topology is the absence of inherent negative voltage generation, necessitating the addition of an H-bridge inverter as a polarity generator. This increases the Total Switching Loss per unit (TSVpu) of the converter. Nonetheless, the topology displays a reduced component count compared to similar alternatives discussed in the comparative analysis section.

In conclusion, this report underscores the significance of innovative MLI designs and low switching frequency techniques for enhancing power conversion system efficiency and stability. It provides insights for optimizing MLI setups for various applications, contributing to advancements in power electronics and renewable energy systems.Additionally, MLI technology finds applications in diverse fields such as renewable energy integration, motor drives, and grid-tied systems, offering solutions for efficient energy management and grid stability topology exhibits a reduced component count compared to similar other topology discussed in comparative analysis section.

The following future work is possible for proposed topology:

1. As the proposed topology is utilizing H-bridge inverter as a polarity generator hence the stress on the switches is high which increases the Total Switching Loss per unit (TSV_{pu}) of the converter.

2. Hardware validation is also required for practical application.

3. Work on research paper named as " An Improved 19 level asymmetrical topology with reduced component count and cost factor." is in progress.

References

[1] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A.M. Prats and M. A. Perez, “Multilevel Converters: An Enabling Technology for High-Power Applications”, IEEE Proceeding, Vol 97,No. 11, pp.1786 – 1817, November 2009.

[2] B. Rajender, "A dissertation submitted in partial fulfillment of the requirements for the award of the degree of Master of Technology in Electrical Engineering with specialization in Electric Drives and Power Electronics," Indian Institute of Technology Roorkee, June 2011.

[3] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, “Multilevel inverter topologies with reduced device count: A review,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135−151, Jan. 2016.

[4] H. P. Vemuganti, D. Sreenivasarao, S. K. Ganjikunta, H. M. Suryawanshi and H. Abu-Rub, "A survey on reduced switch count multilevel inverters", *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 80-111, Jan. 2021.

[5] E. Samadaei, A. Sheikholeslami, S. A. Gholamian and J. Adabi, "A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters," in *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 987-996, Feb. 2018, doi: 10.1109/TPEL.2017.2675381.

[6] E. Samadaei, M. Kaviani, and K. Bertilsson, “A 13-levels module (K-type) with two DC sources for multilevel inverters,” IEEE Trans. Ind. Electron., vol. 66, no. 7, pp. 5186–5196, Jul. 2019.

[7] Y. Ounejjar, K. Al-Haddad, and L.-A. Gregoire, “Packed U cells multilevel converter topology: Theoretical study and experimental validation,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1294–1306, Apr. 2011.

[8] K. K. Gupta and S. Jain, “A novel multilevel inverter based on switched DC sources,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269−3278, Jul. 2014.

[9] V. Nair R, K. Gopakumar and L. G. Franquelo, "A Very High Resolution Stacked Multilevel Inverter Topology for Adjustable Speed Drives", *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2049-2056, March 2018.

[10] Jena, Kasinath & Kumar, Dhananjay & Hemanth Kumar, B & Kavali, Janardhan & Singh, Arvind & Naidoo, Raj & Bansal, Ramesh. (2023). A Single DC Source Generalized Switched Capacitors Multilevel Inverter with Minimal Component Count. International Transactions on Electrical Energy Systems. 2023. 1-12. 10.1155/2023/3945160.

[11] M. Kumari, M. D. Siddique, A. Sarwar, M. Tariq, S. Mekhilef and A. Iqbal, "Recent trends and review on switched-capacitor-based singlestage boost multilevel inverter", *Int. Trans. Elect. Energy Syst.*, vol. 31, no. 3, 2021.

[12] S. Behara, N. Sandeep and U. R. Yaragatti, "Design and Implementation of Transformer-Based Multilevel Inverter Topology With Reduced Components," in *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4632-4639, Sept.-Oct. 2018.

[13] V. Thiyagarajan and P. Somasundaram, "Simulation of New Symmetric and Asymmetric Multilevel Inverter Topology with Reduced Number of Switches", *2018 4th International Conference on Electrical Energy Systems (ICEES)*, pp. 315-319, 2018.

[14] M. D. Siddique et al., "Single phase symmetrical and asymmetrical design of multilevel inverter topology with reduced number of switches", *Proc. IEEE IEEMA Eng. Infinite Conf.*, pp. 1-6, 2018.

[15] R. Barzegarkhoo, M. Moradzadeh, E. Zamiri, H. M. Kojabadi, and F. Blaabjerg, ``A new boost switched-capacitor multilevel converter with reduced circuit devices," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6738_6754, Aug. 2018.

[16] M. S. B. Arif, U. Mustafa, S. B. M. Ayob, J. Rodriguez, A. Nadeem and M. Abdelrahem, "Asymmetrical 17-Level inverter topology with reduced total standing voltage and device count", *IEEE Access*, vol. 9, pp. 69710-69723, 2021.

[17] Shehu, Gaddafi & Kunya, Abdullahi & Shanono, Ibrahim & Yalcinoz, Tankut. (2016). A Review of Multilevel Inverter Topology and Control Techniques. International Journal of Automation and Control. 4. 233-241. 10.18178/joace.4.3.233-241.

[18] Z. Sarwer *et al*., "Implementation of a Novel Variable Structure Nearest Level Modulation on Cascaded H-Bridge Multilevel Inverter," in *IEEE Access*, vol. 9, pp. 133974-133988, 2021, doi: 10.1109/ACCESS.2021.3113704.

[19] Z. A. Al-Jawary, "Study and Evaluation of Distributed Power Electronic Converters in Photovoltaic Generation Applications," Ph.D. dissertation, University of Valladolid, Department of Electronic Technology, Ph.D. program in Industrial Engineering, Valladolid, Spain, Mar. 2022.

[20] U. Mustafa, M. S. B. Arif, R. Kennel and M. Abdelrahem, "Asymmetrical eleven-level inverter topology with reduced power semiconductor switches total standing voltage and cost factor", *IET Power Electronics*, vol. 15, pp. 395-411, 04 2022.

[21] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An IndustryBased Survey of Reliability in Power Electronic Converters," IEEE Trans. Ind. Appl., vol. 47, no. 3, pp. 1441 1451, 2011.

[22] Alavi, O.; Hooshmand Viki, A.; Shamlou, S. A Comparative Reliability Study of Three Fundamental Multilevel Inverters Using Two Different Approaches. *Electronics* **2016**, *5*,18.

[23] US Department of Defense: MIL-HDBK-217F (NOTICE 2), Military Handbook Reliability Prediction of Electronic Equipment. Defense Technical Information Center: Alexandria, USA (1995)

[24] Alishah RS, Hosseini SH, Babaei E, Sabahi M. A new general multilevel converter topology based on cascaded connection of submultilevel units with reduced switching components, DC sources, and blocked voltage by switches. IEEE Trans Ind Electron. 2016;63 (11):7157-7164.

[25] Ngo, B., Nguyen, M., Kim, J., Zare, F.: Single-phase multilevel inverter based on switched-capacitor structure. IET Power Electron. 11(11), 1858–1865 (2018)

[26] Dhanamjayulu, C., Prasad, D., Padmanaban, S., Maroti, P.K., Holm-Nielsen, J.B., Blaabjerg, F.: Design and implementation of seventeen level inverter with reduced components. IEEE Access. 9, 16746–16760 (2021)
[27]. Seifi, A., Hosseini, S.H., Hagh, M.T., Hosseinpour, M.:New multilevel inverter based on reduced switch basic cell for high voltage levels. IET Power Electron. 1–13 (2024).

[28] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, ``A new general multilevel converter topology based on cascaded connection of submultilevel units with reduced switching components, DC sources, and blocked voltage by switches," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11,pp. 7157_7164, Nov. 2016.

[29] E. Babaei, S. Laali and Z. Bayat, "A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches," IEEE Trans. Ind. Electron., vol. 62, no. 2, pp. 922-929, Feb. 2015.

[30] S. T. Meraj, N. Z. Yahaya, K. Hasan, and A. Masaoud, ``Single phase 21 level hybrid multilevel inverter with reduced power components employing low frequency modulation technique," *Int. J. Power Electron. Drive Syst.*,vol. 11, no. 2, p. 810, Jun. 2020.

[31] Dargahi, V., Sadigh, A.K., Abarzadeh, M., Pahlavani, M.R.A., Shoulaie, A.: Flying capacitor reduction in an improved double flying capacitor multicell converter controlled by a modified modulation method. IEEE Trans. Power Electron. 27(9), 3875–3887 (2012).

[32] E. Babaei, S. Laali and S. Alilu, "Cascaded Multilevel Inverter With Series Connection of Novel H-Bridge Basic Units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6664-6671, Dec. 2014.

[33] Hosseini Montazer B, Olamaei J, Hosseinpour M, Mozafari B. A generalized diode containing bidirectional topology for multilevel inverter with reduced switches and power loss. Int J Circ Theor Appl. 2021;1–20