FILTER AND ACTIVE CIRCUITS DESIGN: PRE LAB REPORT

Q1A)

Solving for BPF inductors and capcitors from LPF g-tables:

Q1a.)

$N=3$, $\Delta = 0.02$, $\omega_0 = 2\pi(60\times10^6 \times 100)$, $R_s = 50\Omega$

$= 2\pi(60\times10^8)$

$= 3.7699\times10^{10}$

$= 37.69$ G rad/sec

$L_1' = \dfrac{g_1 R_s}{\Delta \omega_0} \Rightarrow j_1 = 0.6708 \rightarrow L_1' = 4.4494\times10^{-8}$ H

$C_1' = \dfrac{\Delta}{\omega_0 g_1 R_s} = 1.5821\times10^{-14}$ F

$L_2' = \dfrac{\Delta R_s}{\omega_0 g_2} \Rightarrow g_2 = 1.003 \longrightarrow L_1' = 2.64528\times10^{-11}$ H

$C_2' = \dfrac{g_2}{\Delta \omega_0 R_s} = 2.6612\times10^{-11}$ F

$L_3' = L_1'$

$C_3' = C_1'$

Q1B)

b) Design the filter using microstrip resonators coupled with chip capacitors as shown in Fig. 2. The substrate parameters are H=1.27 mm, ε_r= 9.8. Use LineCalc or [Microstrip Cal] to get dimensions.

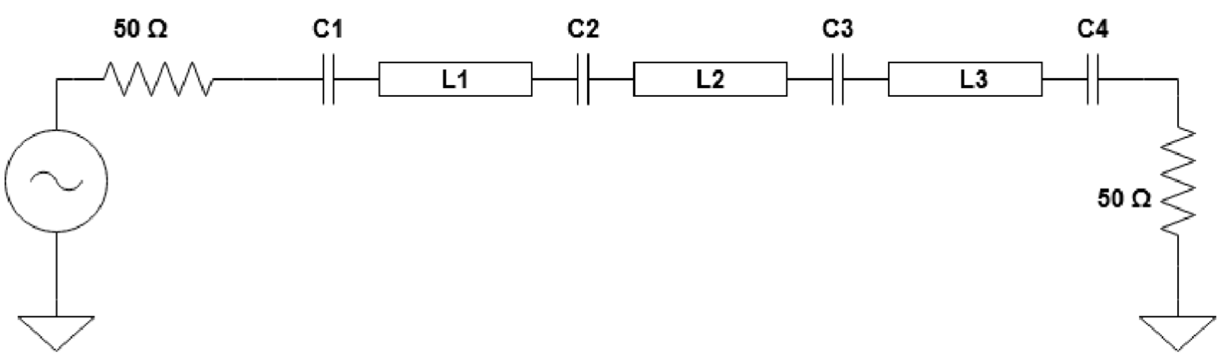
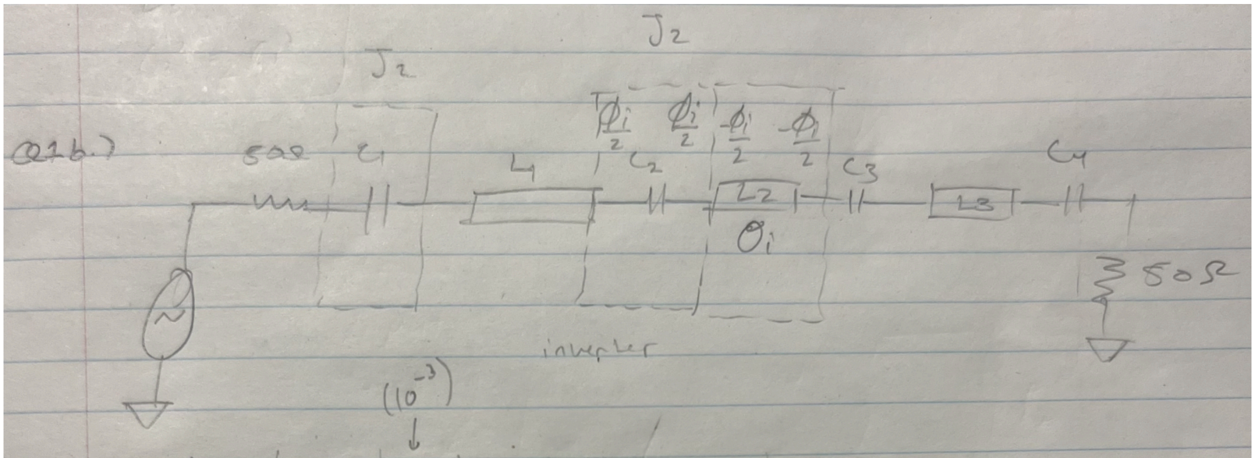


Figure 2: Third order BPF using capacitively coupled series resonators

Capacitance Values



n	g_n	$Z_0 J_n$	B (10^{-3})	C	ϕ_i	θ_i
1	0.6708	0.21641	4.54	12.04 pF	$-24.42°$	$165.597°$
2	1.003	0.0383	0.7671	2.03479×10^{-14} F	$-4.387°$	$175.613°$
3	0.6708	0.0383	0.7671	2.03479×10^{-14} F	$-4.387°$	$165.597°$
4	1.00	0.21641	4.54	12.04 pF	$-24.42°$	

L1 = L3

εr: 9.8 | Tanδ: 0.00 | GHz | Rho: 1

Height: 50 mils | Thickness: 1.37795 mils | Frequency: 6 GHz

Analysis/Synthesis Values

Width: 48.77291 mils | Zo: 50.00 Ohms

Length: 344.51639 mils | Angle: 165.597 degrees

Analyze | Synthesize

εeff: 5.129 | Loss: 0.012 dB

L2

εr:	9.8		Tanδ:	0.00	GHz	Rho:	1
Height:	50	mils	Thickness:	1.37795	mils	Frequency:	6	GHz

Analysis/Synthesis Values

Width:	48.77291	mils	Zo:	50.00	Ohms
Length:	365.35419	mils	Angle:	175.613	degrees
	Analyze			Synthesize	
εeff:	5.129		Loss:	0.013	dB

Q2

First checking for stability

Q2.) lets start by solving for stability:

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} = 1.7374 > 1$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} = 0.5358 \angle -85.25^\circ$$

$$|\Delta| = 0.5358 < 1$$

$\therefore$ device is unconditionally stable.

finding Γ_s & Γ_L $\left(\Delta = S_{11}S_{22} - S_{12}S_{21} = 0.5358 \angle 85.23^\circ\right)$

$$\Gamma_s = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \qquad \Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$
$$= 1.0468$$
$$C_1 = S_{11} - \Delta S_{22}^*$$
$$= 0.5206 \angle 97.294$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2$$
$$= 0.3794$$
$$C_2 = S_{22} - \Delta S_{11}^*$$
$$= 0.1828 \angle 164.69^\circ$$

$\therefore \Gamma_s = 0.904 \angle -97.29^\circ$

$(-0.1147 - i\,0.8967)$

$\therefore \Gamma_L = 0.7604 \angle -164.69^\circ$

$(-0.7334 - i\,0.2007)$

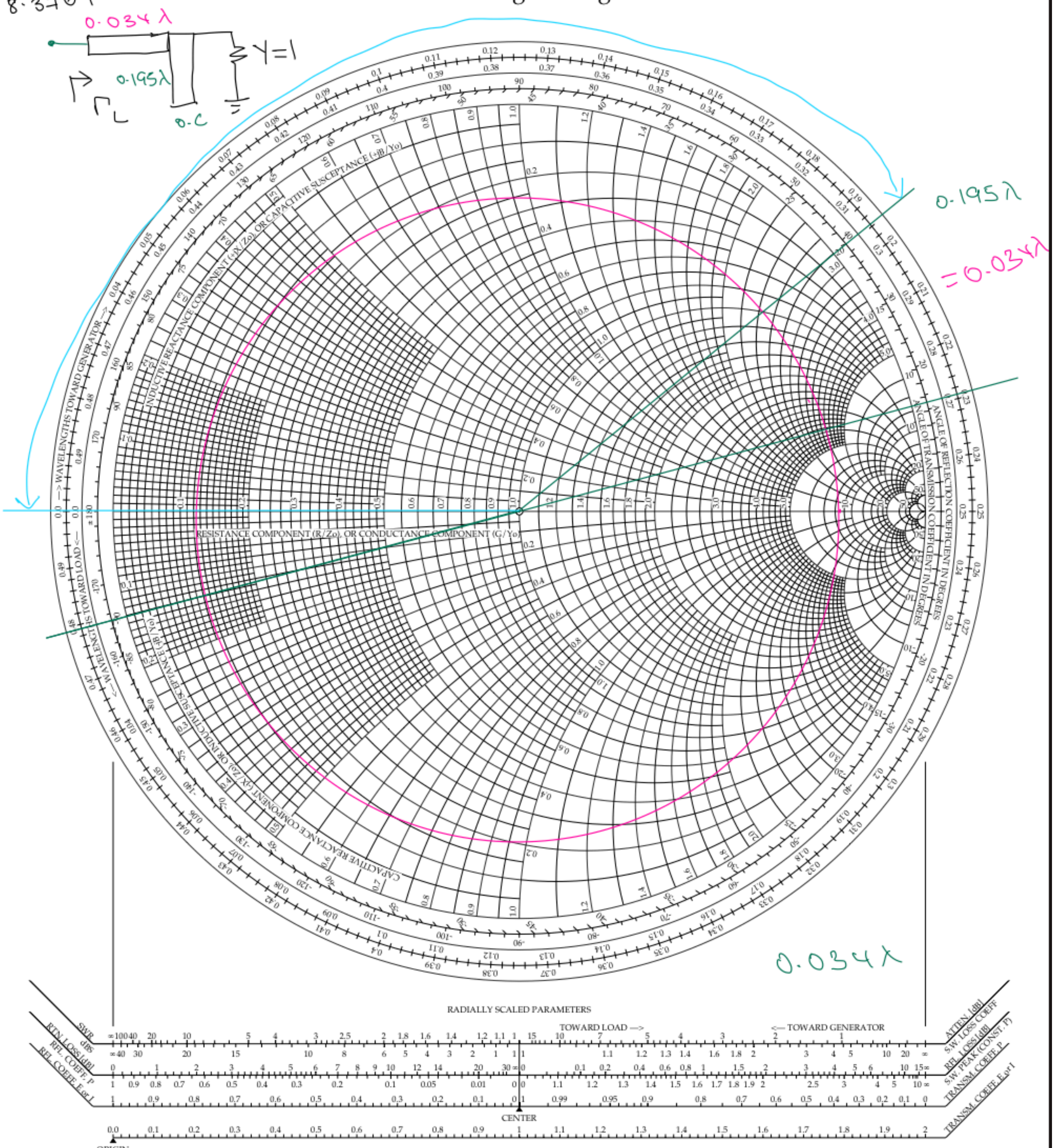
Now working with the Smith Chart:

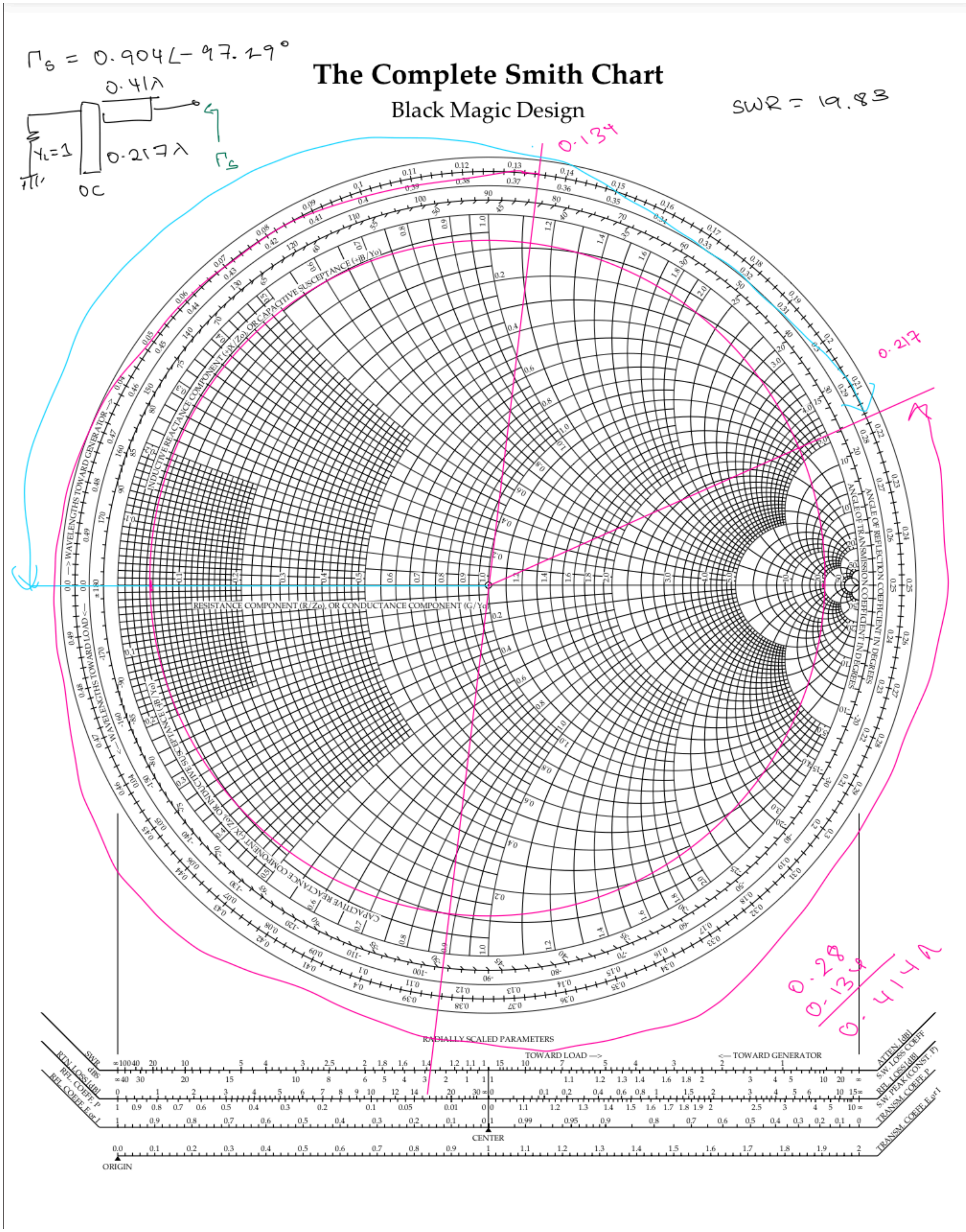
$\Gamma_L = 0.7604 \angle -164.69$

The Complete Smith Chart

Black Magic Design

8.3764





Now solving for maximum gain:

maximum gain can be computed from:

$$G_{T\,max} = \frac{1}{1 - |\Gamma_s|^2} \cdot |S_{21}|^2 \cdot \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}$$

$$= 30.2836$$

FILTER AND ACTIVE CIRCUITS DESIGN: POST LAB REPORT

Prelab calculations have been highlighted in previous pages. Below these calculations are summarized using tables.

2. Design Requirements

a. Chebyshev Bandpass Filter

- **Design using lumped circuit elements**

$\Delta = 0.02$

$w_o = 37.696$G rad/sec

	[H]		[F]
	$4.4494 \cdot 10^{-8}$		$1.5821 \cdot 10^{-14}$ $1.5821 \cdot 10-14$
	$2.64528 \cdot 10^{-11}$		$2.6612 \cdot 10^{-11}$ $2.6612 \cdot 10-11$
	$4.4494 \cdot 10^{-8}$ $4.4494 \cdot 10^{-8}$		$1.5821 \cdot 10^{-14}$ $1.5821 \cdot 10-14$

- **Design using microstrip resonators**

	g_n	Z_oJ_n	B	C	ϕ_i	θ_i

	0.6708	0.21641	4.54	12.04pF	-24.42	165.597
	1.003	0.0383	0.7671	2.03479 * 10 ^ -14	-4.387	175.613
	0.6708	0.0383	0.7671	12.04pF	-4.387	165.597
	1.000	0.21641	4.54	2.03479 * 10 ^ -14	-24.42	

L1 = L3:

	g_n
Width	48.77291 mils
Length	344.51639 mils
Zo	50 ohms
Angle	165.597 degrees
e_eff	5.129
Loss	0.012 dB

L2

	g_n
Width	48.77291 mils
Length	365.35419 mils
Zo	50 ohms
Angle	175.613 degrees
e_eff	5.129

Loss	0.013 dB

b. Amplifier

$$k = 1.7374 > 1$$

$$\Delta = 0.5358 \angle -85.25$$

$$|\Delta| = 0.5358 < 1$$

, leading us to conclude that teh device is unconditionally stable

Γ_L	$0.7604 \angle -164.69$ $0.7604 \angle -164.69$	0.034 λ	0.195 λ
Γ_S	$0.904 \angle -97.29$ $0.904 \angle -97.29$	0.41 λ	0.217 λ

We then get that:

$$Gt\max = 30.2836$$

Gtmax = 30.2836

3. & 4. Schematics of ADS circuits & comments on S-Parameter graphs

PART 1A

Part 1

I. Use ADS to simulate the lumped elements BPF

Construct the circuit shown in Fig. 3 using the values you got from the prelab calculation.

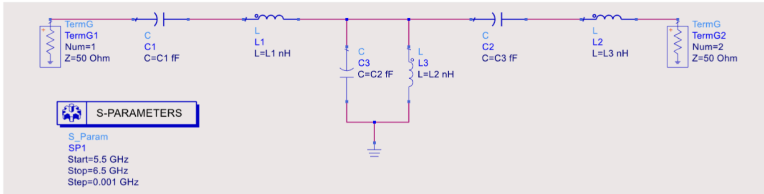
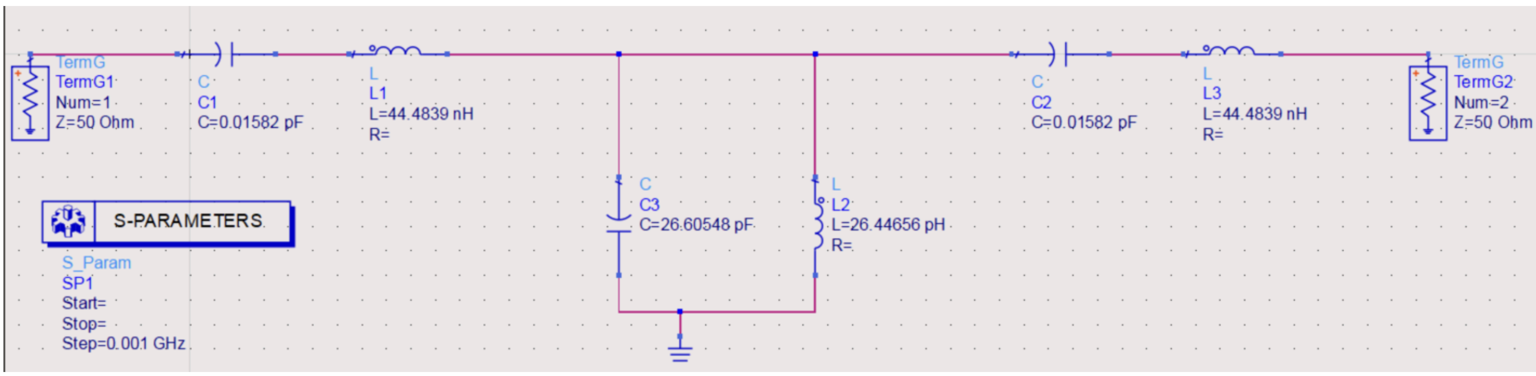
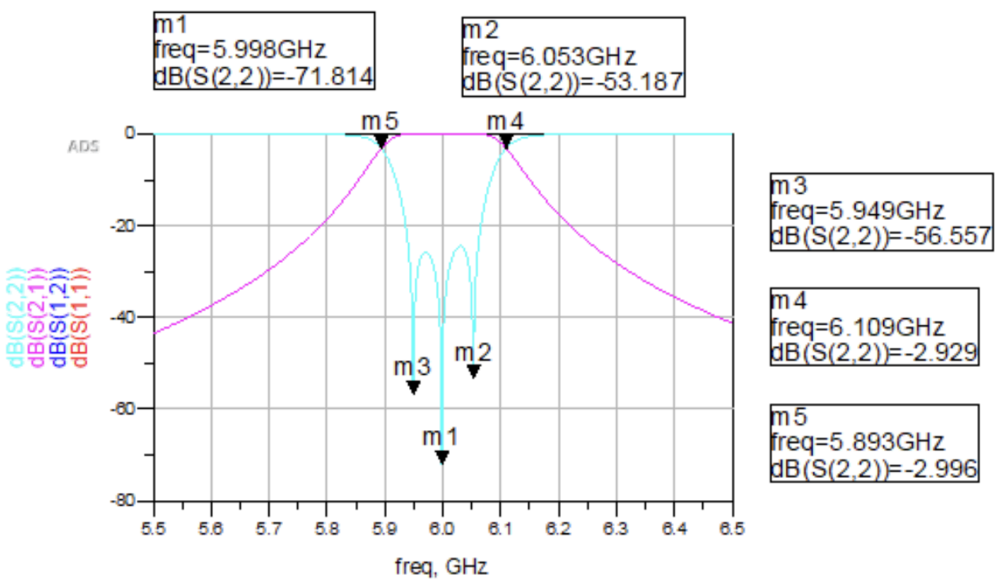


Figure 4: Schematic of BPF with lumped elements

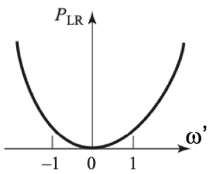
Simulate and plot S_{11} and S_{21} of this filter at center frequency with 1 GHz span. Determine the bandwidth and insertion loss from the graph and compare them with the theoretical calculated values.

Schematic & Simulations:

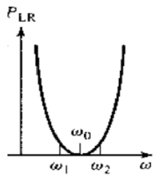




Lowpass filter:



Bandpass filter:



$$\omega = \omega_0 \;\rightarrow\; \omega' = 0$$
$$\omega = \omega_1 \;\rightarrow\; \omega' = -1$$
$$\omega = \omega_2 \;\rightarrow\; \omega' = +1$$

From Lowpass to Bandpass:

$$\omega' = \frac{\omega_0}{\omega_2 - \omega_1}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)$$
$$= \frac{1}{\Delta}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)$$
$$\omega_0 = \sqrt{\omega_1 \omega_2}$$
$$\Delta = \frac{\omega_2 - \omega_1}{\omega_0}$$

fractional bandwidth of the passband

Comment on graphs: We see that we have simulated a third order bandpass filter. First let's consider how parameters were solved. As we analyze the transitions on the right, we know a lowpass filter (low P_LR and lower frequencies) can be realized as a bandpass filter (low P_LR in both sides of center frequency). Therefore, by using given formulas (seen in prelab calculations) we can solve for a bandpass equivalent circuit, which converts series inductors to a series combination of an inductor and capacitor, and a shunt capacitor is converted to a parallel inductor and capacitor.

Now, we notice that the graph shows S(1,2) & S(2,1) at 0 dB and resonance frequencies while S(2,2) & S(1,1) at have dropped below –25 dB at resonant frequencies, but why does this occur and make sense? We were assigned to create a 0.0138 dB ripple Chebyshev filter, which could be done using the tables and formulas provided in lectures, they are formulated to create assigned ripples at certain frequencies, if correct numbers were used, we could achieve the bandpass filter response, otherwise, fine-tuning of inductors and capacitors to alter the bandpass filter response to what is expected.

<u>PART 1B</u>

II. <u>Use ADS to simulate the capacitively coupled series resonator BPF</u>

Construct the circuit shown in Fig. 4 using the values you obtained from prelab calculation.

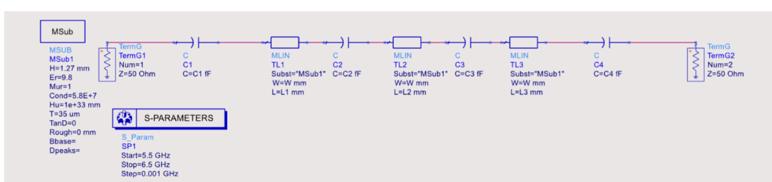
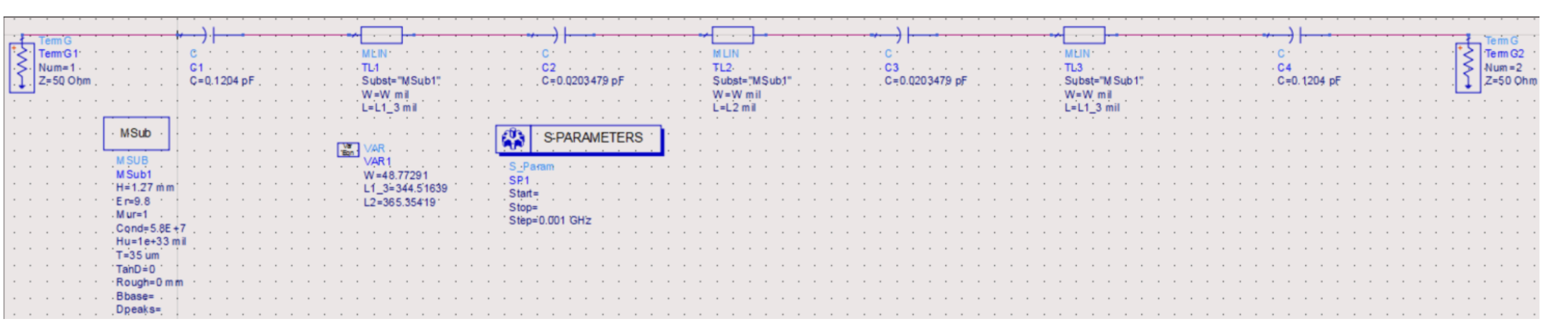
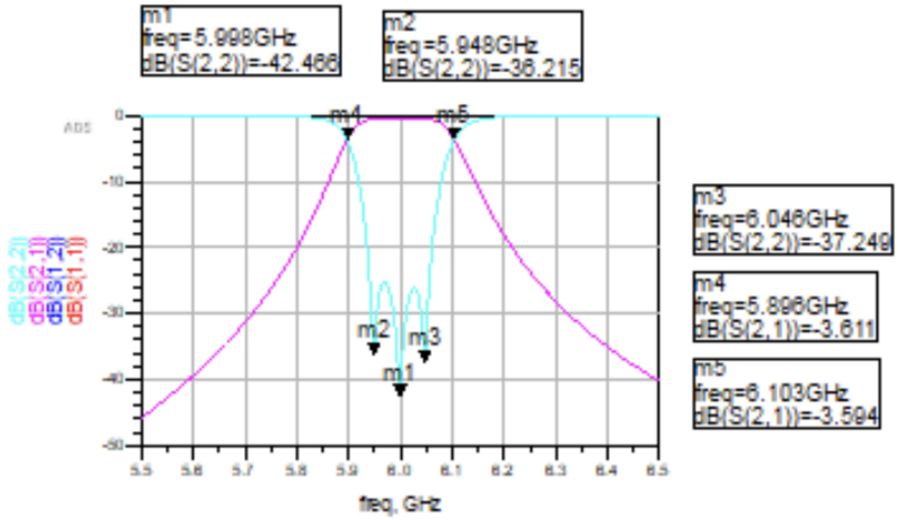


Figure 5: Schematic of BPF with capacitively coupled resonators

Simulate and plot the s-parameters of this filter at center frequency with 1 GHz span. Determine the bandwidth and insertion loss from the graph and compare the results to the BPF with ideal lumped elements.

Schematic & Simulations:





Comments on graphs: We notice that the S-parameter simulations provide the same output as the previous part, this makes sense as the above circuit is represented by the same low pass filter g table as the bandpass filter. Therefore, the values of the capacitances and transmission line lengths (which comes from the solved theta values (seen in prelab)) are derived from the same g values of the 0.0138dB ripple (which is why we see a similar response).

Additionally, the reason why we see 3 poles is because each transmission line represents a resonator that while the capacitors represent inverters with some physical dimensions.

<u>PART 2A</u>

Part 2

I. <u>Simulate the amplifier with optimal source and load impedances</u>

Use the values you got in the prelab for Γ_s & Γ_L to get optimized source and load impedance for the amplifier as shown in Fig. 5. (The purpose of this step is to check your calculation for Γ_s & Γ_L, before realizing the matching network).

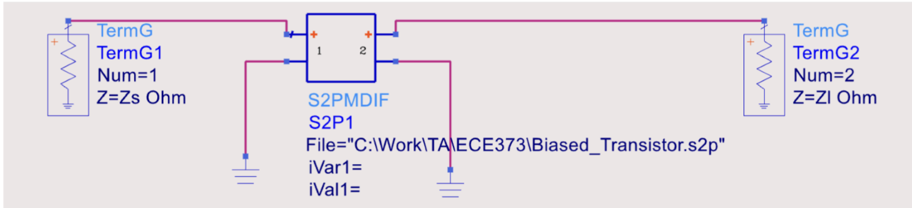
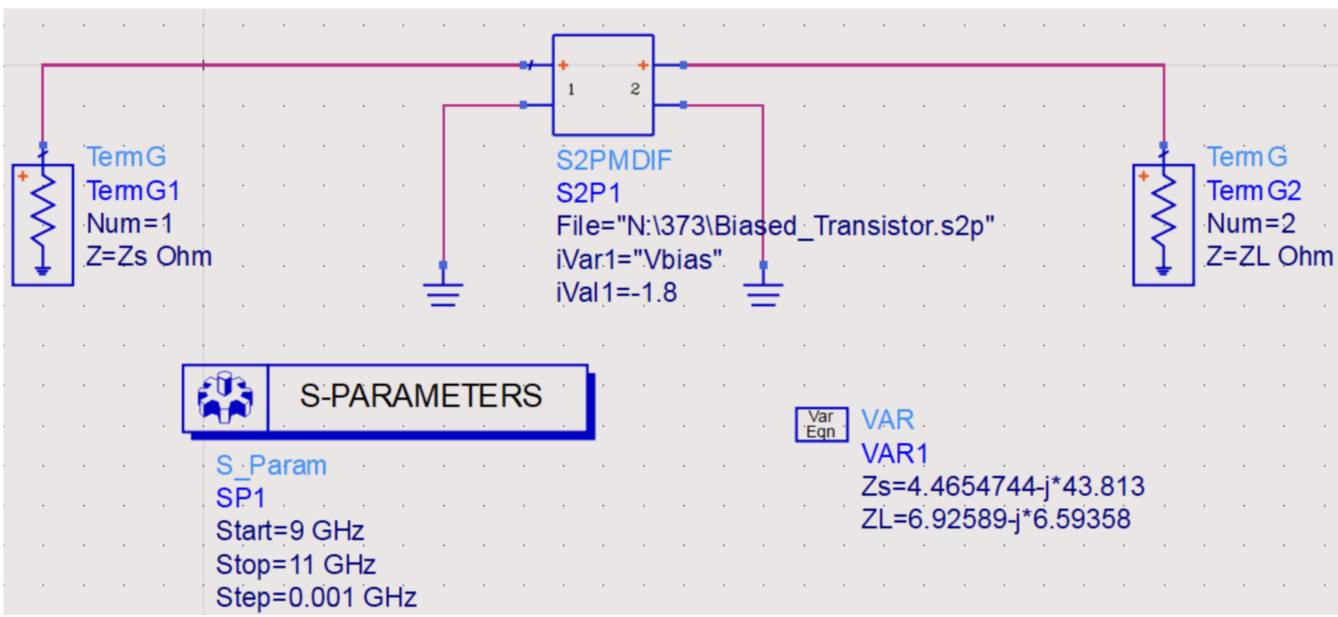


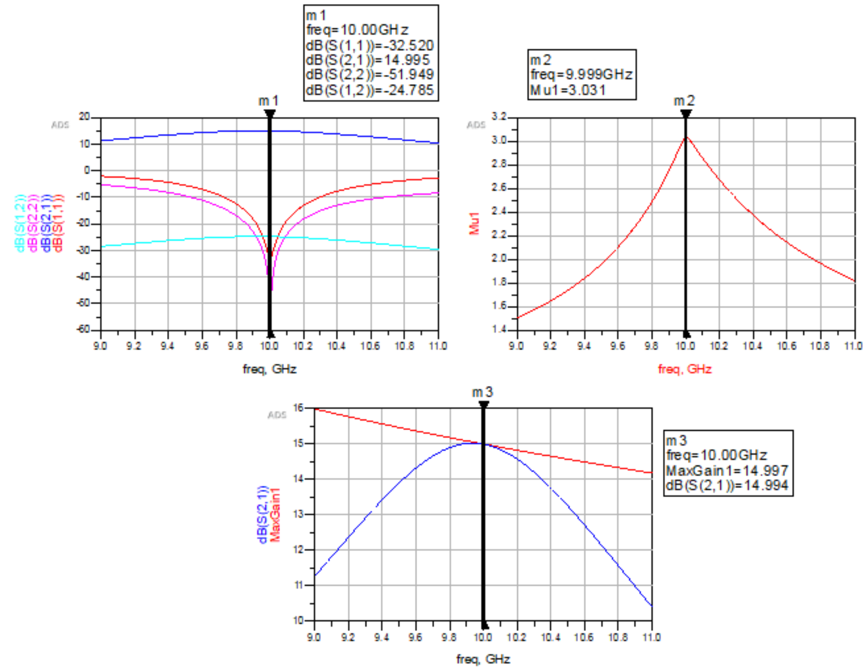
Figure 6: Amplifier simulation with the optimal ZS and ZL values.

To add the transistor amplifier to the schematic, open the **S2PMDIF** component in the "Data Items" palette and browse for the transistor S2P file "Biased_Transistor.s2p". Change the file type to be "S2PMDIF". For $iVar1$, enter "$Vbias$" (with quotes) and for $iVal1$, **enter the $\boldsymbol{Vbias}$ value corresponding to your lab group number (refer to Table II).**

Simulate and plot the s-parameters of this amplifier from 9 GHz to 11 GHz, as well as the maximum available gain (MaxGain component). Also plot the stability factor (Mu component). Ensure that your gain reaches the maximum possible gain at 10 GHz, and that your design is matched at 10 GHz. Report the matching, gain, and bandwidth achieved (bandwidth defined as $|S_{11}|$, $|S_{22}|$ <-10 dB).

Schematic & Simulations:





Comments on graph: Firstly, the graph representing the S-parameters shows:

- S(1,1) at –30 dB, this represents matching and efficient power transmission into the biased transistor amplifier
- S(2,1) at +15 dB, we know positive dB on a log scale means the numerator is greater than the denominator, which means that our output power is greater than the input power (representing an amplification)
- S(1,2) at –24 dB, this could represent a unilateral transistor (power amplification is one way), which is why we see a low dB
- S(2,2) at –50 dB, again to similar reasons to S(1,1); we see matching to create a low dB

The next graph we analyze the maximum gain of the transistor and S(2,1). Before talking about this, we should realize that the max gain of a transistor will tend to decrease at higher frequencies (since higher frequencies result in larger parasitic reactance's, affecting the overall gain), for this reason the red curve linearly decreases at higher frequencies. In the graph, we notice that at 10GHz, the transistor has a maximum gain of 14.994 dB (this can be shown by analyzing transistor circuitry of the given file path), which makes sense as the transistor (which functions best at 10GHz) also peaks power efficiency at 10GHz. The point of intersection between the blue and red curved shows maximum performance given the devices matching design (we mention matching to realize the peak in S(2,1)).

Additionally, mu, or the stability factor should be a value greater than 1 at the designed frequency. Therefore, having a value of 3.031 shows stability of the transistor at 10GHz

<u>PART 2B</u>

II. Simulate the amplifier with the matching networks

Now set the input and output port impedances to 50 Ω and insert the matching networks implemented as microstrip lines and stubs and re-simulate the amplifier as shown in Fig. 6.

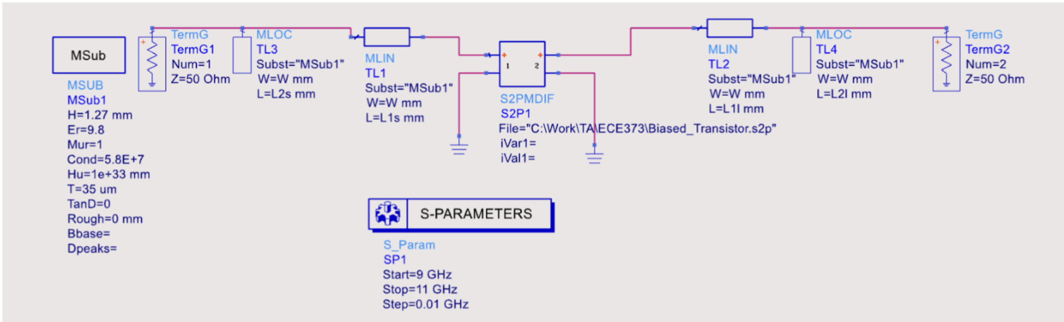
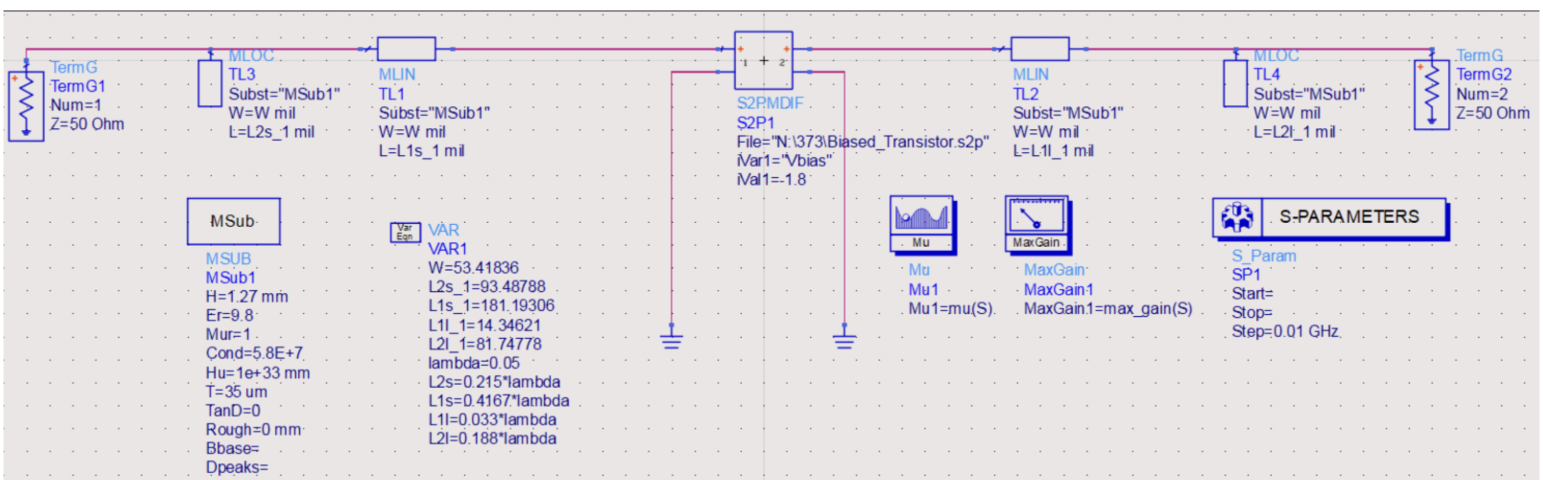


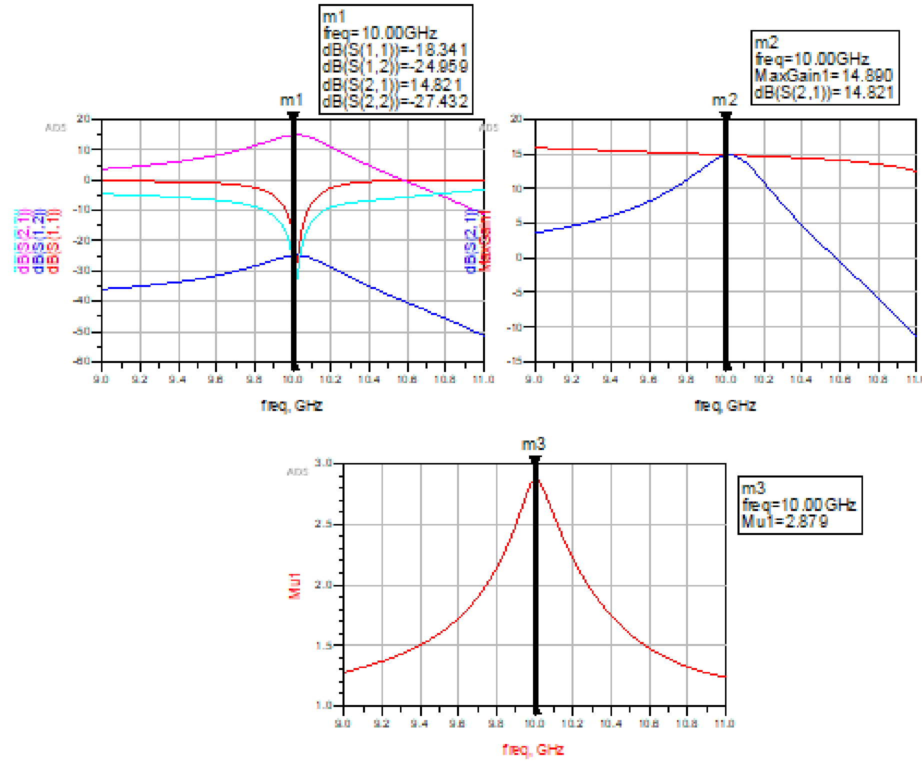
Figure 7: Amplifier design using actual matching networks

Note that for simplification, we didn't add the Tee junctions for the microstrip stub matching network to make sure that ADS results match your calculations. Add the microstrip T-junctions afterwards and tune the matching network parameters to get the maximum gain back at 10 GHz.

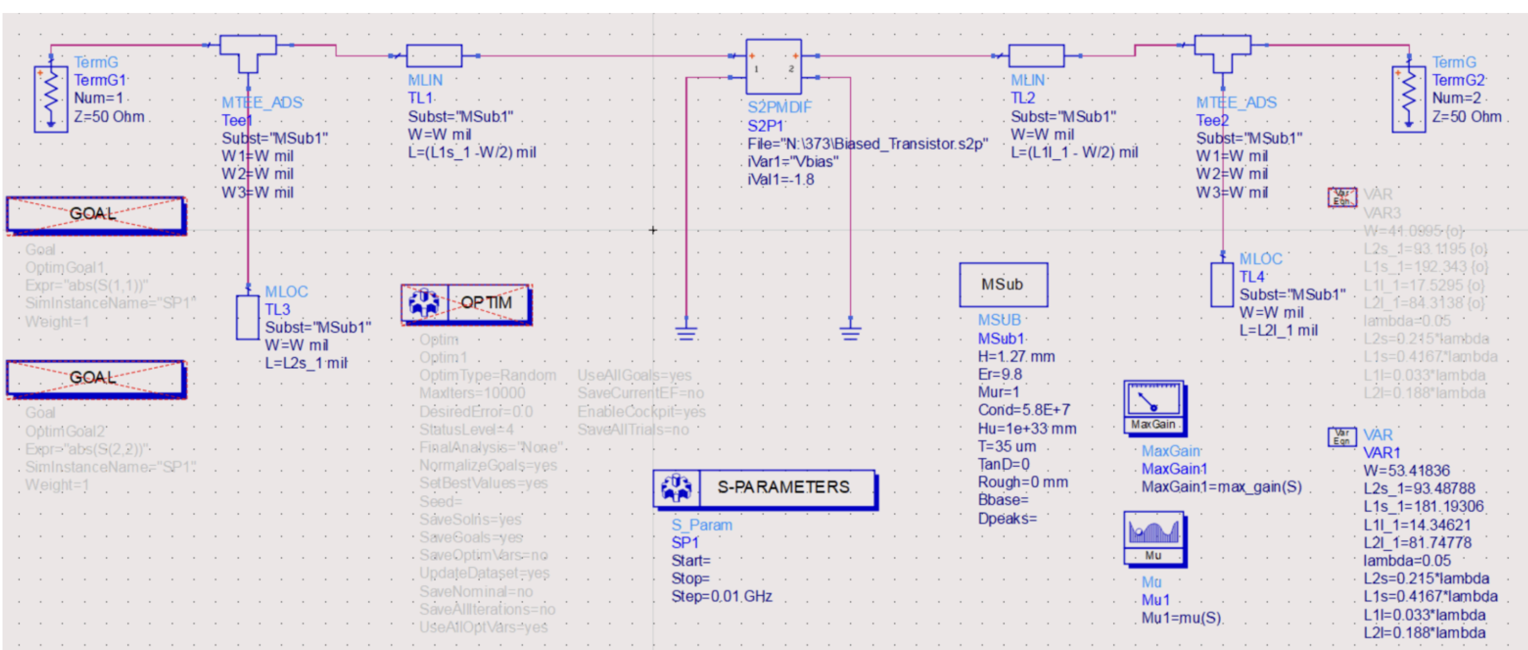
Simulate and plot the s-parameters of this amplifier from 9 GHz to 11 GHz, as well as the maximum available gain and stability factor. Ensure that your gain reaches the maximum possible gain at 10 GHz, and that your design is matched at 10 GHz. Report the matching, gain, and bandwidth achieved with the final design (bandwidth defined as $|S_{11}|$, $|S_{22}|$ <-10 dB). Compare the gain and bandwidth with the previous case.

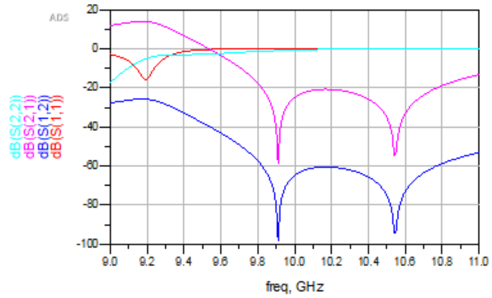
These are our simulations before the TEE junctions are included:

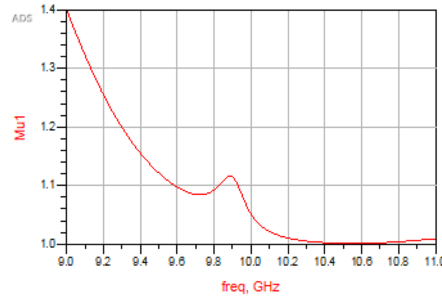


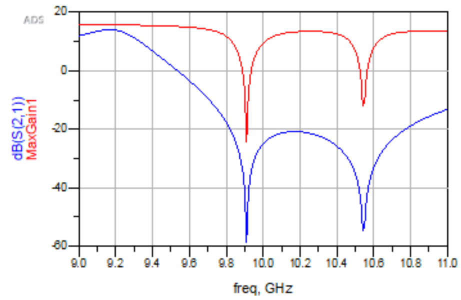


These are our simulations after the TEE junctions are included and before we optimized:

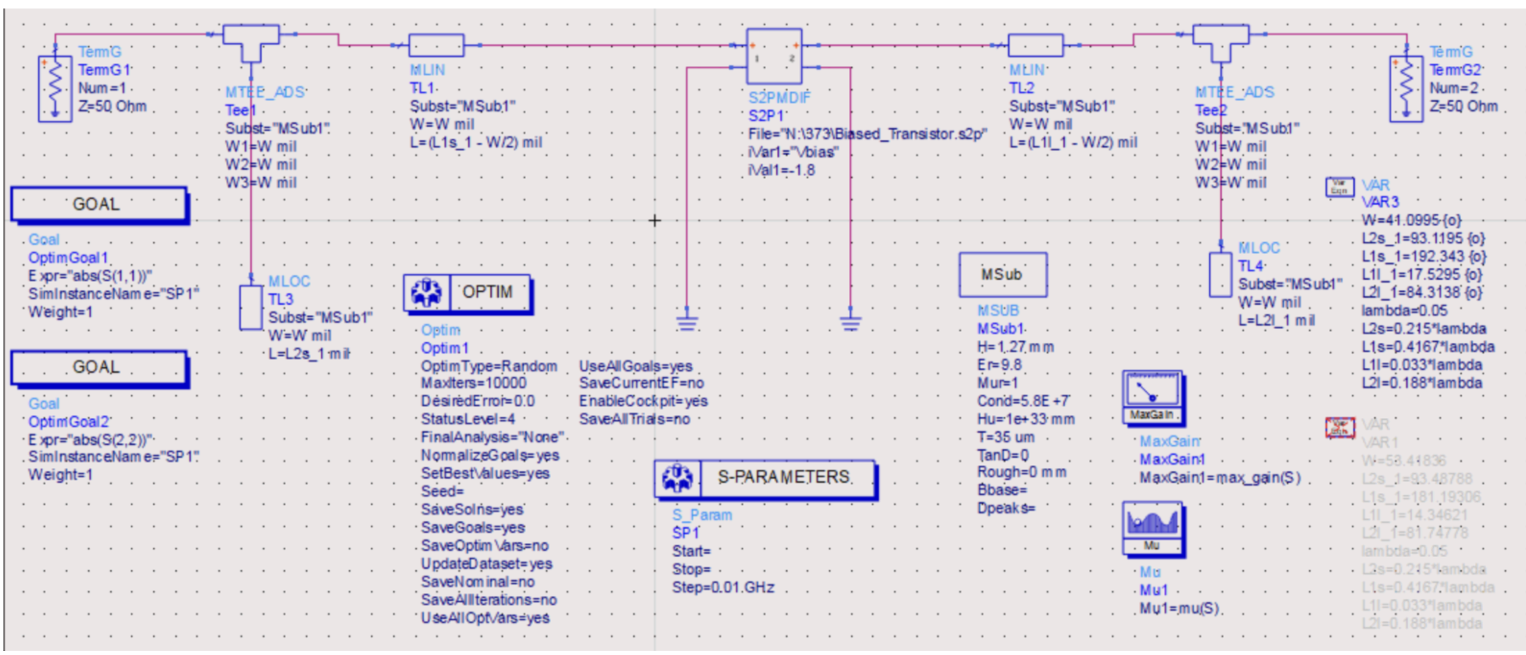


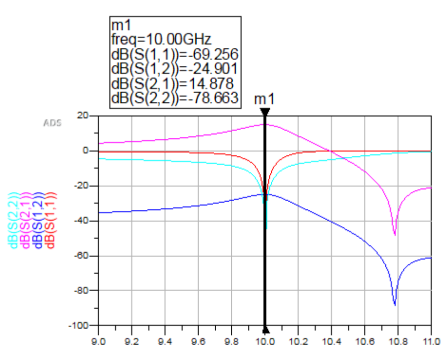


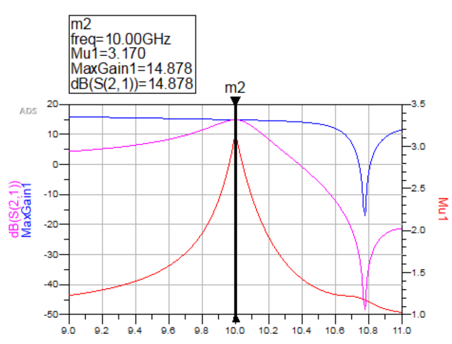




These are our simulations after optimizing:







Comments on above graphs: We notice in the first simulation (simulation of transmission line and open circuit stubs), we notice that our results mirror the results in the prior experiment. This makes sense as the gamma_s and gamma_l that were previously formulated as now represented by distances observed on a smith chart. By solving for distances (as functions of lambda seen in the prelab) we can create an equivalent circuit that is terminated by loads on both sides.

In the second simulation (including the tee junction and without optimization), we notice that our graphs display skewed results. This occurs due to the realistic addition in length (or width) when creating this schematic by hand. We know that an open-circuit stub cannot be directly connected to a transmission line with the use of a tee junction. Therefore, when adding the tee junction, we notice that:

- From S parameter graph: we see poor power amplification and poor matching networks
- From mu graph: we notice the stability factor has decreased significantly
- From max gain and S(2,1) graph: again, poor matching, so lower power efficiency at the designed frequency

In our final simulation (post-optimized tee junction), we set concurrent goals to have the absolute value of S(1,1) and S(2,2) below a certain threshold (0 dB) and optimize until desired results are achieved (results like first simulation). As seen in the schematic, values and W and L (referring to lengths of all transmission lines and stubs) have changed to optimize around 10GHz.

Trade-offs in Matching, Bandwidth, and Insertion Loss.

Matching vs Bandwidth: A good impedance matching will maximize power transfer (return loss) at a certain frequency – in Part 1 for lumped element circuits we see this at 6GHz. However, getting good matching across a wide bandwidth is a challenge why? Resonant structures usually have narrowed behavior. Wider bandwidth equals decreased quality of match.

Matching vs Insertion Loss: A better matching usually requires more complex networks, which means additional components. But what does this mean for insertion loss? This can increase insertion loss due to the introduction of resistive losses (e.g transmission lines) into the circuit.

- To improve matching, use more stages in the matching network, but this could increase insertion loss.
- To improve bandwidth, you can use multi-resonator designs or stagger-tuning techniques, which distribute the resonance over a wider range.
- To reduce insertion loss, select high-quality components with low equivalent series resistance (ESR) and minimize the use of lossy transmission lines.

Chebyshev filters and tuning:

Chebyshev filters use lumped elements or distributed elements. On a PCB:

- Lumped-element Chebyshev filters may require adjustments because real-world inductors and capacitors have tolerances, parasitic inductance, and resistance, which can shift the filter's response.
- Distributed-element filters (e.g., capacitively coupled resonators) depend on microstrip or stripline structures, which are more precise but still subject to manufacturing tolerances and substrate variations.

Adjustment (Tuning): To make them realizable without tuning, you would need highly accurate PCB fabrication and components. Alternatively, adding tunable elements (e.g., varactors or adjustable inductors) allows post-fabrication tuning.

Port with the Lowest Bandwidth

In the amplifier design, we see that the BW is limited by $|S11| < -10dB$ or $|S22| < -10dB$.
The input port has the lowest bandwidth because:

- It interacts directly with the load impedance, which often introduces greater variations over frequency compared to the source impedance at the input port.
- Poor output matching, as seen in the second simulation (skewed results due to tee junction), leads to lower power efficiency and a narrower bandwidth.

Designing for maximum gain with unstable transistor

Challenges:

An unstable transistor could oscillate if the impedance seen at the input or output falls within its unstable region.

Designing for maximum gain requires pushing the source and load impedances close to the transistor's unstable regions, increasing the risk of oscillation.

Stabilization Techniques:

Use resistive loading to reduce the transistor's gain in the unstable regions (e.g., series resistors or RC networks).

Add a stability network, such as a series RC circuit or a parallel RC circuit, to shift the unstable regions out of the operating range.

Select matching network impedances that keep the transistor within the stable operating range (stability circles on Smith Chart help identify safe regions).

Also, looking at the second simulation, we can see that adding realistic elements (T-junction) skews the results due to increased L or W in the schematic, leading to poo power amplification, decreased stability and reduced power efficiency. This shows the importance of accurate modelling and post fabrication tuning.