ECE445 Project 2 - Spring 2025

Mux Design with Minimum Critical Path Delay

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Percentage Contributions:

Anthony Zhelnakov contributed to 50% of this project. He worked on analytically identifying which circuit would minimize delay, and designing the different subcircuits and their components. He also worked on the schematics and optimized transistor dimensions. Ahsen Qureshi contributed to 50% of this project. He worked on analytically identifying which circuit would minimize delay, and designing the different subcircuits and their components. He also did the layout portion of the project and helped with the schematics.

Part 1:

Below is a full description of the cells created for this design, with a transistor-level schematic of each cell and an overall schematic design of the circuit.

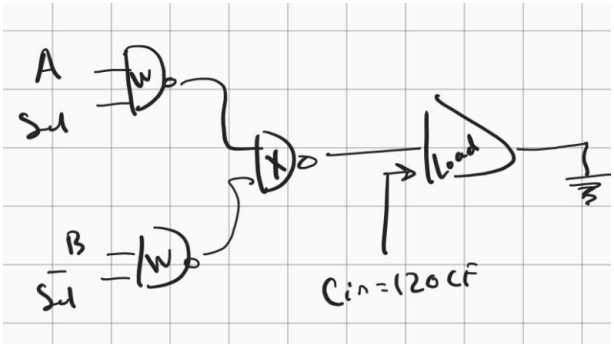


Figure 1a: Overall schematic design of Mux with load inverter before solving for N

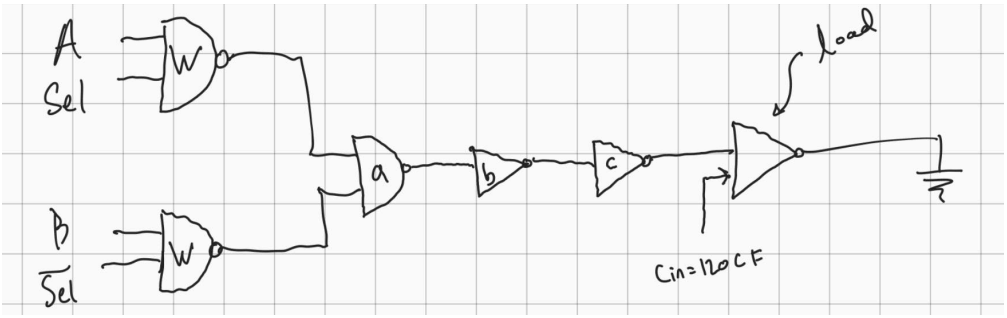


Figure 1b: Overall schematic design of Mux with load inverter after solving for N

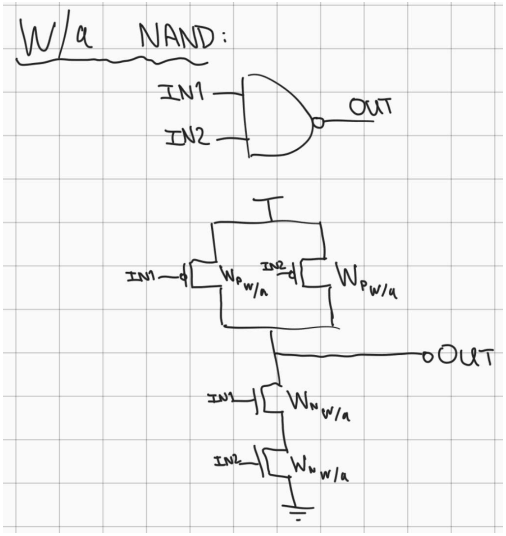


Figure 2: Transistor-level schematic of NAND2 cell

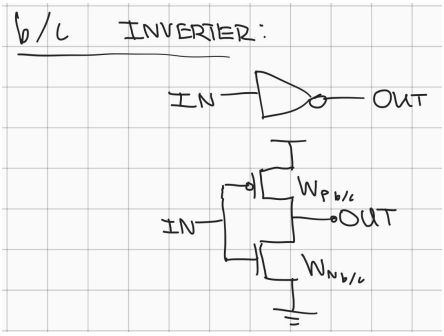


Figure 3: Transistor-level schematic of INV (B & C Inverter) cell

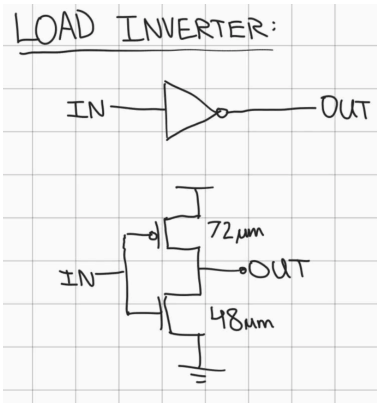


Figure 4: Transistor-level schematic of INV (load Inverter) cell

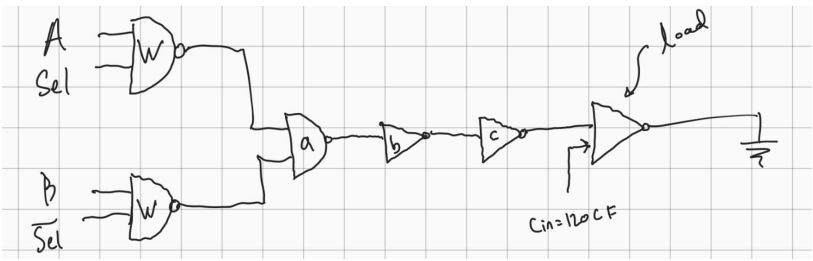
Below is a table listing the width of each transistor in the circuit:

Table 1: Transistor width of Mux circuit

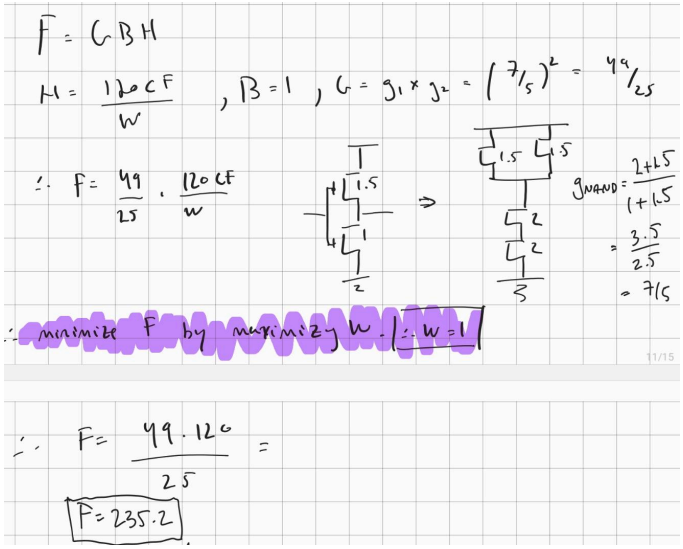
	W NAND2	**A NAND2**	**B INV**	**C INV**
W_n (μm)	0.57143	1.5984	3.1298	12.25964
W_p (μm)	0.42857	1.1988	4.6947	18.3854

Below is an explanation of the design and optimization process with hand calculations for the critical path delay normalized to the reference (minimum-width) inverter.

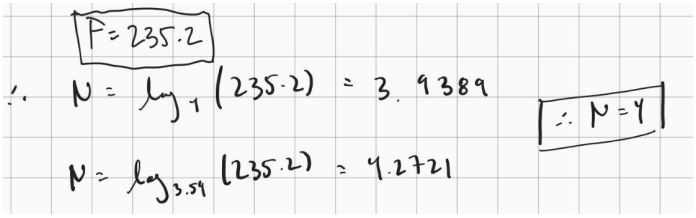
1. Drawing the circuit: the circuit below is constructed in two paths, one that depends on Sel, while the other depends on Sel'. We first simplified the function from a NAND2 → INV → NOR2 → INV → load to NAND2 → NAND2 → load, W\which also achieved the correct driving functionality of the Mux. Additionally, the load inverter is represented using a 120C capacitance. We represent it this way because the sum of the NMOS and PMOS widths is 120um, which creates an input capacitance of 120C.



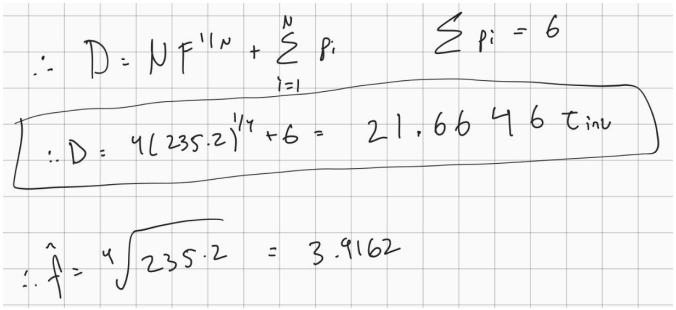
2. Next, we want to ensure each stage has the same stage effort (f_{opt}). We do this by solving for F = GBH and taking the n^{th} root of F.



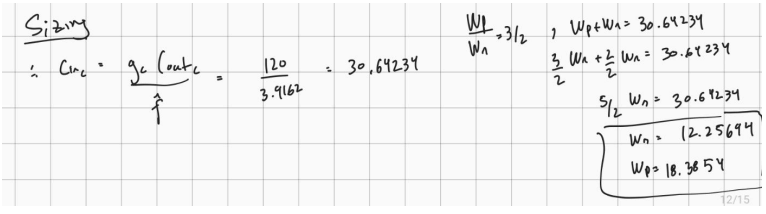
3. Now, solving for the optimal number of stages, N:

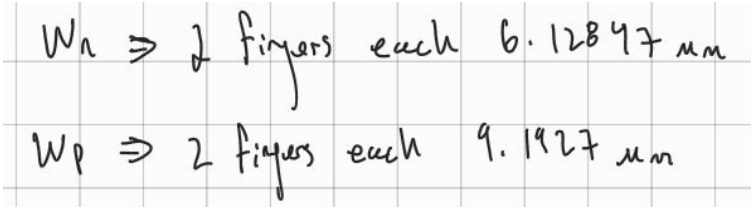


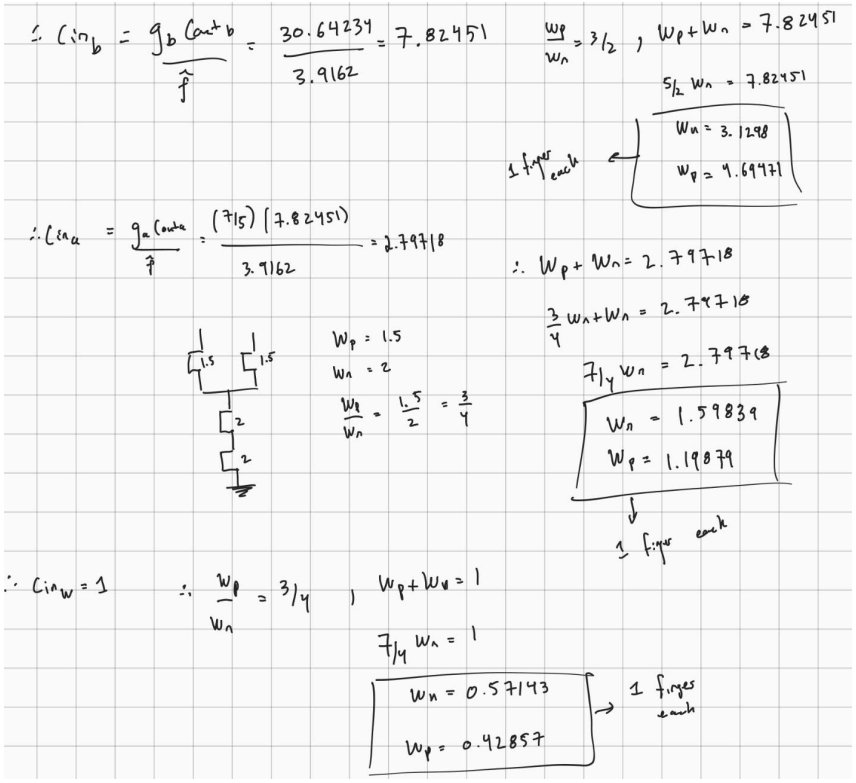
4. Now, solving for the optimal delay:



5. Solving for cell input capacitances and gate sizes:







6. To test the performance of our MUX, we will simulate pulse tests on the Sel and Sel* signals independently while keeping the A & B inputs fixed. The best design will then have close matching between propagation times due to either signal and minimized critical path propagation delay (the time it takes for the output to reach 50% of its stable output state after the input reaches 50%).

Part 2:

i)

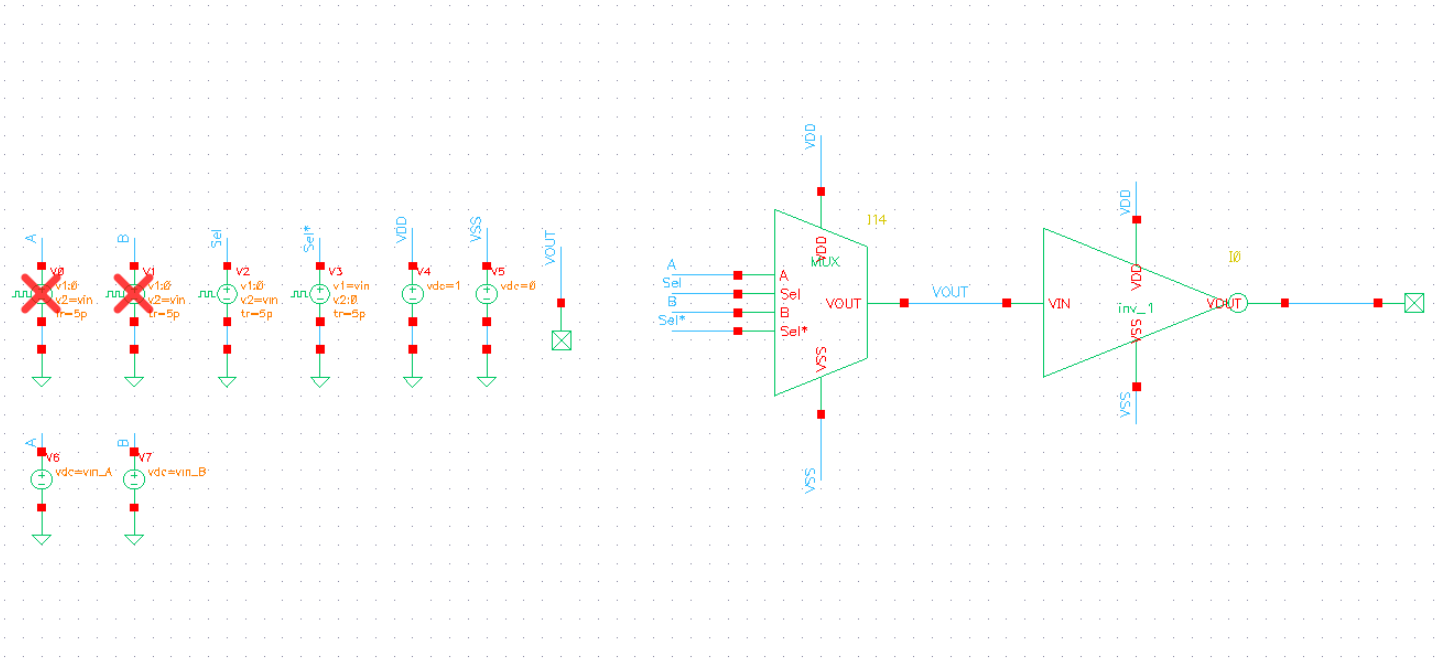


Figure 5: Testbench Schematic (Note: VOUT should be labelled as Y instead)

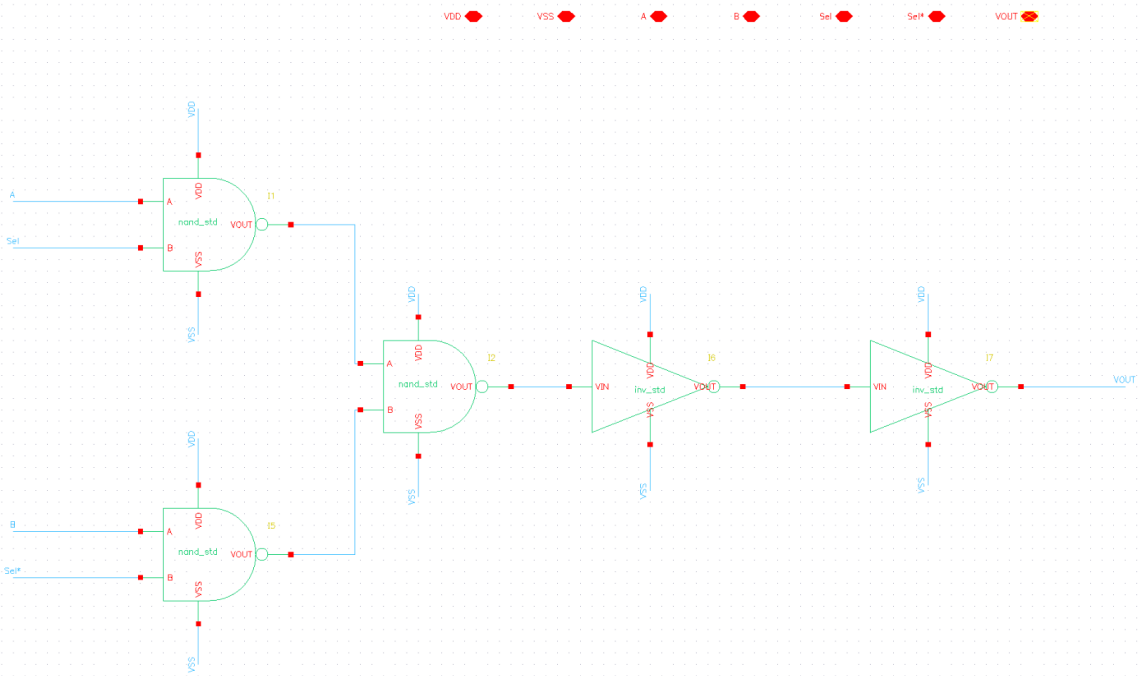


Figure 6: Mux Schematic

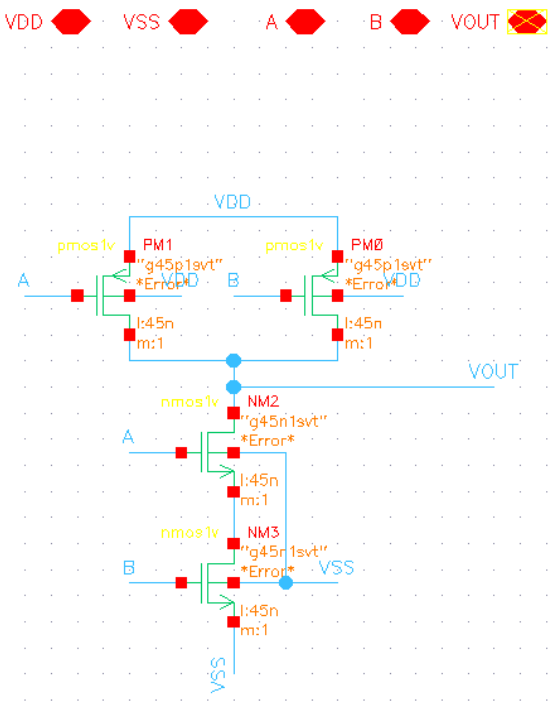


Figure 7: NAND Gate Transistor-Level Schematic

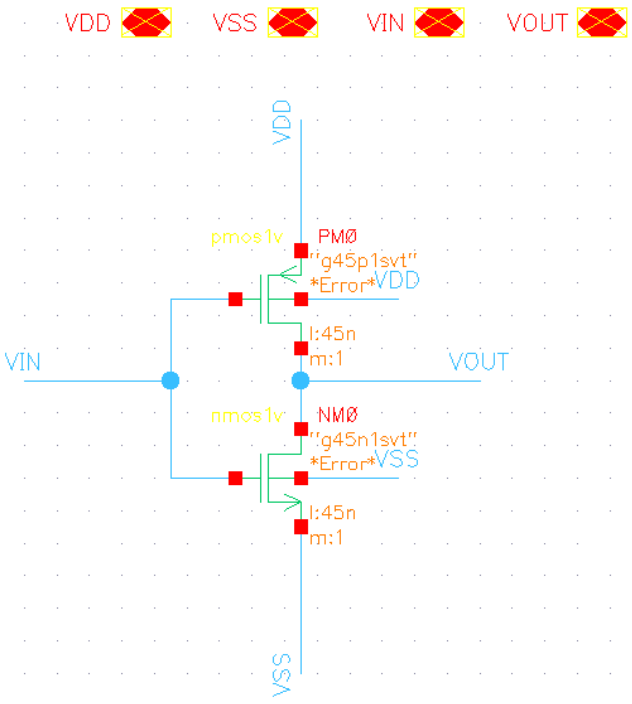


Figure 8: Inverter Transistor-Level Schematic

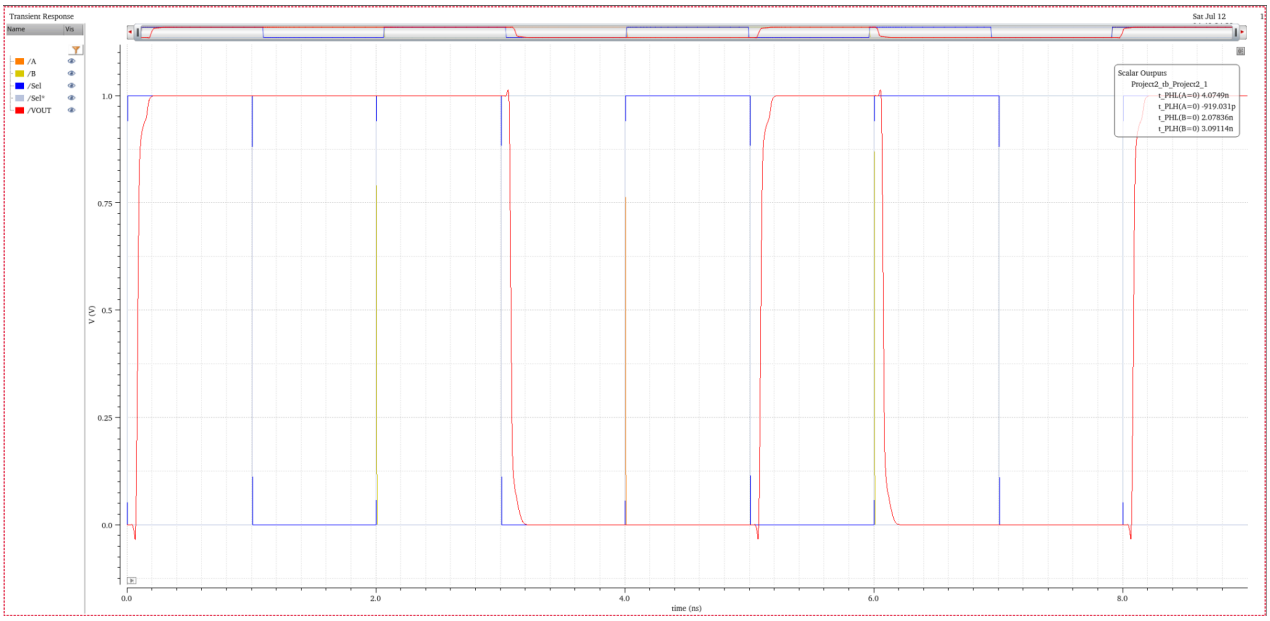


Figure 9: Waveforms of A, B, Sel, Sel* and Y from t = 0 to t = 9 ns (Note: VOUT should be labelled as Y instead)

ii)

Table 2: Old (calculated) and updated (tuned) transistor dimensions

Gate	**Transistor**	**Fingers**	**Calculated**	**Tuned**
			Finger Width (um)	Finger Width (um)
W	P	1	0.42857	0.42857
	N	1	0.57143	0.57143
A	P	1	1.19879	0.95
	N	1	1.59839	1.3
B	P	1	4.69471	2.85
	N	1	3.1298	3.1
C	P	2	18.3854	4.05
	N	2	12.25694	6.1

Tuning Explanation:

The input (W) NAND gate's dimensions were left unchanged as changing it through trial and error gave worse results. As for the remainder of the gates, the NMOS widths were slightly decreased to lower parasitic capacitance (C_d), and the PMOS widths were decreased because analytically, delay decreases with smaller $r = W_p/W_n$ ratio. See figure 10. Note that final obtained values were motivated by the aforementioned reasons but were ultimately determined by running many simulations and finding the best results (we were feeling lucky). Also note that strangely, keeping gate C's PMOS finger count as 2 instead of 1 gave less delay.

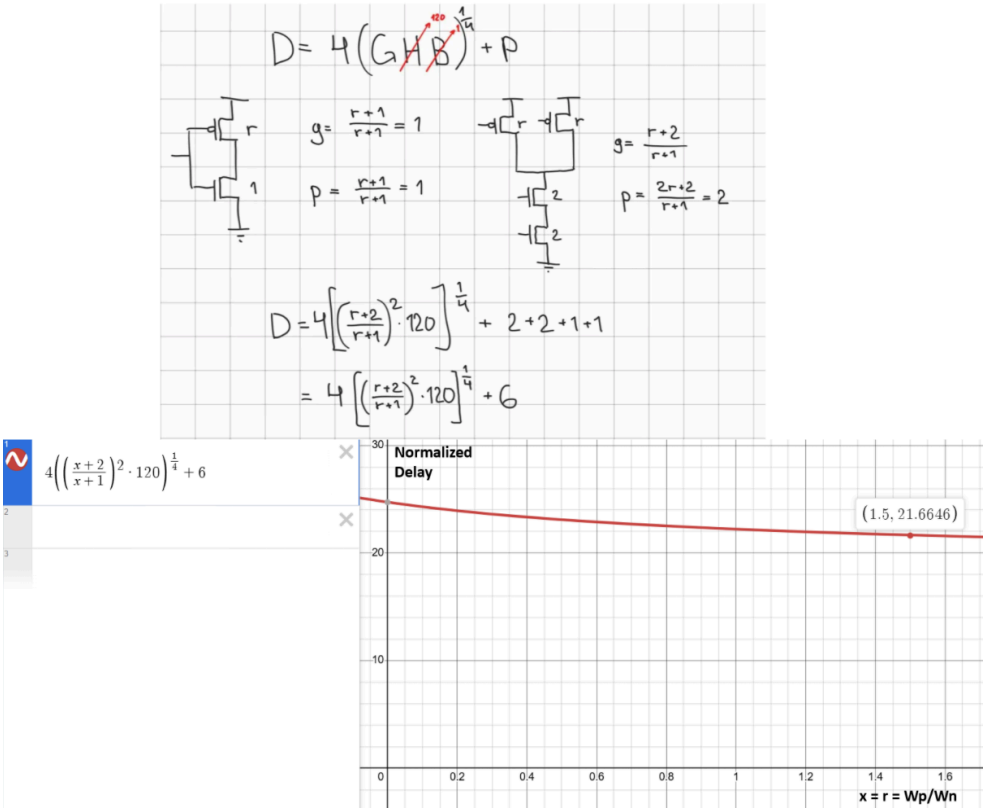


Figure 10: Analytical relationship between delay and W_p/W_n ratio

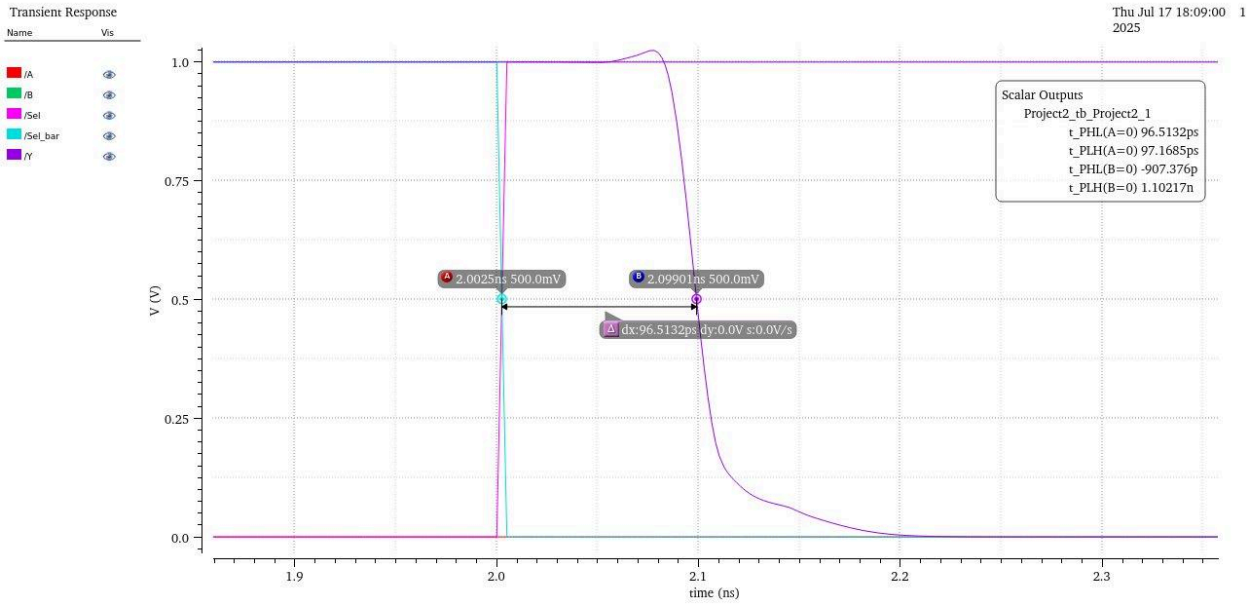


Figure 11: Waveform screenshot showing t_{pHL_01}

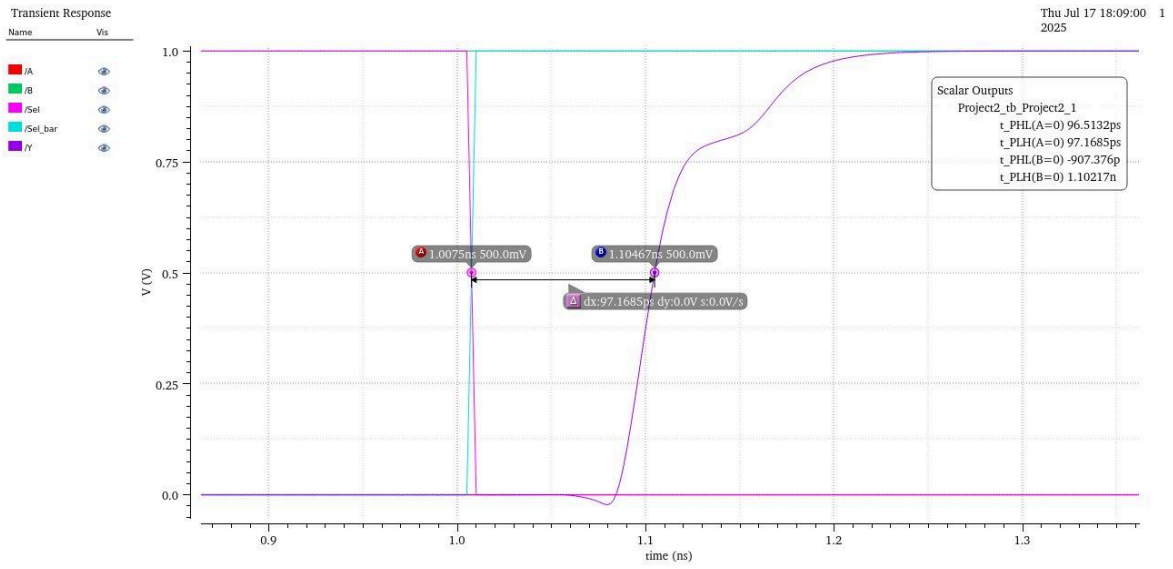


Figure 12: Waveform screenshot showing t_{pLH_01}

Originally, with the calculated values, the simulated delays were:

a) For A = 0 B = V_{DD}:
   t_{pHL_01} = 104 ps
   t_{pLH_01} = 106 ps
b) For A = V_{DD} B = 0:
   t_{pHL_10} = 97.57 ps
   t_{pLH_10} = 102.9 ps

Using Cadence's calculator to quickly obtain delay times between the appropriate rising/falling edges, we fine tuned the circuit. The final results are listed below:

a) For A = 0 B = V_{DD}:
   t_{pHL_01} = 96.5132 ps
   t_{pLH_01} = 97.1685 ps
b) For A = V_{DD} B = 0:
   t_{pHL_10} = 91.15 ps
   t_{pLH_10} = 93.51 ps
c) Thus, the critical delay of the circuit is **t_c = 97.1685 ps**