(TLB為 page table 的快取). (main memory 為 disk 之快取)

- TLB可視為分頁表的快取，所以必須包含分頁表的記憶體管理相關資訊。每一次的TLB存取都以虛擬頁碼為索引。如果命中便可轉成實體位址，然後將reference bit設為1。如果是寫入的話，dirty bit也會被設為1。
- 若TLB發生失誤，我們必須先確認是分頁錯誤或僅僅是TLB失誤。如果此分頁存在記憶體中，那麼TLB失誤只是轉換資訊失誤。處理器可以藉由分頁表讀入轉換資訊到TLB，然後再重新存取TLB。如果分頁不在記憶體中，那麼TLB失誤代表真正的分頁錯誤。此時由作業系統來處理分頁錯誤。
- TLB失誤可以靠硬體或軟體來處理。實際上這兩種方法之間的效能差異只有一點點，因為其基本的動作是一樣的。
- 多數系統使用較小且完全關聯式的TLB，因為完全關聯式的對映方式有較小的失誤率，此外因TLB較小所以完全關聯式對映方式的成本不會太高。

TLB是 fully associative，因fully associative有較小的 miss rate

- 在完全關聯式對映方式中實作LRU法則是非常的昂貴。因為TLB失誤比分頁錯誤容易發生，所以必須以成本較低的方法處理，因此一般系統僅提供隨機置換策略。

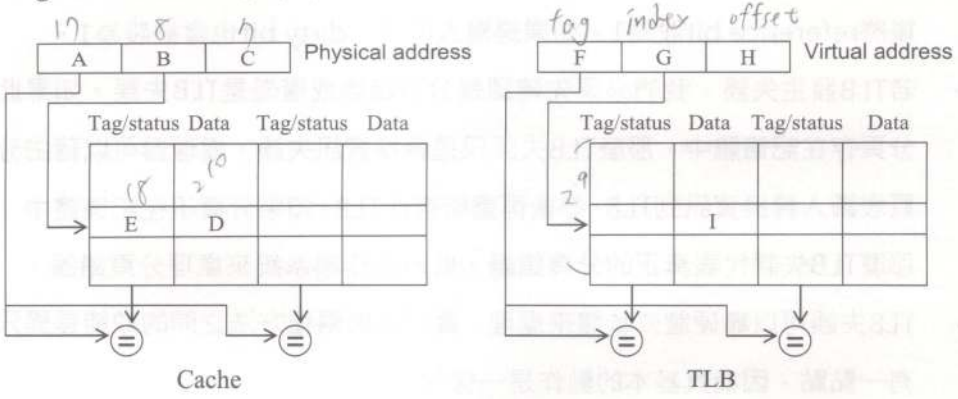
- instruction TLB is in IF stage.
- data TLB is in EX stage.

練習

Consider a memory system with the following parameters:

- Translation Lookaside Buffer (TLB) has 512 entries and is 2-way set associative.
- 64Kbyte L1 Data Cache has 128 byte lines and is also 2-way set associative.
- Virtual addresses are 64-bits and physical addresses are 32 bits.
- 8KB page size.

Below are diagrams of the cache and TLB. What is the number of bits in the diagrams labeled A, B, C,...



Answer

A	B	C	D	E	F	G	H	I
17	8	7	1024	18	42	9	13	19

練習

The following table is a stream of virtual addresses. Assume 4 KB pages, a four-entry fully associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number.

4095, 31272, 15789, 15000, 7193, 4096, 8912

TLB

Valid	Tag	Physical Page Number
1	11	12
1	7	4
1	3	6
0	4	9

Page table

Valid	Physical page or in disk
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

Given the address stream above, and the shown initial state of the TLB and page table, show the final state of the system. Also list for each reference if it is a hit in the TLB, a hit in the page table, or a page fault.

Answer: (H: Hit in TLB, M: Miss in TLB hit in page table, PF: Page Fault)

VA	4095	31272	15789	15000	7193	4096	8912
VPN	0	7	3	3	1	1	2
H/M/PF	M	H	H	H	PF	H	PF

TLB

Valid	Tag	Physical Page Number
1	1	13
1	7	4
1	3	6
1	2	14

Page table

Valid	Physical page or in disk
1	5
1	13
1	14
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

整合虛擬記憶體、TLB、與快取

➢ 下圖說明了CPU、虛擬記憶體、TLB、與快取之存取關係。