DM163

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8x3-CHANNEL CONSTANT CURRENT LED DRIVER

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DM163

8x3-CHANNEL CONSTANT CURRENT LED DRIVERS

General Description

The DM163 is a LED driver that comprises shift registers, data latches, 8x3-channel constant current circuitry with current value set by 3 external resistors, and 64 x 256 gray level PWM (Pulse Width Modulation) function unit. Each channel provides a maximum current of 60 mA. The grayscale data are separated into BANK0 and BANK1 respectively, selected by SELBK pin. BANK0 is 6-bits grayscale data and the BNAK1 is 8-bits grayscale data. Depending on the system requirement, both PWM banks could be utilized jointly to achieve maximum 8+6 bit grayscale performance. Alternatively, users can choose either 64-graylevel bank or 256-graylevel bank for dot correction, and the remaining bank as image data.

DM163 could also be constructed as a PWM controller for LED drivers. When VDDH is connected to VDD, each of the 24 output channels outputs can act as an inverse digital signal for controlling the LED driver.

Features

- 24 Output Channels
- 8 + 6-bits PWM grayscale Control
- Constant Current Output: 5mA to 60mA
- LED Power Supply Voltage up to 17V
- VDD=3V to 5.5V
- Varied Output Current Level Set By 3 External Resistors
- Serial Shift-In Architecture for Grayscale Data

Block Diagram

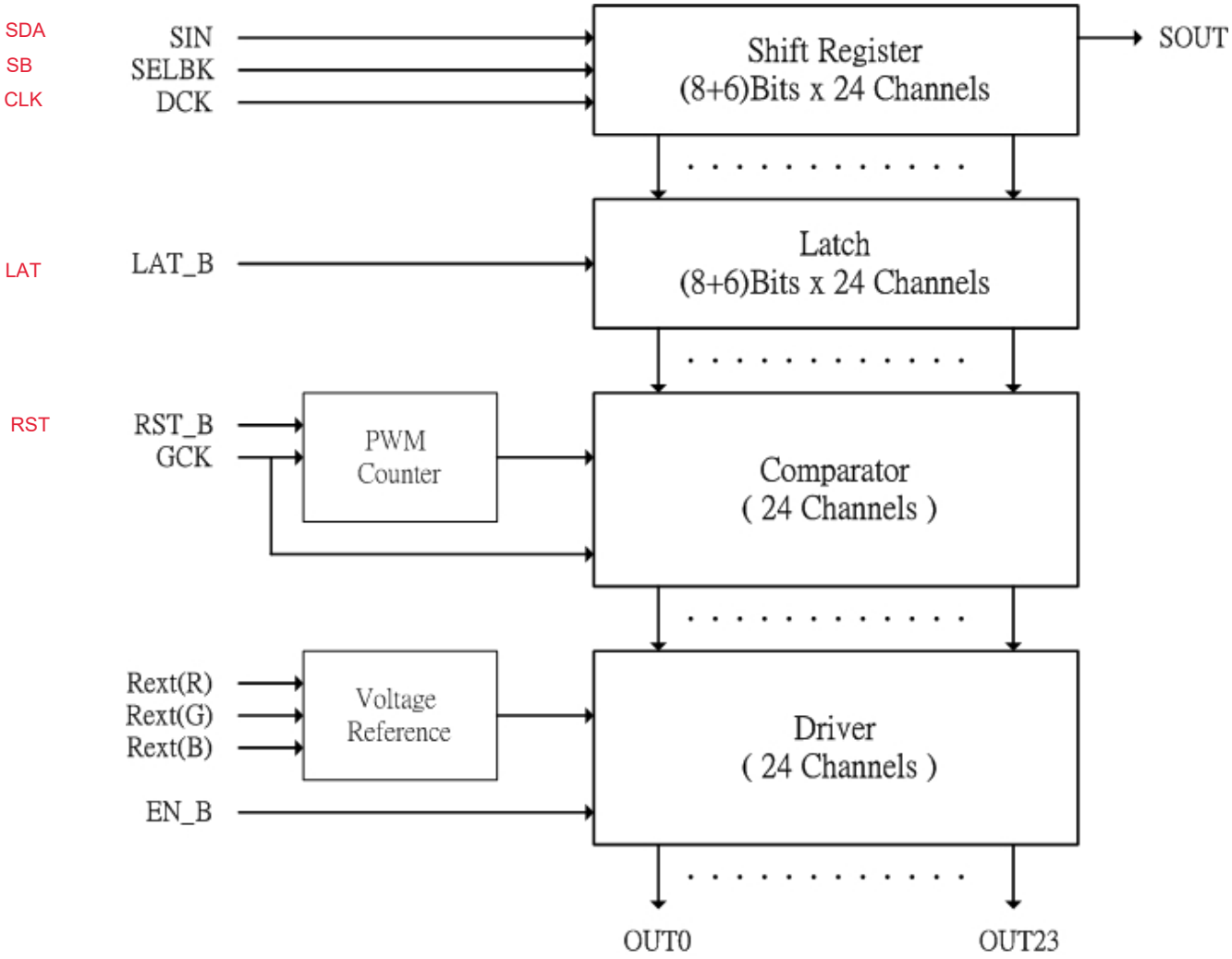

Figure 1. Functional Schematic of Whole Chip

The schematic of DM163 comprises of several fundamental units as shown in Figure 1. The grayscale data are input onto the DM163 by the **SIN** pin and transferred according to the synchronous clock **DCK**. Meanwhile, in order to separate the data into two groups, **SELBK** is designed as a switch control pin. When a sequence of data is already transferred onto the chip, the **LAT_B**="H" is set to convey it into the comparator unit. Compared with the counter signals, the grayscale data will determine the PWM control signal to display varied luminance at driver output. The **Rext** resistors are able to set diverse output current levels. The detailed schematic of each channel is shown as Figure 2.

Block Diagram

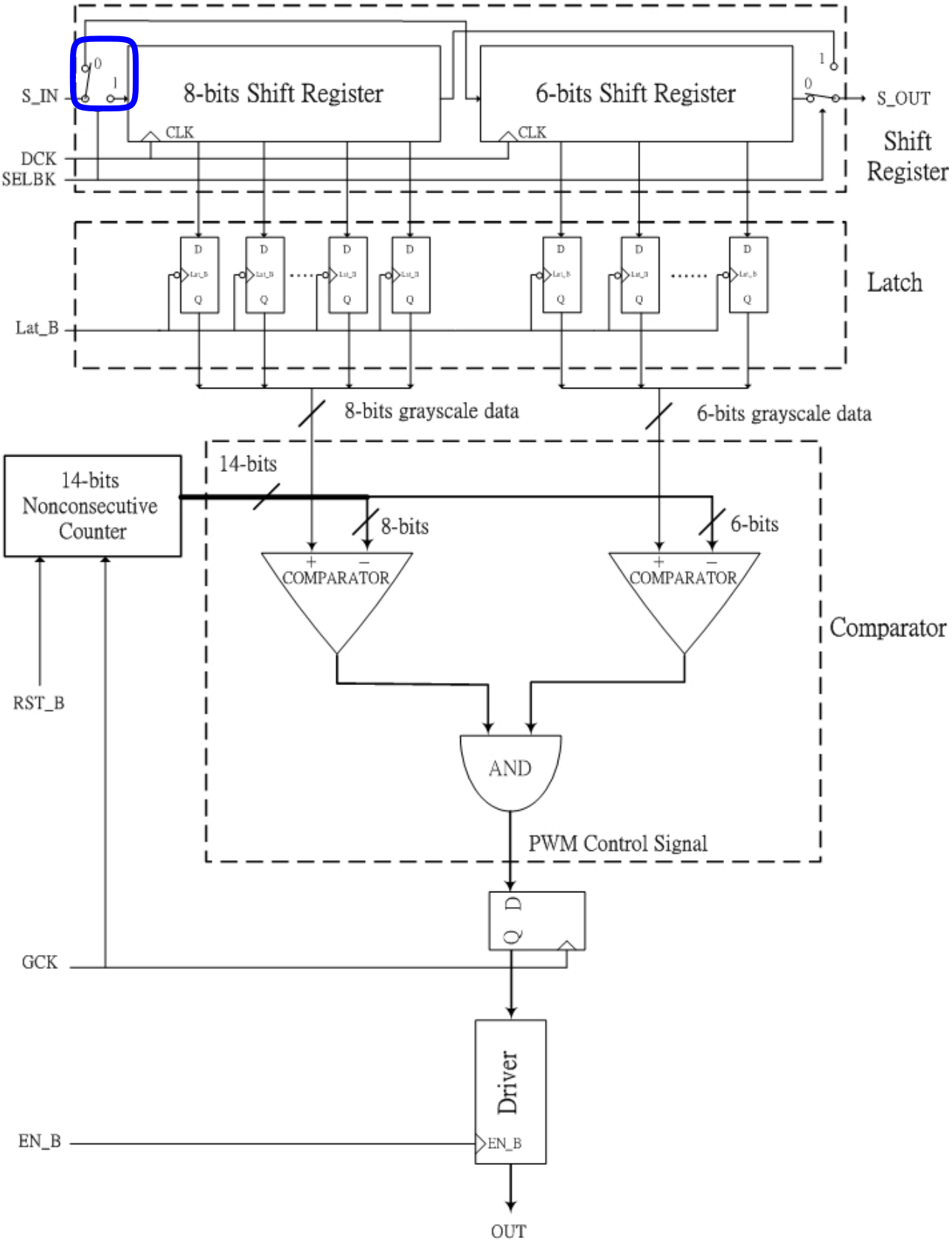

Figure 2. The Detailed Schematic of Each Channel

Pin Connection (Top view)

QFP44

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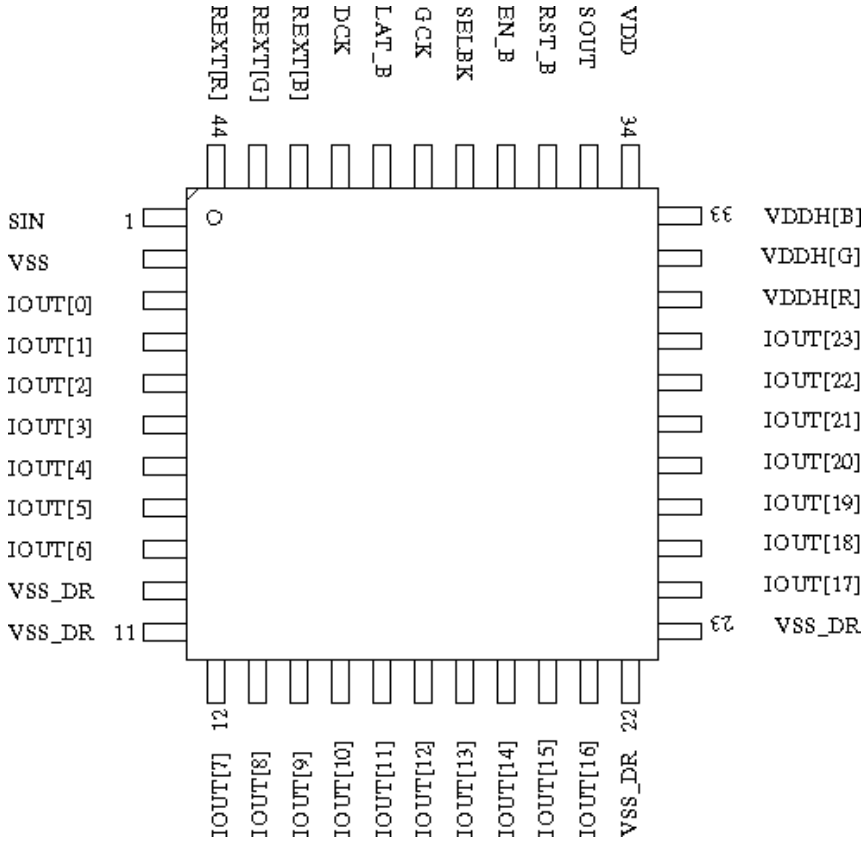

Pin No.	NAME	Pin No.	NAME	Pin No.	NAME	Pin No.	NAME
1	SIN	12	IOUT[7]	23	VSS_DR	34	VDD
2	VSS	13	IOUT[8]	24	IOUT[17]	35	SOUT
3	IOUT[0]	14	IOUT[9]	25	IOUT[18]	36	RST_B
4	IOUT[1]	15	IOUT[10]	26	IOUT[19]	37	EN_B
5	IOUT[2]	16	IOUT[11]	27	IOUT[20]	38	SELBK
6	IOUT[3]	17	IOUT[12]	28	IOUT[21]	39	GCK
7	IOUT[4]	18	IOUT[13]	29	IOUT[22]	40	LAT_B
8	IOUT[5]	19	IOUT[14]	30	IOUT[23]	41	DCK
9	IOUT[6]	20	IOUT[15]	31	VDDH[R]	42	REXT[B]
10	VSS_DR	21	IOUT[16]	32	VDDH[G]	43	REXT[G]
11	VSS_DR	22	VSS_DR	33	VDDH[B]	44	REXT[R]

QFN40

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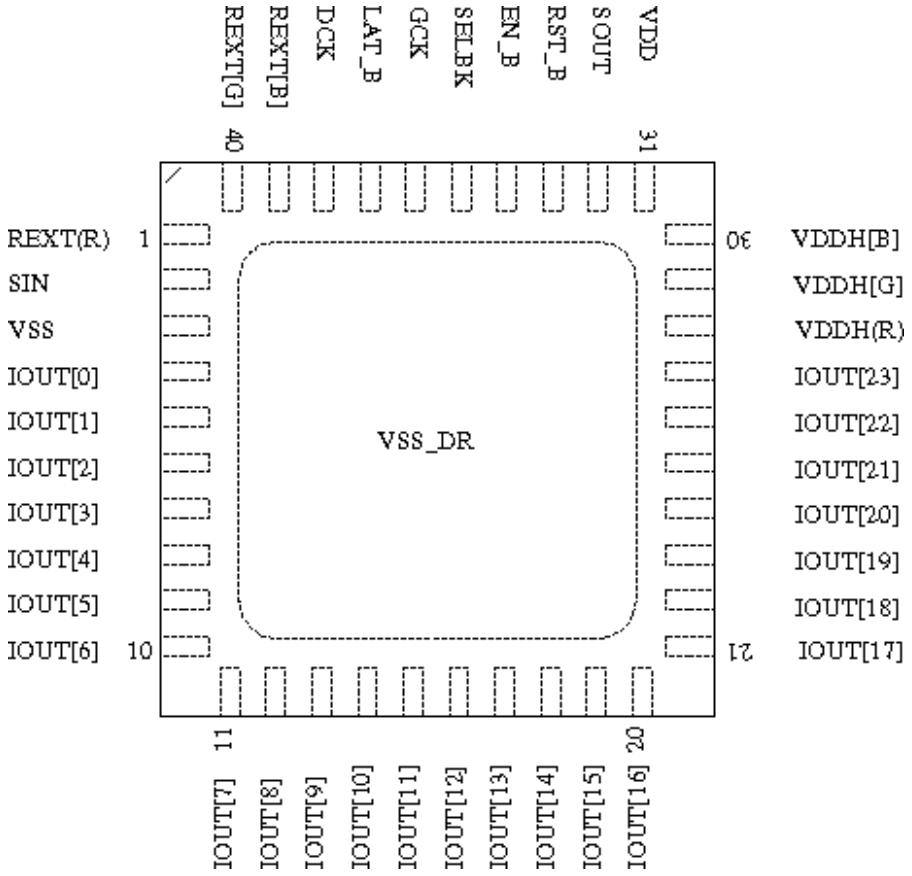


Pin No.	NAME	Pin No.	NAME	Pin No.	NAME	Pin No.	NAME
1	REXT[R]	11	IOUT[7]	21	IOUT[17]	31	VDD
2	SIN	12	IOUT[8]	22	IOUT[18]	32	SOUT
3	VSS	13	IOUT[9]	23	IOUT[19]	33	RST_B
4	IOUT[0]	14	IOUT[10]	24	IOUT[20]	34	EN_B
5	IOUT[1]	15	IOUT[11]	25	IOUT[21]	35	SELBK
6	IOUT[2]	16	IOUT[12]	26	IOUT[22]	36	GCK
7	IOUT[3]	17	IOUT[13]	27	IOUT[23]	37	LAT_B
8	IOUT[4]	18	IOUT[14]	28	VDDH[R]	38	DCK
9	IOUT[5]	19	IOUT[15]	29	VDDH[G]	39	REXT[B]
10	IOUT[6]	20	IOUT[16]	30	VDDH[B]	40	REXT[G]

Pin Description

PIN NAME	FUNCTION	QFP pin number	QFN pin number
VDDH (R) VDDH (G) VDDH (B)	Output protection pins. They could be connected independently or to LED supplies (VLED).	31 32 33	28 29 30
VDD	Power supply terminal.	34	31
VSS	Ground terminal.	2	3
VSS_DR	Driver ground	10, 11, 22, 23	Thermal pad
SDA SIN	Serial input for grayscale data.	1	2
SOUT	Serial output for grayscale data.	35	32
CLK DCK	Synchronous clock input for serial data transfer. The input data of SIN is transferred at rising edges of DCK.	41	38
SB SELBK	If SELBK is H, shift-in date would be stored in the 8-bit BANK 1. If SELBK is L, shift-in date would be stored in the 6-bit BANK 0.	38	35
LAT LAT_B	When LAT_B converts from H to L, grayscale data in both shift register banks are latched.	40 Does not clear banks!!	37
GCK	Clock input for PWM operation.	39	36
REXT(R) REXT(G) REXT(B)	External resistor connected between REXT and GND for driver current setting. REXT(R) controls outputs OUT0, 3, 6, 9, 12, 15, 18, 21. REXT(G) controls outputs OUT1, 4, 7, 10, 13, 16, 19, 22. REXT(B) controls outputs OUT2, 5, 8, 11, 14, 17, 20, 23.	44 43 42	1 40 39
IOUT0~23	LED driver outputs.	3, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15,16, 17, 18, 19, 20,21, 24, 25, 26, 27,28, 29, 30	4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27
EN_B	Input terminal of output enable. All outputs are OFF when EN_B is H.	37	34
RST_B	The IC is initialized when RST_B low. There is an internal pull-up on this pin. This pin couldn't be floating. Before using the IC, it must be reset first. If each channel is assigned to drive multiple LEDs, IC should be reset before each LED data latch to prevent from flashing.	36 Just set RST to one and keep it there	33

Maximum Ratings (Ta=25°C, Tj(max) = 140°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ~ 7.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V
Output Current	I_{OUT}	60	mA
Output Voltage	V_{OUT}	-0.3 ~ 17	V
DCK Frequency	F_{DCK}	20	MHz
GCK Frequency	F_{GCK}	20	MHz
GND Terminal Current	I_{GND}	1440	mA
Power Dissipation	P_D	1.36 (QFP44); 3.63 (QFN40) (Ta=25°C)	W
Thermal Resistance	$R_{th(j-a)}$	84.42 (QFP44); 31.67 (QFN40)	℃/W
Operating Temperature	Top	-40 ~ 85	℃
Storage Temperature	Tstg	-55 ~ 150	℃

Recommended Operating Condition

DC Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	3		5.5	V
Output Voltage	V_{OUT}	—	—	—	17	V
Output Current	I_O	OUTn	5	—	60	mA
	I_{OH}	SERIAL-OUT	—	—	2	
	I_{OL}	SERIAL-OUT	—	—	-2	
Input Voltage	V_{IH}	—	0.8 V_{DD}	—	V_{DD}+0.2	V
	V_{IL}	—	-0.2	—	0.2 V_{DD}	

AC Characteristics (V_{DD} = 5.0 V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
DCK Frequency	F_{DCK}	Cascade operation	—	—	20	MHz
DCK pulse duration	t_{wh} / t_{wl}	High or low level	15	—	—	ns
DCK rise/fall time	t_r / t_f	—	—	—	20	ns
GCK Frequency	F_{GCK}	—	1	—	20	MHz
GCK pulse duration	t_{wh} / t_{wl}	High or low level	15	—	—	ns
GCK rise/fall time	t_r / t_f	—	—	—	20	ns
Set-up Time for SIN	tsetup(D)	Before DCK rising edge	2	—	—	ns
Hold Time for SIN	thold(D)	After DCK rising edge	3	—	—	ns
Set-up Time for DCK	tsetup(L)	Before LAT_B falling edge	3	—	—	ns
LAT_B Pulse Width	tw LAT	—	5	—	—	ns
Set-up Time for LAT_B	Tsetup(G)	Before GCK rising edge	13	—	—	ns
Set-up Time for SELBK	Tsetup(S)	Before DCK rising edge	5	—	—	ns
Hold Time for SELBK	Thold(S)	After DCK rising edge	1	—	—	ns

AC Characteristics (V_{DD} = 3.3 V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
DCK Frequency	F_{DCK}	Cascade operation	—	—	20	MHz
DCK pulse duration	t_{wh} / t_{wl}	High or low level	15	—	—	ns
DCK rise/fall time	t_r / t_f	—	—	—	20	ns
GCK Frequency	F_{GCK}	Cascade operation	1	—	20	MHz
GCK pulse duration	t_{wh} / t_{wl}	High or low level	15	—	—	ns
GCK rise/fall time	t_r / t_f	—	—	—	20	ns
RST_B pulse duration	twrst_b	Low level	100	—	—	ns
Set-up Time for SIN	tsetup(D)	Before DCK rising edge	2	—	—	ns
Hold Time for SIN	thold(D)	After DCK rising edge	5	—	—	ns
Set-up Time for DCK	tsetup(L)	Before LAT_B falling edge	5	—	—	ns
LAT_B Pulse Width	tw LAT	—	7	—	—	ns
Set-up Time for LAT_B	Tsetup(G)	Before GCK rising edge	23	—	—	ns
Set-up Time for SELBK	Tsetup(S)	Before DCK rising edge	9	—	—	ns
Hold Time for SELBK	Thold(S)	After DCK rising edge	1	—	—	ns

Electrical Characteristics (V_{DD} = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage “H” Level	V_{IH}	—	0.8 V_{DD}	—	V_{DD}	V
Input Voltage “L” Level	V_{IL}	—	GND	—	0.2 V_{DD}	
Output Leakage Current	I_{leak}	V_{OH} = 17 V	—	—	± 0.1	uA
Output Voltage (SOUT)	V_{OL}	I_{OL} = 2 mA	—	—	0.2	V
	V_{OH}	I_{OH} = -2 mA	4.8	—	—	
Output Current (Channel-Channel)	I_{OL1}	V_{OUT} = 1.0V R_{EXT} = 2.6kΩ	—	± 3	± 5	%
Output Current (Chip-Chip)	I_{OL3}	V_{OUT} = 1.0V R_{EXT} = 2.6kΩ	—	± 4	± 10	%
Supply Voltage Regulation	% / V_{DD}	R_{EXT} = 3kΩ	—	—	2	% / V
Supply Current[1]	$I_{DD, analog}$	VDD=5V, R_{EXT} = 1kΩ	—	42.2	43.4	mA
	$I_{DD, digital}$	VDD=5V, Cload=2pF, DCK=GCK=1MHz	—	1	1.5	

[1] I_{LED} excluded.

Switching Characteristics (V_{DD} = 3.3V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SOUT Rise time	t_{or}	VIH=VDD VIL=GND REXT=3KΩ CL=13pF	—	4	5	ns
SOUT Fall time	t_{of}		—	4	5	ns
SOUT Propagation delay (L to H)	t_{pLH}		—	24	30	ns
SOUT Propagation delay (H to L)	t_{pHL}		—	20	25	ns
IOUT Rise time	t_{or}	VIH=VDD VIL=GND REXT=3KΩ VLED=3.3V RL=120Ω CL=33pF	—	15	18	ns
IOUT Fall time	t_{of}		—	20	25	ns
IOUT Propagation delay After GCK or EN_B (L to H / OFF to ON)	t_{pLH}		—	35	37	ns
IOUT Propagation delay After GCK or EN_B (H to L / ON to OFF)	t_{pHL}		—	30	35	ns

Switching Characteristics (V_{DD} = 5.0V, Ta = 25°C)

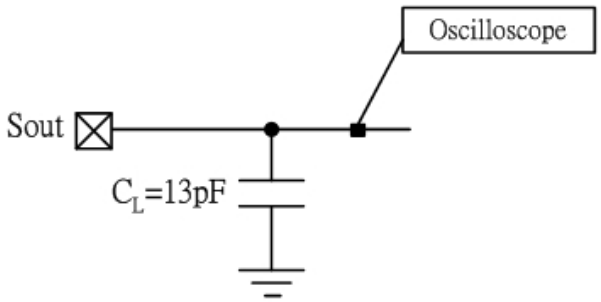
CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SOUT Rise time	t_{or}	VIH=VDD VIL=GND REXT=3KΩ CL=13pF	—	4	5	ns
SOUT Fall time	t_{of}		—	4	6	ns
SOUT Propagation delay (L to H)	t_{pLH}		—	19	25	ns
SOUT Propagation delay (H to L)	t_{pHL}		—	17	23	ns
IOUT Rise time	t_{or}	VIH=VDD VIL=GND REXT=3KΩ VLED=5.0V RL=120Ω CL=33pF	—	4	6	ns
IOUT Fall time	t_{of}		—	15	18	ns
IOUT Propagation delay After GCK or EN_B (L to H / OFF to ON)	t_{pLH}		—	26	30	ns
IOUT Propagation delay After GCK or EN_B (H to L / ON to OFF)	t_{pHL}		—	20	25	ns

Input Capacitance (Ta = 25°C)

INPUT NODE	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SIN	C_{SIN}	—	—	3	—	pF
DCK	C_{DCK}	—	—	3	—	pF
GCK	C_{GCK}	—	—	3	—	pF
LAT_B	C_{LAT_B}	—	—	3	—	pF
EN_B	C_{EN_B}	—	—	3	—	pF
RST_B	C_{RST_B}	—	—	3	—	pF
SELBK	C_{SELBK}	—	—	3	—	pF

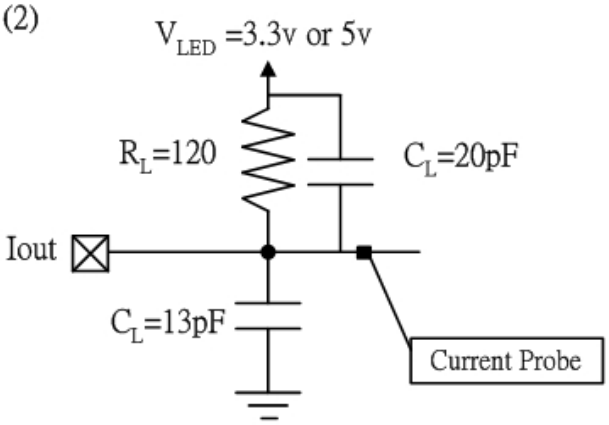
Parameter Measurement

(1)



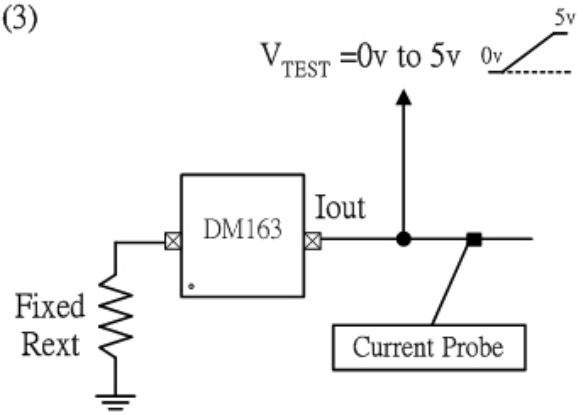
1. t_{or} & t_{of} of Sout
2. Sout propagation delay t_{PLH} and t_{PHL}

(2)



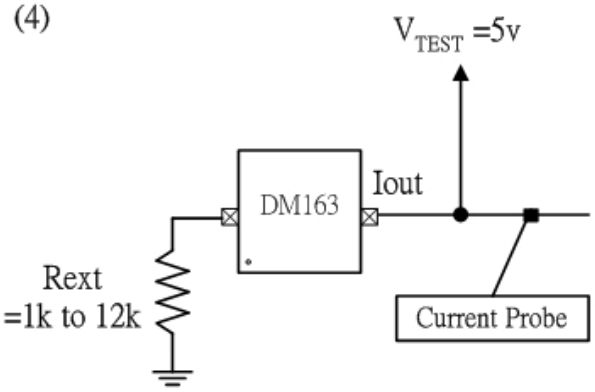
1. t_{or} & t_{of} of Iout
2. Iout propagation delay t_{PLH} and t_{PHL}

(3)



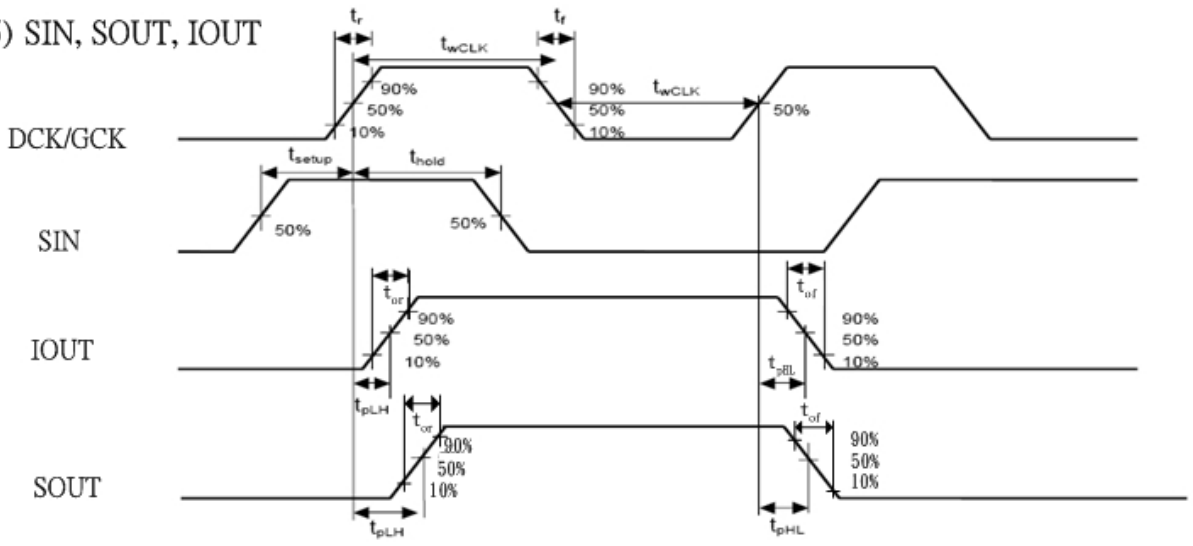
Vout V.S. Iout

(4)



Rext V.S. Iout

(5) SIN, SOUT, IOUT



Serial Shift-In Luminance Data (Shift Register Architecture)

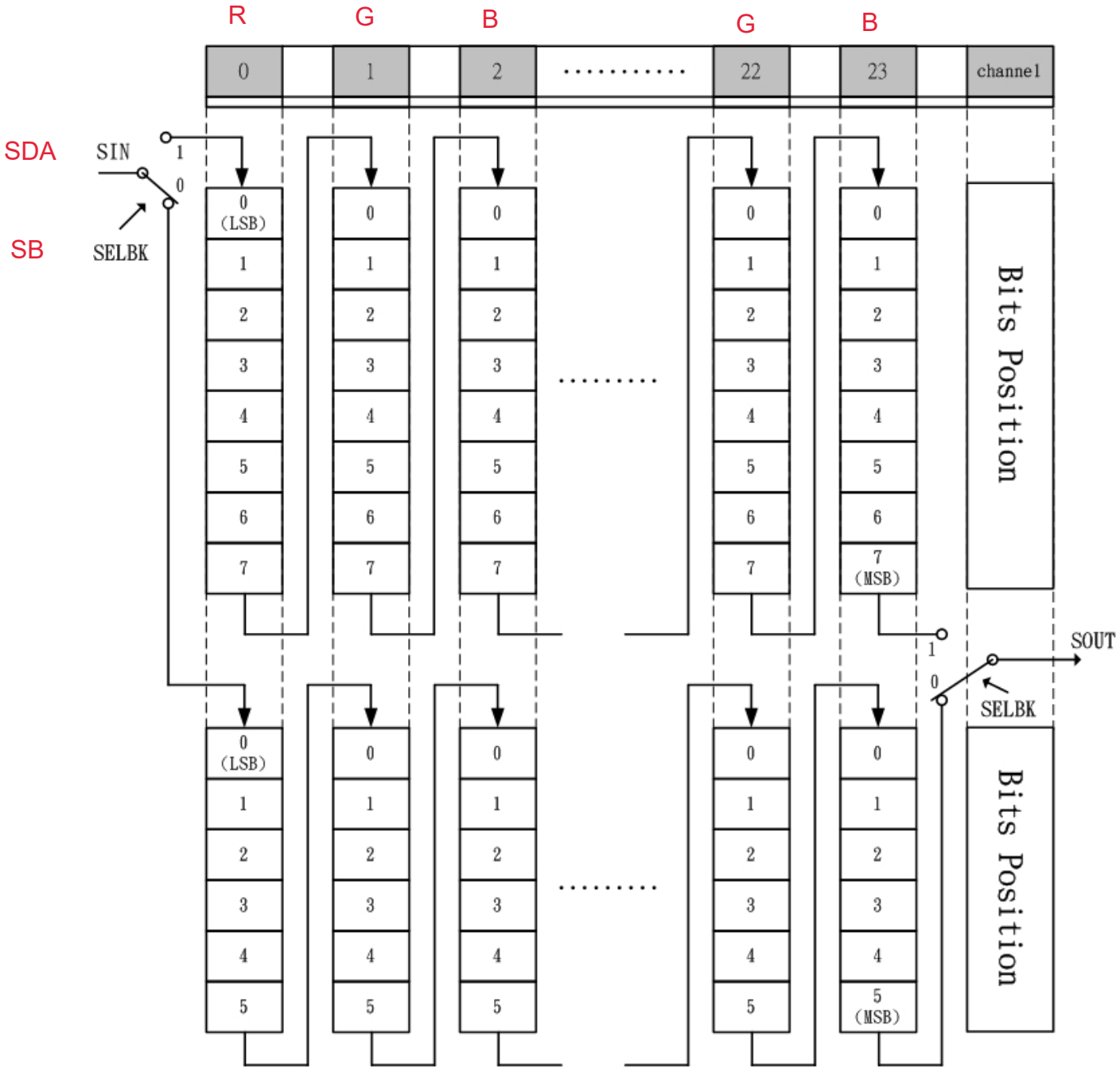


Figure 3. Serial Shift-In Luminance Data Structure

This serial shift (shift register) architecture follows a FIFO (first-in first-out) formate. The MSB (Most Significant Bit), both 8th bit and 6th bit at the 23rd channel, is the first data bit that shift into the driver. And the LSB (Least Significant Bit) data, the 1st bit at the 1st channel, is the last bit in the data sequence. Furthermore, the SELBK control signal is set to determine in which bank the data are placed.

Timing Diagram

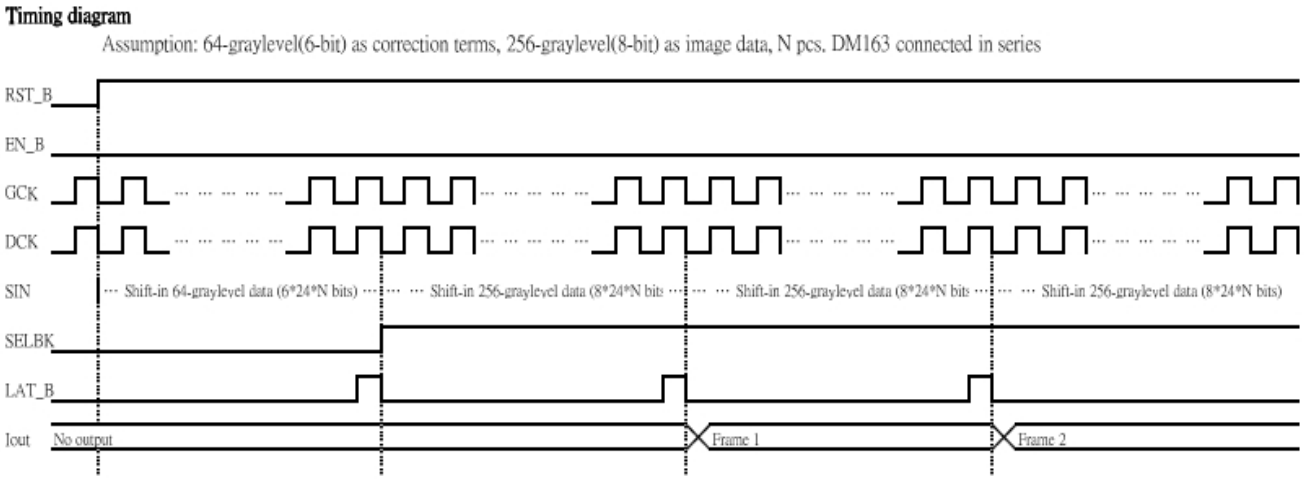


Figure 4. Timing diagram when 6bits are correction terms and 8bits are image terms

When 6 bits are correction terms and 8 bits are image terms (as shown in Fig 4), users must set the controller signals according to below sequences:

(1) Set SELBK=L (Bank 0) and begin shift in 6 bits correction data
(2) Set LAT_B=H to update the correction data after all correction data are in place
(3) Set SELBK=H (Bank 1) and begin shift in 8 bits image data
(4) Set LAT_B=H to update image data after 8 bit image are all in place. DM163 will utilize the 8 bits image data to determine the grayscale of each channel
(5) Repeat steps (3) and (4)

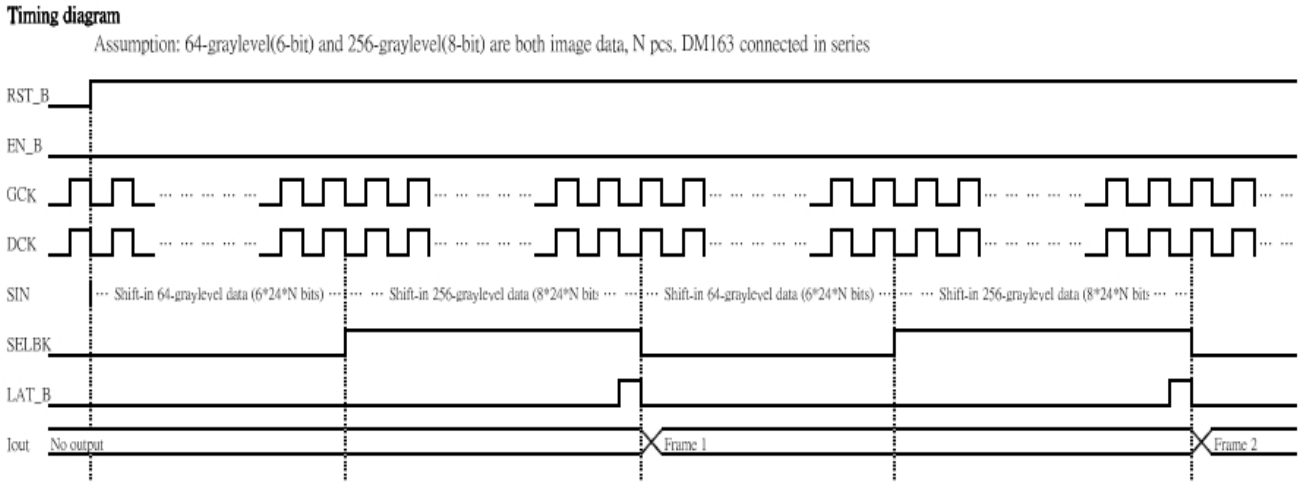


Figure 5. Timing diagram when both 6bits and 8bits are used as image terms

When both 6 bits and 8 bits bank are used for images terms (As shown in Fig. 5), users should set the controller signal in accordance to the following:

(1) Set SELBK=L (Bank 0) and begin shift in 6 bits correction data

(2) Set SELBK=H (Bank 1) and begin shift in 8 bits image data

(3) Set LAT_B=H to update image data after both 8 bit and 6 bit image data are all inplace.

(4) Repeat steps (1) to (3)

Timing Diagram

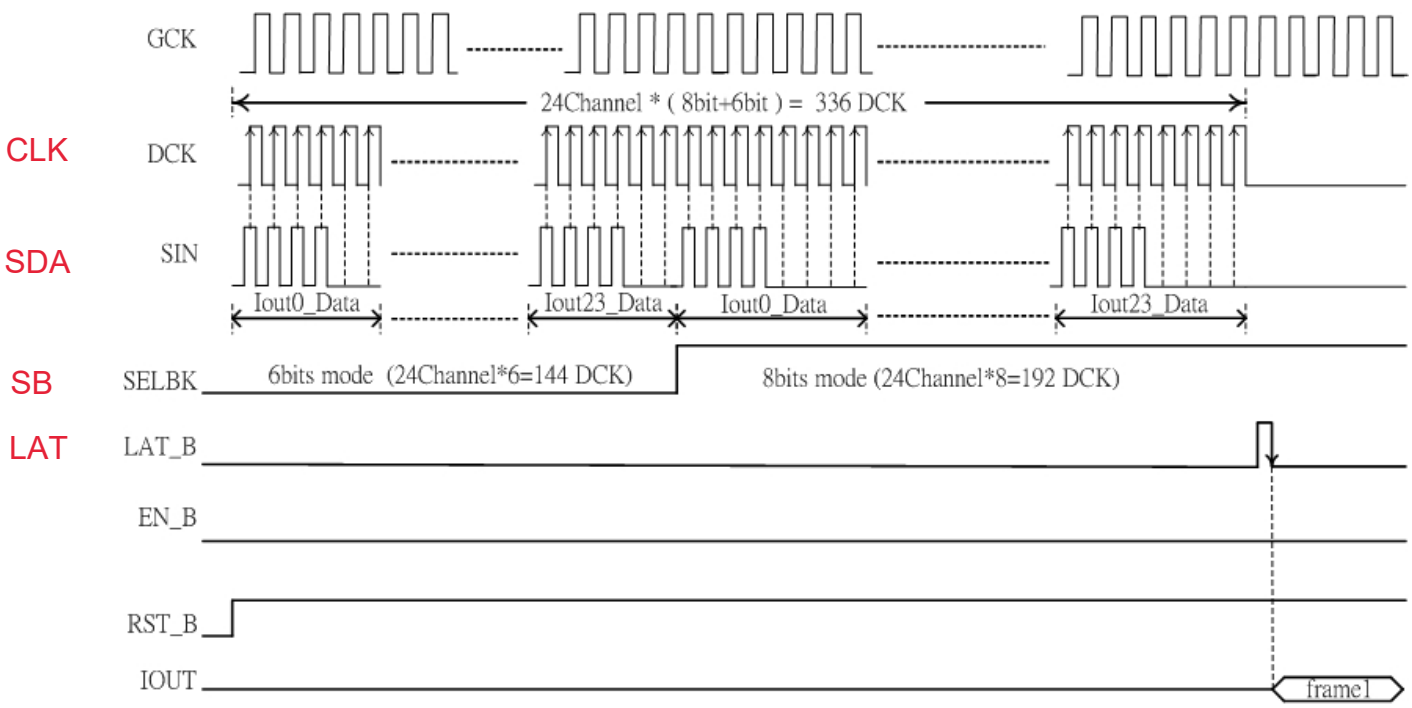


Figure 6. Detailed timing diagram of data transference

Figure 6 shows the detailed timing diagram of data transference. The synchronous clock DCK is designed to trigger at the positive edge. And the LAT_B triggers at the negative edge. To completely fill up both 6 bit and 8 bit shift register, a total of 336 DCK count is required (144 DCK for 6bits mode and 192 DCK for 8bits mode). Example depicted in figure 6 shows 6'b001111 data at 6bits bank and 8'b00001111 at 8bits bank respectively. Therefore, the average output current is (15/256) x (15/64) x Iout.

Formula I (out, avg)= (BANK 1/256) x (BANK 0/64) x Iout, provides a useful way to calculate the input data and the output current. Iout is the reference current value shown in figure 12. Users could utilize the formula Iout =47*Vrext / Rext to get an approximate value of Iout.

Particular Phenomenon

DM163 incorporates a different PWM counter, as described in Figure 2, hence its output waveform demonstrate a very different characteristics compare to conventional PWM counter.

(1) Nonconsecutive counter

The non-consecutive PWM counter incorporate by DM163 demonstrated a waveform pattern similar to Figure 7. Its waveform is spread-out into each PWM cycle, resulting lots of intermediate pulses during each PWM cycle. In Fig 7, if all the intermediate pulses are added up, it would equal to 50% luminance which is the same as the conventional method. By spreading out the PWM pulses, this approach can help prevent LED from flickering in lower grayscale situation.

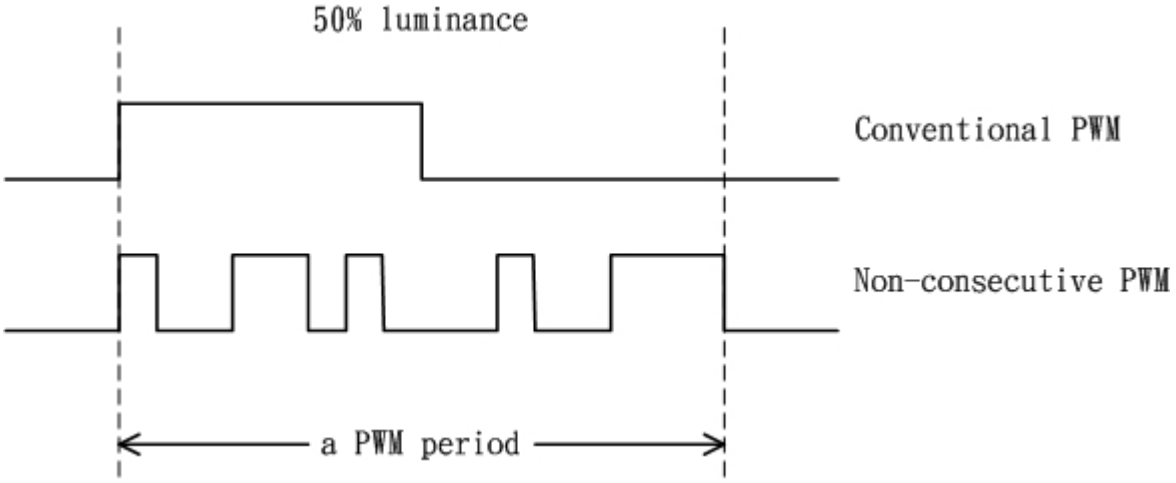


Figure 7. An Example of Nonconsecutive PWM Signal

(2) 8+6 bits Comparator

The comparator illustrated in Fig 2 is another one of the unique designs in DM163. The comparator's output will be "H" only when value at "+" is larger then the value at "-" (in other word, comparator will be "L" when value in"+" equals to value in "-" or value in "+" is less than value in "-"). Only when both 8 bit and 6 bit comparator are "H" will there be current in the output channel.

Due to this unique comparator design, DM163 exhibit a very distinct output characters in two certain scenario. In the first case, DM163 output will always be "OFF" when either one of the 8 bit or 6 bit bank is filled with 0. In 2nd scenario, when all bit value at both 8 bit and 6 bit bank are loaded "H", DM163 output will exhibit its highest luminance value (but not 100% luminance value). Due to the nature of comparators design, PWM control signal will be zero in the condition of 8bits counter=8'bFF or 6bits counter=6'b3F. Consequently, the PWM control signal will be 0 for 2^8+2^6+1 GCK rather than always high.

Application Diagram

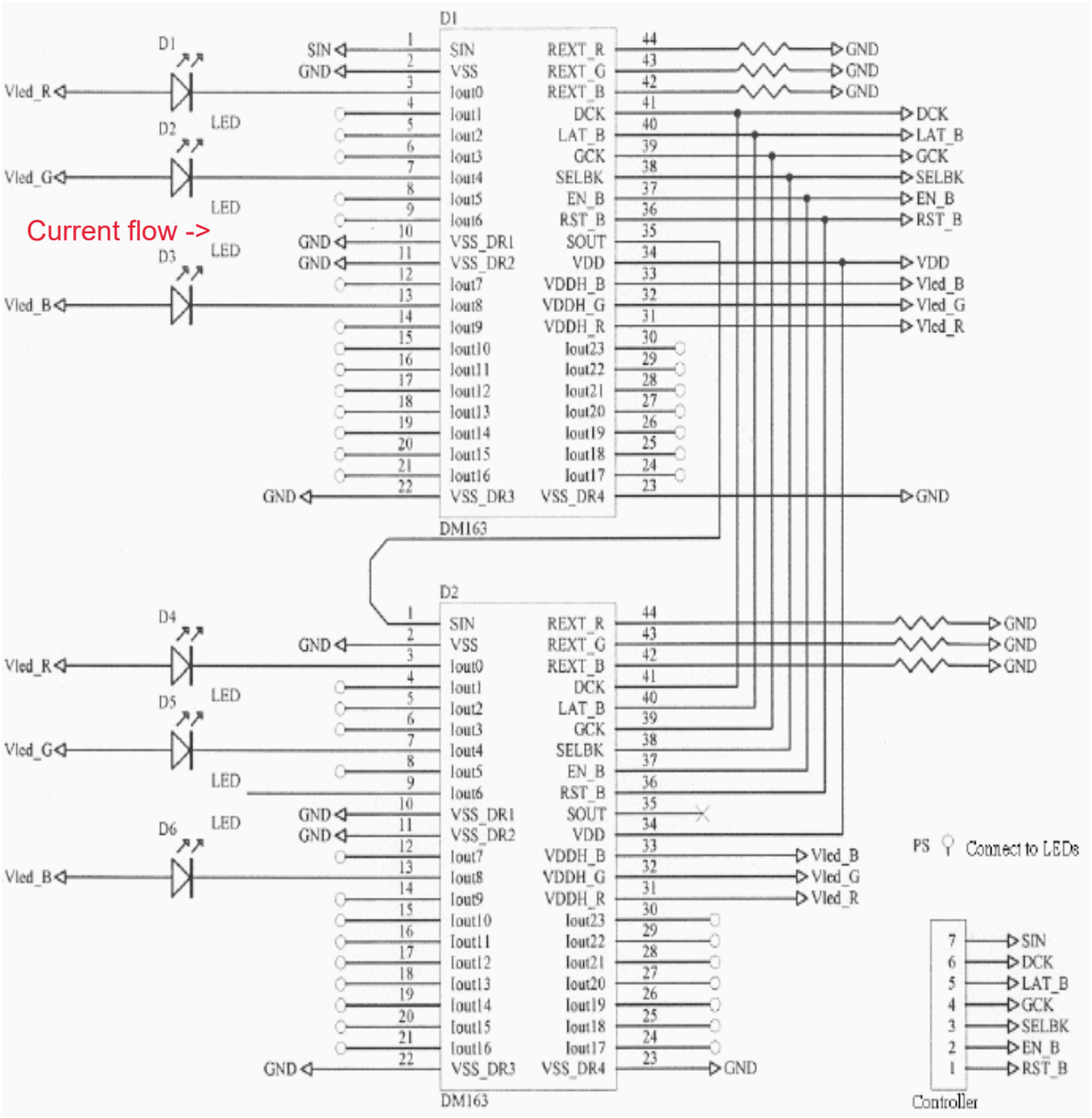


Figure 10. Application Diagram

Note:

1. The RST_B should be connected to controller to initialize the IC.
2. VDDH_R/G/B should be connected to Vled_R/G/B respectively. The Vled_R/G/B are power supply of Red/Green/Blue LEDs.
3. VSS_DR is the ground pin of LEDs. And it could be connected to VSS.

Application Diagram (Cont.)

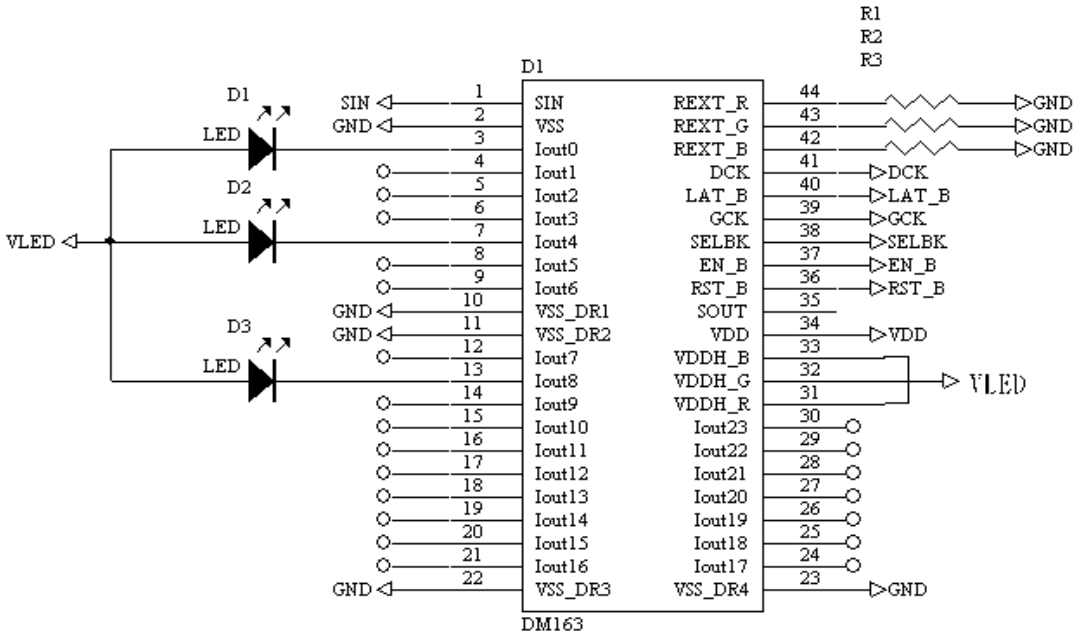


Figure 11. Application Diagram of anode-common LED

Driver Output Current (V_{DD} = 3.3V and 5.0V, Ta = 25°C)

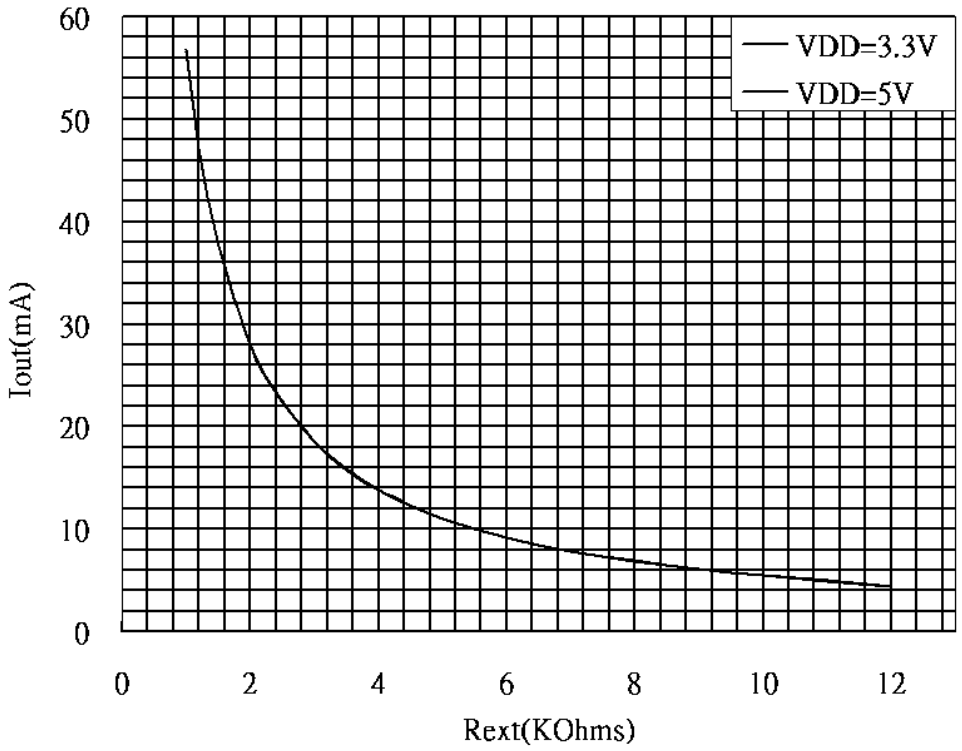


Figure 12. R_{EXT} vs. Output Current

Driver Output Current (Cont.)

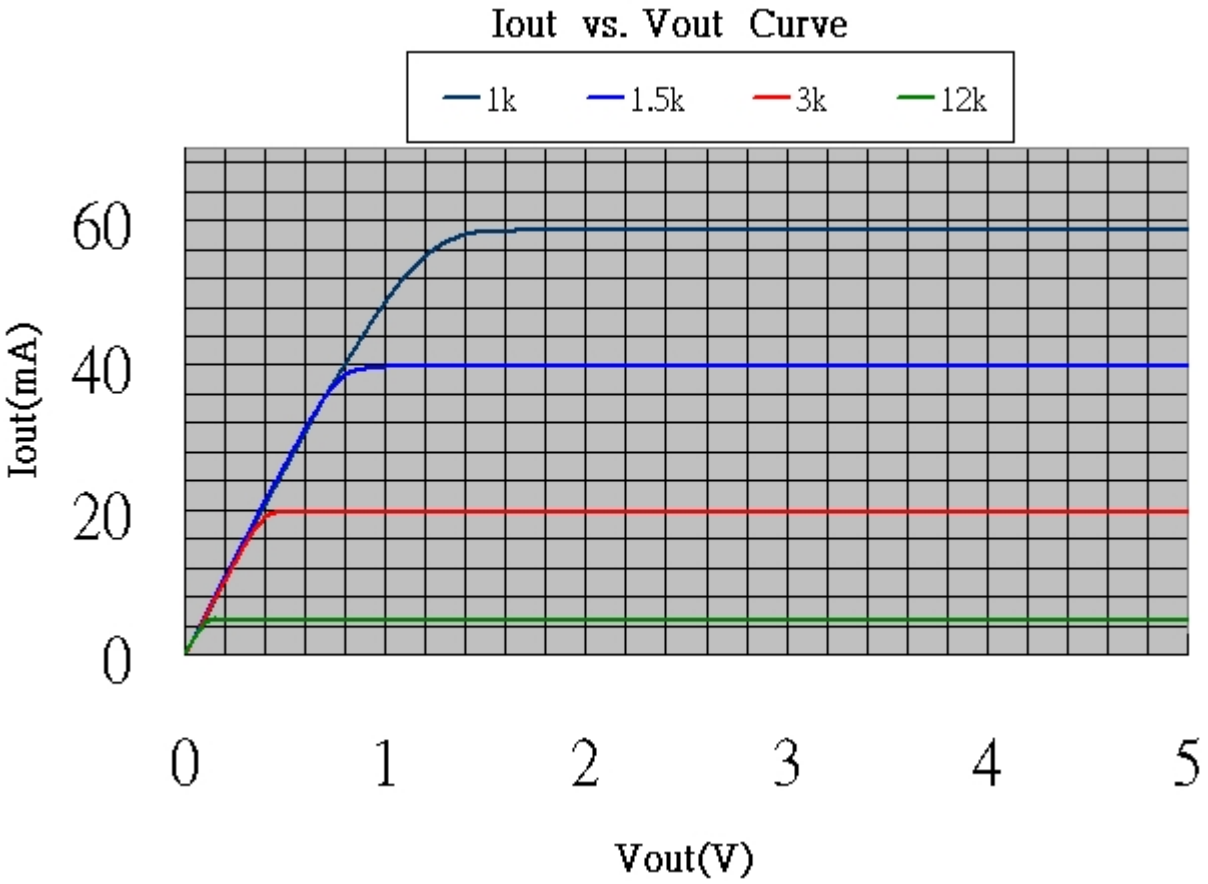


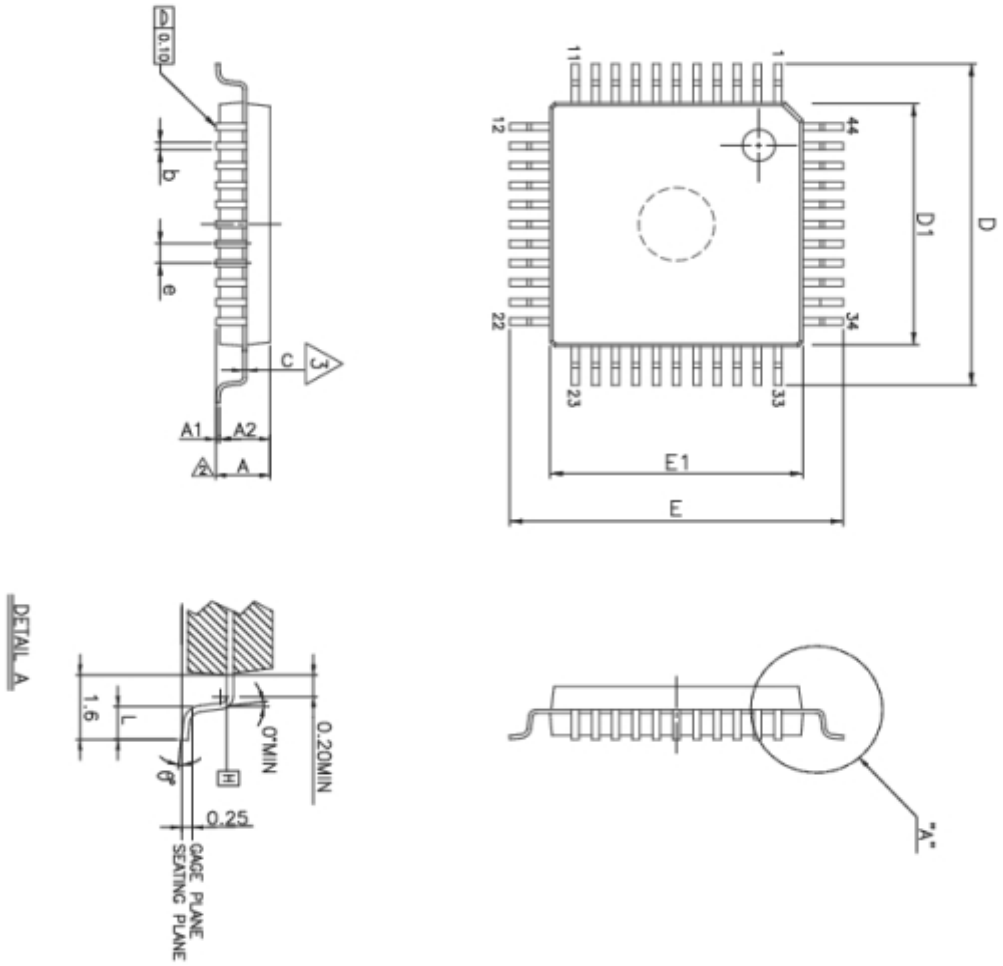
Figure 13. Vout vs. Output Current

The curve shown in Fig 12 is the average result of a large number of samples. Due to chip-to-chip variation in Vrext, users may observe a different Iout-Vout curve than above. However, the curves of VDD=5v and VDD=3.3v should be close to each other when the same chip is tested because DM163 utilizes a negative feedback circuit to keep the average voltage of Vrext pins close to constant, regardless of the VDD. Therefore, the Iout-to-Rext curve should not be seriously influenced by VDD variation.

The Fig 13 illustrates the relation between Vout and Iout. Iout is the constant value when Vout exceeds the voltage of turning point. In other words, Iout is independent of the fluctuation of Vout if IC is biased in this condition.

Package Outline Dimension

QFP44



3	SYMBOLS	MIN.	NOM	MAX.
	A	–	–	2.7
	A1	0.25	0.30	0.35
	A2	1.9	2.0	2.2
3	b		0.3 (TYP.)	
	D	13.00	13.20	13.40
	D1	9.9	10.00	10.10
	E	13.00	13.20	13.40
	E1	9.9	10.00	10.10
	L	0.73	0.88	0.93
	e		0.80 (TYP.)	
3	θ°	0	–	7
	C	0.1	0.15	0.2

UNIT : mm

NOTES:

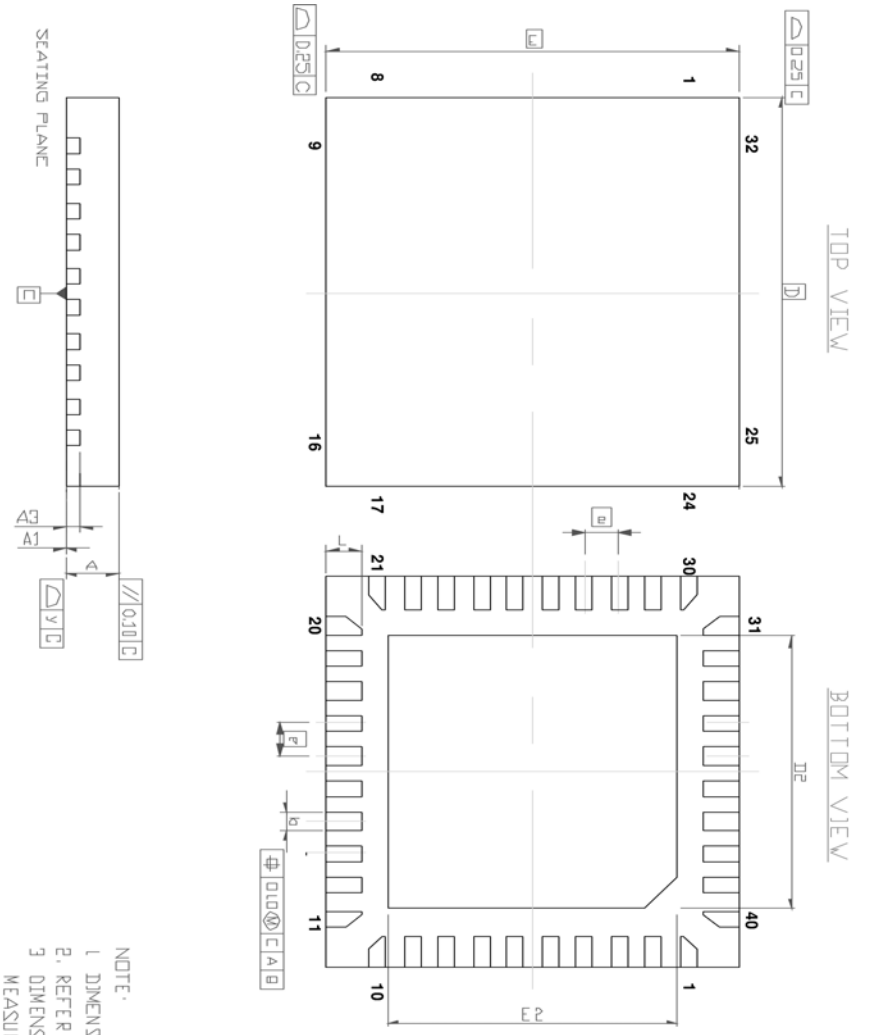
1.JEDEC OUTLINE:MO-108 AA-1

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

QFN40



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.8	2.0
A3		0.25 REF			9.84 REF	
b	0.18	0.23	0.30	7.1	9.1	11.8
D		6.00 BSC			236.2 BSC	
D2	1.75	3.70	4.25	68.9	145.7	167.3
E		6.00 BSC			236.2 BSC	
E2	1.75	3.70	4.25	68.9	145.7	167.3
e		0.50 BSC			19.7 BSC	
L	0.30	0.40	0.50	11.8	15.8	19.7
y		0.10			3.9	

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