Lab #3 Lab Report

Creating Registers for a Microprocessor

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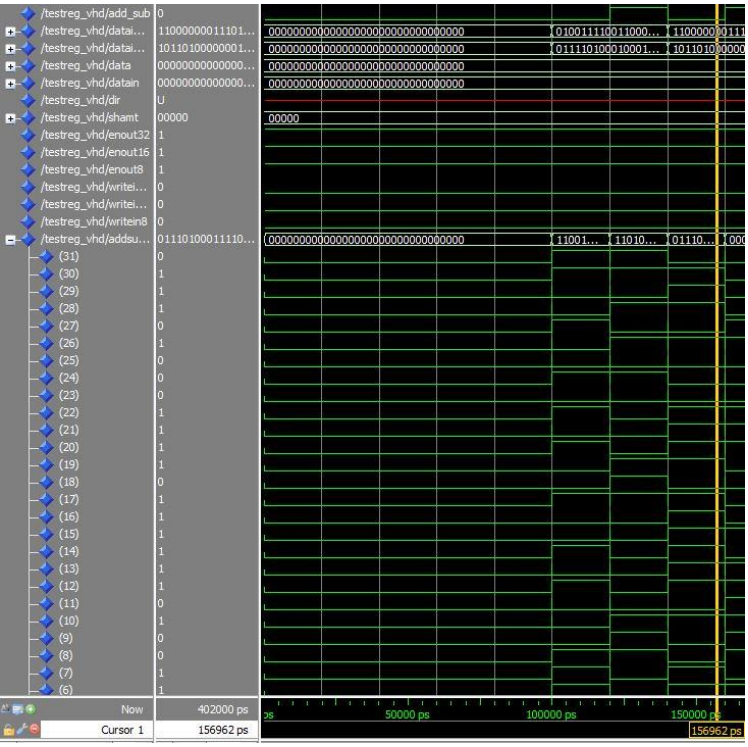
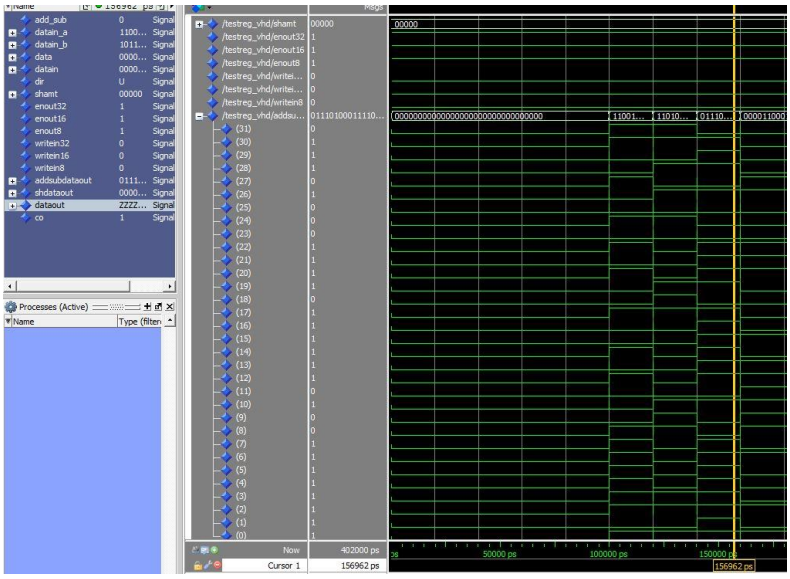
ECEGR 2220

Adder/Subtracter:

VHDL Results:

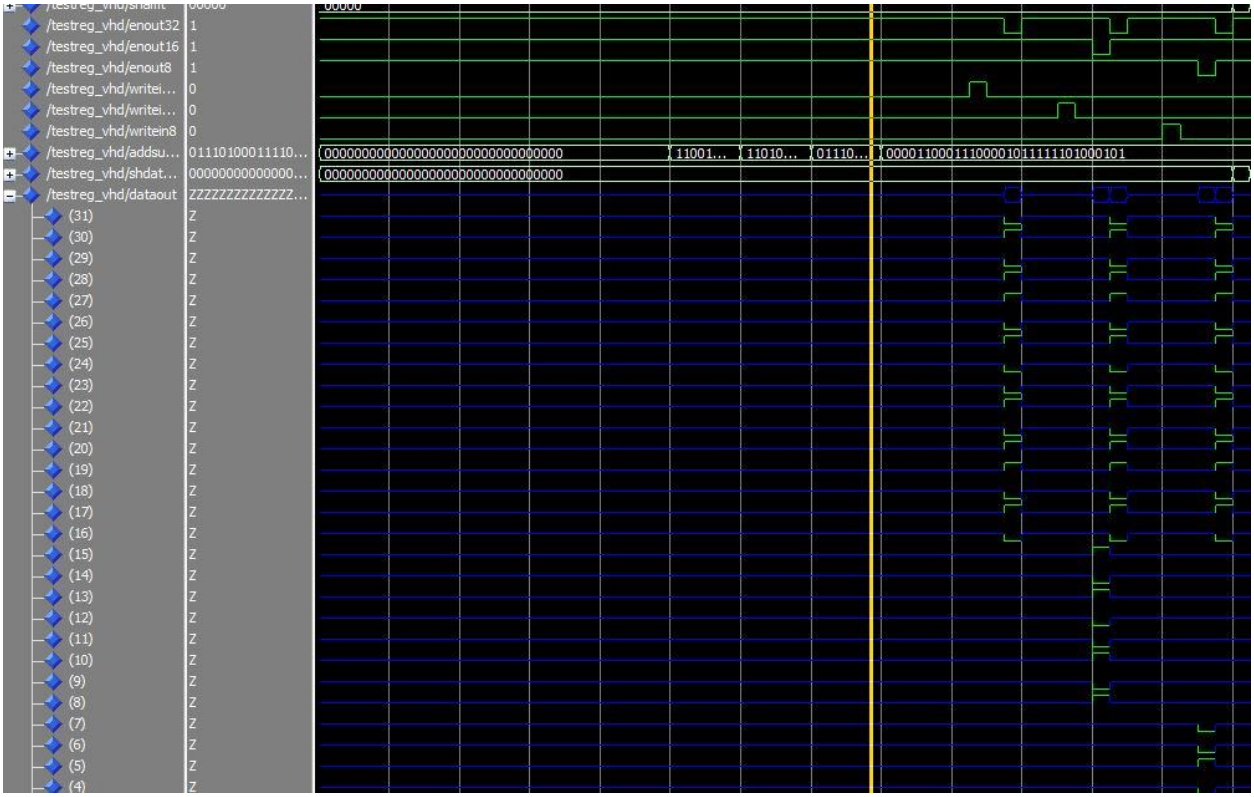




These results come first in the test program and are thus being reported on first. As the results display there is a clear change in outputs as the add_sub variable is switched. The VHDL Code uses the fulladder code and inverts depending on whether or not the add_sub is switched.

Register 32:

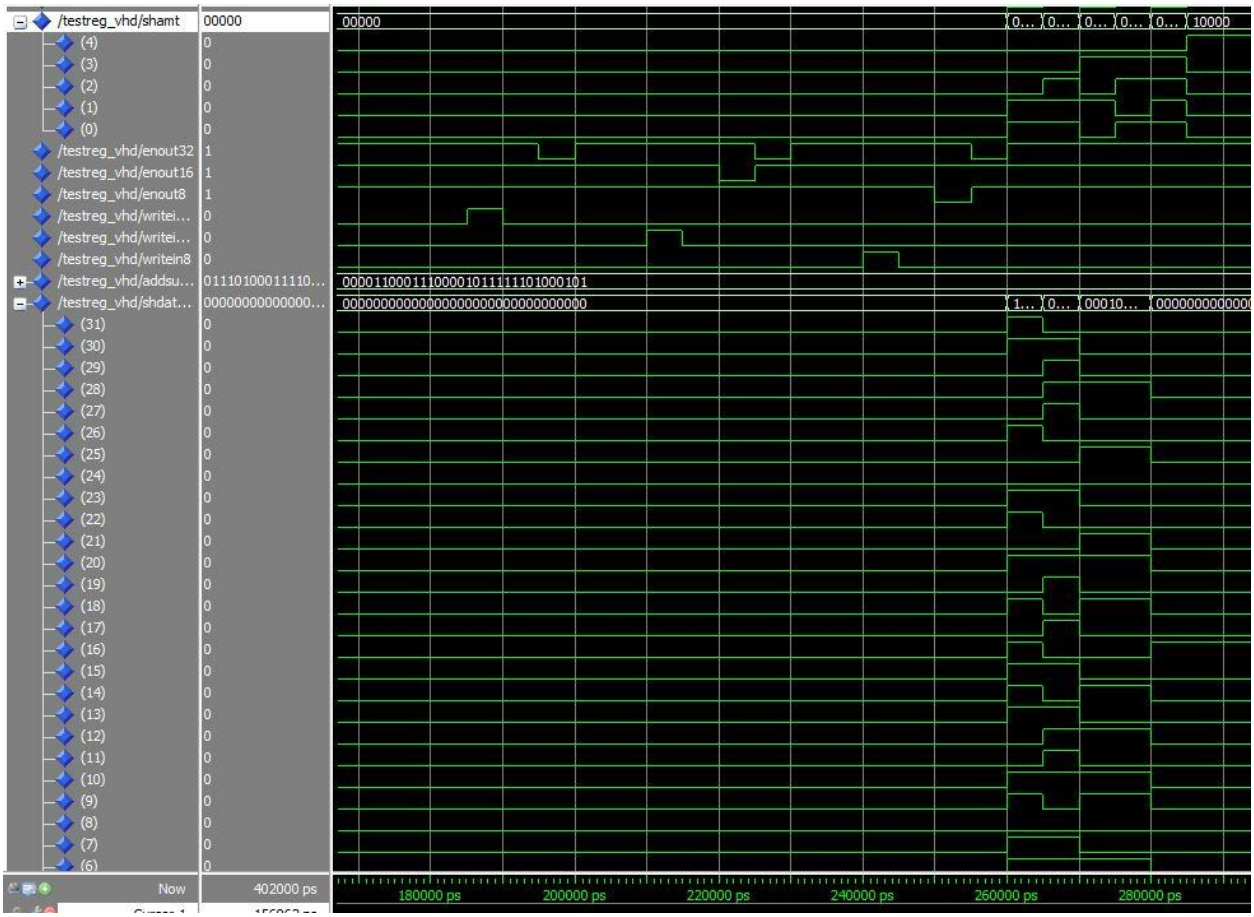
VHDL Results:



If the register 32 is working it can be assumed that the register 8 is working because register 32 uses the register 8 to alter its components. The results show a clear influence on the data when the various enouts are switched. Register32 VHDL code used register8 which used bitstorage to control and alter the outputs.

Shift Register:

VHDL Results:



These results show that as shamt is altered the outputs are responding to the shift. The code first takes into account the directions specified of the shift and then shifts accordingly.