Lab #5 Lab Report: Fixed Memory and Register Bank

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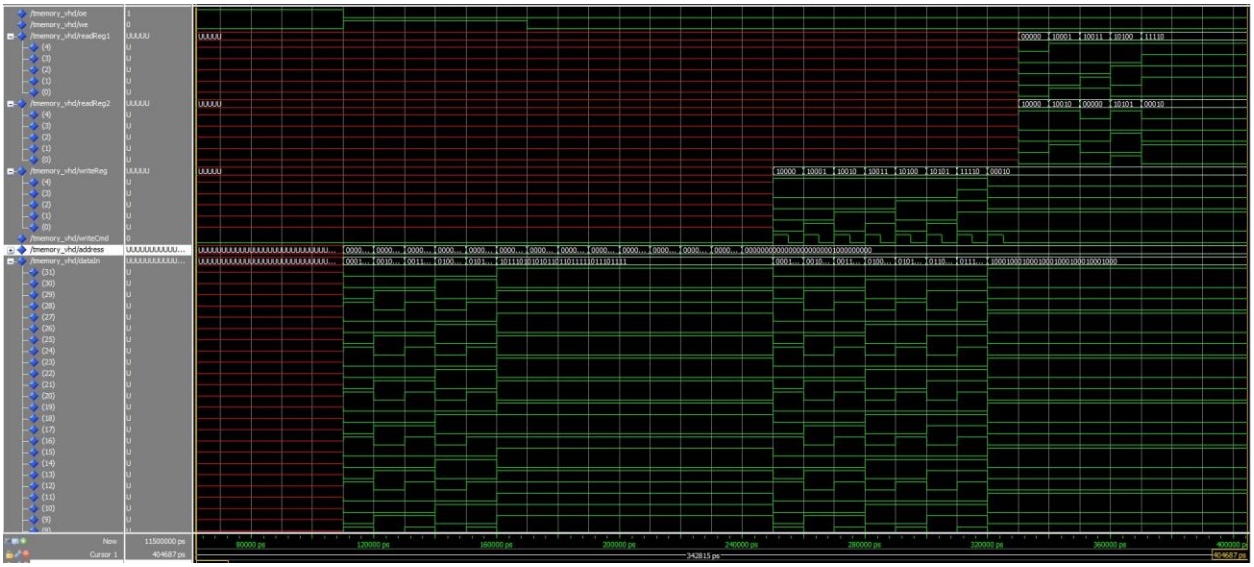
RAM design:

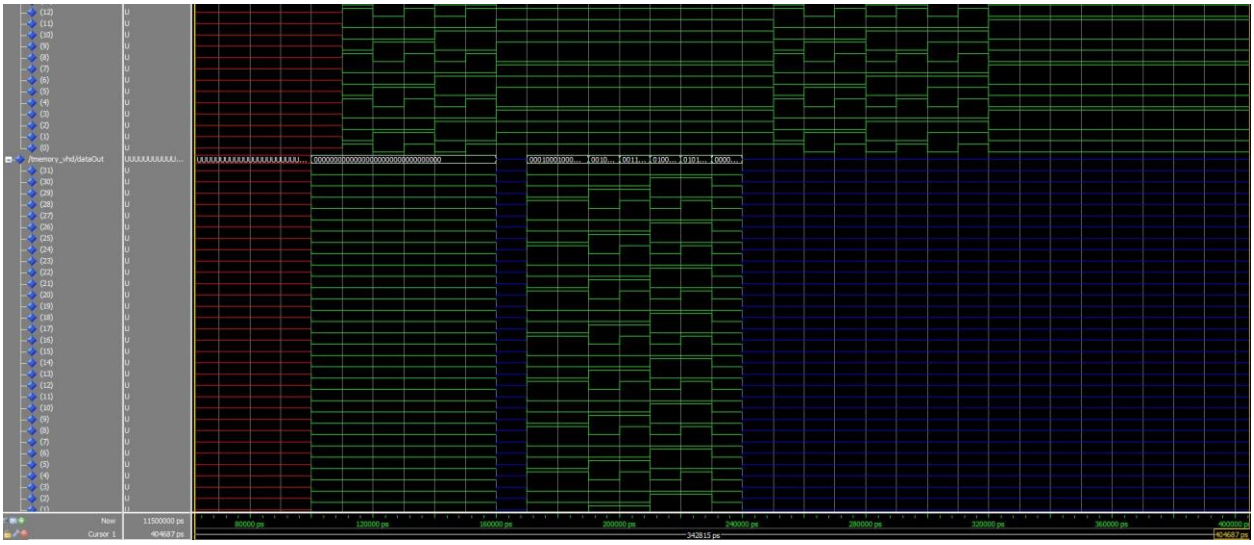
The RAM was created using a process of the clock, reset, and output and write enables. Within this process reset was implemented when set to 1, which sets the output to 0. From the clock and based on the settings of the output and write enables the output was controlled to be given the input. If output enable was set to 0, the output received Z.

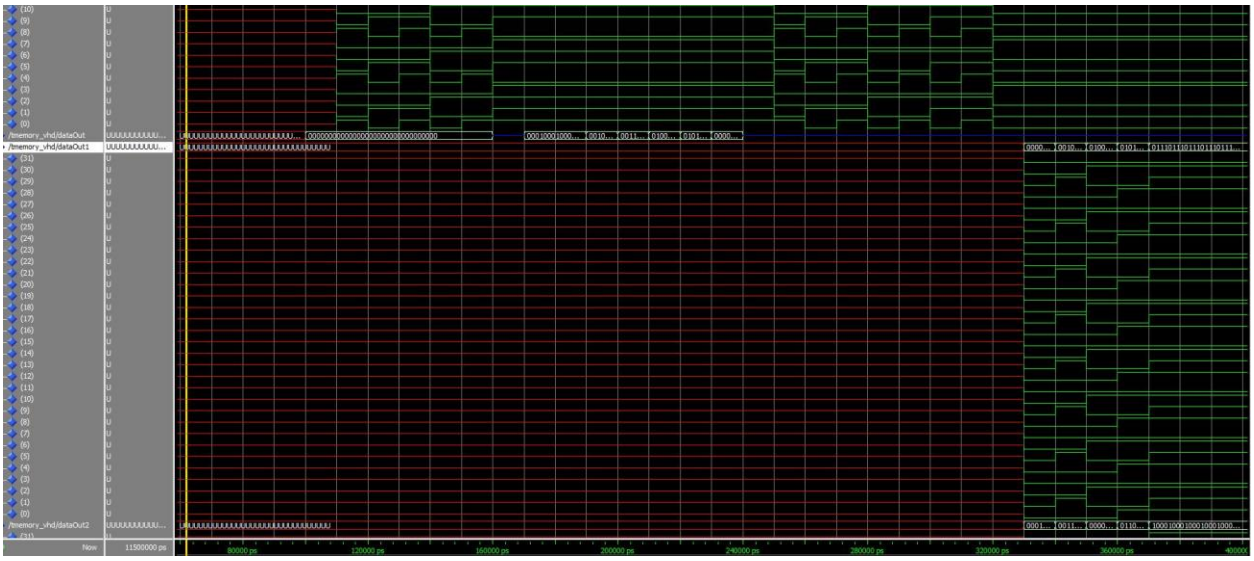
Register Bank design:

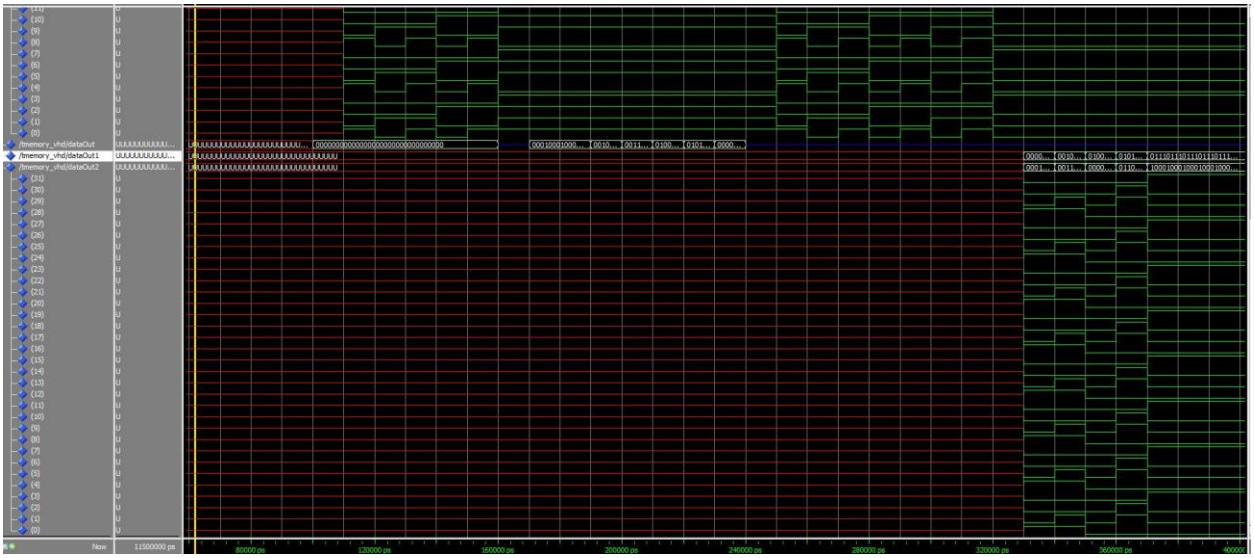
The register bank waits until the write command is given and then writes data from either of the read registers into their corresponding outputs.

Simulation Results:









The outputs change as expected according to the test bench and RAM and register bank.

The address space is only 30 bits because the other two bits are for the opcode.