AHWABAN MUKHERJEE | 22EC37001

B.Tech.(Hons.) in ELECTRONICS AND ELECTRICAL COMMUNICATION ENGINEERING and M.Tech. in MICROELECTRONICS AND VLSI CIRCUITS

EDUCATION

Year	Degree/Exam	Institute	CGPA/Marks
2027	M.TECH Dual Degree 5Y	IIT Kharagpur	8.55 / 10
2021	Class XII Board (CBSE)	Indira Gandhi Memorial High School, Barasat	93%
2019	Class X Board (CBSE)	Sudhir Memorial Institute, Madhyamgram	93%

PROJECTS

Design of Frequency Multiplier using Phase Locked Loop | Prof. Mrigank Sharad **Aug'24 - Oct'24**
- Designed a 128-factor frequency multiplier using a **type-II PLL** for high-speed data transmission at **5GHz,** with less than **4µs** locking time
- Designed a **current-starved ring VCO** with a **digital control** for similar **tuning ranges** and locking voltages across all the **process corners**
- Designed a **128**-factor **frequency divider** using both dynamic and static flip-flops and a **phase-frequency detector** using **TSPC** flip-flops
- A **charge pump** and a 2nd order **LPF** generate the control voltage for the **VCO** with an overshoot of about **9%** across all process corners

Design of 2-Stage Operational Transconductance Amplifiers | Self Project **Jun'24 - Jul'24**
- Designed a **single-ended 2-Stage OTA** with a **cascoded** output stage and **Miller compensation** with **pole-zero** cancellation for **90dB** low-frequency gain at a **50°** phase margin for a **110MHz** unity-gain bandwidth, **50dB** PSRR and **41dB** CMRR in the **TSMC 65nm** technology node
- Designed a similar **fully-differential OTA** with a **split-differential CMFB** for **60dB** gain, **45°** PM, **488MHz** UGB, **17dB** PSRR and **59dB** CMRR
- Made the layout of a **2-Stage OTA** with the **common centroid** methodology and ran **DRC** and **LVS** in the **UMC 180nm** technology node

Design of MIPS32 Pipelined Processor | Self Project **May'25 - Jun'25**
- Designed a **5-stage pipelined** processor with **32** GPRs of **32-bit** width and a unified word-adressable memory of **4KB** for the **MIPS32 ISA**
- Described all the pipeline stages and integrated them into a top-level module in **Verilog HDL** for executing **I, R** and **J-type** instructions
- Designed **hazard** and **forwarding units** to resolve hazards due to data dependencies in the pipeline without hardcoded NOP instructions
- Validated pipeline behaviour and hazards from timing waveforms by custom **machine code** programs stored in the instruction memory

Design of Quarter-Rate Clock and Data Recovery Circuit | Prof. Mrigank Sharad **Nov'24 - Present**
- Designed a **quadrature VCO** at **2.5GHz** generating a 4-phase clock with **digital control** for same **tuning range** across all **process corners**
- Designed quarter-rate phase and frequency detectors and lock detector and obtained design specifications for the charge pump at 10GHz

Design of Latched Ripple-Carry Adder | VLSI Laboratory Course Project | Prof. Pradip Mandal **Mar'25 - Apr'25**
- Designed a ring oscillator with 7 inverter stages and a clock driver to generate a **2.4GHz** clock signal with capacity to drive a **fanout of 64**
- Designed CMOS logic gates, latches and flip-flops at the gate level and sized them with **parametric simulations** for equal transition times
- Designed a 4-bit ripple carry adder and a 4-bit PIPO register and integrated them to a **pipeline** with thorough **timing analysis** at all levels

CERTIFICATIONS

VLSI Summer School | Prof. Mrigank Sharad **May'24 - Jul'24**
- Designed a high-bandwidth 2-stage OTA without a mirror-pole for a **57dB** gain and a **54°** PM at **328MHz** UGB in the TSMC 65nm node
- Designed a **folded cascode** OTA with both NMOS and PMOS inputs for rail-to-rail ICMR and gain of **48dB** at **46°** PM for a UGB of **101MHz**
- Designed **supply independent** biasing, sample-and-hold circuits, **dynamic latches** and **dynamic comparators** for high-speed applications
- Designed as a course project a **low-latency** seizure detection scheme at 100MHz for µV-order EEG signals with a preamplifier, comparator and a **Strong ARM Latch** generating clock signals and a synchronous binary counter generating **detection spikes** on threshold overflow

SKILLS AND EXPERTISE

Software : Cadence Virtuoso | Xilinx Vivado | Simulink | Ansys HFSS | LTspice | ROS/ROS2 | Keil µVision | Silvaco Atlas | Solidworks
Programming Languages : Verilog HDL | 8051 Assembly | MATLAB | C/C++ | Python

COURSEWORK INFORMATION

Electronics : Analog Electronics* | Digital Electronics* | Computer Architecture | VLSI Engg.* | RF and Microwave Engineering* | Network Theory* | Digital Signal Processing (I and II)* | Signals and Systems* | Control Systems | Communication (I and II)* | Analog and Mixed Signal IC Design** | Testing and Verification of Circuits** | VLSI Process Technology**
Mathematics and CS : Algorithms | Programming and Data Structures* | Linear Algebra | Convex Optimization | Probability and Statistics
**Include both theory and laboratory components, **Ongoing*

AWARDS AND ACHIEVEMENTS

- Secured **All India Rank 1460** in **JEE Advanced 2022** and **8540** in **JEE Main 2022** out of 906K candidates
- Secured **General Merit Rank 185** in **WBJEE 2022** out of 81K candidates

POSITIONS OF RESPONSIBILITY

Mobile Robotics Head | Autonomous Ground Vehicles Research Group | Prof. Debashish Chakravarty | IIT Kharagpur
- **Leading** the hardware module of the group working on FPGA-based **deep-learning acclerators** for applications in computer vision
- Selected and oversaw the training of next batches of students in the group, for the **hardware, vision, SLAM** and **planning** modules
- Worked on a **TMLR** reproducibility report submission for **MLRC 2024** on the modeling of dynamic 3-D scenes by implicit representations in the **Hexplanes** and **K-Planes** approaches as opposed to the conventional **NeRF** methods by experiments on various standard datasets

EXTRA CURRICULAR ACTIVITIES

- Volunteered for the **NCC** and obtained the **B Certificate,** with 2 years of **drill, weapon** and **social** training and an annual **training camp**
- **Mentoring** and closely guiding 3 EC undergraduates of the '24 batch in academics, co-curriculars and other overall developmental areas
- Managed GMUN, internship and placement training, and various other events as an **associate member** in **Communiqué**, IIT Kharagpur
- Reported and present on various campus events like the Gymkhana elections, GC and Inter-IIT as a **junior reporter** in **Awaaz**, IIT Kharagpur

!Self declared by the student, CDC could not verify the relevant documents