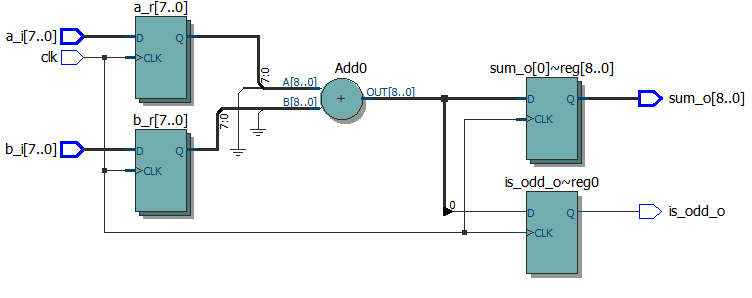
1.

2. Changed non-blocking assignments to blocking

3.

a) 26 flip flops/registers

b) 39,600 flip flops/registers

c) 9 combinational functions

d) 39600 combination functions

4.

Fmax = 548.85 MHz

Cycletime = 1/548.85 MHz = .00182199 MHz

5.

|  |  |  |  |
| --- | --- | --- | --- |
| Width | Fmax | # of combinational functions | # of registers (flip-flops) used |
| 8 | 548.85 MHz | 9 | 26 |
| 16 | 416.32 MHz | 17 | 50 |
| 32 | 311.24 MHz | 33 | 98 |
| 64 | 196.16 MHz | 65 | 194 |

6.

a) I expect the rs and rd val to be changed to the values stored in the corresponding addresses that were just changed, regardless of where the clock is at the time.

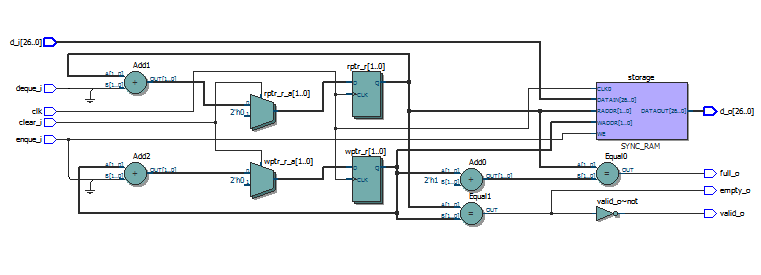
b) I expect the rs and rd val to be the same value, which is the value stored in the single address that rs and rd addr are assigned to.

c) I expect the old value of the register to be read until there is a positive clock edge. At the positive clock edge the write will occur and the read value will be updated.

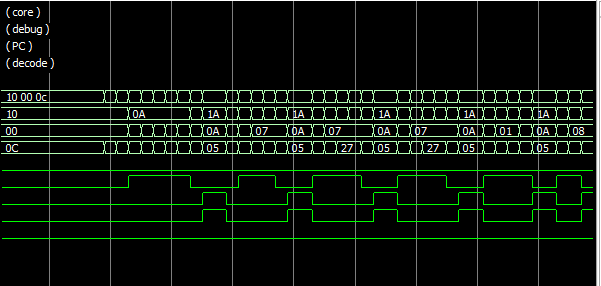
7.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Configuration | Fmax | # of combinational functions | # of registers (flip-flops) used | # of memory bits |
| 8 16-bit regs | 452.69 MHz | n/a | 26 | 256 |
| 16 16-bit regs | 442.09 MHz | n/a | 29 | 512 |
| 32 16-bit regs | 447.23 MHz | n/a | 32 | 1024 |
| 32 64-bit regs | 421.05 MHz | 21 | 80 | 4096 |
| 256 32-bit regs |  | Exceeds max # of pins |  |  |

8.



9.



10.

3327 cycles

160 instructions

11.

-2069 registers

-2142 functions

-16834 memory bits

-Info (11798): Fitter preparation operations ending: elapsed time is 00:00:12

Error (11802): Can't fit design in device

-

- #cycles = 3327 and if Fmax is 500MHz then cycle time is 1/500

3327x 1/500 = 6.664cycles x MHz