

# BC66-OpenCPU

# Hardware Design

**LPWA Module Series**

Rev. BC66-OpenCPU\_Hardware\_Design\_V1.2

Date: 2019-05-06

Status: Released



**Our aim is to provide customers with timely and comprehensive service. For any assistance, please contact our company headquarters:**

**Quectel Wireless Solutions Co., Ltd.**

7<sup>th</sup> Floor, Hongye Building, No.1801 Hongmei Road, Xuhui District, Shanghai 200233, China

Tel: +86 21 5108 6236

Email: [info@quectel.com](mailto:info@quectel.com)

**Or our local office. For more information, please visit:**

<http://www.quectel.com/support/sales.htm>

**For technical support, or to report documentation errors, please visit:**

<http://www.quectel.com/support/technical.htm>

Or email to: [support@quectel.com](mailto:support@quectel.com)

**GENERAL NOTES**

QUECTEL OFFERS THE INFORMATION AS A SERVICE TO ITS CUSTOMERS. THE INFORMATION PROVIDED IS BASED UPON CUSTOMERS' REQUIREMENTS. QUECTEL MAKES EVERY EFFORT TO ENSURE THE QUALITY OF THE INFORMATION IT MAKES AVAILABLE. QUECTEL DOES NOT MAKE ANY WARRANTY AS TO THE INFORMATION CONTAINED HEREIN, AND DOES NOT ACCEPT ANY LIABILITY FOR ANY INJURY, LOSS OR DAMAGE OF ANY KIND INCURRED BY USE OF OR RELIANCE UPON THE INFORMATION. ALL INFORMATION SUPPLIED HEREIN IS SUBJECT TO CHANGE WITHOUT PRIOR NOTICE.

**COPYRIGHT**

THE INFORMATION CONTAINED HERE IS PROPRIETARY TECHNICAL INFORMATION OF QUECTEL WIRELESS SOLUTIONS CO., LTD. TRANSMITTING, REPRODUCTION, DISSEMINATION AND EDITING OF THIS DOCUMENT AS WELL AS UTILIZATION OF THE CONTENT ARE FORBIDDEN WITHOUT PERMISSION. OFFENDERS WILL BE HELD LIABLE FOR PAYMENT OF DAMAGES. ALL RIGHTS ARE RESERVED IN THE EVENT OF A PATENT GRANT OR REGISTRATION OF A UTILITY MODEL OR DESIGN.

***Copyright © Quectel Wireless Solutions Co., Ltd. 2019. All rights reserved.***

# About the Document

## History

Revision	Date	Author	Description
1.0	2018-08-31	Brooke WANG/ Newgate HUA	Initial
1.1	2018-11-14	Newgate HUA	Updated supported bands and involved RF parameters of BC66-OpenCPU.  1. Enabled USB interface and added its related description (Chapters 2.3, 3.2, 3.3 & 3.7). 2. Enabled additional five GPIO interfaces. 3. Optimized the description of the module's operating modes (Chapter 3.4). 4. Added a note for the reference design of power supply (Chapter 3.6.2).
1.2	2019-05-06	Speed SUN/ Allan LIANG	5. Added ADC sample range (Chapter 3.12). 6. Added the current consumption values for band 4 and the testing conditions (Chapter 5.2). 7. Updated the module's recommended stencil thickness and peak reflow temperatures (Chapter 7.2). 8. Updated multiplexed pins and their functions (Appendix B).

## Contents

About the Document.....	2
Contents.....	3
Table Index.....	5
Figure Index.....	6
<b>1 Introduction .....</b>	<b>7</b>
1.1. Safety Information.....	8
<b>2 Product Concept.....</b>	<b>9</b>
2.1. General Description .....	9
2.2. Key Features.....	10
2.3. Functional Diagram.....	12
2.4. Development Board .....	12
<b>3 Application Interfaces .....</b>	<b>13</b>
3.1. General Description .....	13
3.2. Pin Assignment .....	14
3.3. Pin Description .....	15
3.4. Operating Modes.....	19
3.5. Power Saving Mode (PSM).....	20
3.6. Power Supply .....	21
3.6.1. Power Supply Pins .....	21
3.6.2. Reference Design for Power Supply.....	22
3.7. Power on/off Scenarios.....	23
3.7.1. Turn on .....	23
3.7.2. Turn off .....	24
3.7.3. Reset the Module .....	25
3.8. USB Interface.....	27
3.9. UART Interfaces.....	28
3.9.1. Main UART Port .....	29
3.9.2. Debug UART Port .....	29
3.9.3. Auxiliary UART Port .....	30
3.9.4. UART Application .....	30
3.10. SPI Interface .....	32
3.11. USIM Interface .....	33
3.12. ADC Interface.....	35
<b>4 Antenna Interface.....</b>	<b>36</b>
4.1. Pin Definition .....	36
4.2. Operating Frequencies .....	36
4.3. RF Antenna Reference Design .....	37
4.4. Reference Design of RF Layout .....	38
4.5. Antenna Requirements .....	40

4.6.	RF Output Power .....	41
4.7.	RF Receiving Sensitivity .....	42
4.8.	Recommended RF Connector for Antenna Installation .....	43
<b>5</b>	<b>Electrical and Reliability Characteristics .....</b>	<b>45</b>
5.1.	Operation and Storage Temperatures.....	45
5.2.	Current Consumption.....	45
5.3.	Electrostatic Discharge .....	47
<b>6</b>	<b>Mechanical Dimensions .....</b>	<b>49</b>
6.1.	Mechanical Dimensions of the Module .....	49
6.2.	Recommended Footprint .....	51
6.3.	Top and Bottom Views of the Module .....	52
<b>7</b>	<b>Storage, Manufacturing and Packaging.....</b>	<b>53</b>
7.1.	Storage.....	53
7.2.	Manufacturing and Soldering.....	54
7.3.	Packaging .....	55
7.3.1.	Tape and Reel Packaging .....	55
<b>8</b>	<b>Appendix A References.....</b>	<b>57</b>
<b>9</b>	<b>Appendix B Multiplexed Pins .....</b>	<b>60</b>

## Table Index

TABLE 1: FREQUENCY BANDS OF BC66-OPENCPU MODULE .....	9
TABLE 2: BC66-OPENCPU KEY FEATURES .....	10
TABLE 3: I/O PARAMETERS DEFINITION .....	15
TABLE 4: PIN DESCRIPTION .....	15
TABLE 5: OVERVIEW OF OPERATING MODES .....	19
TABLE 6: POWER SUPPLY PINS .....	22
TABLE 7: PWRKEY PIN .....	23
TABLE 8: RESET PIN .....	25
TABLE 9: PIN DEFINITION OF USB INTERFACE .....	27
TABLE 10: PIN DEFINITION OF UART INTERFACES .....	28
TABLE 11: PIN DEFINITION OF SPI INTERFACE .....	33
TABLE 12: PIN DEFINITION OF USIM INTERFACE .....	34
TABLE 13: PIN DEFINITION OF ADC INTERFACE .....	35
TABLE 14: PIN DEFINITION OF NB-IOT ANTENNA INTERFACE .....	36
TABLE 15: MODULE OPERATING FREQUENCIES .....	36
TABLE 16: ANTENNA CABLE INSERTION LOSS REQUIREMENTS .....	40
TABLE 17: REQUIRED ANTENNA PARAMETERS .....	40
TABLE 18: RF OUTPUT POWER .....	41
TABLE 19: RF RECEIVING SENSITIVITY (WITH RF RETRANSMISSIONS) .....	42
TABLE 20: OPERATION AND STORAGE TEMPERATURES .....	45
TABLE 21: MODULE CURRENT CONSUMPTION (3.3V VBAT POWER SUPPLY) .....	46
TABLE 22: ELECTROSTATIC DISCHARGE CHARACTERISTICS (25°C, 45% RELATIVE HUMIDITY) .....	48
TABLE 23: RECOMMENDED THERMAL PROFILE PARAMETERS .....	54
TABLE 24: RELATED DOCUMENTS .....	57
TABLE 25: TERMS AND ABBREVIATIONS .....	57
TABLE 26: MULTIPLEXED PINS AND THEIR FUNCTIONS .....	60

## Figure Index

FIGURE 1: BC66-OPENCPU FUNCTIONAL DIAGRAM .....	12
FIGURE 2: PIN ASSIGNMENT .....	14
FIGURE 3: MODULE OPERATING MODES .....	20
FIGURE 4: MODULE POWER CONSUMPTION IN DIFFERENT MODES.....	20
FIGURE 5: TIMING OF WAKING UP MODULE FROM PSM.....	21
FIGURE 6: REFERENCE CIRCUIT FOR POWER SUPPLY .....	22
FIGURE 7: TURN ON THE MODULE USING DRIVING CIRCUIT .....	23
FIGURE 8: TURN ON THE MODULE USING KEYSTROKE .....	24
FIGURE 9: POWER ON TIMING .....	24
FIGURE 10: POWER OFF TIMING (TURN OFF BY AT COMMAND).....	25
FIGURE 11: POWER OFF TIMING (POWER OFF BY DISCONNECTING VBAT) .....	25
FIGURE 12: REFERENCE DESIGN OF RESET WITH A DRIVING CIRCUIT .....	26
FIGURE 13: REFERENCE DESIGN OF RESET WITH A BUTTON.....	26
FIGURE 14: RESET TIMING.....	26
FIGURE 15: USB INTERFACE REFERENCE DESIGN .....	27
FIGURE 16: REFERENCE DESIGN OF MAIN UART PORT .....	29
FIGURE 17: REFERENCE DESIGN OF DEBUG UART PORT .....	30
FIGURE 18: REFERENCE DESIGN OF AUXILIARY UART PORT.....	30
FIGURE 19: REFERENCE CIRCUIT WITH VOLTAGE LEVEL TRANSLATOR CHIP.....	31
FIGURE 20: REFERENCE CIRCUIT WITH TRANSISTOR CIRCUIT .....	31
FIGURE 21: SKETCH MAP FOR RS-232 INTERFACE MATCH.....	32
FIGURE 22: REFERENCE DESIGN OF SPI INTERFACE WITH A TRANSLATOR CHIP .....	33
FIGURE 23: REFERENCE DESIGN OF USIM INTERFACE WITH A 6-PIN USIM CARD CONNECTOR .....	34
FIGURE 24: REFERENCE DESIGN OF NB-IOT ANTENNA INTERFACE .....	38
FIGURE 25: MICROSTRIP LINE DESIGN ON A 2-LAYER PCB.....	38
FIGURE 26: COPLANAR WAVEGUIDE LINE DESIGN ON A 2-LAYER PCB.....	39
FIGURE 27: COPLANAR WAVEGUIDE LINE DESIGN ON A 4-LAYER PCB (LAYER 3 AS REFERENCE GROUND) .....	39
FIGURE 28: COPLANAR WAVEGUIDE LINE DESIGN ON A 4-LAYER PCB (LAYER 4 AS REFERENCE GROUND) .....	39
FIGURE 29: DIMENSIONS OF THE U.FL-R-SMT CONNECTOR (UNIT: MM).....	43
FIGURE 30: MECHANICALS OF U.FL-LP CONNECTORS .....	43
FIGURE 31: BC66-OPENCPU TOP AND SIDE DIMENSIONS (UNIT: MM) .....	49
FIGURE 32: TAPE DIMENSIONS (UNIT: MM).....	56
FIGURE 33: REEL DIMENSIONS (UNIT: MM) .....	56

# 1 Introduction

This document defines the BC66-OpenCPU module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand BC66-OpenCPU module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, customers can use BC66-OpenCPU to design and set up mobile applications easily.



## 1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating BC66-OpenCPU module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.



The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.



In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

## 2 Product Concept

### 2.1. General Description

OpenCPU is a solution where the module acts as a main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of OpenCPU solution. Especially, its advantage in reducing the product cost is greatly valued by customers. With OpenCPU solution, development flow for wireless application and hardware design will be simplified. Main features of OpenCPU solution are listed below:

- Simplifies the development of embedded applications, and shortens product development cycle
- Simplifies circuit design, and reduces product cost
- Decreases the size of terminal products
- Reduces power consumption
- Supports firmware and APP bin upgrade via DFOTA
- Anti-copy technology to enhance product safety
- Improves products' cost-performance ratio, and enhances products' competitiveness

BC66-OpenCPU is a high-performance NB-IoT module with extremely low power consumption. It is designed to communicate with infrastructures of mobile network operators through NB-IoT radio protocols (3GPP Rel.13 and 3GPP Rel.14\*). And it supports a broad range of frequency bands as listed below.

**Table 1: Frequency Bands of BC66-OpenCPU Module**

Mode	BC66-OpenCPU
H-FDD	B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/B20/B25/B26*/B28/B66

BC66-OpenCPU is an SMD type module with LCC package, and has an ultra-compact profile 17.7mm × 15.8mm × 2.0mm. These make it can be easily embedded into size-constrained applications and provide reliable connectivity with the applications.

BC66-OpenCPU provides abundant external interfaces (USB, UART, GPIO, SPI, ADC, etc.) and protocol stacks (UDP/TCP, MQTT, LwM2M, etc.), which provide great convenience for customers' applications.

Due to compact form factor, ultra-low power consumption and extended temperature range, BC66-OpenCPU is a best choice for a wide range of IoT applications, such as smart metering, bike sharing, smart wearables, smart parking, smart city, security and asset tracking, home appliances, agricultural and environmental monitoring, etc. It is able to provide a complete range of SMS\* and data transmission services to meet customers' demands.

The module fully complies with the RoHS directive of the European Union.

**NOTE**

“\*” means under development.

## 2.2. Key Features

The following table describes the detailed features of BC66-OpenCPU module.

**Table 2: BC66-OpenCPU Key Features**

Feature	Details
Power Supply	<ul style="list-style-type: none"> <li>Supply voltage: 2.1V ~ 3.63V</li> <li>Typical supply voltage: 3.3V</li> </ul>
Power Saving	<ul style="list-style-type: none"> <li>Typical power consumption: 3.5uA</li> </ul>
Frequency bands	<b>LTE Cat NB1:</b> <ul style="list-style-type: none"> <li>B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/B20/B25/B26*/B28/B66</li> </ul>
Transmitting Power	<ul style="list-style-type: none"> <li>23dBm±2dB</li> </ul>
USIM Interface	<ul style="list-style-type: none"> <li>Support 1.8V USIM card</li> </ul>
USB Interface	<ul style="list-style-type: none"> <li>Conform to USB 1.1 specifications, with maximum data transfer rate up to 12Mbps</li> <li>Used for software debugging and upgrading</li> <li>Support USB serial driver under Windows/Linux operating systems</li> </ul>
UART Interfaces	<b>Main UART Port:</b> <ul style="list-style-type: none"> <li>Used for AT command communication and data transmission.</li> <li>By default, the module is in auto-baud mode, and it supports automatic baud rates not exceeding 115200bps. When powering on the module, the MCU has to send <b>AT</b> command consecutively to synchronize baud rate with the module. When <b>OK</b> is returned, it indicates the baud rate has been synchronized successfully. When the module is woken up from PSM or</li> </ul>

	<p>idle mode, the baud rate synchronized during start-up will be used directly.</p> <ul style="list-style-type: none"> <li>Also can be used for firmware upgrade, and in such case, the baud rate is 921600bps by default.</li> </ul> <p><b>Debug UART Port:</b></p> <ul style="list-style-type: none"> <li>Used for firmware debugging</li> <li>Default baud rate: 115200bps</li> </ul> <p><b>Auxiliary UART Port:</b></p> <ul style="list-style-type: none"> <li>Used for firmware debugging</li> <li>Hardware flow control* supported</li> <li>Default baud rate: 115200bps</li> </ul>
Network Protocols	<ul style="list-style-type: none"> <li>UDP/TCP/LwM2M/MQTT/DTLS/SNTP/CoAP*/PPP*/TLS*/HTTP*/HTTPS*</li> </ul>
SMS*	<ul style="list-style-type: none"> <li>Text/PDU Mode</li> </ul>
Data Transmission	<ul style="list-style-type: none"> <li>Single-tone: 25.5kbps (DL)/16.7kbps (UL)</li> <li>Multi-tone: 25.5kbps (DL)/62.5kbps (UL)</li> </ul>
AT Commands	<ul style="list-style-type: none"> <li>3GPP TS 27.005/3GPP TS 27.007 AT commands (3GPP Rel. 13/Rel.14*) and Quectel enhanced AT commands</li> </ul>
Firmware Upgrade	<ul style="list-style-type: none"> <li>Upgrade firmware via DFOTA, USB or main UART port</li> </ul>
Real Time Clock	<ul style="list-style-type: none"> <li>Supported</li> </ul>
Physical Characteristics	<ul style="list-style-type: none"> <li>Size: (17.7±0.15)mm × (15.8±0.15)mm × (2.0±0.2)mm</li> <li>Weight: 1.2g±0.2g</li> </ul>
Temperature Range	<ul style="list-style-type: none"> <li>Operation temperature range: -35°C ~ +75°C <sup>1)</sup></li> <li>Extended temperature range: -40°C ~ +85°C <sup>2)</sup></li> <li>Storage temperature range: -40°C ~ +90°C</li> </ul>
Antenna Interface	<ul style="list-style-type: none"> <li>50Ω impedance control</li> </ul>
RoHS	<ul style="list-style-type: none"> <li>All hardware components are fully compliant with EU RoHS directive</li> </ul>

## NOTES

- <sup>1)</sup> Within operation temperature range, the module is 3GPP compliant.
- <sup>2)</sup> Within extended temperature range, the module remains the ability to establish and maintain an SMS\*, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P<sub>out</sub> might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.
- "\*" means under development.

## 2.3. Functional Diagram

The following figure shows a block diagram of BC66-OpenCPU and illustrates the major functional parts.

- Radio frequency
- Baseband
- Power management
- Peripheral interfaces

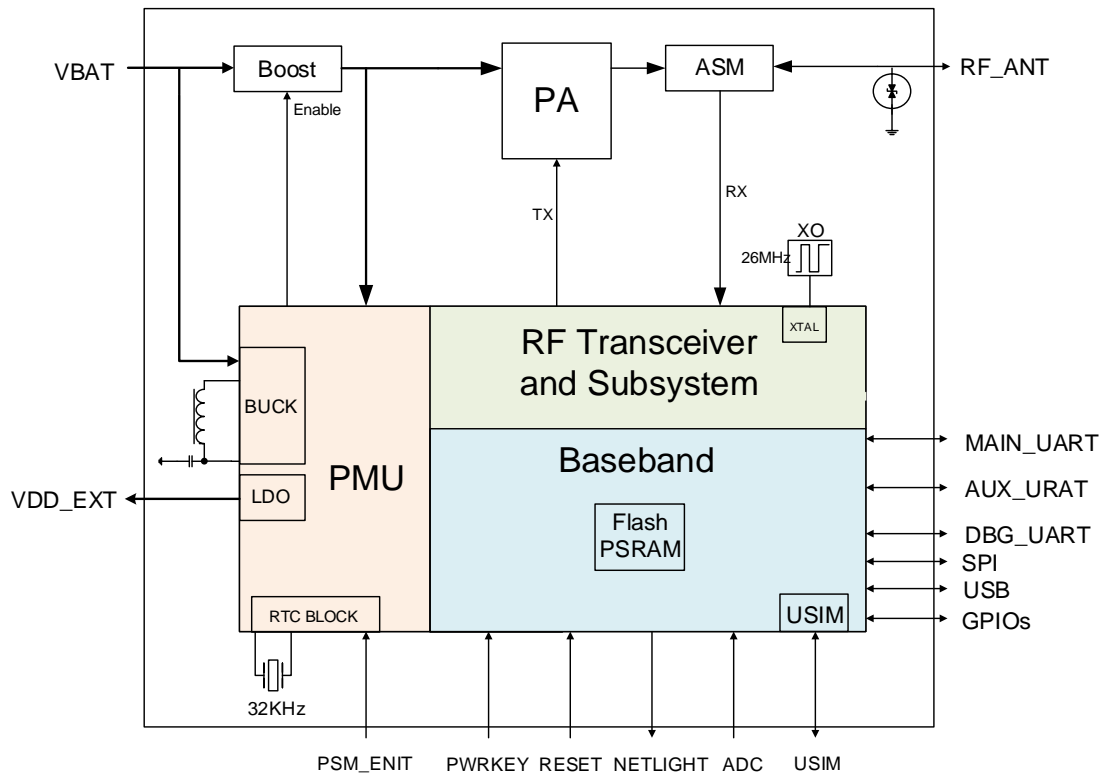


Figure 1: BC66-OpenCPU Functional Diagram

### NOTE

“\*” means under development.

## 2.4. Development Board

Quectel provides a complete set of development tools to facilitate the use and testing of BC66-OpenCPU module. The development tool kit includes the TE-B board, USB cable, antenna and other peripherals. For more details, please refer to **document [1]**.

# 3 Application Interfaces

## 3.1. General Description

BC66-OpenCPU is equipped with a total of 58 pins, including 44 LCC pins and 14 LGA pins. The subsequent chapters will provide detailed descriptions of the following functions/pins/interfaces:

- PSM
- Power Supply
- PWRKEY
- RESET
- USB Interface
- UART Interfaces
- SPI Interface
- USIM Interface
- ADC Interface

## 3.2. Pin Assignment

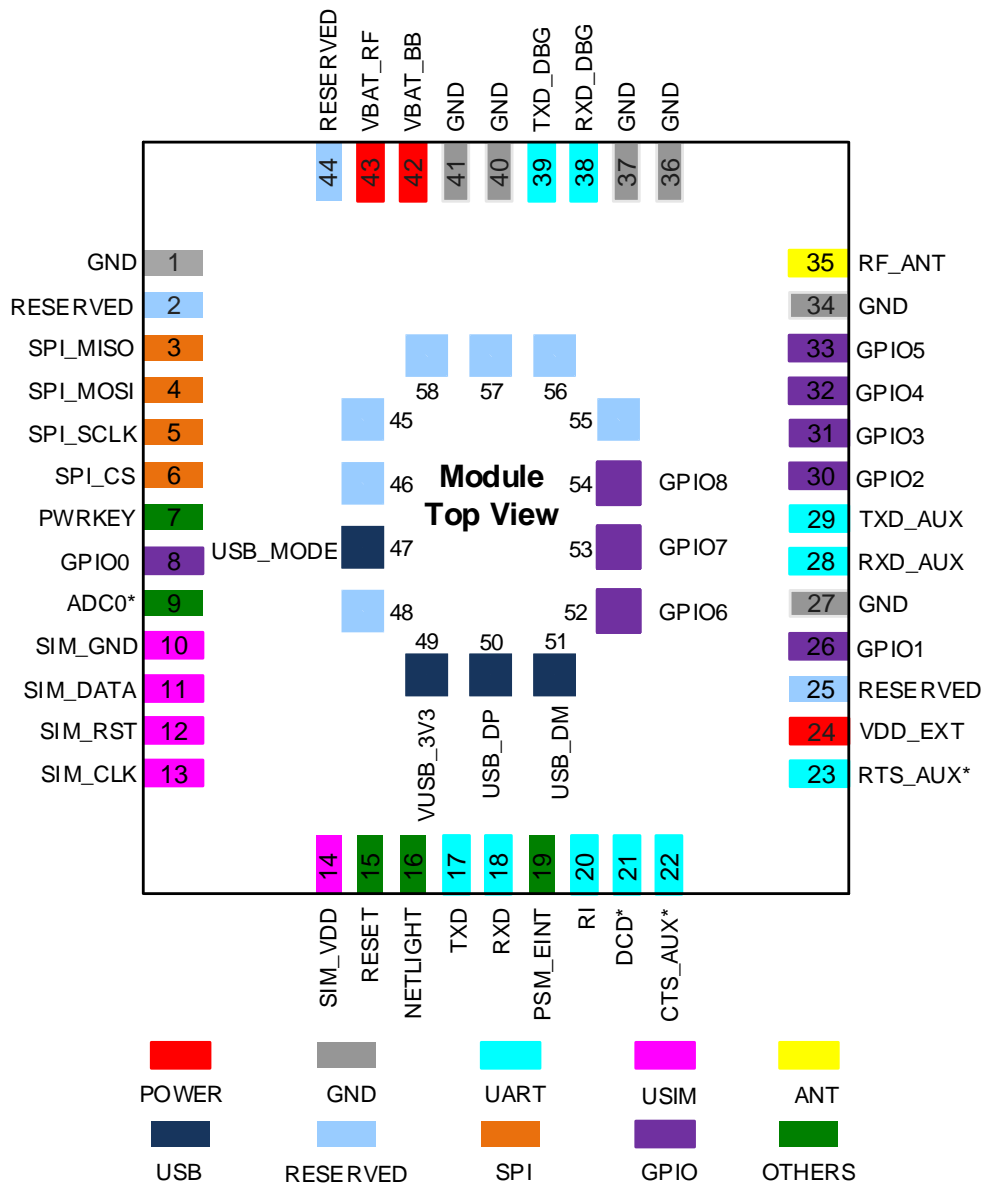


Figure 2: Pin Assignment

### NOTES

1. Keep all reserved pins unconnected.
2. "\*" means under development.

### 3.3. Pin Description

The following table describes the pin definition of BC66-OpenCPU module in details.

**Table 3: I/O Parameters Definition**

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
IO	Bidirectional
PI	Power input
PO	Power output

**Table 4: Pin Description**

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	42	PI	Power supply for the module's baseband part	Vmax=3.63V Vmin=2.1V Vnorm=3.3V	
VBAT_RF	43	PI	Power supply for the module's RF part	Vmax=3.63V Vmin=2.1V Vnorm=3.3V	
VDD_EXT	24	PO	1.8V output power supply	Vnorm=1.8V	No voltage output in PSM mode. It is intended to supply power for the module's pull-up circuits, and is thus not recommended to be used as the power supply for external circuits.
GND	1, 27, 34,	GND			



36, 37, 40,  
41

#### Power Key Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	7	DI	Pull down PWRKEY to turn on the module	$V_{ILmax}=0.3*VBAT$ $V_{IHmin}=0.7*VBAT$	

#### Reset Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESET	15	DI	Reset the module		Active low.

#### PSM\_EINT Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PSM_EINT	19	DI	Dedicated external interrupt pin. Used to wake up the module from PSM.		

#### Network Status Indication

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
NETLIGHT	16	DO	Network status indication		

#### ADC Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	9	AI	General purpose analog to digital converter interface	Voltage range: 0V~1.4V	

#### Main UART Port

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RXD	18	DI	Receive data from TXD of DTE		1.8V power domain.
TXD	17	DO	Transmit data to RXD of DTE		

#### Auxiliary UART Port

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RXD_AUX	28	DI	Receive data from TXD of DTE		1.8V power domain.
TXD_AUX	29	DO	Transmit data to RXD of DTE		
CTS_AUX*	22	DO	Clear to send		
RTS_AUX*	23	DI	Request to send		
DCD*	21	DO	Data carrier detection		

#### Debug UART Port

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RXD_DBG	38	DI	Receive data		1.8V power domain.
TXD_DBG	39	DO	Transmit data		

#### Ringing Signal

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RI	20	DO	Ring indication signal		1.8V power domain.

#### USIM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SIM_VDD	14	DO	USIM card power supply	V <sub>norm</sub> =1.8V	
SIM_RST	12	DO	USIM card reset signal	V <sub>OL</sub> max=0.15×SIM_VDD V <sub>OH</sub> min=0.85×SIM_VDD	
SIM_DATA	11	IO	USIM card data signal	V <sub>IL</sub> max=0.25×SIM_VDD V <sub>IH</sub> min=0.75×SIM_VDD V <sub>OL</sub> max=0.15×SIM_VDD V <sub>OH</sub> min=0.85×SIM_VDD	
SIM_CLK	13	DO	USIM card clock signal	V <sub>OL</sub> max=0.15×SIM_VDD V <sub>OH</sub> min=0.85×SIM_VDD	
SIM_GND	10	GND	Specified ground for USIM card		

#### Antenna Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RF_ANT	35	IO	RF antenna interface		50Ω characteristic impedance.

### GPIO Interfaces

GPIO0	8	IO	General purpose Input/output interfaces	1.8V power domain.
GPIO1	26	IO		
GPIO2	30	IO		
GPIO3	31	IO		
GPIO4	32	IO		
GPIO5	33	IO		
GPIO6	52	IO		
GPIO7	53	IO		
GPIO8	54	IO		

### SPI Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_MISO	3	DI	Master input slave output of SPI interface		1.8V power domain.
SPI_MOSI	4	DO	Master output slave input of SPI interface		
SPI_SCLK	5	DO	Serial clock signal of SPI interface		
SPI_CS	6	DO	Chip selection of SPI interface		

### USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_MODE	47	DI	Pull down the pin to achieve USB download function		1.8V power domain.
VUSB_3V3	49	PI	USB power supply	Vnorm=3.3V	
USB_DP	50	IO	USB differential data (+)		Conform to USB 1.1 specifications. Request 90 $\Omega$ differential impedance.
USB_DM	51	IO	USB differential data (-)		

#### Reserved Pins

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESERVED	2, 25, 44~46, 48, 55~58				Keep these pins unconnected.

#### NOTE

“(\*)” means under development.

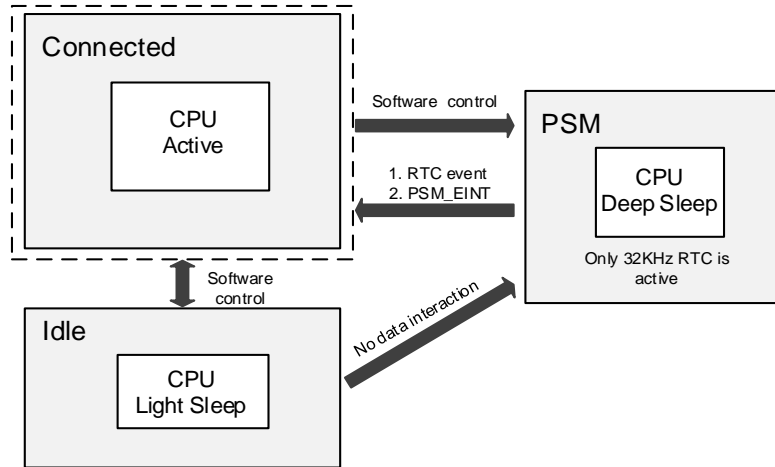
BC66-OpenCPU provides 23 GPIOs, some of which can be multiplexed into other functions. When the default function is not used, the corresponding pin can be configured into GPIO. For details about multiplexed pins, please refer to **Appendix B**.

## 3.4. Operating Modes

The following table briefly describes the three operating modes of the module.

**Table 5: Overview of Operating Modes**

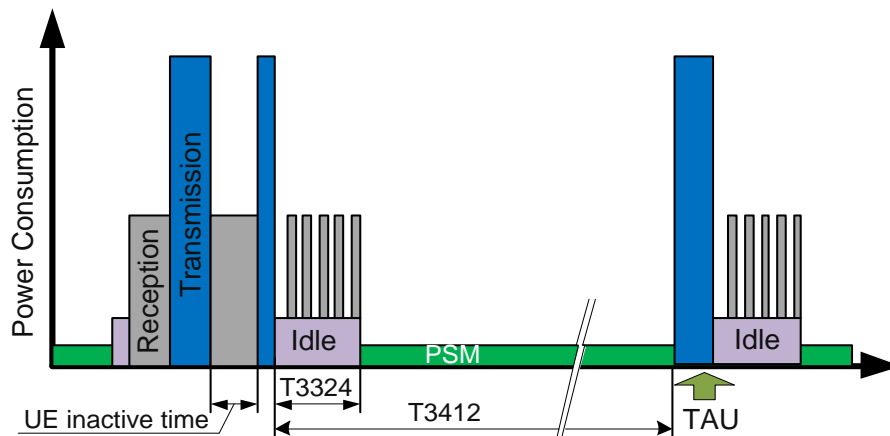
Mode	Description of Operating Modes	
Normal Operation	Connected	In connected mode, the module is in “Active” status. All functions of the module are available and all processors are active; radio transmission and reception can be performed. Transitions to idle mode or PSM can be initiated in connected mode.
	Idle	In idle mode, the module is in “Light Sleep” status and network connection is maintained in DRX/eDRX state; paging messages can be received. Transitions to connected mode or PSM can be initiated in idle mode.
	PSM	In PSM, the module is in “Deep Sleep” status and only the 32kHz RTC is working. CPU is powered off; the network is disconnected and thus cannot receive downlink data. Transitions to connected mode can be initiated in PSM.



**Figure 3: Module Operating Modes**

### 3.5. Power Saving Mode (PSM)

Based on system performance, the module consumes an ultra-low current (3.5μA typical power consumption) in PSM. PSM is designed to reduce power consumption of the module and improve battery life. The following figure shows the power consumption of the module in different modes.



**Figure 4: Module Power Consumption in Different Modes**

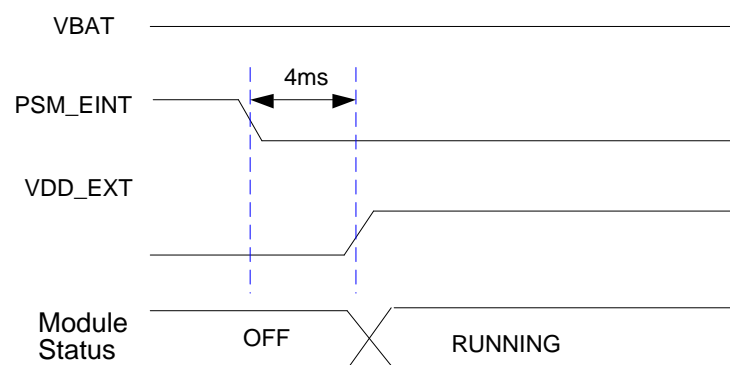
The procedure for entering PSM is as follows: the module requests to enter PSM in “ATTACH REQUEST” message during attach/TAU (Tracking Area Update) procedure. Then the network accepts the request and provides an active time value (T3324) to the module and the mobile reachable timer starts. When the T3324 timer expires, the module enters PSM for duration of T3412 (periodic TAU timer). Please note that

the module cannot request PSM when it is establishing an emergency attachment or initializing the PDN (Public Data Network) connection.

When the module is in PSM, it cannot be paged and stops access stratum activities such as cell reselection, but T3412 is still active.

Either of the following methods can make the module exit from PSM:

- After the T3412 timer expires, the module will exit PSM automatically.
- Pulling down PSM\_EINT (falling edge) will wake the module up from PSM. The timing of waking up the module from PSM is illustrated below.



**Figure 5: Timing of Waking up Module from PSM**

**NOTE**

Among all GPIO interrupts, only the dedicated external interrupt pin PSM\_EINT can successfully wake up the module from PSM. The module cannot be woken up by any other general purpose GPIO interrupts.

## 3.6. Power Supply

### 3.6.1. Power Supply Pins

BC66-OpenCPU provides two VBAT pins for connection with an external power supply. The table below describes the module's VBAT and ground pins.

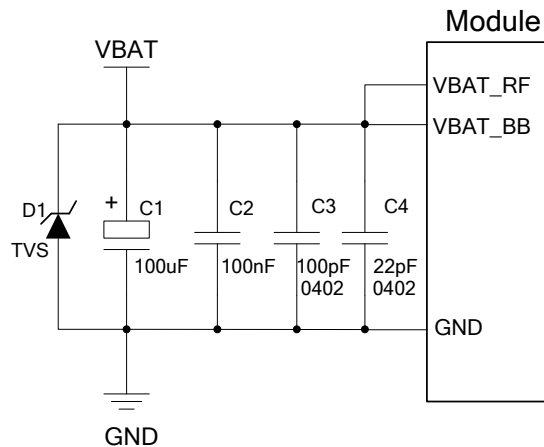
**Table 6: Power Supply Pins**

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_BB	42	Power supply for the module's baseband part	2.1	3.3	3.63	V
VBAT_RF	43	Power supply for the module's RF part	2.1	3.3	3.63	V
GND	1, 27, 34, 36, 37, 40, 41	GND				

### 3.6.2. Reference Design for Power Supply

Power design for a module is critical to its performance. It is recommended to use a low quiescent current LDO with output current capacity of 0.5A as the power supply for the module. A Li-MnO<sub>2</sub>/2S alkaline battery can also be used as the power supply. The supply voltage of the module ranges from 2.1V to 3.63V. When the module is working, please make sure its input voltage will never drop below 2.1V, otherwise the module will be abnormal.

For better power performance, it is recommended to place a 100uF tantalum capacitor with low ESR (ESR=0.7Ω) and three ceramic capacitors (100nF, 100pF and 22pF) near the VBAT pins. Also, it is recommended to add a TVS diode on the VBAT trace (near VBAT pins) to improve surge voltage withstand capability. In principle, the longer the VBAT trace is, the wider it should be. A reference circuit for power supply is illustrated in the following figure.



**Figure 6: Reference Circuit for Power Supply**

#### NOTE

During the module's power-on or reset, an instantaneous current of 700mA will be generated for a period

of 200us. To decrease the current, it is recommended to connect a large-capacitance capacitor to VBAT. If the load capacity of power supply is insufficient, then a 100uF tantalum capacitor is recommended.

## 3.7. Power on/off Scenarios

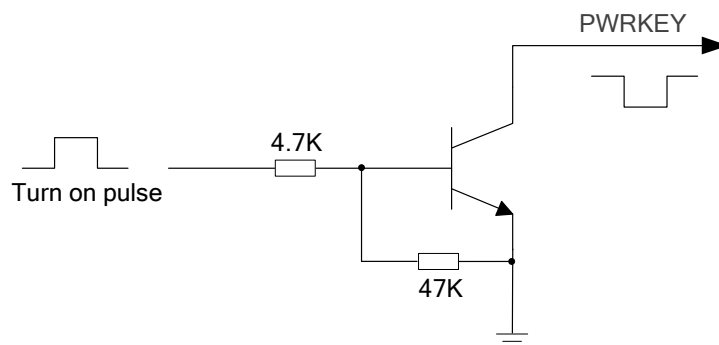
### 3.7.1. Turn on

BC66-OpenCPU can be turned on by driving the PWRKEY pin to a low level voltage for at least 500ms.

**Table 7: PWRKEY Pin**

Pin Name	Pin No.	Description	PWRKEY Pull-down Time
PWRKEY	7	Pull down PWRKEY to turn on the module	≥500ms

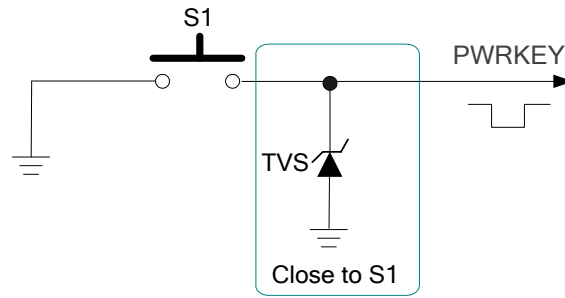
It is recommended use an open drain/collector driver to control the PWRKEY. A simple reference design is illustrated in the following figure.



**Figure 7: Turn on the Module Using Driving Circuit**

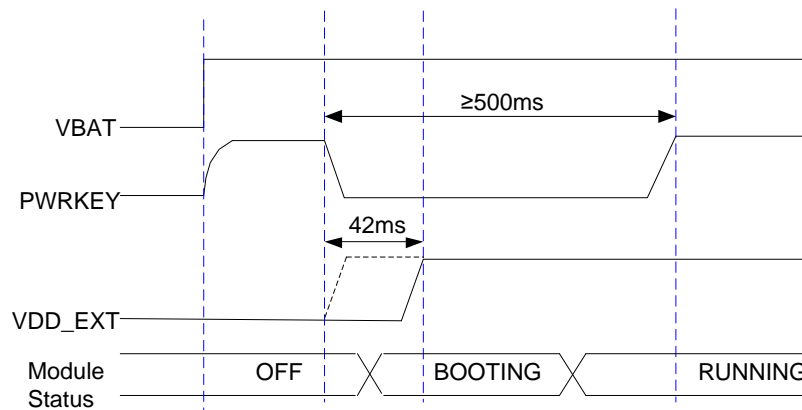
Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference design is shown in the following figure.





**Figure 8: Turn on the Module Using Keystroke**

The power on timing is illustrated in the following figure.



**Figure 9: Power on Timing**

**NOTE**

PWRKEY cannot be pulled down all the time, otherwise the module will not be able to enter into PSM.

### 3.7.2. Turn off

BC66-OpenCPU can be turned off through any of the following methods:

- Turn off the module by **AT+QPOWD=0**.
- In emergent conditions, the module can be powered off through disconnecting VBAT power supply.
- The module will be powered off automatically when VBAT drops below 2.1V.

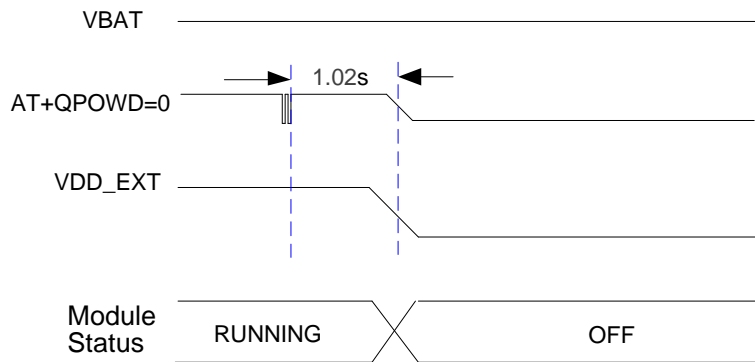


Figure 10: Power off Timing (Turn off by AT Command)

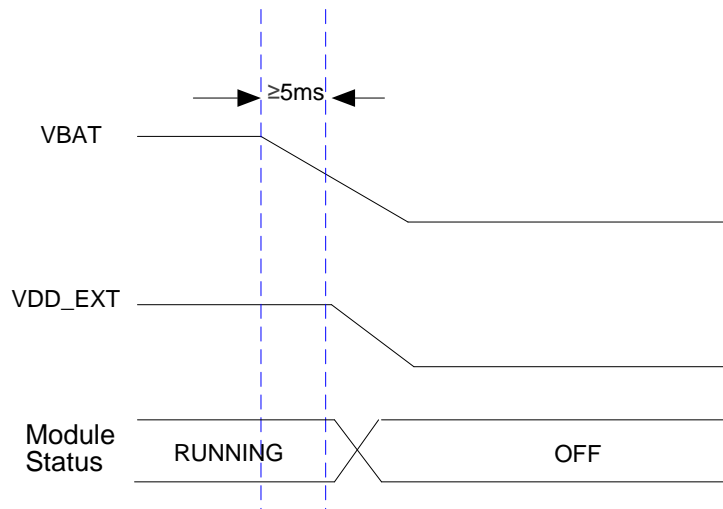


Figure 11: Power off Timing (Power off by Disconnecting VBAT)

### 3.7.3. Reset the Module

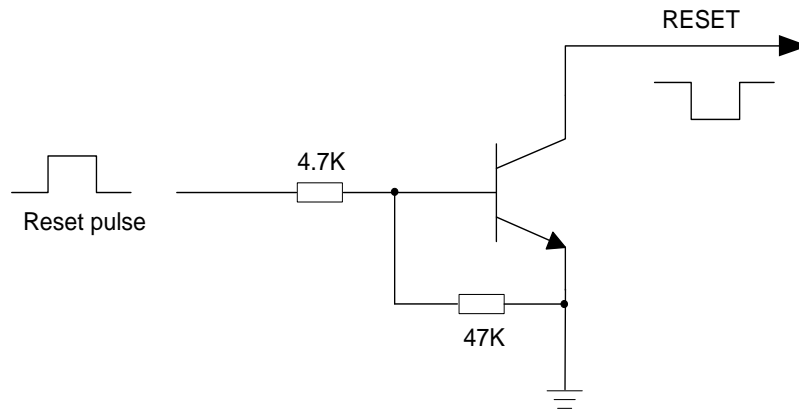
Driving the RESET pin to a low level voltage for at least 50ms will reset the module.

Table 8: Reset Pin

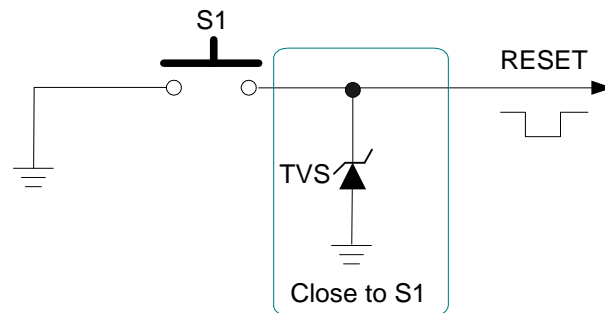
Pin Name	Pin No.	Description	Reset Pull-down Time
RESET	15	Reset the module. Active low.	≥50ms

The recommended circuits of resetting the module are shown below. An open drain/collector driver or

button can be used to control the RESET pin.

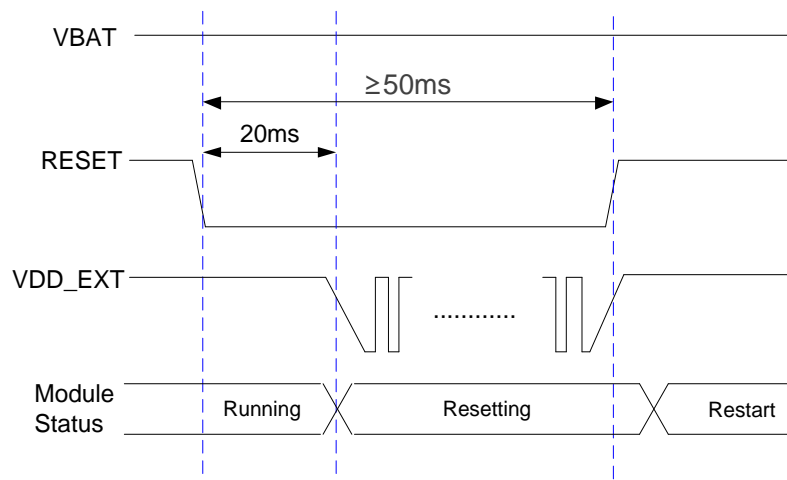


**Figure 12: Reference Design of RESET with a Driving Circuit**



**Figure 13: Reference Design of RESET with a Button**

The reset timing is illustrated in the following figure.



**Figure 14: Reset Timing**

### 3.8. USB Interface

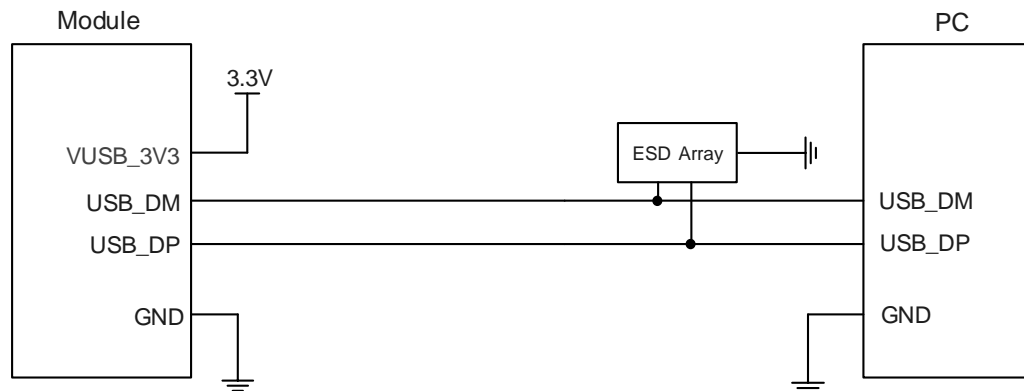
The USB interface of BC26-OpenCPU module conforms to USB 1.1 specifications and supports full speed (12Mbps) mode. The interface can be used for software debugging and software upgrading, and supports USB serial driver under Windows/Linux operating systems.

The following table is the pin definition of USB interface:

**Table 9: Pin Definition of USB Interface**

Pin Name	Pin No.	I/O	Description	Note
USB_MODE	47	DI	Pull down the pin to achieve USB download function	1.8V power domain.
VUSB_3V3	49	PI	USB power supply	Vnorm=3.3V
USB_DP	50	IO	USB differential data (+)	Conform to USB 1.1 specifications.
USB_DM	51	IO	USB differential data (-)	Require 90Ω differential impedance.

The following is a reference design of USB interface:



**Figure 15: USB Interface Reference Design**

In the circuit design of USB interface, in order to ensure the performance of USB, the following principles are suggested in the circuit design:

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.

- Do not route signal traces under power supply, RF signal traces and other sensitive signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 3pF.
- Keep the ESD protection components as close to the USB connector as possible.

#### NOTES

1. USB\_MODE must be pulled down so as to realize USB download function.
2. When the USB interface is used for log capturing, the module will not be able to enter PSM.
3. When using USB function of the module, an external 3.3V power supply should be provided.

## 3.9. UART Interfaces

The module provides three UART ports: main UART port, debug UART port and auxiliary UART port. The module is designed as DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection.

**Table 10: Pin Definition of UART Interfaces**

Interface	Pin Name	Pin No.	Description	Comment
Main UART Port	TXD	17	Transmit data to RXD of DTE	
	RXD	18	Receive data from TXD of DTE	
Debug UART Port	RXD_DBG	38	Receive data from TXD of DTE	
	TXD_DBG	39	Transmit data to RXD of DTE	
Auxiliary UART Port	RXD_AUX	28	Receive data from TXD of DTE	1.8V power domain
	TXD_AUX	29	Transmit data to RXD of DTE	
	CTS_AUX*	22	Clear to send (connect to CTS of DTE)	
	RTS_AUX*	23	Request send data (connect to RTS of DTE)	
	DCD*	21	Data carrier detection	
Ringin Signal	RI	20	Ring indication signal	

**NOTE**

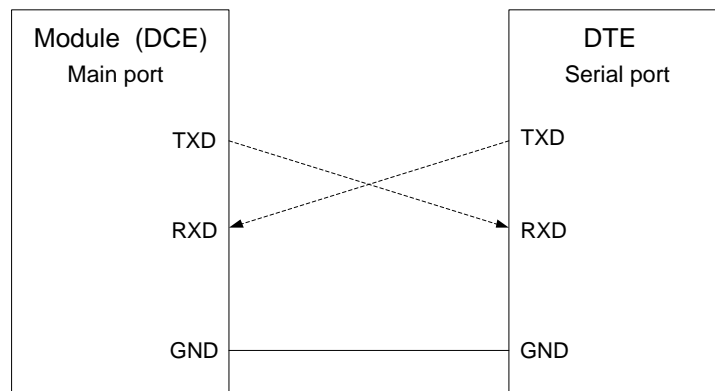
“\*” means under development.

### 3.9.1. Main UART Port

The main UART port supports AT command communication, data transmission and firmware upgrade.

- By default, the module is in auto-baud mode and it supports automatic baud rates not exceeding 115200bps. When powering on the module, the MCU has to send **AT** command consecutively to synchronize baud rate with the module. When **OK** is returned, it indicates the baud rate has been synchronized successfully. When the module is woken up from PSM or idle mode, the baud rate synchronized during start-up will be used directly.
- When the port is used for firmware upgrade, the baud rate is 921600bps by default.

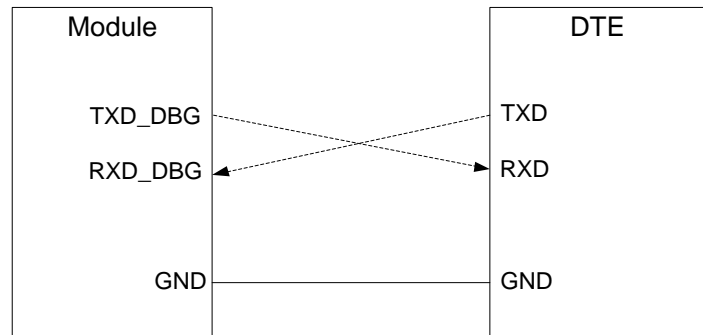
The figure below shows the connection between DCE and DTE.



**Figure 16: Reference Design of Main UART Port**

### 3.9.2. Debug UART Port

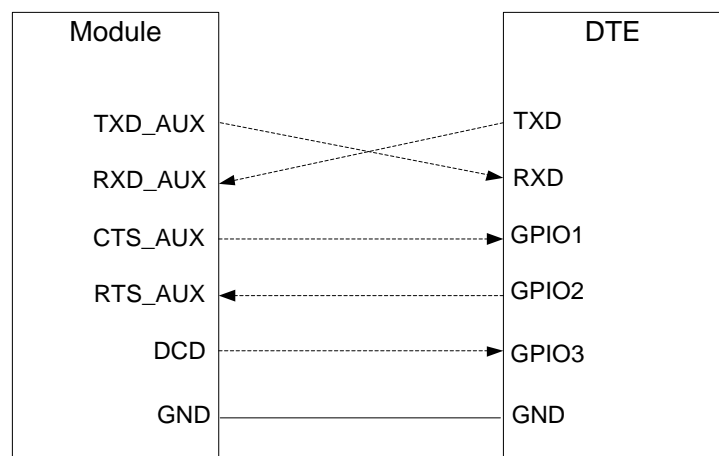
Through debug tools, the debug UART port can be used to output logs for firmware debugging. Its baud rate is 115200bps by default. The following is a reference design of debug UART port.



**Figure 17: Reference Design of Debug UART Port**

### 3.9.3. Auxiliary UART Port

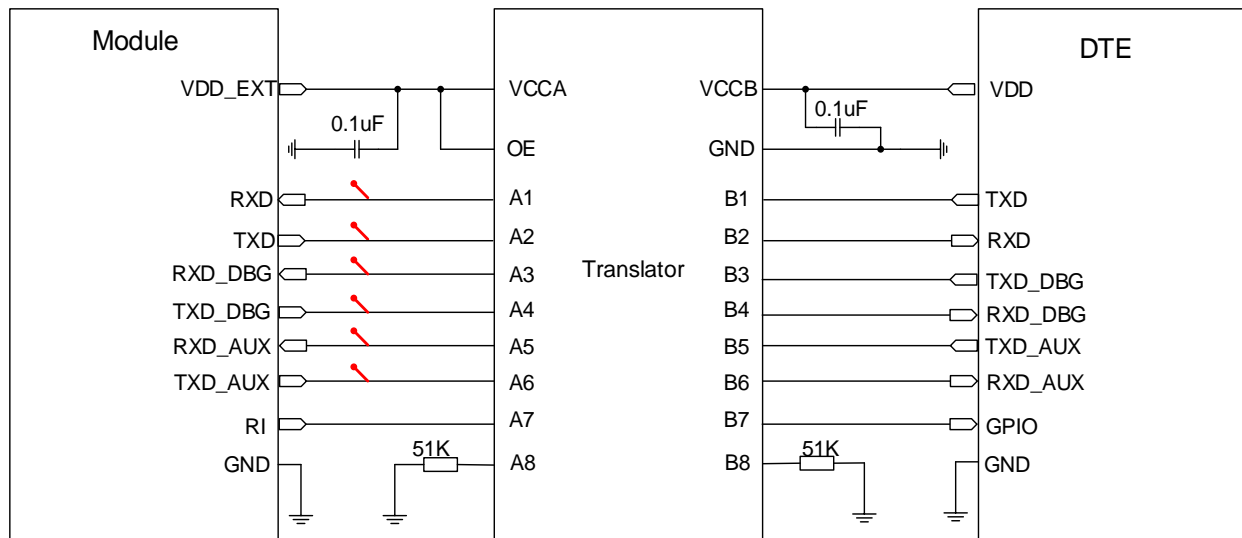
The auxiliary UART port is designed as a general purpose UART for communication with DTE. It also supports log output for firmware debugging, and hardware flow control\*. Its baud rate is 115200bps by default. The following is a reference design of auxiliary UART port.



**Figure 18: Reference Design of Auxiliary UART Port**

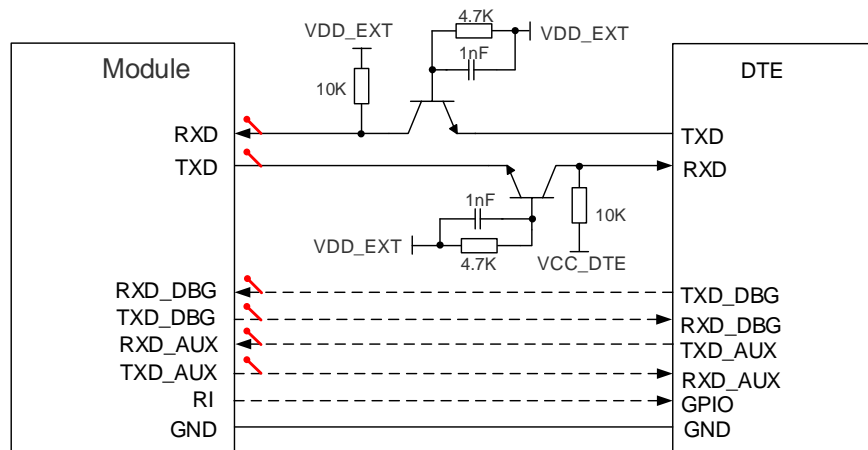
### 3.9.4. UART Application

The module provides 1.8V UART interfaces. A level translator should be used if the application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* (please visit <http://www.ti.com> for more information) is recommended. The following figure shows a reference design.



**Figure 19: Reference Circuit with Voltage Level Translator Chip**

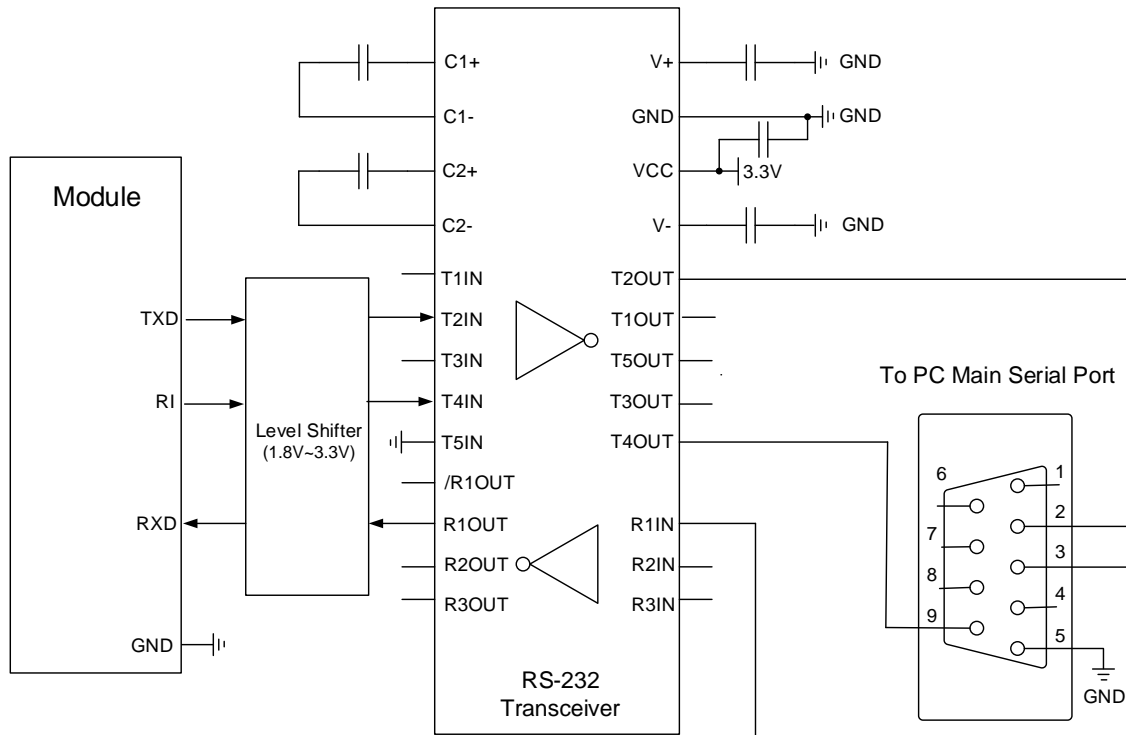
Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.



**Figure 20: Reference Circuit with Transistor Circuit**

The following circuit shows a reference design for the communication between the module and a PC with standard RS-232 interface. Please make sure the I/O voltage of level shifter which connects to module is 1.8V.






**Figure 21: Sketch Map for RS-232 Interface Match**

Please visit vendors' websites to select a suitable RS-232 transceiver, such as: <http://www.exar.com> and <http://www.maximintegrated.com>.

#### NOTES

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
2. In the above voltage level translation reference circuits, the circuit design for DCD and CTS\_AUX is similar to that of TXD\_AUX, and the design for RTS\_AUX is similar to that of RXD\_AUX.
3. “” represents the test point of UART interfaces. It is recommended to reserve the test points of VBAT and PWRKEY, for convenient firmware upgrade and debugging when necessary.

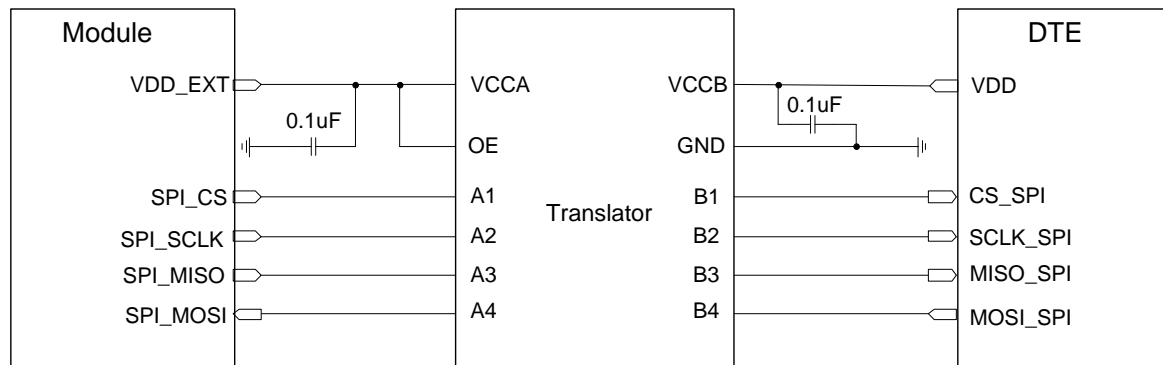
### 3.10. SPI Interface

BC66-OpenCPU provides one SPI master interface. The following table shows the pin definition of SPI interface.

**Table 11: Pin Definition of SPI Interface**

Pin Name	Pin No.	I/O	Description	Comment
SPI_MISO	3	DI	Master input slave output of SPI interface	1.8V power domain
SPI_MOSI	4	DO	Master output slave input of SPI interface	
SPI_SCLK	5	DO	Clock signal of SPI interface	
SPI_CS	6	DO	Chip selection of SPI interface	

The module provides a 1.8V SPI interface. A level translator between the module and host should be used if the application is equipped with a 3.3V processor or device interface. A voltage level translator that supports SPI data rate is recommended. The following figure shows a reference design.



**Figure 22: Reference Design of SPI Interface with a Translator Chip**

### 3.11. USIM Interface

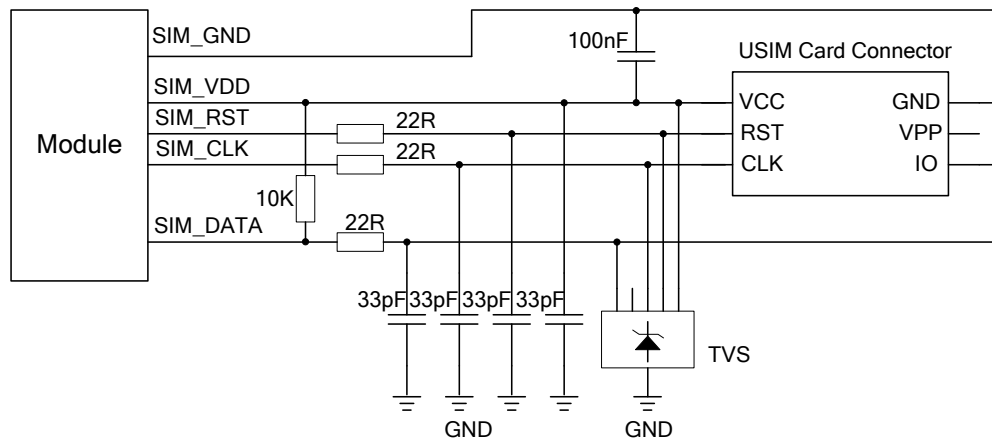
The module provides a USIM interface compliant to ISO/IEC 7816-3, enabling the module to access to external USIM cards.

The external USIM card is powered by an internal regulator in the module and supports 1.8V power supply.

**Table 12: Pin Definition of USIM Interface**

Pin Name	Pin No.	Description	Comment
SIM_VDD	14	Power supply for USIM card	Voltage accuracy: $1.8V \pm 5\%$ . Maximum supply current: about 60mA.
SIM_CLK	13	Clock signal of USIM card	
SIM_DATA	11	Data signal of USIM card	
SIM_RST	12	Reset signal of USIM card	
SIM_GND	10	Specified ground for USIM card	

A reference design for USIM interface with a 6-pin USIM card connector is illustrated below.



**Figure 23: Reference Design of USIM Interface with a 6-pin USIM Card Connector**

For more information of USIM card connector, please visit <http://www.amphenol.com> or <http://www.molex.com>.

In order to enhance the reliability and availability of USIM card in application, please follow the criteria below in USIM circuit design:

- Keep the placement of USIM card connector as close as possible to the module. Keep the trace length as less than 200mm as possible.
- Keep USIM card signals away from RF and VBAT traces.
- Assure the trace between the ground of module and that of USIM card connector is short and wide. Keep the trace width of ground no less than 0.5mm to maintain the same electric potential. The decouple capacitor between SIM\_VDD and GND should be not more than  $1\mu F$  and be placed close to the USIM card connector.
- To avoid cross talk between SIM\_DATA and SIM\_CLK, keep them away from each other and shield them separately with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array. For more

information of TVS diode, please visit <http://www.onsemi.com>. The ESD protection device should be placed as close to USIM card connector as possible, and make sure the USIM card signal lines go through the ESD protection device first and then to the module. The 22Ω resistors should be connected in series between the module and the USIM card connector so as to suppress EMI spurious transmission and enhance ESD protection. Please note that the USIM peripheral circuit should be close to the USIM card connector.

- Place the RF bypass capacitors (33pF) close to the USIM card connector on all signal traces to improve EMI suppression.

### 3.12. ADC Interface

The module provides a 10-bit ADC input channel to read the voltage value. The interface is available in active mode only and must be woken up first in sleep modes.

**Table 13: Pin Definition of ADC Interface**

Pin Name	Pin No.	Description	Sample Range
ADC0	9	Analog to digital converter interface	0V ~ 1.4V

## 4 Antenna Interface

The pin 35 is the RF antenna pad. The antenna port has an impedance of 50Ω.

### 4.1. Pin Definition

Table 14: Pin Definition of NB-IoT Antenna Interface

Pin Name	Pin No.	Description
RF_ANT	35	NB-IoT antenna interface
GND	34, 36, 37	Ground

### 4.2. Operating Frequencies

Table 15: Module Operating Frequencies

Frequency Band	Receiving Frequency	Transmitting Frequency
B1	2110MHz~2170MHz	1920MHz~1980MHz
B2	1930MHz~1990MHz	1850MHz~1910MHz
B3	1805MHz~1880MHz	1710MHz~1785MHz
B4	2110MHz~2155MHz	1710MHz~1755MHz
B5	869MHz~894MHz	824MHz~849MHz
B8	925MHz~960MHz	880MHz~915 MHz
B12	729MHz~746MHz	699MHz~716MHz

B13	746MHz~756MHz	777MHz~787MHz
B17	734MHz~746MHz	704MHz~716MHz
B18	860MHz~875MHz	815MHz~830MHz
B19	875MHz~890MHz	830MHz~845MHz
B20	791MHz~821MHz	832MHz~862MHz
B25	1930MHz~1995MHz	1850MHz~1915MHz
B26*	859MHz~894MHz	814MHz~849MHz
B28	758MHz~803MHz	703MHz~748MHz
B66	2110MHz~2200MHz	1710MHz~1780MHz

**NOTE**

“\*” means under development.

### 4.3. RF Antenna Reference Design

BC66-OpenCPU provides an RF antenna pad for external NB-IoT antenna connection.

- The RF trace on host PCB connected to the module's RF antenna pad should be coplanar waveguide or microstrip, whose characteristic impedance should be close to 50Ω.
- BC66-OpenCPU comes with ground pads which are next to the antenna pad in order to give a better grounding.
- In order to achieve better RF performance, it is recommended to reserve a  $\pi$  type matching circuit and place the  $\pi$ -type matching components (R1/C1/C2) as close to the antenna as possible. By default, the capacitors (C1/C2) are not mounted and a 0Ω resistor is mounted on R1.

A reference design of the RF interface is shown as below.

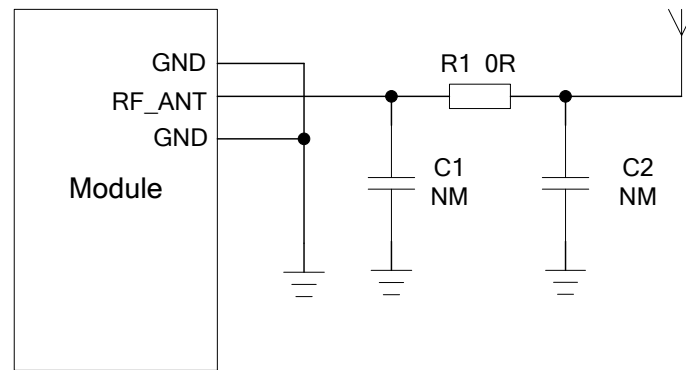


Figure 24: Reference Design of NB-IoT Antenna Interface

#### 4.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as  $50\Omega$ . The impedance of the RF traces is usually determined by the trace width ( $W$ ), the materials' dielectric constant, the distance between signal layer and reference ground ( $H$ ), and the clearance between RF trace and ground ( $S$ ). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures.

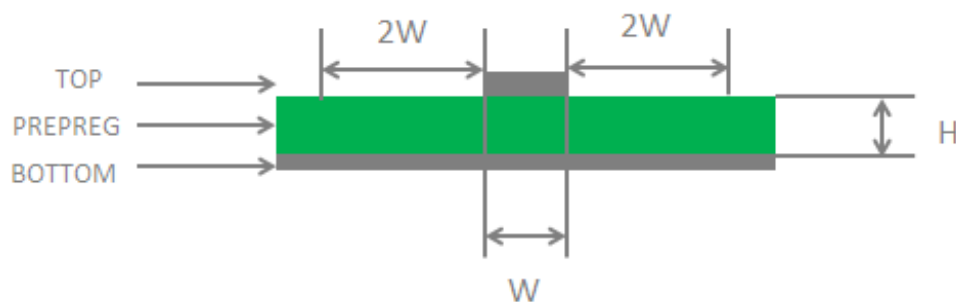


Figure 25: Microstrip Line Design on a 2-layer PCB

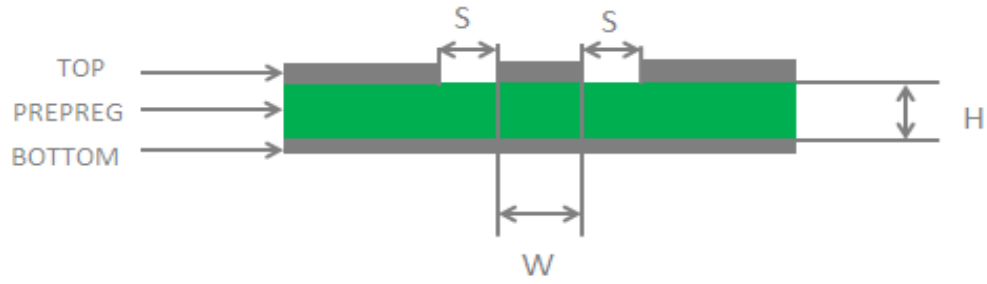


Figure 26: Coplanar Waveguide Line Design on a 2-layer PCB

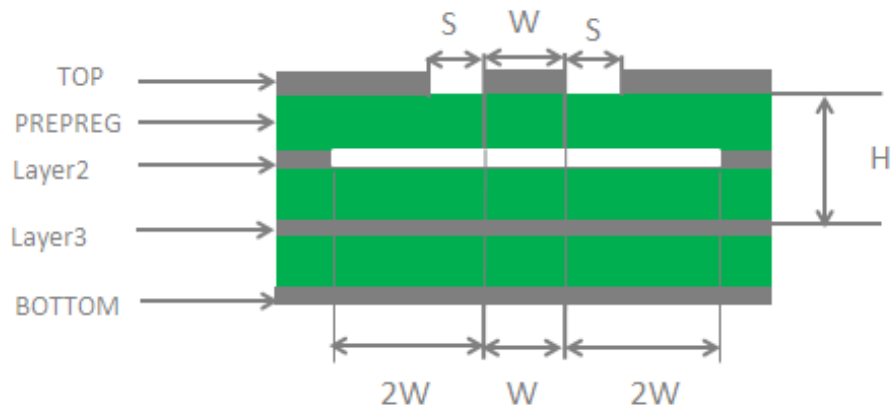


Figure 27: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

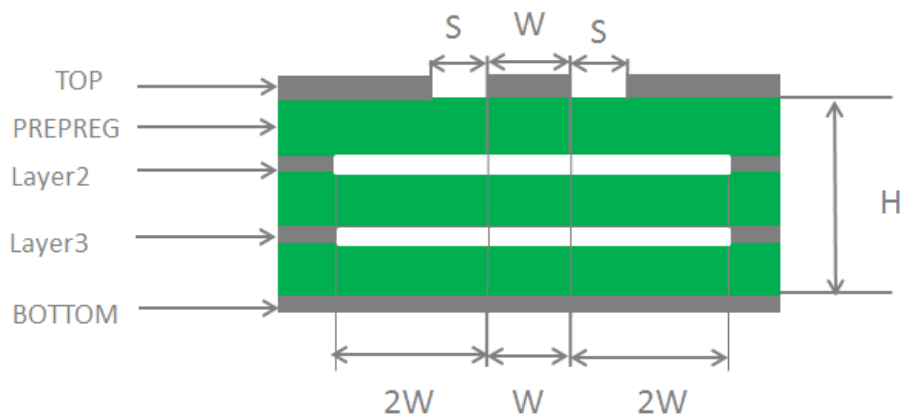


Figure 28: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:



- Use impedance simulation tool to control the characteristic impedance of RF traces as 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2\*W).

For more details, please refer to **document [2]**.

## 4.5. Antenna Requirements

To minimize the loss on RF trace and RF cable, please pay attention to the antenna design. The following tables show the requirements on NB-IoT antenna.

**Table 16: Antenna Cable Insertion Loss Requirements**

Band	Requirements
LTE B5/B8/B12/B13/B17/B18/B19/B20/B26*/B28	Cable Insertion loss <1dB
LTE B1/B2/B3/B4/B25/B66	Cable Insertion loss <1.5dB

### NOTE

“\*” means under development.

**Table 17: Required Antenna Parameters**

Parameters	Requirements
Frequency Range	699MHz~2200MHz
VSWR	≤ 2
Efficiency	> 30%
Max Input Power (W)	50
Input Impedance (Ω)	50

## 4.6. RF Output Power

Table 18: RF Output Power

Frequency Band	Max.	Min.
B1	23dBm±2dB	<-39dBm
B2	23dBm±2dB	<-39dBm
B3	23dBm±2dB	<-39dBm
B4	23dBm±2dB	<-39dBm
B5	23dBm±2dB	<-39dBm
B8	23dBm±2dB	<-39dBm
B12	23dBm±2dB	<-39dBm
B13	23dBm±2dB	<-39dBm
B17	23dBm±2dB	<-39dBm
B18	23dBm±2dB	<-39dBm
B19	23dBm±2dB	<-39dBm
B20	23dBm±2dB	<-39dBm
B25	23dBm±2dB	<-39dBm
B26*	TBD	TBD
B28	23dBm±2dB	<-39dBm
B66	23dBm±2dB	<-39dBm

### NOTES

1. The design conforms to the NB-IoT radio protocols in *3GPP Rel.13* and *3GPP Rel.14*.
2. "\*" means under development.

## 4.7. RF Receiving Sensitivity

Table 19: RF Receiving Sensitivity (with RF Retransmissions)

Frequency Band	Receiving Sensitivity
B1	-129dBm
B2	-129dBm
B3	-129dBm
B4	-129dBm
B5	-129dBm
B8	-129dBm
B12	-129dBm
B13	-129dBm
B17	-129dBm
B18	-129dBm
B19	-129dBm
B20	-129dBm
B25	-129dBm
B26*	TBD
B28	-129dBm
B66	-129dBm

### NOTE

“\*” means under development.

## 4.8. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by *HIROSE*.

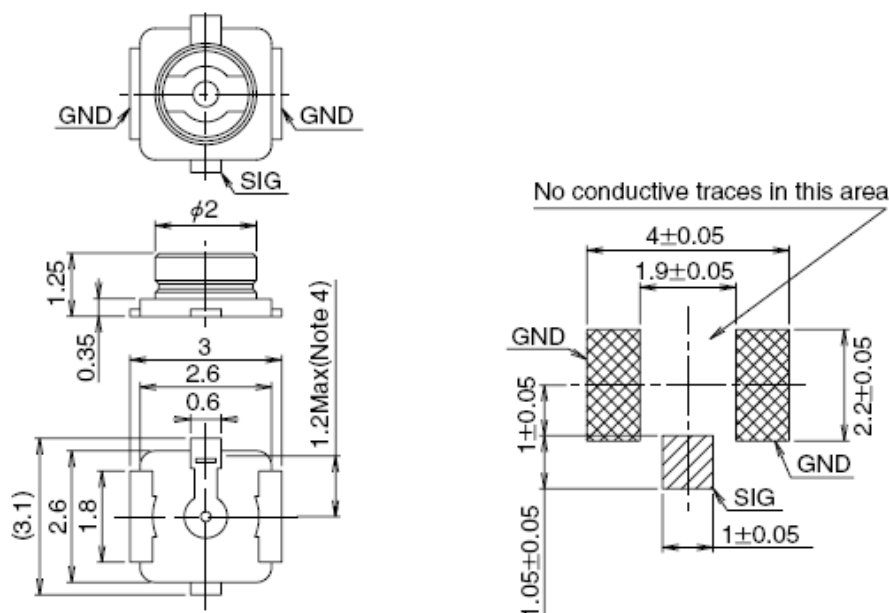


Figure 29: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 30: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

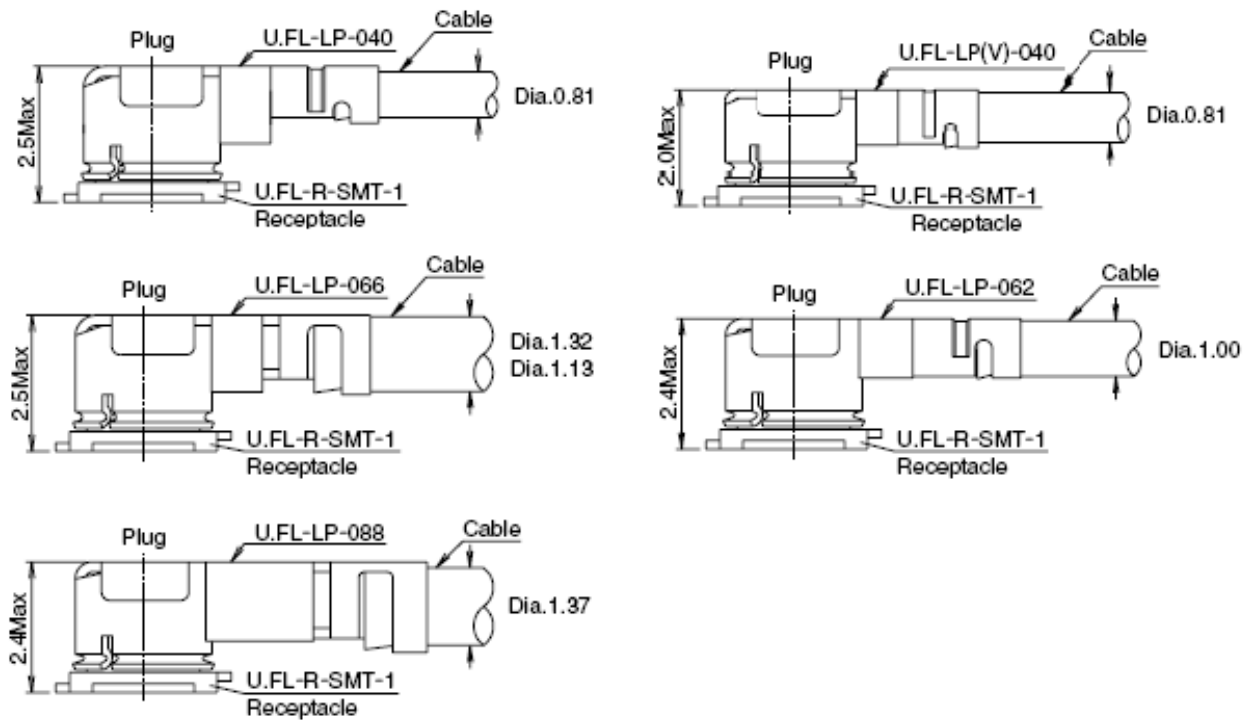


Figure 28: Space Factor of Mated Connector (Unit: mm)

For more details, please visit <http://www.hirose.com>.

# 5 Electrical and Reliability Characteristics

## 5.1. Operation and Storage Temperatures

The following table lists the operation and storage temperatures of the module.

**Table 20: Operation and Storage Temperatures**

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range <sup>1)</sup>	-35	+25	+75	°C
Extended Temperature Range <sup>2)</sup>	-40		+85	°C
Storage Temperature Range	-40		+90	°C

### NOTES

- <sup>1)</sup> Within operation temperature range, the module is 3GPP compliant.
- <sup>2)</sup> Within extended temperature range, the module remains the ability to establish and maintain an SMS\*, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P<sub>out</sub> might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.

## 5.2. Current Consumption

The table below lists the current consumption of BC66-OpenCPU under different states.

**Table 21: Module Current Consumption (3.3V VBAT Power Supply)**

Parameter	Mode	Description	Min.	Ave.	Max. <sup>2)</sup>	Unit
I <sub>VBAT</sub>	PSM	Deep Sleep		3.5		μA
		eDRX=81.92s, PTW=40.96s		288		μA
	Idle	@DRX=1.28s		541		μA
		@DRX=2.56s		434		μA
	Active <sup>1)</sup>	Single-tone (15kHz subcarrier spacing)	B1 @23dBm	100	285	mA
			B2 @23dBm	103	294	mA
			B3 @23dBm	107	308	mA
			B4 @23dBm	107	307	mA
			B5 @23dBm	107	303	mA
			B8 @23dBm	113	325	mA
			B12 @23dBm	134	393	mA
			B13 @23dBm	111	319	mA
			B17 @23dBm	133	392	mA
			B18 @23dBm	110	316	mA
			B19 @23dBm	109	311	mA
			B20 @23dBm	109	301	mA
			B25 @23dBm	103	293	mA
			B26* @23dBm	TBD	TBD	mA
			B28 @23dBm	128	375	mA
			B66 @23dBm	109	312	mA
		Single-tone (3.75kHz subcarrier spacing)	B1 @23dBm	193	302	mA
			B2 @23dBm	187	296	mA
			B3 @23dBm	215	335	mA

Parameter	Mode	Description	Min.	Ave.	Max. <sup>2)</sup>	Unit
		B4 @23dBm		237	311	mA
		B5 @23dBm		215	330	mA
		B8 @23dBm		224	344	mA
		B12 @23dBm		250	395	mA
		B13 @23dBm		203	316	mA
		B17 @23dBm		258	409	mA
		B18 @23dBm		198	313	mA
		B19 @23dBm		198	314	mA
		B20 @23dBm		215	329	mA
		B25 @23dBm		187	297	mA
		B26* @23dBm		200	313	mA
		B28 @23dBm		250	398	mA
		B66 @23dBm		200	316	mA

#### NOTES

- <sup>1)</sup> Power consumption under instrument test condition.
- <sup>2)</sup> The “maximum value” in “Connected” mode refers to the maximum pulse current during RF emission.
- “\*” means under development.

### 5.3. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module’s electrostatic discharge characteristics.



**Table 22: Electrostatic Discharge Characteristics (25°C, 45% Relative Humidity)**

Test	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna interface	±5	±10	kV
Other interfaces	±0.5	±1	kV

## 6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimetre (mm), and the tolerances for dimensions without tolerance values are  $\pm 0.05\text{mm}$ .

### 6.1. Mechanical Dimensions of the Module

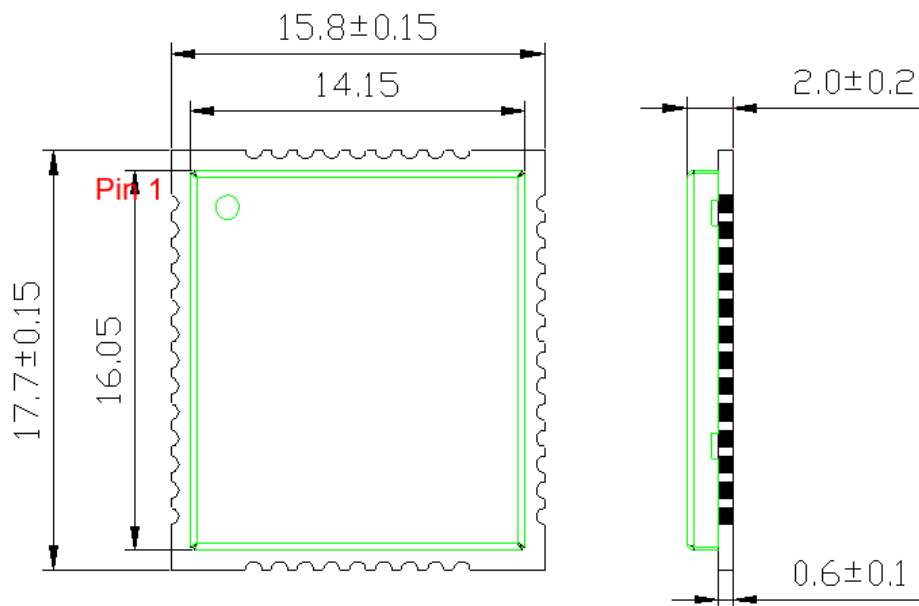


Figure 31: BC66-OpenCPU Top and Side Dimensions (Unit: mm)

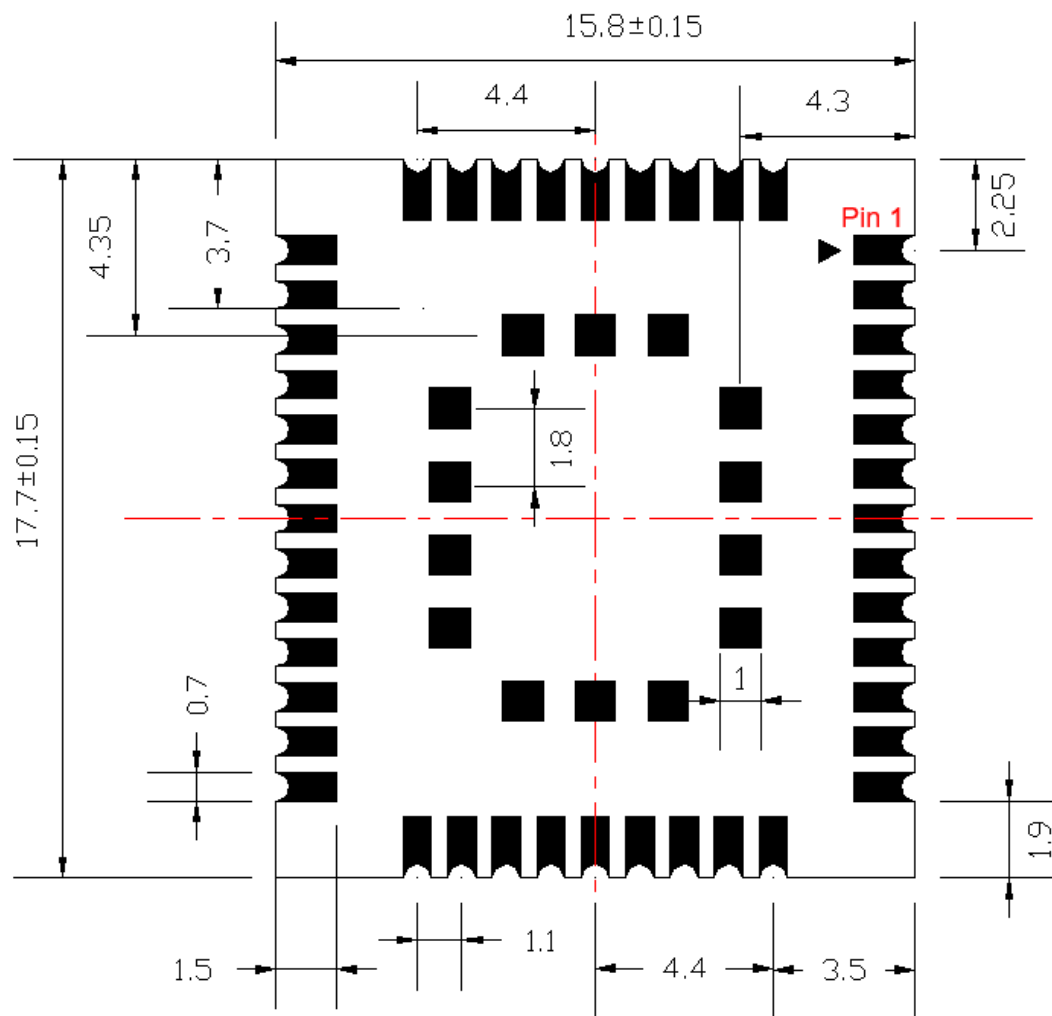


Figure 30: Module Bottom Dimension (Bottom View)

## 6.2. Recommended Footprint

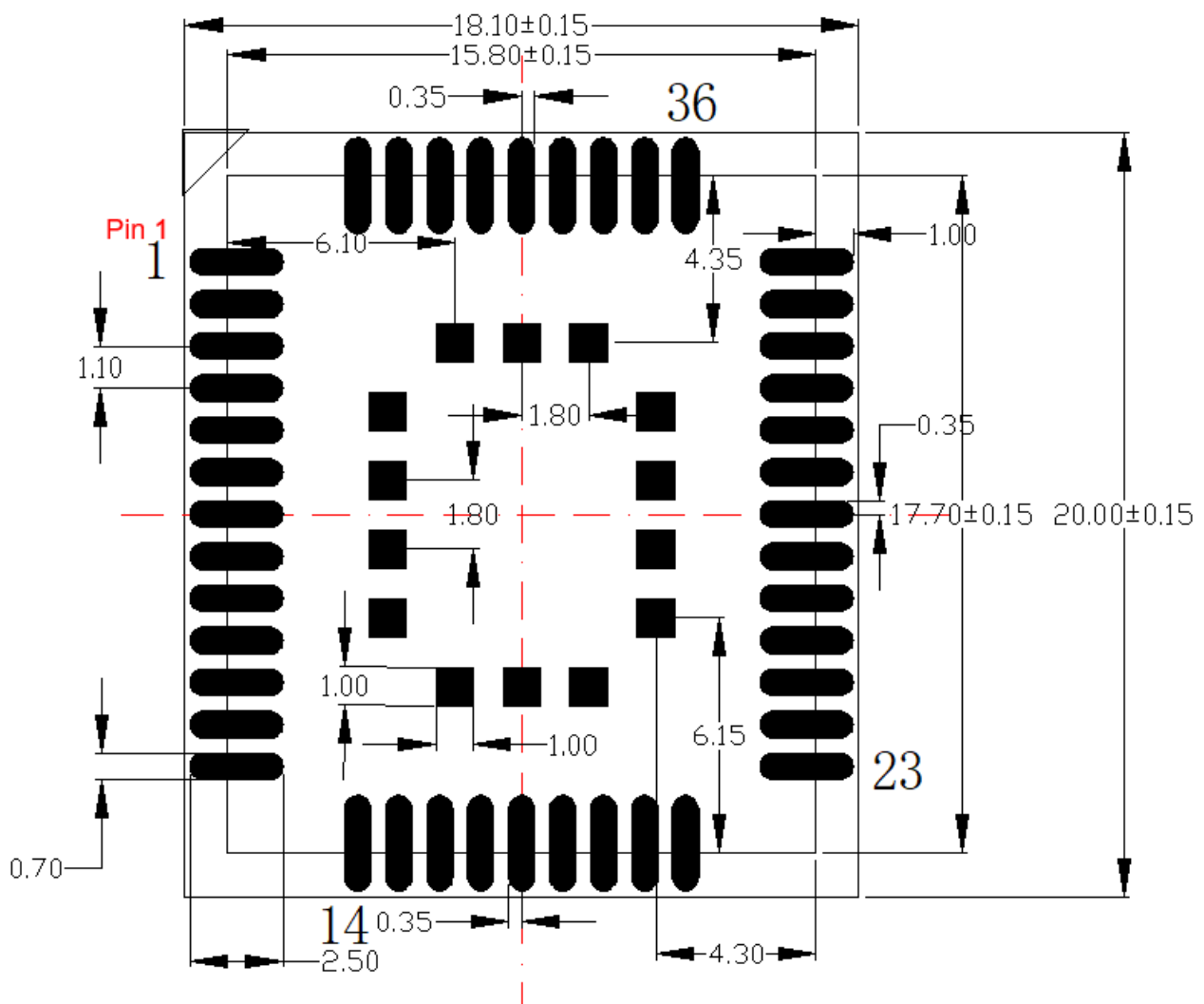


Figure 31: Recommended Footprint (Unit: mm)

### NOTE

The module should be kept about 3mm away from other components on the host PCB.

### 6.3. Top and Bottom Views of the Module



Figure 32: Top View of the Module

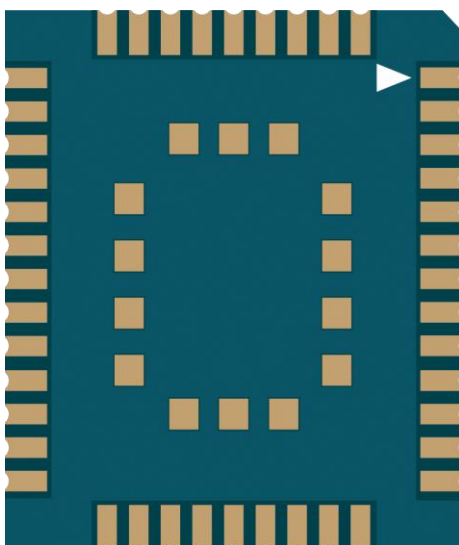


Figure 33: Bottom View of the Module

**NOTE**

These are renderings of BC66-OpenCPU module. For authentic dimension and appearance, please refer to the module that you receive from Quectel.

# 7 Storage, Manufacturing and Packaging

## 7.1. Storage

BC66-OpenCPU module is stored in a vacuum-sealed bag. It is rated at MSL 3, and storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40°C/90%RH.
2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
  - Mounted within 168 hours at the factory environment of ≤30°C/60%RH.
  - Stored at <10%RH.
3. Devices require baking before mounting, if any circumstance below occurs.
  - When the ambient temperature is 23°C±5°C and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
  - Device mounting cannot be finished within 168 hours at factory conditions of ≤30°C/60%.
4. If baking is required, devices may be baked for 8 hours at 120°C±5°C.

### NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120°C) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

## 7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm~0.20mm. For more details, please refer to **document [3]**.

It is suggested that the peak reflow temperature is 238~245°C, and the absolute maximum reflow temperature is 245°C. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

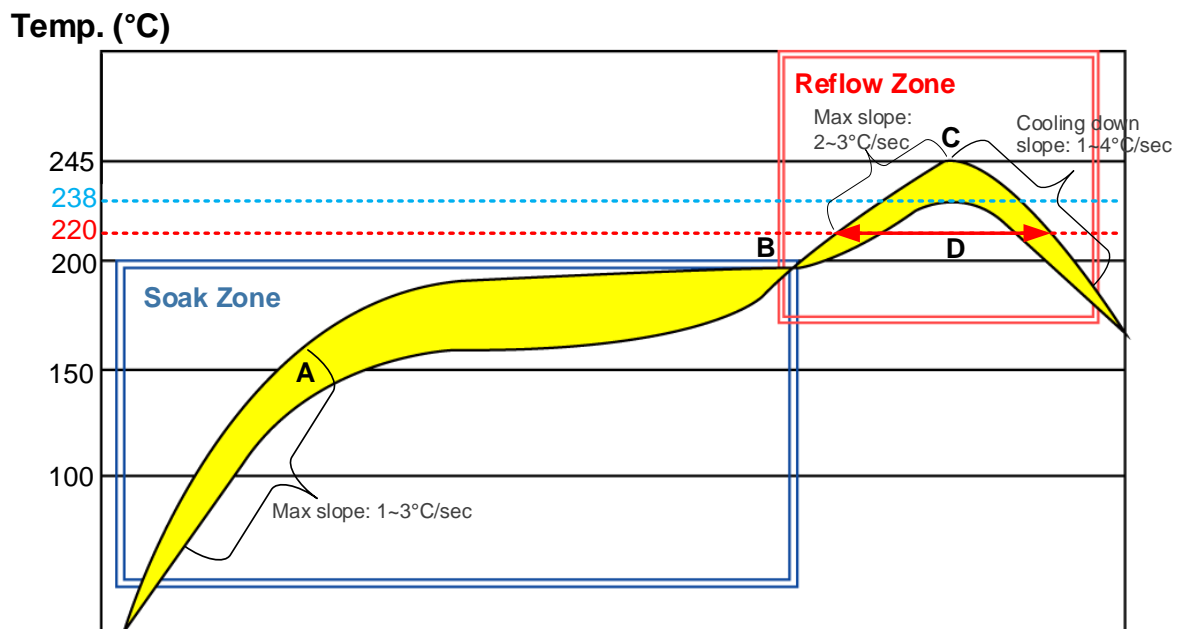


Figure 34: Recommended Reflow Soldering Thermal Profile

Table 23: Recommended Thermal Profile Parameters

Factor	Recommendation
<b>Soak Zone</b>	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec

Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

#### NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.

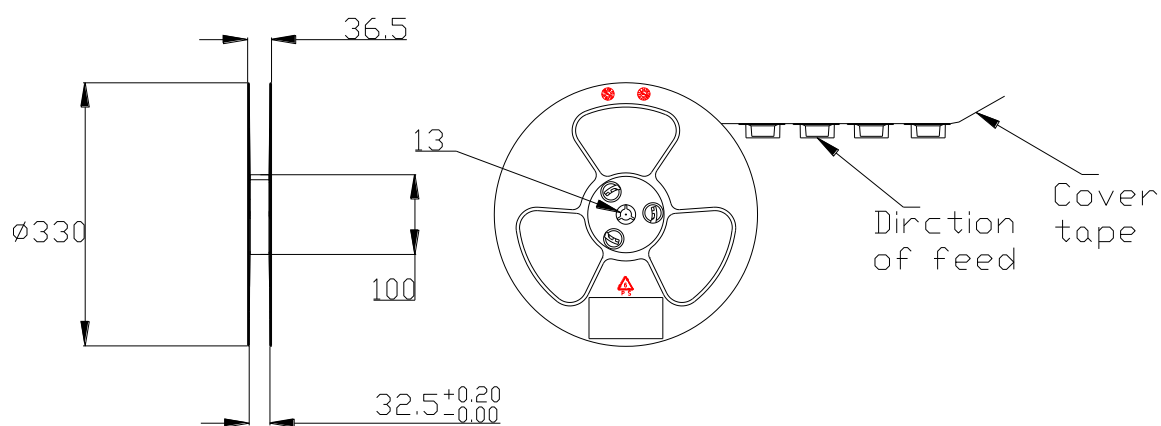
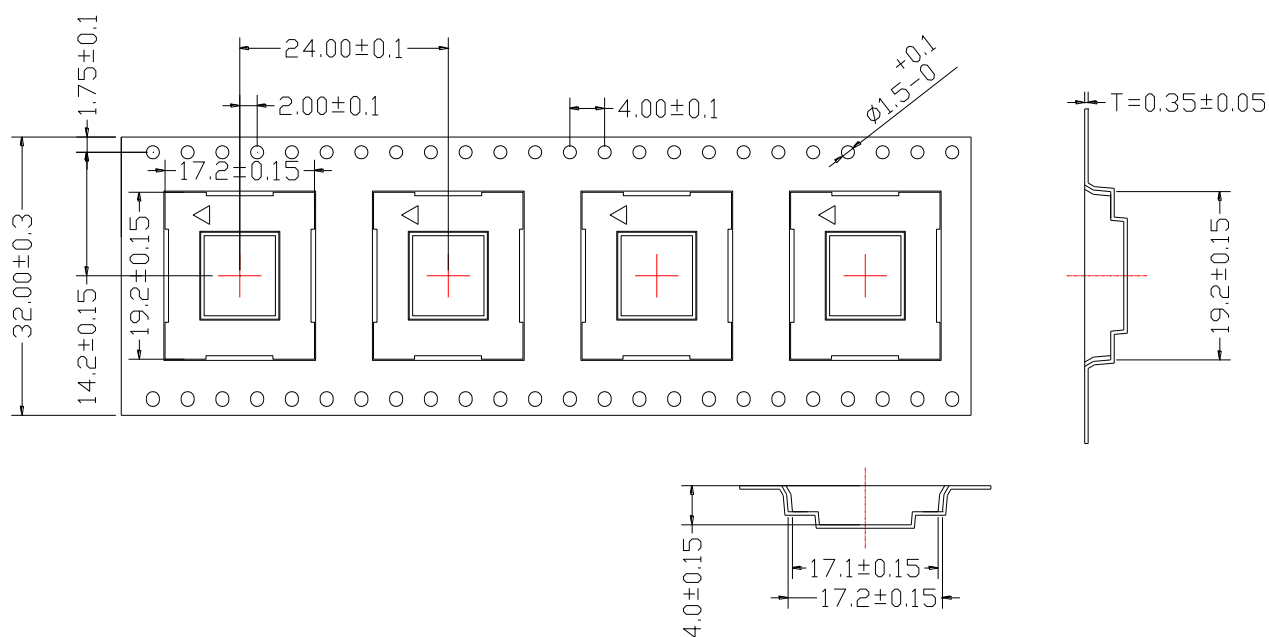
## 7.3. Packaging

The modules are stored in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

### 7.3.1. Tape and Reel Packaging

The reel is 330mm in diameter and each reel contains 250 modules.





## 8 Appendix A References

**Table 24: Related Documents**

SN	Document Name	Remark
[1]	Quectel_BC66-TE-B_User_Guide	BC66-TE-B User Guide
[2]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[3]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide

**Table 25: Terms and Abbreviations**

Abbreviation	Description
ADC	Analog-to-Digital Converter
CoAP	Constrained Application Protocol
DCE	Data Communications Equipment (typically module)
DTE	Data Terminal Equipment (typically computer, external controller)
DTLS	Datagram Transport Layer Security
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FTP	File Transfer Protocol
H-FDD	Half Frequency Division Duplexing
HTTP	Hyper Text Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
I/O	Input/Output
kbps	Kilo Bits Per Second

LED	Light Emitting Diode
Li-MnO <sub>2</sub>	Lithium-manganese Dioxide
Li-2S	Lithium Sulfur
LTE	Long Term Evolution
LwM2M	Lightweight M2M
MQTT	Message Queuing Telemetry Transport
NB-IoT	Narrow Band- Internet of Things
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PSM	Power Save Mode
RF	Radio Frequency
RTC	Real Time Clock
RXD	Receive Data
SMS	Short Message Service
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TE	Terminal Equipment
TXD	Transmitting Data
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
URC	Unsolicited Result Code
USIM	Universal Subscriber Identification Module
VSWR	Voltage Standing Wave Ratio
V <sub>max</sub>	Maximum Voltage Value

V <sub>norm</sub>	Normal Voltage Value
V <sub>min</sub>	Minimum Voltage Value
V <sub>IHmax</sub>	Maximum Input High Level Voltage Value
V <sub>IHmin</sub>	Minimum Input High Level Voltage Value
V <sub>ILmax</sub>	Maximum Input Low Level Voltage Value
V <sub>ILmin</sub>	Minimum Input Low Level Voltage Value
V <sub>Imax</sub>	Absolute Maximum Input Voltage Value
V <sub>Inorm</sub>	Absolute Normal Input Voltage Value
V <sub>Imin</sub>	Absolute Minimum Input Voltage Value
V <sub>OHmax</sub>	Maximum Output High Level Voltage Value
V <sub>OHmin</sub>	Minimum Output High Level Voltage Value
V <sub>OLmax</sub>	Maximum Output Low Level Voltage Value
V <sub>OLmin</sub>	Minimum Output Low Level Voltage Value

## 9 Appendix B Multiplexed Pins

Table 26: Multiplexed Pins and Their Functions

Pin No.	Pin Name	Default Mode	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7	Reset State <sup>1)</sup>	Driving Current
3	SPI_MISO	0	GPIO	/	SPI_MISO	/	/	/	/	EINT	I,PD	4mA
4	SPI_MOSI	0	GPIO	/	SPI_MOSI	/	/	/	/	EINT	I,PD	4mA
5	SPI_SCLK	0	GPIO	/	SPI_SCLK	/	/	/	/	EINT	I,PD	4mA
6	SPI_CS	0	GPIO	/	SPI_CS	/	/	/	/	EINT	I,PD	4mA
8	GPIO0	0	GPIO	/	/	/	/	/	/	/	I,PD	4mA
16	NETLIGHT	0	GPIO	/	/	I2S0_RX		PWM	/	EINT	I,PU	4mA
20	RI	0	GPIO	/	/	I2S0_WS	I2C_SCL	/	/	EINT	I,PD	4mA
21	DCD*	0	GPIO	/	/	I2S0_TX	I2C_SDA	/	/	EINT	I,PD	4mA
22	CTS_AUX* <sup>2)</sup>	0	GPIO	/	/	UART1_RTS	/	/	/	EINT	I,PD	4mA
23	RTS_AUX* <sup>2)</sup>	0	GPIO	/	/	UART1_CT	/	PWM/	/	EINT	I,PD	4mA

S												
26	GPIO1	0	GPIO	I2S0_MCLK	/	/	/	/	/	EINT	I,PD	4mA
28	RXD_AUX <sup>3)</sup>	3	GPIO	/	/	UART1_RX D	/	/	/	/	I,PD	4mA
29	TXD_AUX <sup>3)</sup>	3	GPIO	/	/	UART1_TX D	/	/	/	/	I,PD	4mA
30	GPIO2	0	GPIO	I2S0_CK	UART2_CTS	/	/	/	/	EINT	I,PD	4mA
31	GPIO3	0	GPIO	I2S0_WS	UART2_RTS	/	/	PWM		EINT	I,PD	4mA
32	GPIO4	0	GPIO	I2S0_RX	/	/	/	/	/	/	I,PD	4mA
33	GPIO5	0	GPIO	I2S0_TX	/	/	/	/	/	EINT	I,PD	4mA
38	RXD_DBG <sup>3)</sup>	3	GPIO	/	/	UART2_RX D	/	/	/	/	I,PD	4mA
39	TXD_DBG <sup>3)</sup>	5	GPIO	/	/	/	/	UART2_ TXD	/	/	I,PD	4mA
47	USB_MODE	0	GPIO	/	/	/	/	/	/	EINT	I,PU	4mA
52	GPIO6	0	GPIO	/	/	/	/	/	/	/	I,PU	4mA
53	GPIO7	0	GPIO	/	/	/	/	/	/	/	I,PU	4mA
54	GPIO8	0	GPIO	/	/	/	/	/	/	/	I,PU	4mA

## NOTES

1. <sup>1)</sup> Indicates the status of each pin after reset. ("I" means "input "; "PD" means "internal pull-down"; and "PU" means "internal pull-up".)
2. <sup>2)</sup> Pins 22 and 23 have exchanged the pin function inside the module. Therefore, during external circuit design, please connect pin 22 (CTS\_AUX) to CTS of DTE and pin 23 (RTS\_AUX) to RTS of DTE.
3. <sup>3)</sup> Pins 28/29/38/39 are configured as UART pins by default. After power-on, they will change from LOW to HIGH level and then maintain high level status.
4. Except the default mode, the pin functions in other modes take effect only after software configuration.
5. "\*" means under development.