LIS302DL

MEMS motion sensor

3-axis - ± 2g/± 8g smart digital output "piccolo" accelerometer

Feature

- 2.16 V to 3.6 V supply voltage
- <1 mW power consumption
- I2C/SPI digital output interface
- Click and double click recognition
- Embedded self-test
- ECOPACK® RoHS and "Green" compliant
- 1.8 V compatible IOs
- ± 2g/± 8g dynamically selectable full-scale
- Programmable multiple interrupt generator
- Embedded high pass filter
- 10000g high shock survivability

Description

The LIS302DL is an ultra-compact low-power three axes linear accelerometer. It includes a sensing element and an IC interface able to provide the measured acceleration to the external world through I2C/SPI serial interface. The sensing element, capable of detecting the acceleration, is manufactured using a dedicated process developed by ST to produce inertial sensors and actuators in silicon. The IC interface is manufactured using a CMOS process that allows to design a dedicated circuit which is trimmed to better. The LIS302DL has dynamically user selectable full scales of ± 2g/± 8g and it is capable of measuring accelerations with an output data rate of 100 Hz or 400 Hz.

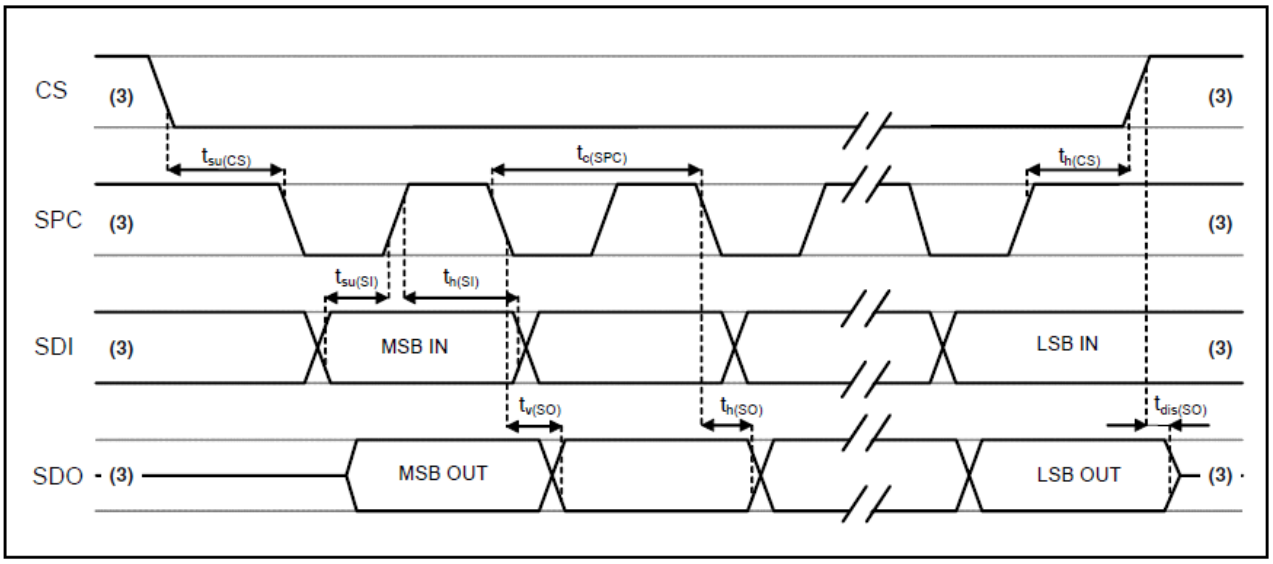
Communication interface characteristics

(Using SPI - Serial Peripheral Interface)

Table 5. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	6		
tdis(SO)	SDO output disable time		50	

Figure 3. SPI slave timing diagram (2)



1. Values are guaranteed at 10MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production
2. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both Input and Output port
3. When no communication is on-going, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors

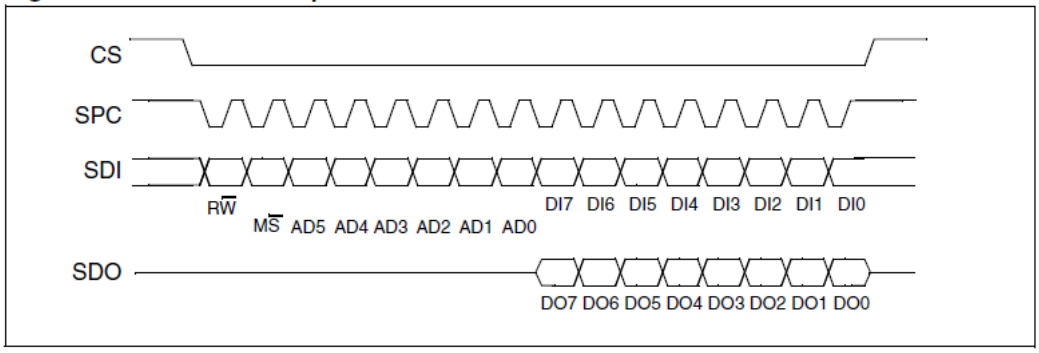
IC interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts into an analog voltage the capacitive unbalancing of the MEMS sensor and by analog-to-digital converters. The acceleration data may be accessed through an I2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller. The LIS302DL features a Data-Ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device. The LIS302DL may also be configured to generate an inertial Wake-Up and Free-Fall interrupt signal accordingly to a programmed acceleration event along the enabled axes. Both Free-Fall and Wake-Up can be available simultaneously on two different pins.

SPI bus interface

The LIS302DL SPI is a bus slave. The SPI allows to write and read the registers of the device. The Serial Interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read & write protocol



CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission).
SDI and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**. Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.
bit 1: MS bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.
bit 2-7: address AD(5:0). This is the address field of the indexed register.
bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When MS bit is 0 the address used to read/write data remains the same for every block. When MS bit is 1 the address used to read/write data is incremented at every block.
The function and the behavior of **SDI** and **SDO** remain unchanged.

Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related address:

Table 16. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (Do not modify)		00-0E			Reserved
Who_Am_I	r	0F	000 1111	00111011	Dummy register
Reserved (Do not modify)		10-1F			Reserved
Ctrl_Reg1	rw	20	010 0000	00000111	
Ctrl_Reg2	rw	21	010 0001	00000000	
Ctrl_Reg3	rw	22	010 0010	00000000	
HP_filter_reset	r	23	010 0011	dummy	Dummy register
Reserved (Do not modify)		24-26			Reserved
Status_Reg	r	27	010 0111	00000000	
--	r	28	010 1000		Not Used
OutX	r	29	010 1001	output	
--	r	2A	010 1010		Not Used
OutY	r	2B	010 1011	output	
--	r	2C	010 1100		Not Used
OutZ	r	2D	010 1101	output	
Reserved (Do not modify)		2E-2F			Reserved
FF_WU_CFG_1	rw	30	011 0000	00000000	
FF_WU_SRC_1(ack1)	r	31	011 0001	00000000	
FF_WU_THS_1	rw	32	011 0010	0000000x	
FF_WU_DURATION_1	rw	33	011 0011	00000000	
FF_WU_CFG_2	rw	34	011 0100	00000000	

Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

• CTRL_REG1 (20h)

Table 18. CTRL_REG1 (20h) register

DR	PD	FS	STP	STM	Zen	Yen	Xen

Table 19. CTRL_REG1 (20h) register description

DR	Data rate selection. Default value: 0 (0: 100 Hz output data rate; 1: 400 Hz output data rate)
PD	Power Down Control. Default value: 0 (0: power down mode; 1: active mode)
FS	Full Scale selection. Default value: 0 (refer to *Table 3* for typical full scale value)
STP, STM	Self Test Enable. Default value: 0 (0: normal mode; 1: self test P, M enabled)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR bit allows to select the data rate at which acceleration samples are produced. The default value is 0 which corresponds to a data-rate of 100Hz. By changing the content of DR to "1" the selected data-rate will be set equal to 400Hz.

PD bit allows to turn on the turn the device out of power-down mode. The device is in powerdown mode when PD= "0" (default value after boot). The device is in normal mode when PD is set to 1.

STP, STM bit is used to activate the self test function. When the bit is set to one, an output change will occur to the device outputs (refer to *Table 3* and *4* for specification) thus allowing to check the functionality of the whole measurement chain.

Zen bit enables the generation of Data Ready signal for Z-axis measurement channel when set to 1. The default value is 1.

Yen bit enables the generation of Data Ready signal for Y-axis measurement channel when set to 1. The default value is 1.

Xen bit enables the generation of Data Ready signal for X-axis measurement channel when set to 1. The default value is 1.

- **OUT_X (29h)**

Table 28. OUT_X (29h) register

XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

X axis output data.

- **OUT_Y (2Bh)**

Table 29. OUT_Y (2Bh) register description

YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

Y axis output data.

- **OUT_Z (2Dh)**

Table 31. FF_WW_CFG_1 (30h) register

AOI	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Z axis output data.

MP45DT02

MEMS audio sensor omnidirectional digital microphone

Features

- Single supply voltage
- 120 dBSPL acoustic overload point
- PDM single-bit output with option for stereo configuration
- ECOPACK®, RoHS, and "Green" compliant
- Low power consumption
- Omnidirectional sensitivity
- HLGA package (SMD-compliant)

Description

The MP45DT02 is a compact, low-power, top-port, omnidirectional, digital MEMS microphone. The MP45DT02 is built with a sensing element and an IC interface with stereo capability. The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process to produce audio sensors. The IC interface is manufactured using a CMOS process that allows designing a dedicated circuit able to provide a digital signal externally in PDM format. The MP45DT02 has an acoustic overload point of 120 dBSPL with a best on the market 61 dB signal-to-noise ratio and -26 dB sensitivity. The MP45DT02 is available in an SMD-compliant package and is guaranteed to operate over an extended temperature range from -30 °C to +85 °C. The MP45DT02's digital output and package size (1.25 mm thick) make this device the best solution for laptop and portable computing applications.

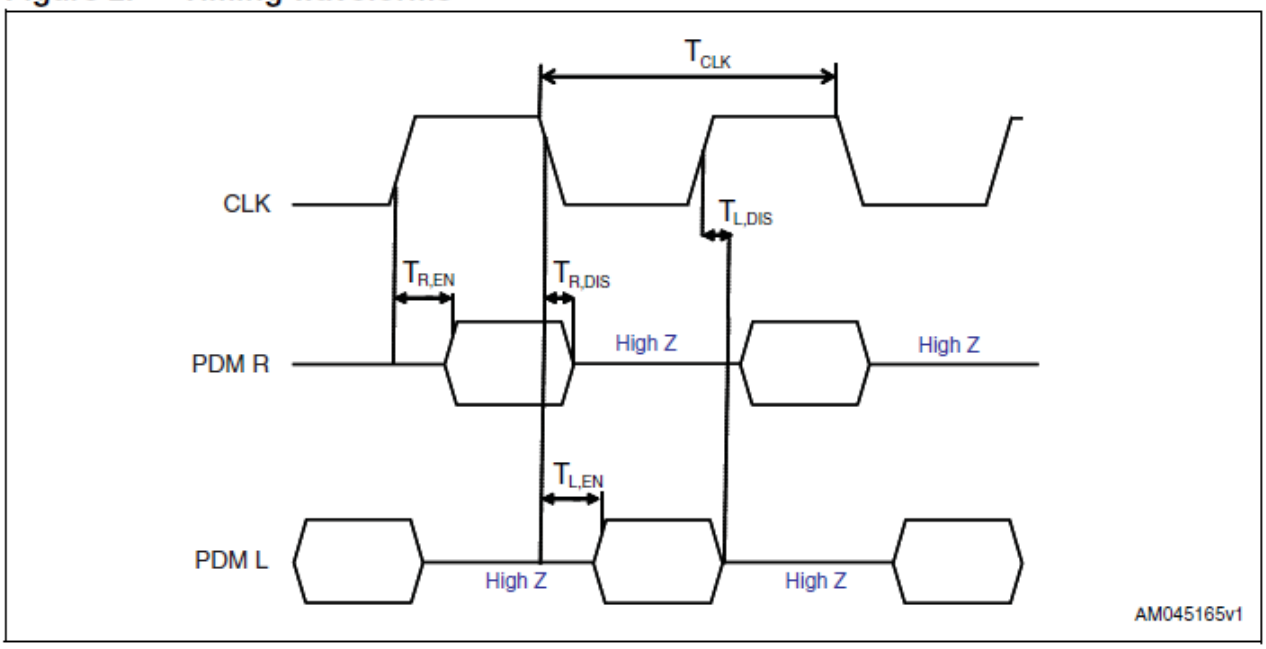
Timing characteristics

Table 5. Timing characteristics

Parameter	Description	Min	Max	Unit
f_{CLK}	Clock frequency for normal mode	1	3.25	MHz
f_{PD}	Clock frequency for power-down mode		0.23	MHz
T_{CLK}	Clock period for normal mode	308	1000	ns
$T_{R,EN}$	Data enabled on DATA line, L/R pin = 1	30(1)		ns
$T_{R,DIS}$	Data disabled on DATA line, L/R pin = 1		16(1)	ns
$T_{L,EN}$	Data enabled on DATA line, L/R pin = 0	30(1)		ns
$T_{L,DIS}$	Data disabled on DATA line, L/R pin = 0		16(1)	ns

1. From design simulations

Figure 2. Timing waveforms



Frequency response

Figure 3. Typical frequency response normalized at 1 kHz

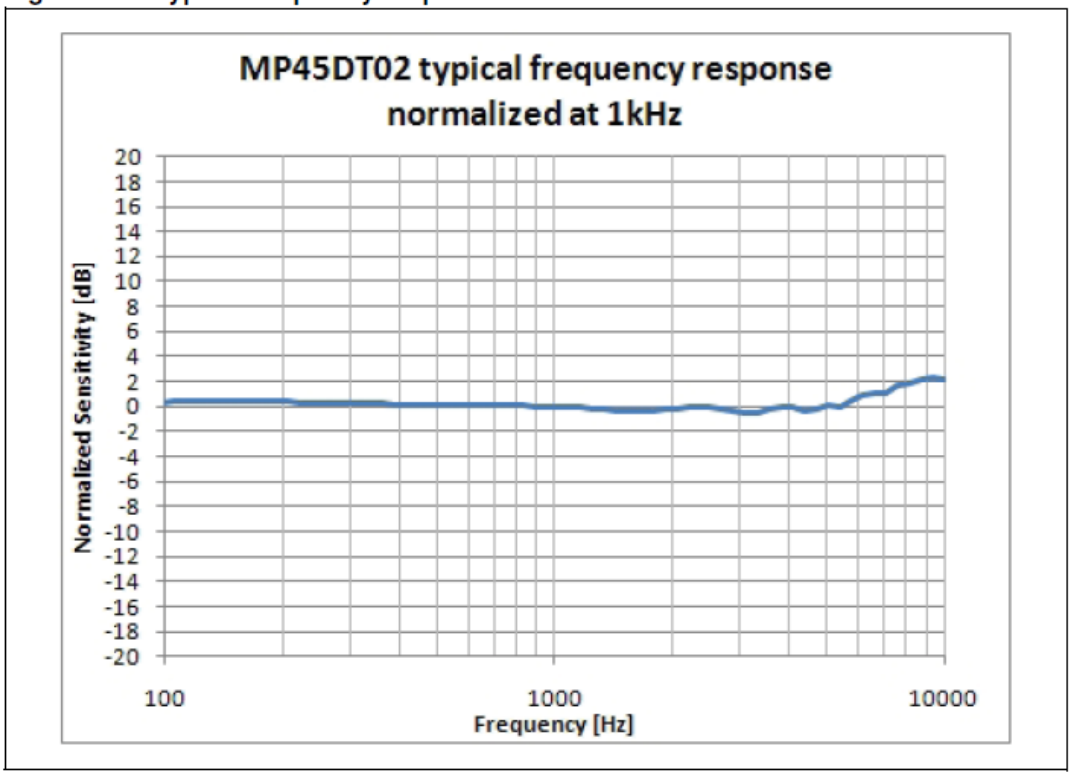


Table 6. Frequency response mask for digital microphones

Frequency / Hz (1)	Lower limit	Upper limit	Unit
20...100	-5	+5	dBr 1kHz
100...8000	-2	+2	dBr 1kHz
8000...10000	-5	+5	dBr 1kHz

1. At T = 20 °C and acoustic stimulus = 1 Pa (94 dB SPL)

CS43L22

Low Power, Stereo DAC w/Headphone & Speaker Amps

FEATURES

■ 98 dB Dynamic Range (A-wtd)
■ 88 dB THD+N
■ Headphone Amplifier - GND Centered
– No DC-Blocking Capacitors Required
– Integrated Negative Voltage Regulator
– 2 x 23 mW into Stereo 16 Ω @ 1.8 V
– 2 x 44 mW into Stereo 16 Ω @ 2.5V
■ Stereo Analog Input Passthrough Architecture
– Analog Input Mixing
– Analog Passthrough with Volume Control
■ Digital Signal Processing Engine
– Bass & Treble Tone Control, De-Emphasis
– PCM Input w/Independent Vol Control
– Master Digital Volume Control and Limiter
– Soft-Ramp & Zero-Cross Transitions
■ Programmable Peak-Detect and Limiter
■ Beep Generator w/Full Tone Control
– Tone Selections Across Two Octaves
– Separate Volume Control
– Programmable On and Off Time Intervals
– Continuous, Periodic, One-Shot Beep Selections

Class D Stereo/Mono Speaker Amplifier

■ No External Filter Required
■ High Stereo Output Power at 10% THD+N
– 2 x 1.00 W into 8 Ω @ 5.0 V
– 2 x 550 mW into 8 Ω @ 3.7 V
– 2 x 230 mW into 8 Ω @ 2.5 V
■ High Mono Output Power at 10% THD+N
– 1 x 1.90 W into 4 Ω @ 5.0 V
– 1 x 1.00 W into 4 Ω @ 3.7 V
– 1 x 350 mW into 4 Ω @ 2.5 V
■ Direct Battery Powered Operation
– Battery Level Monitoring & Compensation
■ 81% Efficiency at 800 mW
■ Phase-Aligned PWM Output Reduces Idle Channel Current
■ Spread Spectrum Modulation
■ Low Quiescent Current

System Features

■ 12, 24, and 27 MHz Master Clock Support in Addition to Typical Audio Clock Rates
■ High Performance 24-bit Converters
  – Multi-bit Delta–Sigma Architecture
  – Very Low 64Fs Oversampling Clock Reduces Power Consumption
■ Low Power Operation
  – Stereo Analog Passthrough: 10 mW @ 1.8 V
  – Stereo Playback: 14 mW @ 1.8 V
■ Variable Power Supplies
  – 1.8 V to 2.5 V Digital & Analog
  – 1.6 V to 5 V Class D Amplifier
  – 1.8 V to 2.5 V Headphone Amplifier
  – 1.8 V to 3.3 V Interface Logic
■ Power Down Management
  – DAC, Pass-through Amplifier, Headphone Amplifier, Speaker Amplifier
■ Flexible Clocking Options
  – Master or Slave Operation
  – Quarter-Speed Mode (i.e. allows 8 kHz Fs while maintaining a flat noise floor up to16kHz)
  – 4 kHz to 96 kHz Sample Rates
■ I²C Control Port Operation
■ Headphone/Speaker Detection Input
■ Pop and Click Suppression

General Description

The CS43L22 is a highly integrated, low power stereo DAC with headphone and Class D speaker amplifiers. The CS43L22 offers many features suitable for low power, portable system applications.

The **DAC output path** includes a digital signal processing engine with various fixed function controls. Tone Control provides bass and treble adjustment of four selectable corner frequencies. Digital Volume controls may be configured to change on soft ramp transitions while the analog controls can be configured to occur on every zero crossing. The DAC also includes de-emphasis, limiting functions and a BEEP generator delivering tones selectable across a range of two full octaves.

The **stereo headphone amplifier** is powered from a separate positive supply and the integrated **charge pump** provides a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates the need for external DC-blocking capacitors.

The **Class D stereo speaker amplifier** does not require an external filter and provides the high efficiency amplification required by power sensitive portable applications. The speaker amplifier may be powered directly from a battery while the internal DC supply monitoring and compensation provides a constant gain level as the battery's voltage decays. The CS43L22 accommodates analog routing of the analog input signal directly to the headphone amplifier. This feature is useful in applications that utilize an FM tuner where audio recovered over-the-air must be transmitted to the headphone amplifier directly.

In addition to its many features, the CS43L22 operates from a low voltage analog and digital core making it ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS43L22 is available in a 40-pin QFN package in Commercial (-40 to +85 °C) grade. The CS43L22 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on page 66 for complete ordering information.

Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple and single (one-shot) beeps. Sixteen on and eight off times are available.

Note: The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, MSTxVOL[7:0], will affect the beep volume, DAC volume may alternatively be controlled using the PCMxVOL[6:0] bits.

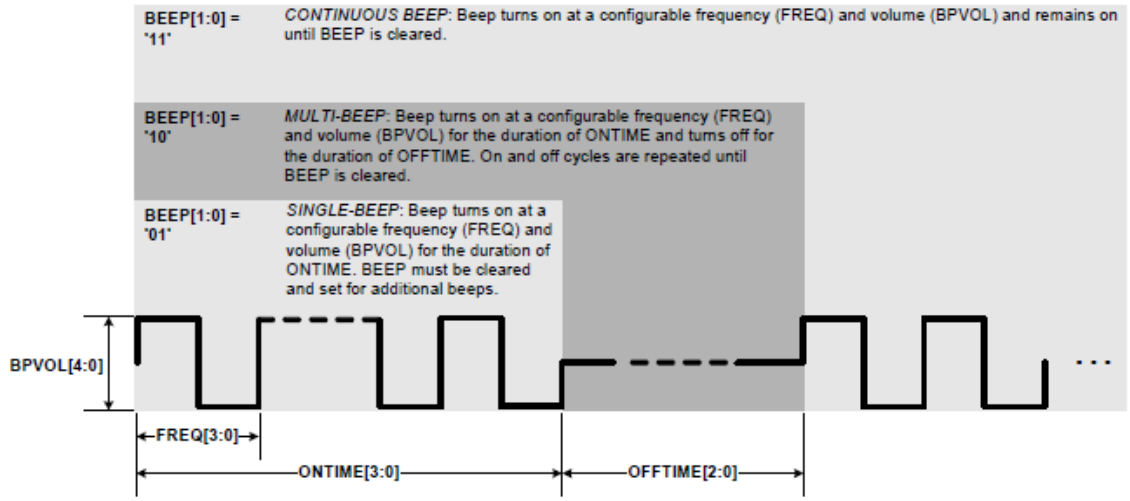


Figure 6. Beep Configuration Options

Referenced Control	Register Location
MSTxVOL[7:0]	"Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)" on page 51
PCMxVOL[6:0]	"PCMx Volume: PCMA (Address 1Ah) & PCMB (Address 1Bh)" on page 47
OFFTIME[2:0]	"Beep Off Time" on page 48
ONTIME[3:0]	"Beep On Time" on page 48
FREQ[3:0]	"Beep Frequency" on page 47
BEEP[1:0]	"Beep Configuration" on page 49
BEEPMIXDIS	"Beep Mix Disable" on page 49
BPVOL[4:0]	"Beep Volume" on page 49

Digital Interface Formats

The serial port operates in standard I²S, Left-Justified, Right-Justified, or DSP Mode digital interface formats with varying bit depths from 16 to 24. Data is clocked into the DAC on the rising edge of SCLK.

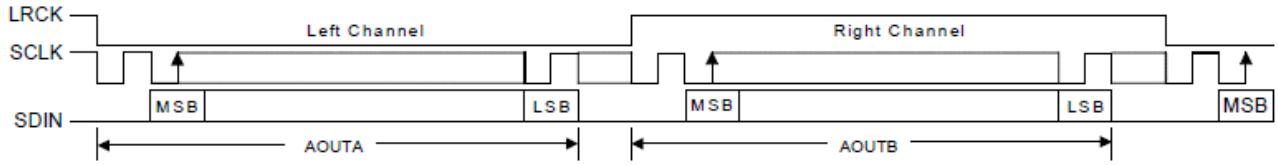


Figure 12. I²S Format

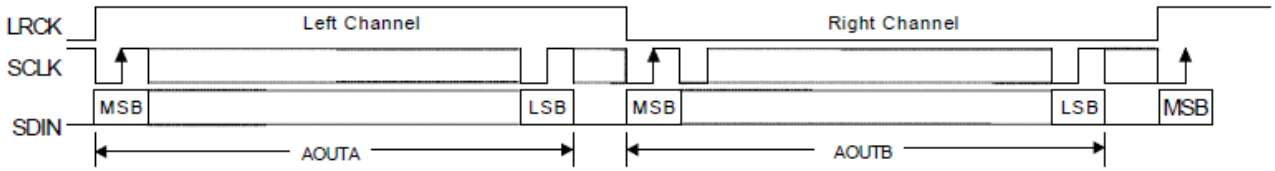


Figure 13. Left-Justified Format

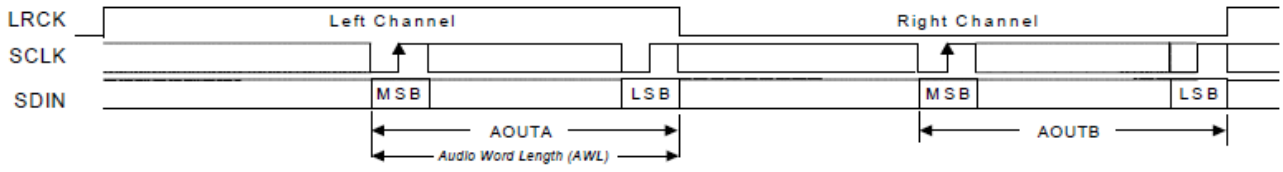


Figure 14. Right-Justified Format

Initialization

The CS43L22 enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma and PWM modulators and control port registers are reset. The internal voltage reference, and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-Down state until the RESET pin is brought high. The control port is accessible once RESET is high and the desired register settings can be loaded per the interface descriptions in the "Register Description" on page 37.

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+, will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

Recommended Power-Up Sequence

1. Hold RESET low until the power supplies are stable.
2. Bring RESET high.
3. The default state of the "Power Ctl. 1" register (0x02) is 0x01. Load the desired register settings while keeping the "Power Ctl 1" register set to 0x01.
4. Load the required initialization settings listed in Required Initialization Settings
5. Apply MCLK at the appropriate frequency, as discussed in Section 4.6. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
6. Set the "Power Ctl 1" register (0x02) to 0x9E.
7. Bring RESET low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

Required Initialization Settings

Various sections in the device must be adjusted by implementing the initialization settings shown below after power-up sequence step 3. All performance and power consumption measurements were taken with the following settings:

1. Write 0x99 to register 0x00.
2. Write 0x80 to register 0x47.
3. Write '1'b to bit 7 in register 0x32.
4. Write '0'b to bit 7 in register 0x32.
5. Write 0x00 to register 0x00.

CONTROL PORT OPERATION

The control port is used to access the registers allowing the CS43L22 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates using an I²C interface with the CS43L22 acting as a slave device

I²C Control

SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. The AD0 pin sets the LSB of the chip address; '0' when connected to DGND, '1' when connected to VL. This pin may be driven by a host controller or directly connected to VL or DGND. The AD0 pin state is sensed and the LSB of the chip address is set upon the release of the RESET signal (a low-to-high transition).

The signal timings for a read and write cycle are shown in Figure 16 and Figure 17. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS43L22 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write).

The upper 6 bits of the address field are fixed at 100101. To communicate with the CS43L22, the chip address field, which is the first byte sent to the CS43L22, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP), which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS43L22 after each input byte is read and is input to the CS43L22 from the microcontroller after each transmitted byte.

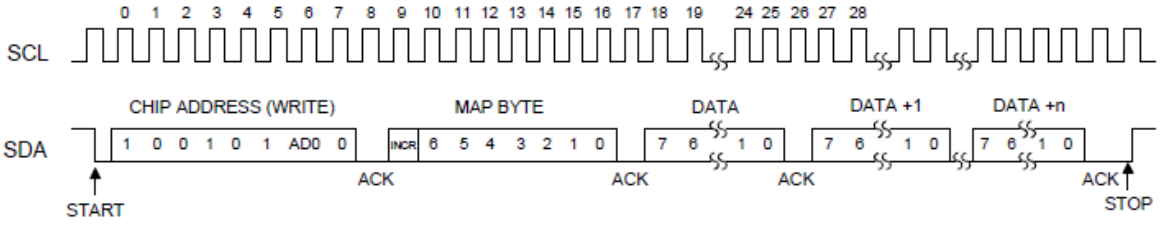


Figure 16. Control Port Timing, I²C Write

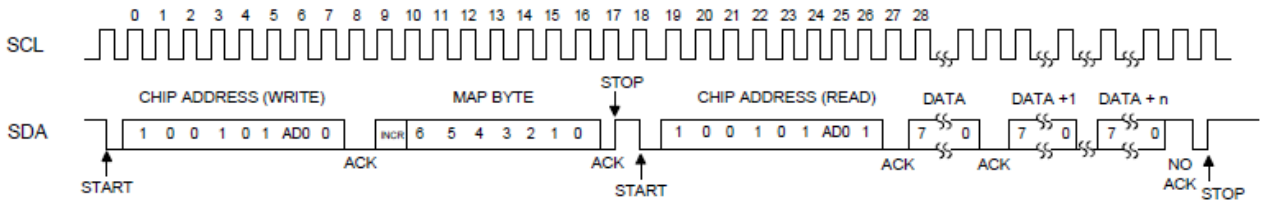


Figure 17. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 17, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send 10010100 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto-increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10010101 (chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

REGISTER DESCRIPTION

All registers are read/write except for the chip I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is shown as shaded in the table. Unless otherwise specified, all "Reserved" bits must maintain their default value.

• Beep & Tone Configuration (Address 1Eh)

7	6	5	4	3	2	1	0
BEEP1	BEEP0	BEEPMIXDIS	TREBCF1	TREBCF0	BASSCF1	BASSCF0	TCEN

Beep Configuration

Configures a beep mixed with the HP/Line and SPK output.

BEEP[1:0]	Beep Occurrence
00	Off
01	Single
10	Multiple
11	Continuous
Application:	"Beep Generator" on page 22

Notes:
1. When used in analog pass through mode, the output alternates between the signal from the Pass-through Amplifier and the beep signal. The beep signal does not mix with the analog signal from the Pass-through Amplifier.
2. Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration.

Beep Mix Disable

Configures how the beep mixes with the serial data input.

BEEPMIXDIS	Beep Output to HP/Line and Speaker
0	Mix Enabled; The beep signal mixes with the digital signal from the serial data input.
1	Mix Disabled; The output alternates between the signal from the serial data input and the beep signal. The beep signal does not mix with the digital signal from the serial data input.
Application:	"Beep Generator" on page 22

Note: This setting must not change when BEEP is enabled.

Treble Corner Frequency

Sets the corner frequency (-3 dB point) for the treble shelving filter.

TREBCF[1:0]	Treble Corner Frequency Setting
00	5 kHz
01	7 kHz
10	10 kHz
11	15 kHz

Bass Corner Frequency

Sets the corner frequency (-3 dB point) for the bass shelving filter.

BASSCF[1:0]	Bass Corner Frequency Setting
00	50 Hz
01	100 Hz
10	200 Hz
11	250 Hz

Tone Control Enable

Configures the treble and bass activation.

TCEN	Bass and Treble Control
0	Disabled
1	Enabled
Application:	"Beep Generator" on page 22

- **Beep Frequency & On Time (Address 1Ch)**

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

Beep Frequency

Sets the frequency of the beep signal.

FREQ[3:0]	**Frequency** *(Fs = 12, 24, 48 or 96 kHz)*	**Pitch**
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7
Application:	"Beep Generator" on page 22	

Notes:

1. This setting must not change when BEEP is enabled.
2. Beep frequency will scale directly with sample rate, Fs, but is fixed at the nominal Fs within each speed mode.

Beep On Time

Sets the on duration of the beep signal.

ONTIME[3:0]	**On Time** *(Fs = 12, 24, 48 or 96 kHz)*
0000	~86 ms
0001	~430 ms
0010	~780 ms
0011	~1.20 s
0100	~1.50 s
0101	~1.80 s
0110	~2.20 s
0111	~2.50 s
1000	~2.80 s
1001	~3.20 s
1010	~3.50 s
1011	~3.80 s
1100	~4.20 s
1101	~4.50 s
1110	~4.80 s
1111	~5.20 s
Application:	"Beep Generator" on page 22

Notes:

1. This setting must not change when BEEP is enabled.
2. Beep on time will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode