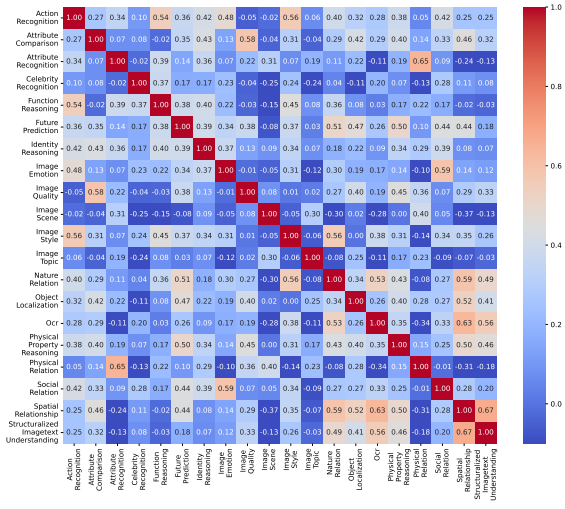
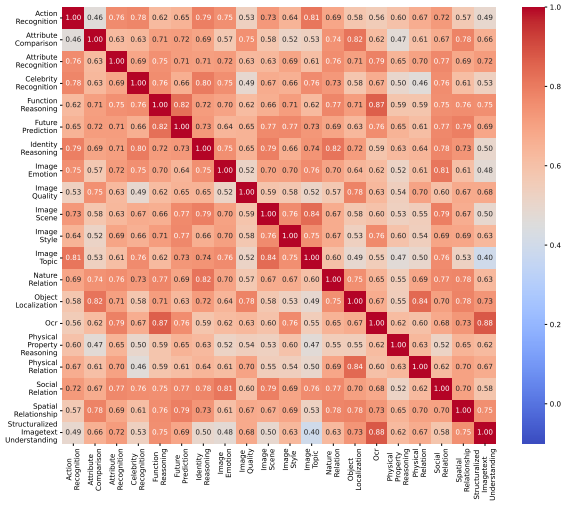
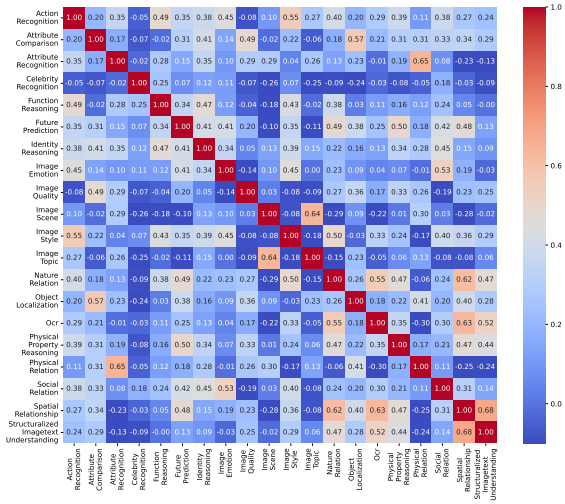


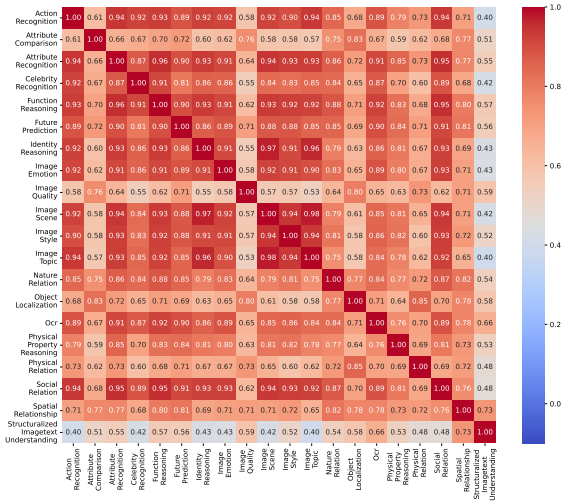
(a) Top-50 SRCC dimensions redundancy map.



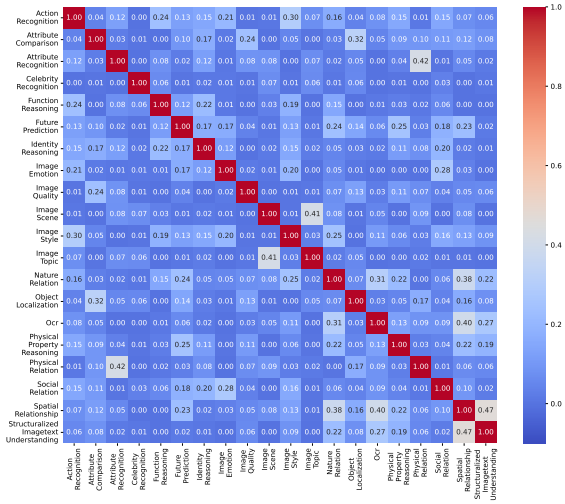
(b) Bottom-50 SRCC dimensions redundancy map.



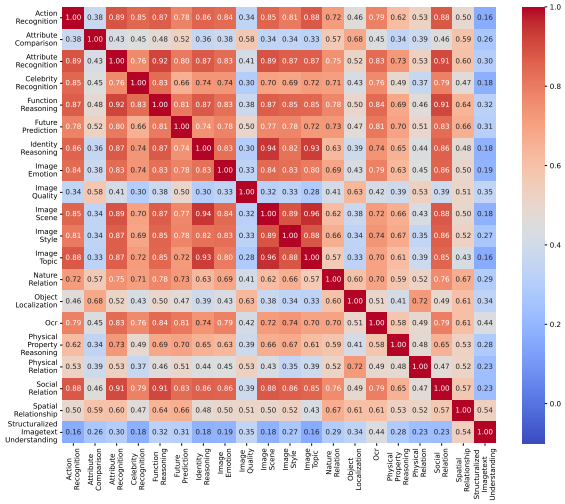
(c) Top-50 PLCC dimensions redundancy map.



(d) Bottom-50 PLCC dimensions redundancy map.

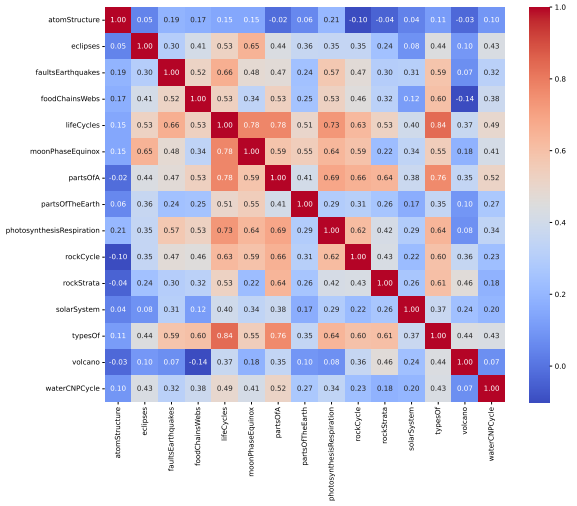


(e) Top-50 R2 dimensions redundancy map.

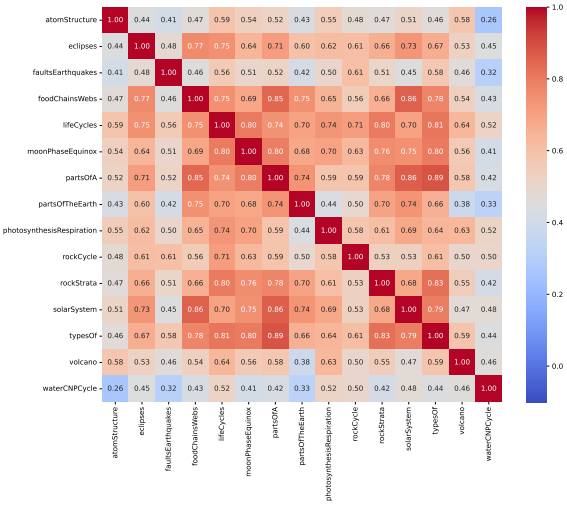


(f) Bottom-50 R2 dimensions redundancy map.

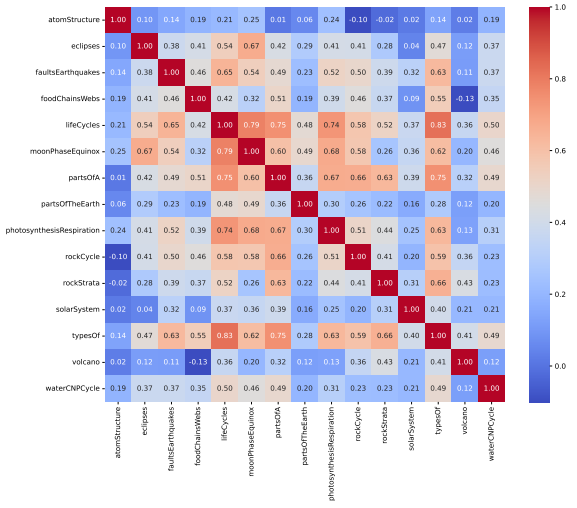
Figure 3. Visualizations of dimensions redundancy for MMBench [23] on Top-50 and Bottom-50 MLLMs.



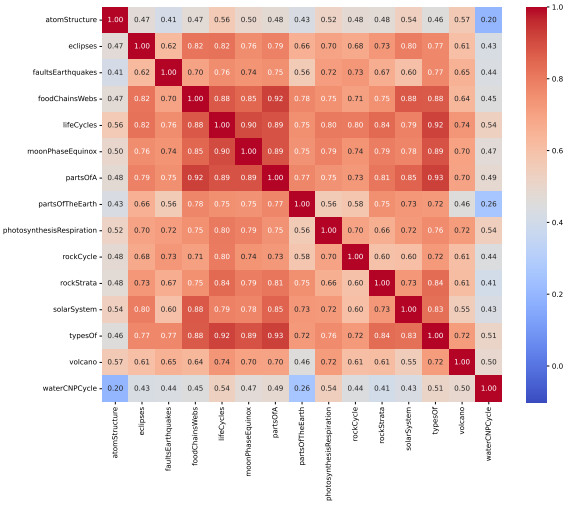
(a) Top-50 SRCC dimensions redundancy map.



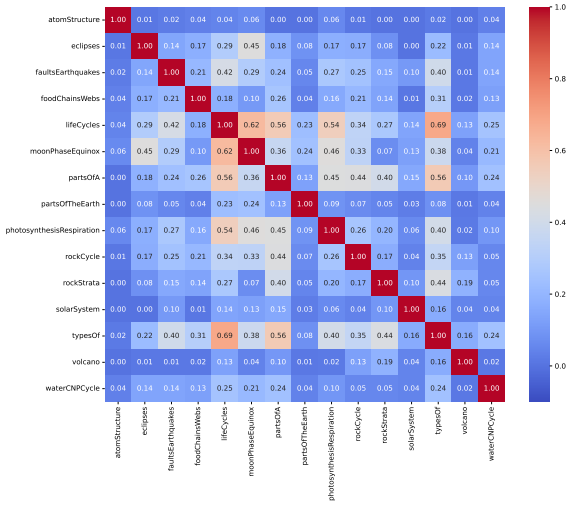
(b) Bottom-50 SRCC dimensions redundancy map.



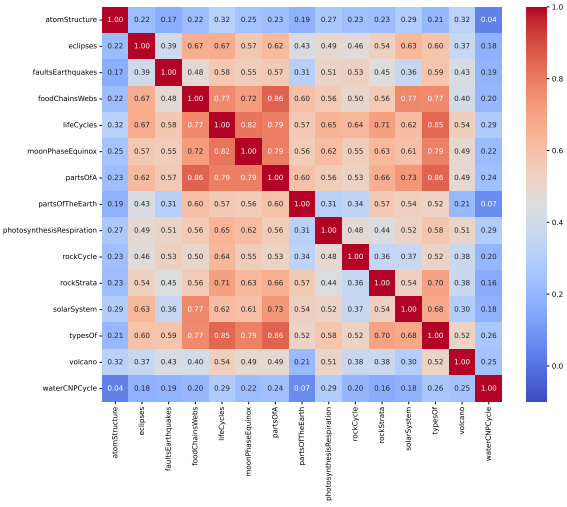
(c) Top-50 PLCC dimensions redundancy map.



(d) Bottom-50 PLCC dimensions redundancy map.

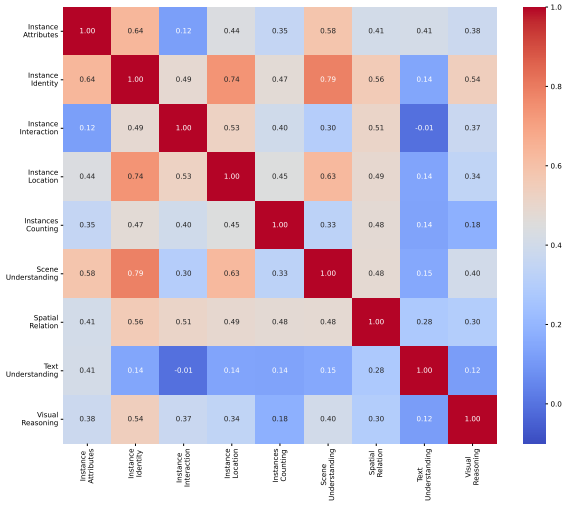


(e) Top-50 R2 dimensions redundancy map.

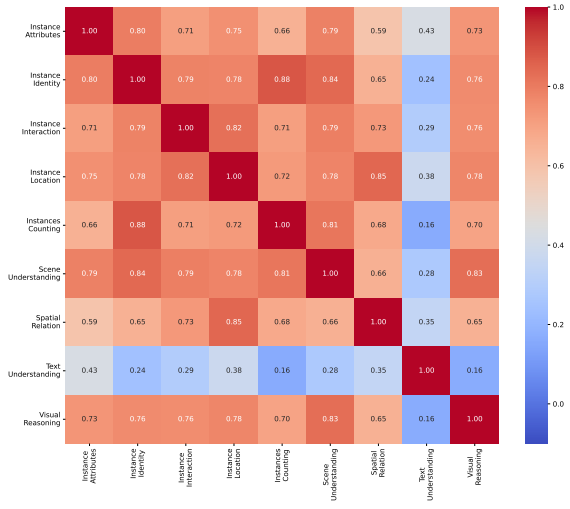


(f) Bottom-50 R2 dimensions redundancy map.

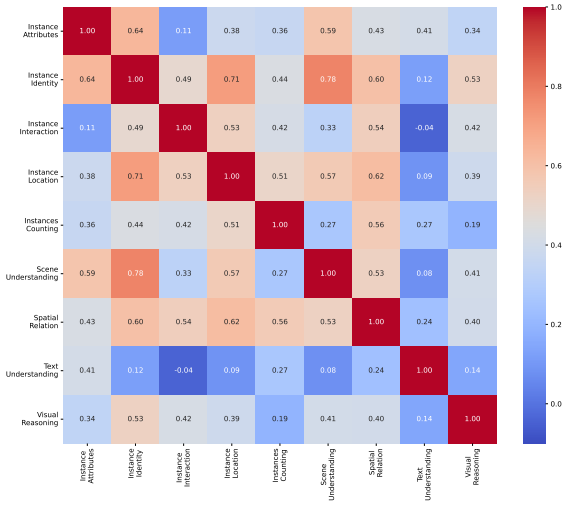
Figure 8. Visualizations of dimensions redundancy for AI2D [13] on Top-50 and Bottom-50 MLLMs.



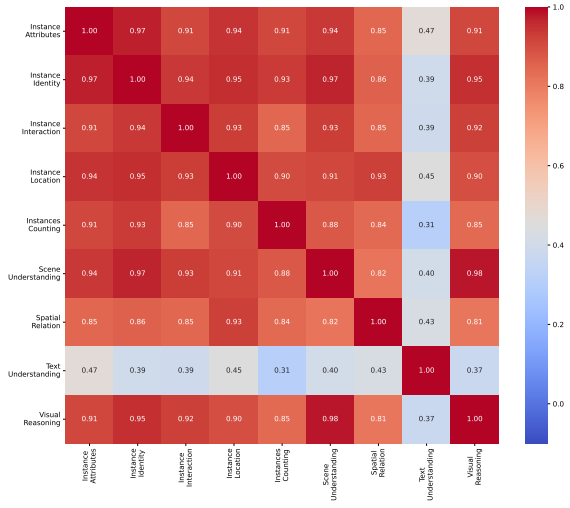
(a) Top-50 SRCC dimensions redundancy map.



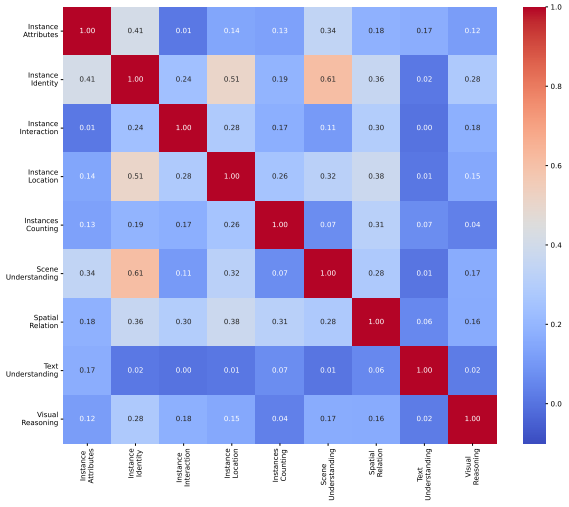
(b) Bottom-50 SRCC dimensions redundancy map.



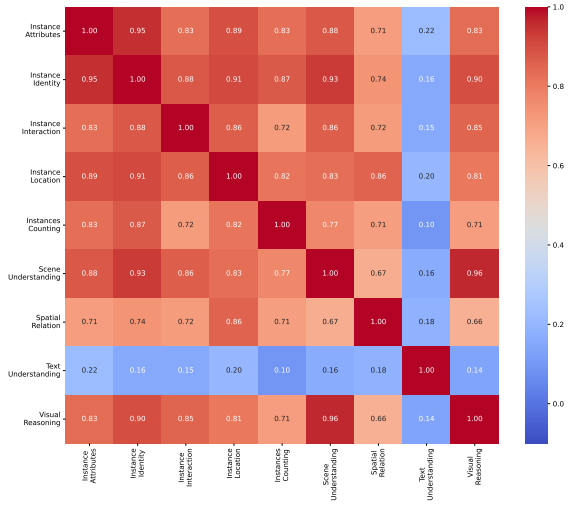
(c) Top-50 PLCC dimensions redundancy map.



(d) Bottom-50 PLCC dimensions redundancy map.



(e) Top-50 R2 dimensions redundancy map.



(f) Bottom-50 R2 dimensions redundancy map.

Figure 9. Visualizations of dimensions redundancy for SEED-Bench [16] on Top-50 and Bottom-50 MLLMs.