Semiconductors:

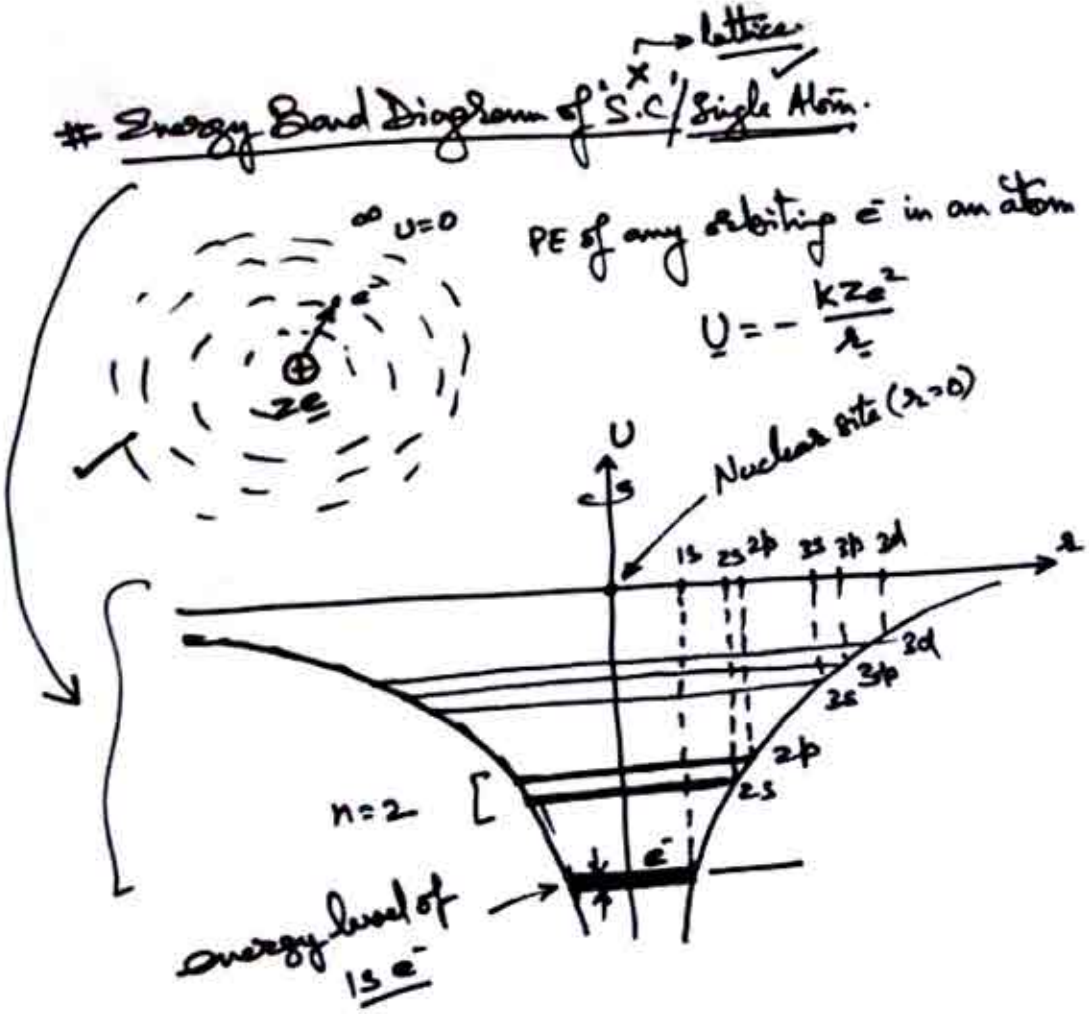
↳ These are materials which are used to control flow of charges in diff applications.

* Many electronic devices are based on S.C. materials which govern & control charge flow in ckts

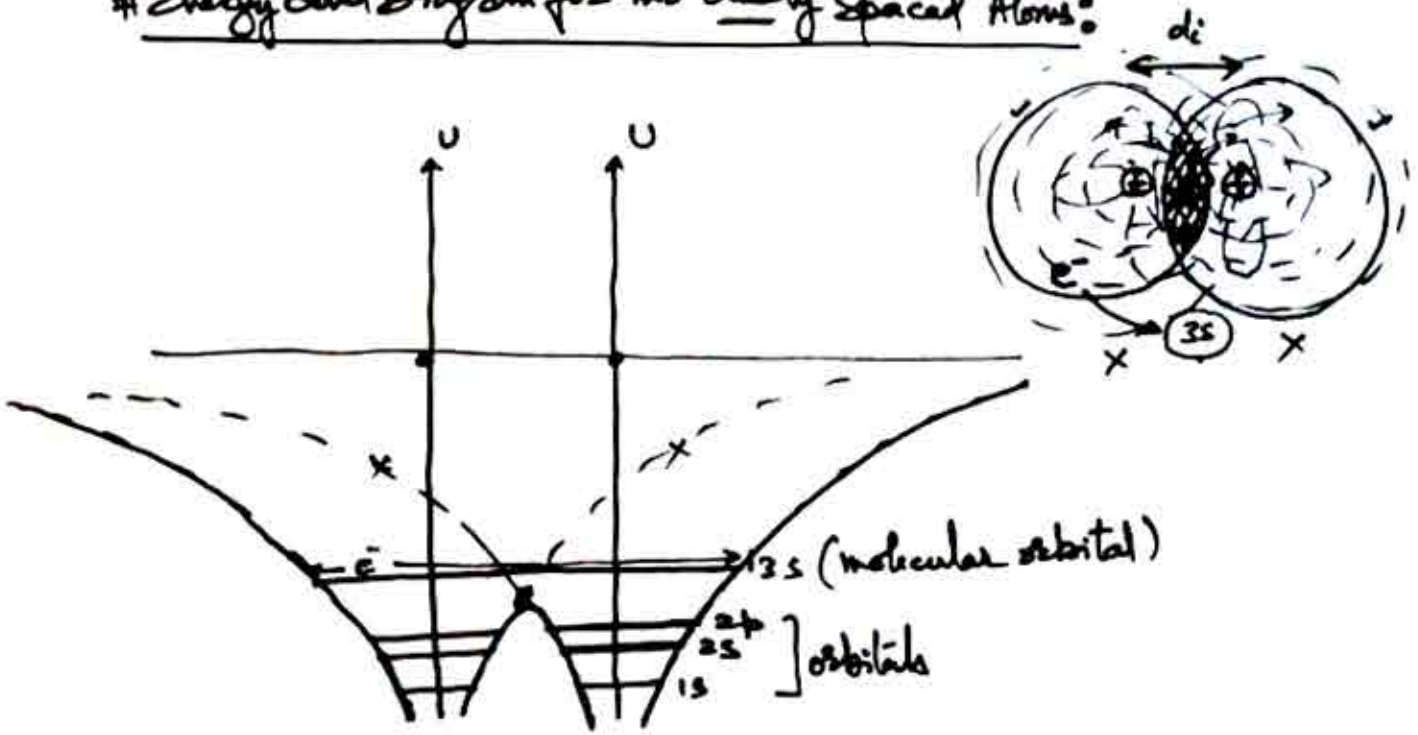
Classification of solids:

- Conductors (α +ve)
- Insulators
- Semiconductors (α -ve) — within a range.
  - insulators at v. low temp
  - at normal temp conduct electricity
  - At v. high temp → these behave like Conductors (α +ve)

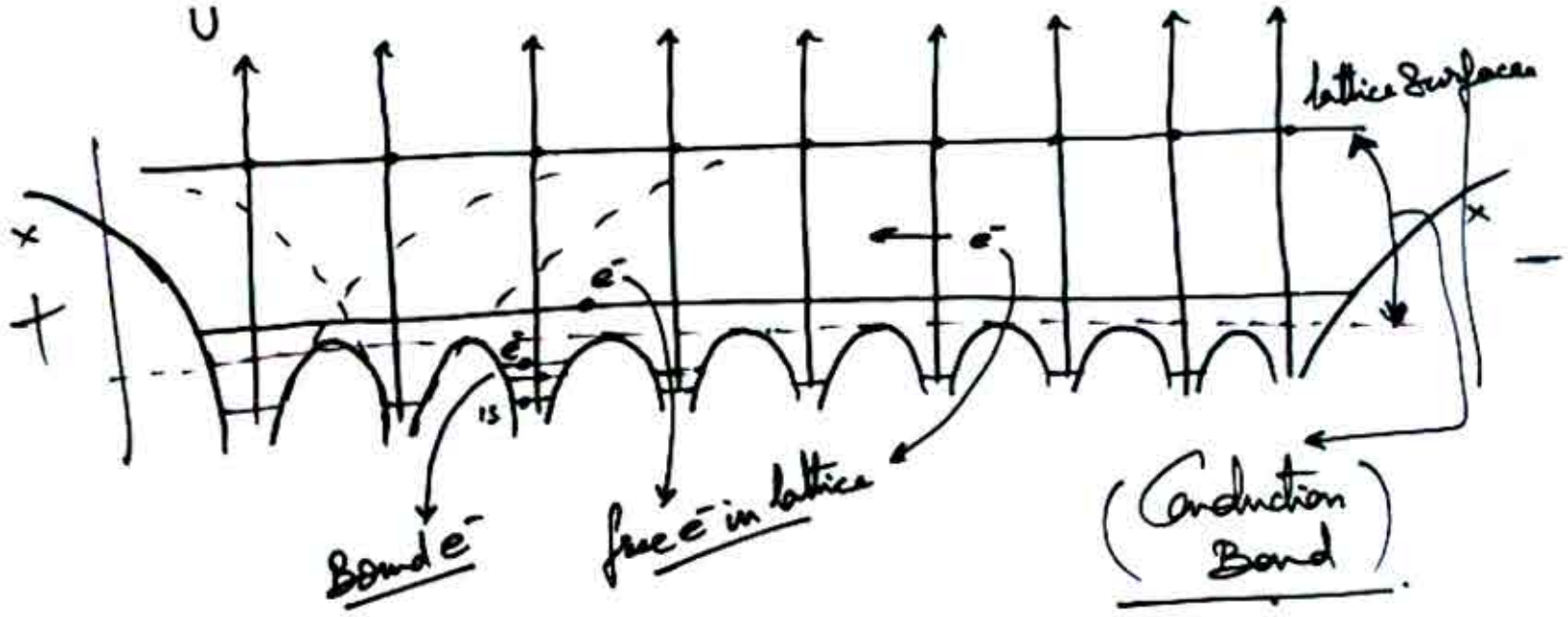
Energy Band Diagram of 'S.C' / Single Atom.



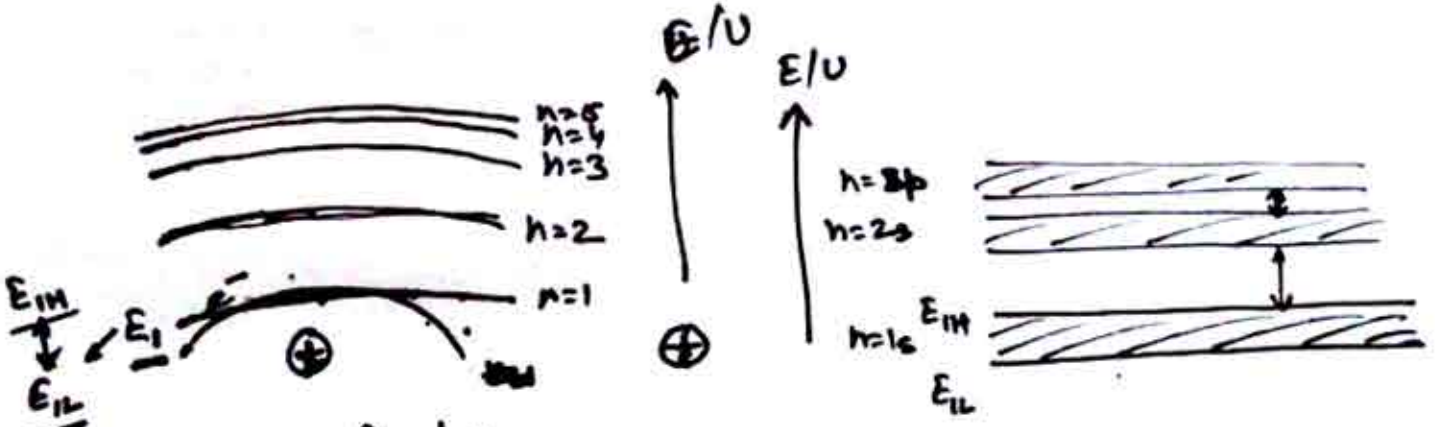
#Energy Band Diagram for two closely spaced Atoms:



* Energy Band diagram for a Solid lattice (multiple atoms):

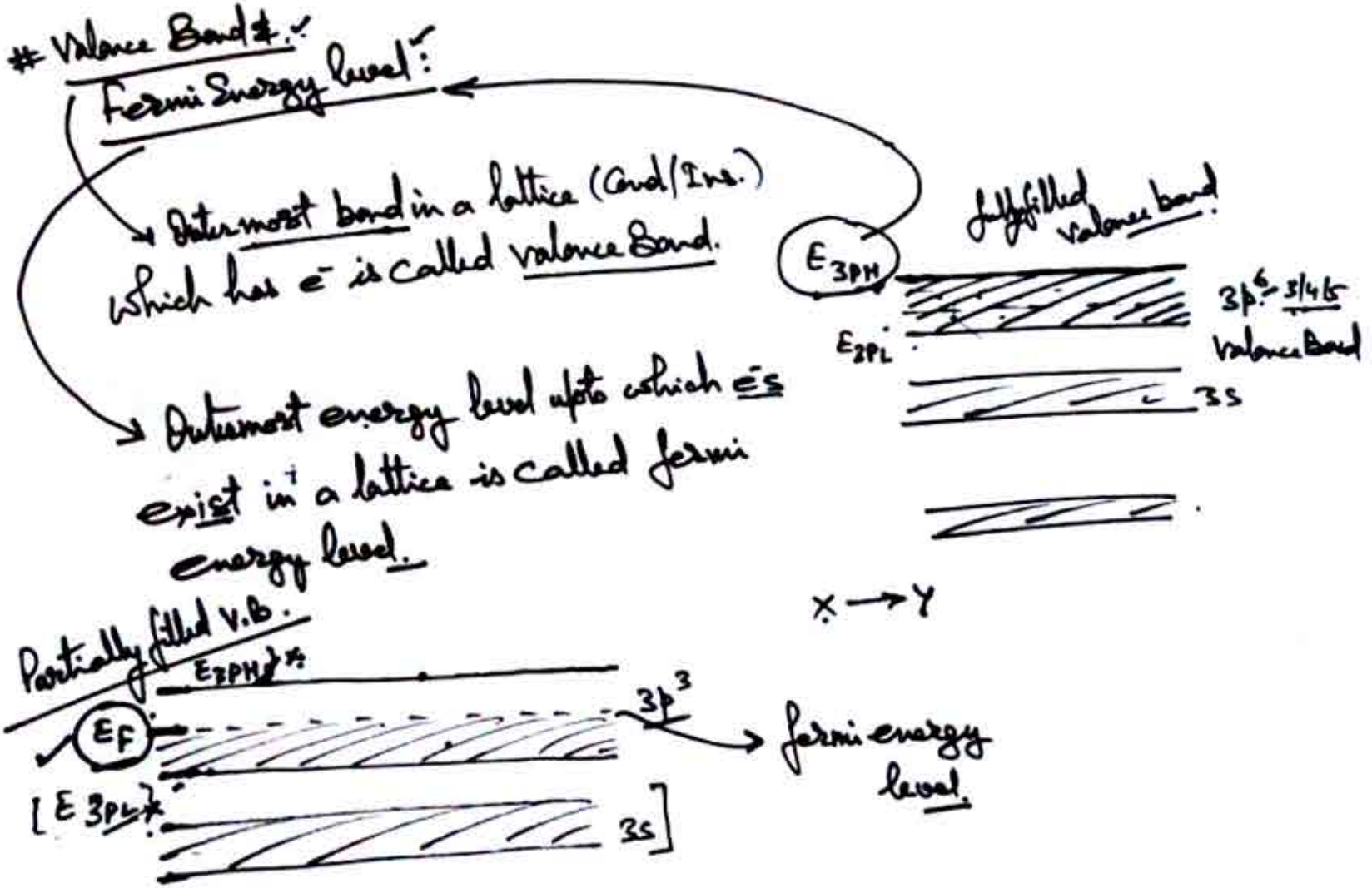


Energy Band modification in Solid lattice :



Energy level diagram for a Single Atom X

Solid lattice Energy Band Diagram of same element X

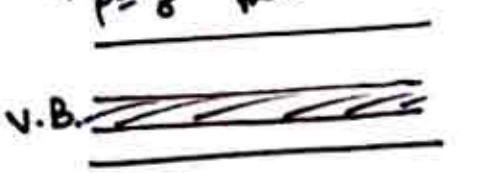

* Valence Band & Fermi Energy level:
Outermost band in a lattice (Cond/Ins.) which has e⁻ is called valence Band.
Outermost energy level upto which e⁻s exist in a lattice is called fermi energy level.
E3PH
fullyfilled valence band
3p⁶ - 3/4 e⁻
E3PL
valence Band
3s
Partially filled V.B.
E3PH
EF
3p³
fermi energy level
[E3PL
3s]
X → Y

Band Structure of Metals (Cond), Insulators & S.C.

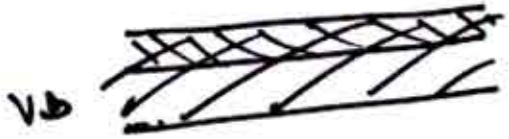
$\sigma = ne\mu$ — free e⁻ density

$\rho = \frac{1}{\sigma}$

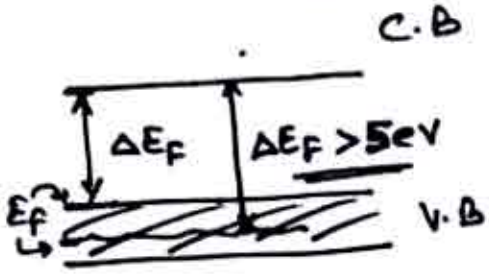
metal-1 $n_1 > n_2$



metal-2



Insulator



ΔE_f → Fermi energy Gap

↓

This is the energy diff. betⁿ Fermi Energy level and lowest energy level of C.B.

S.C are those materials in which

$\Delta E_f < 2eV$

& this energy is absorbed by e^- of V.B. at room temp by thermal agitation so at room temp such materials can conduct electricity.

NOTE: In S.C. as temp increases, due to more shifting of e^- from VB to CB free e^- density in CB increases so conductivity ($\sigma = ne\mu$) increases that's why semiconductors have negative temperature coefficient of resistance.

If temp is increased to a v. high value in S.C. then conduction mobility (μ) decreases drastically & this factor overrides increase in 'n' so after a limit again with temp conductivity starts decreasing and S.C. have +ve α.

In general we study Ge & Si Semiconductors (both are IV gp elements)

$\Delta E_g = 0.72\,eV$ $\Delta E_g = 1.14\,eV$

$$\rho = \rho_0 (1 + \alpha \Delta T)$$

Types of Semiconductors:

In general semiconductors are classified in two types -

① Intrinsic Semiconductors (Pure) ⟶ Ge / Si (IV gr elements)

② Extrinsic Semiconductors (with Impurity) → Doping (Doped S.C) ⟶ These are made by adding III gr or V gr impurities to intrinsic S.C.

NOTE: Impurity is added to increase conductivity of intrinsic S.C.

Total Current in a S.C. is Contributed by both $\bar{e}$ & holes given as

$$I_{sc} = I_e + I_h \approx 2I_e \approx 2I_h.$$ (if nothing is specified in qne)

generally $I_e \geq I_h$ because mobility of holes is less compared to that of free $\bar{e}$s in e.B.

Conductivity of intrinsic S.C.

$$\sigma_{sc} = \sigma_e + \sigma_h$$

$$\sigma = n_e e \mu_e + n_h e \mu_h$$

$$\sigma = n_i e(\mu_e + \mu_h)$$

here $n_i = n_e = n_h$ is called intrinsic carrier Concentration

$$I = I_e + I_h$$

$$= S(n_e e \mu_e + n_h e \mu_h) E$$

$$E = \frac{V}{d}$$

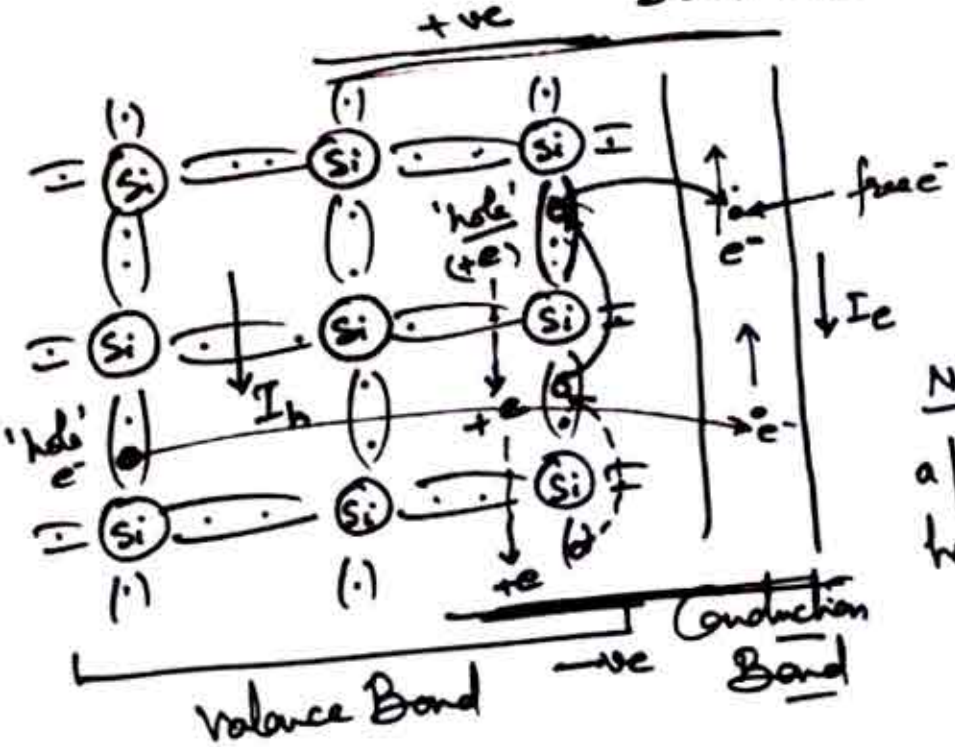
$$I = \frac{SV}{d} n_i e (\mu_e + \mu_h)$$

* Intrinsic Semiconductors :

(Pure). (IV gr elements) (valence e^- – 4)

Solid

In pure lattice of IV gr elements each atoms makes four co-valent bond with neighbouring atoms in stable lattice structure.



NOTE: Due to thermal agitation in pure Si at room temp it is observed that 1 in 10^9 Si atoms one e⁻-h pair is generated/ Contributed.

NOTE: When a p.d. is applied across a pure S.C. then both – e^- in CB and holes in VB Conducts electric current.

e-h Generation, Combination & Recombination in a S.C:

Due to temp when an e-h pair is generated in VB & CB, $(h) \to (e)$ after a short lifetime of excitation e^-s from C.B. drops back (de-excite) to VB & recombine with a hole & get neutralized & released energy as EM wave, which is absorbed by lattice & due e-h pair generation & recombination lattice maintains its thermal equilibrium (const T) and a constant avg intrinsic carrier concentration in CB & VB which depends on temp as

$$n_i = n_e = n_h$$

$$n_i^2 = AT^3 e^{-\frac{\Delta E_f}{kT}} \Rightarrow n_i = n_0 e^{-\frac{\Delta E_f}{2kT}}$$

$(\sqrt{A}T^{3/2})$

#Extrinsic Semiconductors:

In intrinsic S.C. to increase conductivity III gr or V gr impurity is added by which two types of Extrinsic S.C. are made.

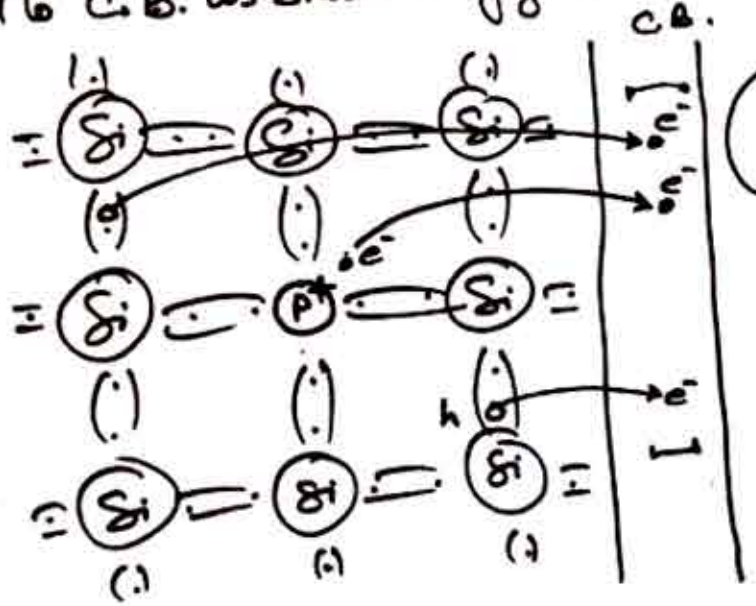
These are —

(1) N-type S.C. → by doping of V gr impurity

(2) P-type S.C → by doping of III gr. elements

Phosphorus

① **N-type S.C.:** When in a Si substrate, P-atoms are added at a concentration of 1 in 10^3 to 1 in 10^5 then due to pentavalent impurity 4th e⁻ becomes loose in Si lattice and with v. less energy it gets excited to C.B. as shown in figure.



$n_e >> n_h$

$n_i \rightarrow$ 1 in 10^8 $\quad n_h \simeq n_i$

$n_e \simeq n_i + n_D$

Donor Concentration (Conc of P-atom)

Due to each impurity atom, one extra e^- is contributed to C.B. concentration of e^- in CB will be excessively higher compared to holes So in such Semiconductor with V group impurity current is mainly contributed by e^-s thats ~~why~~ why it is named N-type S.C and in N-type S.C. e^-s are called majority charge carriers & holes are called minority charge carriers.

Law of mass Action:

In N-type S.C. as in C.B. e^- concentration is v. high, due to this recombination effect of e-h pairs increases & it decreases the overall intrinsic concentration but for any semiconductor relation of n_i, n_e and n_h remain same & it is given as

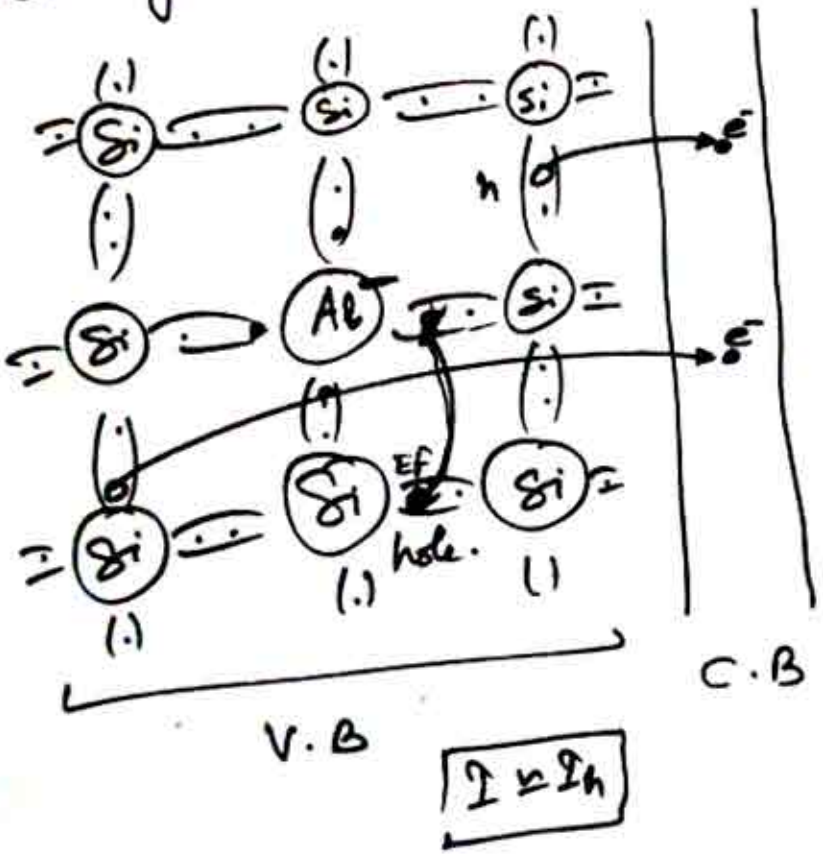
$$n_i^2 = n_e \cdot n_h$$

$$n_e = n_i + n_D \simeq \underline{n_D}$$

$$\Rightarrow \underline{n_h = \left(\frac{n_i^2}{n_D}\right)}$$

(2) P-type S.C:

It is made by adding III gr impurity (Al) in intrinsic S.C at a Conc of 1 in 10^3 to 1 in 10^5 atoms in Substrate.



$n_e \leq n_{ie}$

$n_h = n_{ie} + n_A \simeq n_A$

n_A → Acceptor impurity Concentration

$$n_e = \frac{n_i^2}{n_A}$$ ← intrinsic Conc. / f(T)

in P-type S.C $n_h >> n_e$ here

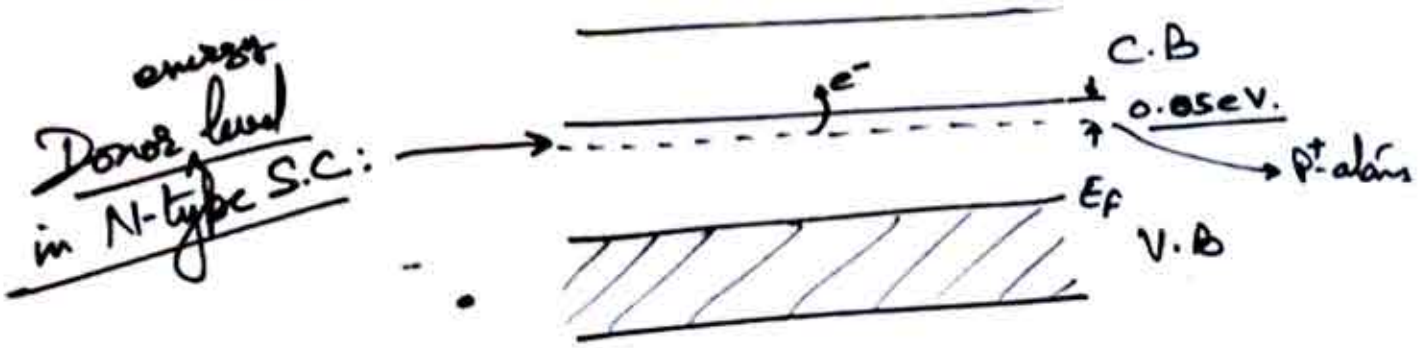
holes → majority charge carriers

e^- → minority charge carriers.

$I \simeq I_h$

Energy levels of Donor & Acceptor impurity :

Donor energy level in N-type S.C :



Acceptor energy level in P-type S.C