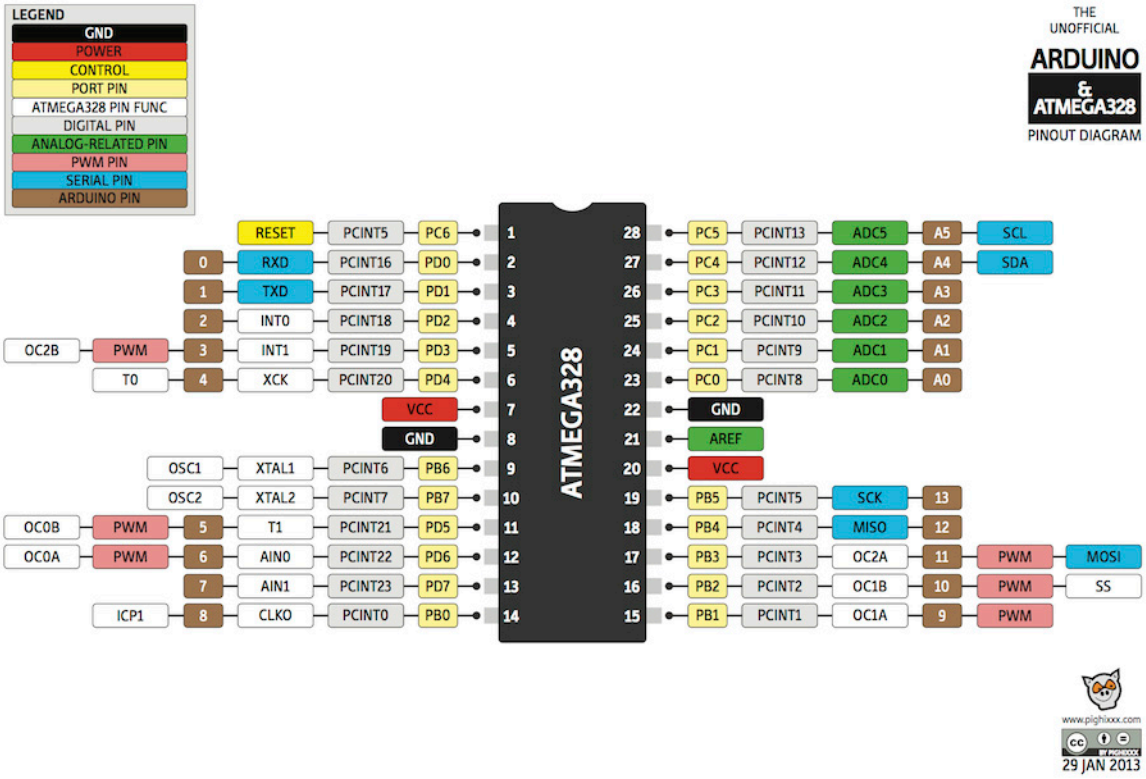
LEGEND
GND
POWER
CONTROL
PORT PIN
ATMEGA328 PIN FUNC
DIGITAL PIN
ANALOG-RELATED PIN
PWM PIN
SERIAL PIN
ARDUINO PIN
THE UNOFFICIAL
ARDUINO & ATMEGA328
PINOUT DIAGRAM
ATMEGA328
RESET PCINT5 PC6 1
0 RXD PCINT16 PD0 2
1 TXD PCINT17 PD1 3
2 INT0 PCINT18 PD2 4
OC2B PWM 3 INT1 PCINT19 PD3 5
T0 4 XCK PCINT20 PD4 6
VCC 7
GND 8
OSC1 XTAL1 PCINT6 PB6 9
OSC2 XTAL2 PCINT7 PB7 10
OC0B PWM 5 T1 PCINT21 PD5 11
OC0A PWM 6 AIN0 PCINT22 PD6 12
7 AIN1 PCINT23 PD7 13
ICP1 8 CLKO PCINT0 PB0 14
28 PC5 PCINT13 ADC5 A5 SCL
27 PC4 PCINT12 ADC4 A4 SDA
26 PC3 PCINT11 ADC3 A3
25 PC2 PCINT10 ADC2 A2
24 PC1 PCINT9 ADC1 A1
23 PC0 PCINT8 ADC0 A0
22 GND
21 AREF
20 VCC
19 PB5 PCINT5 SCK 13
18 PB4 PCINT4 MISO 12
17 PB3 PCINT3 OC2A 11 PWM MOSI
16 PB2 PCINT2 OC1B 10 PWM SS
15 PB1 PCINT1 OC1A 9 PWM
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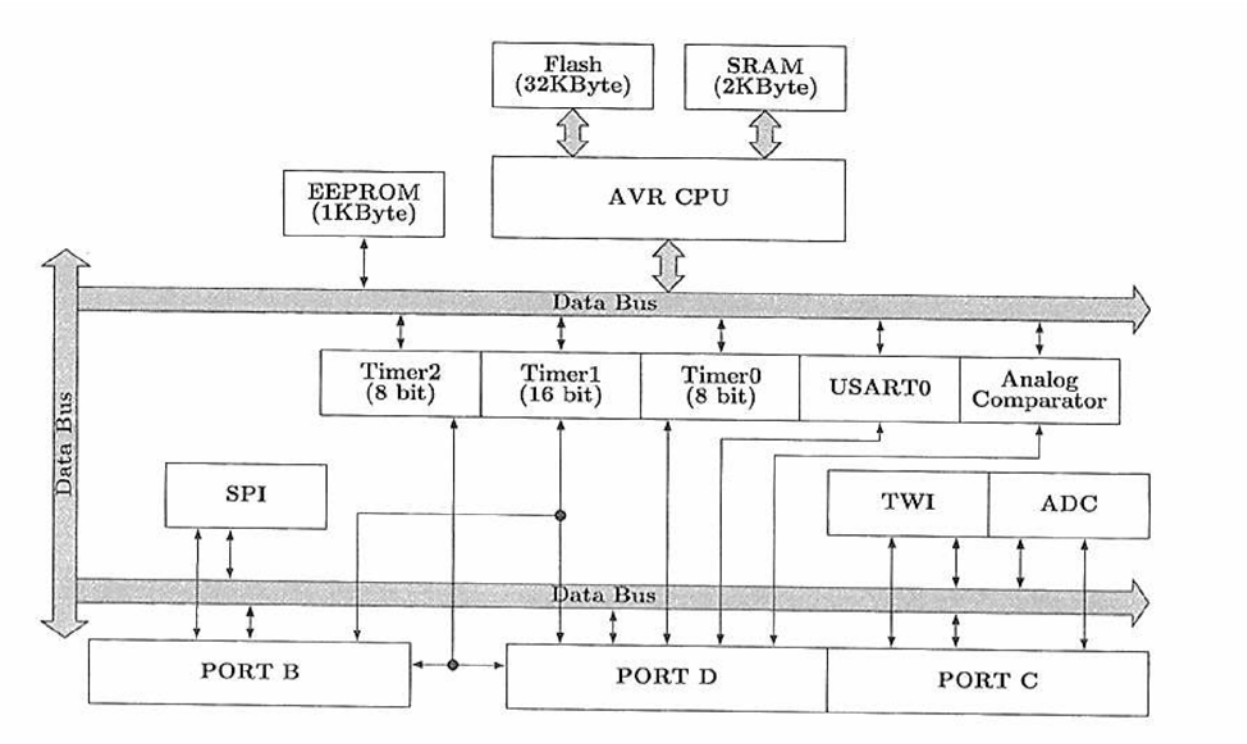
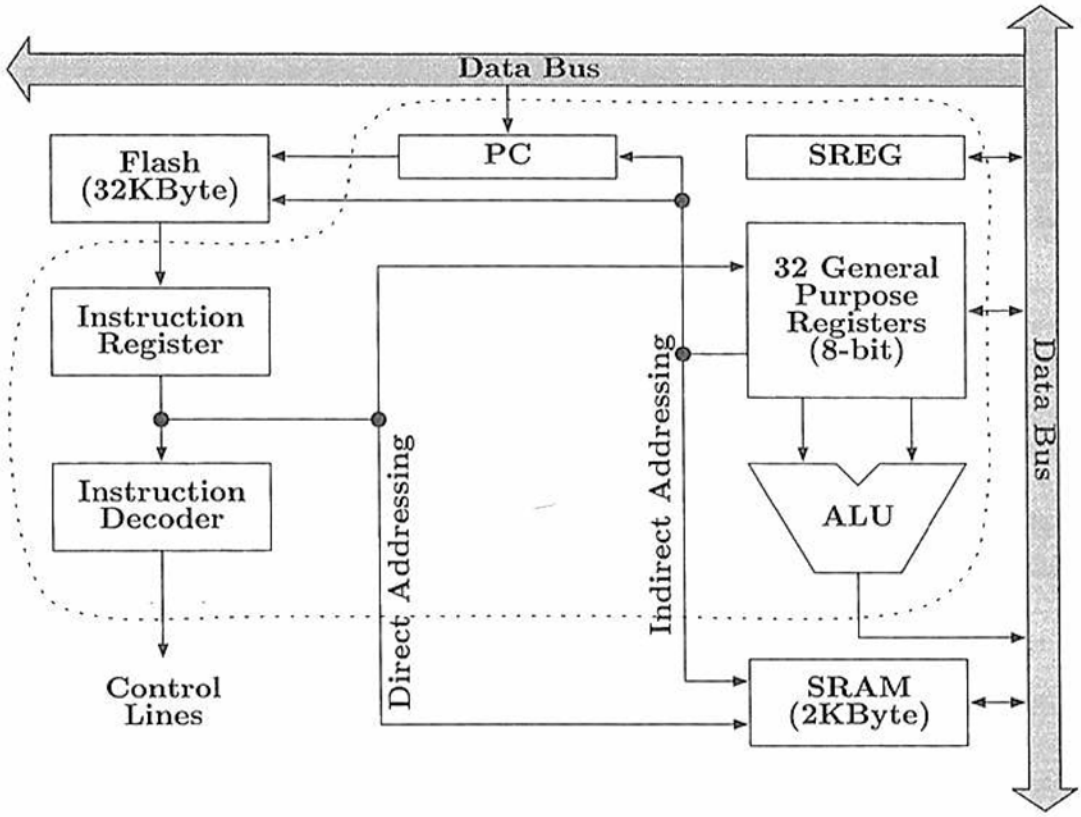
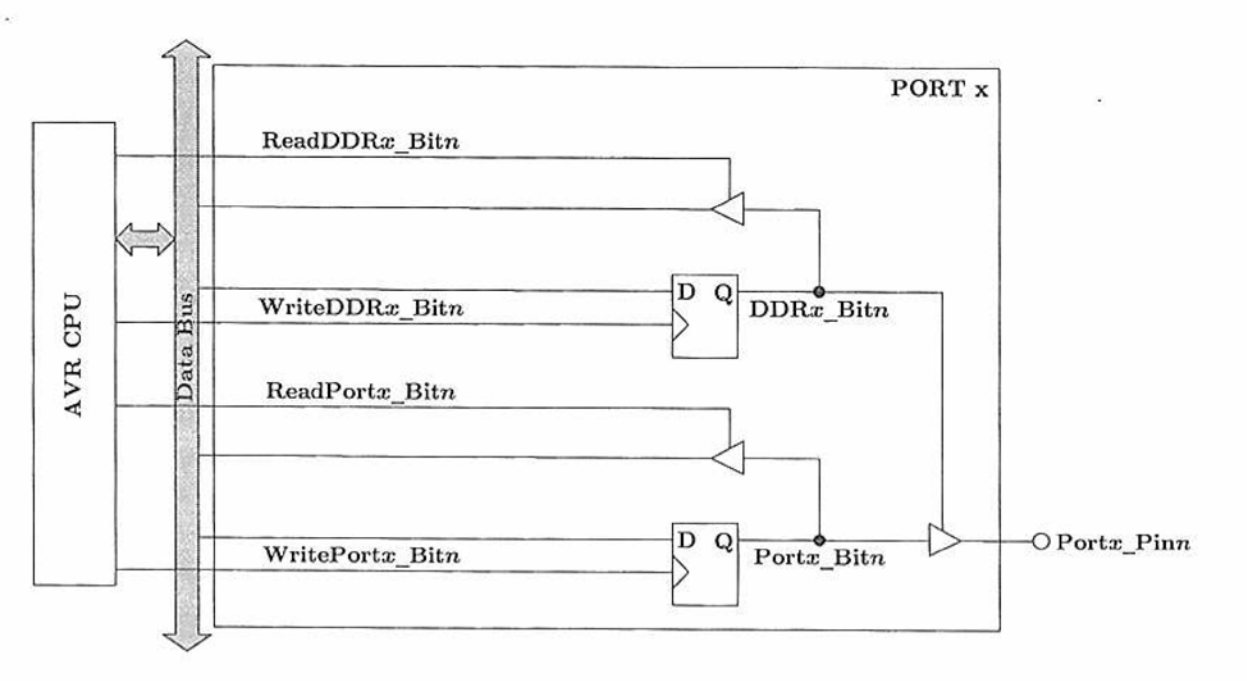
Atmel 328P Block Diagram



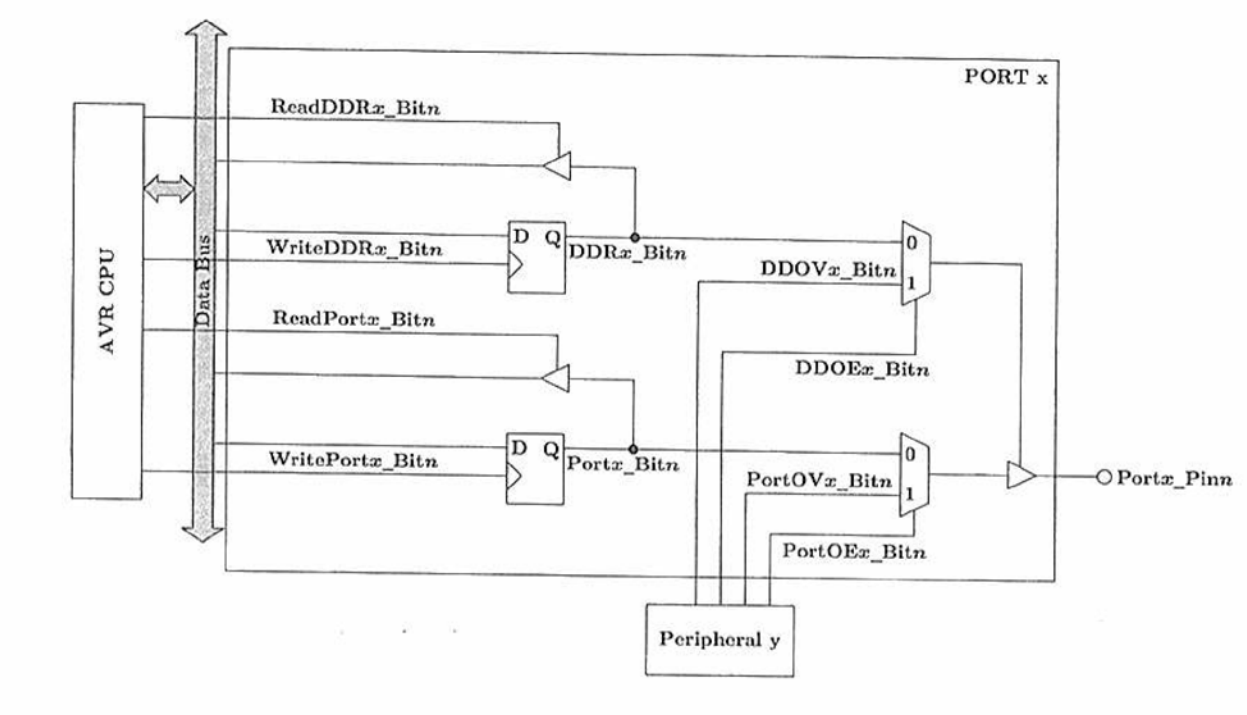
AVR CPU Block Diagram



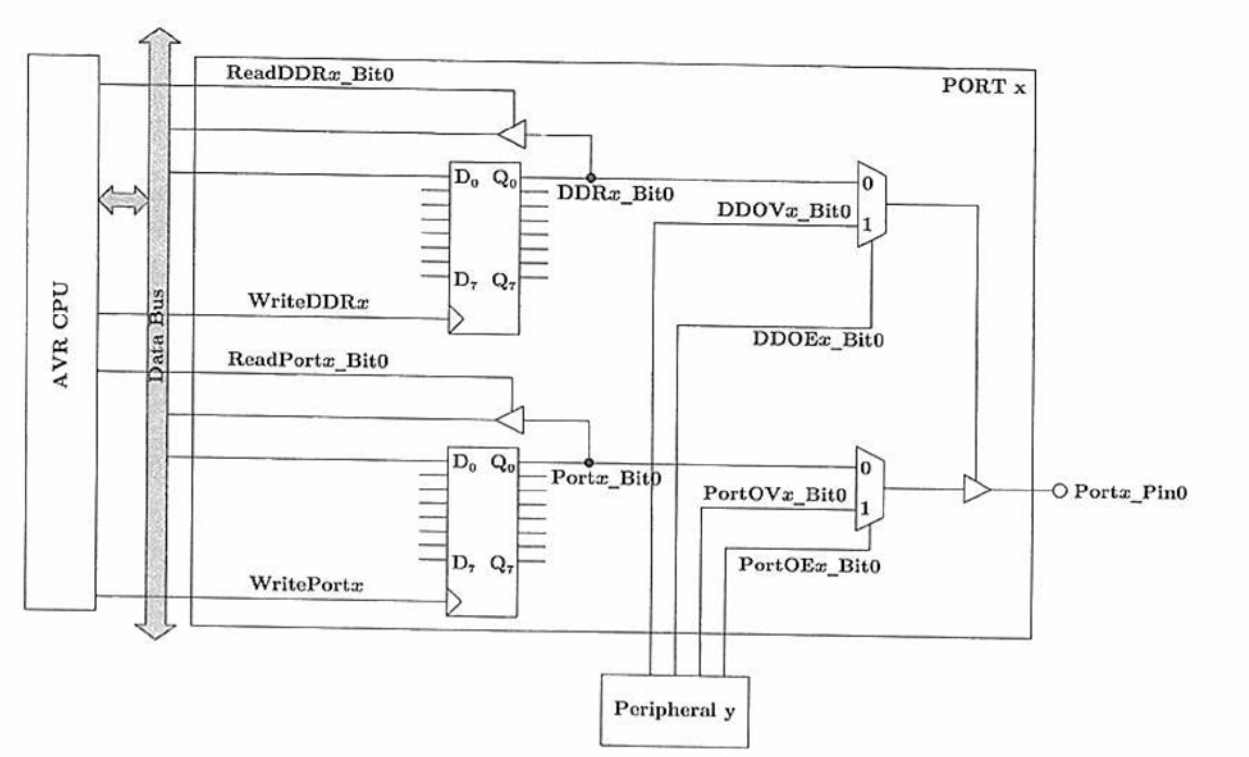
GPIO – Single Output Bit



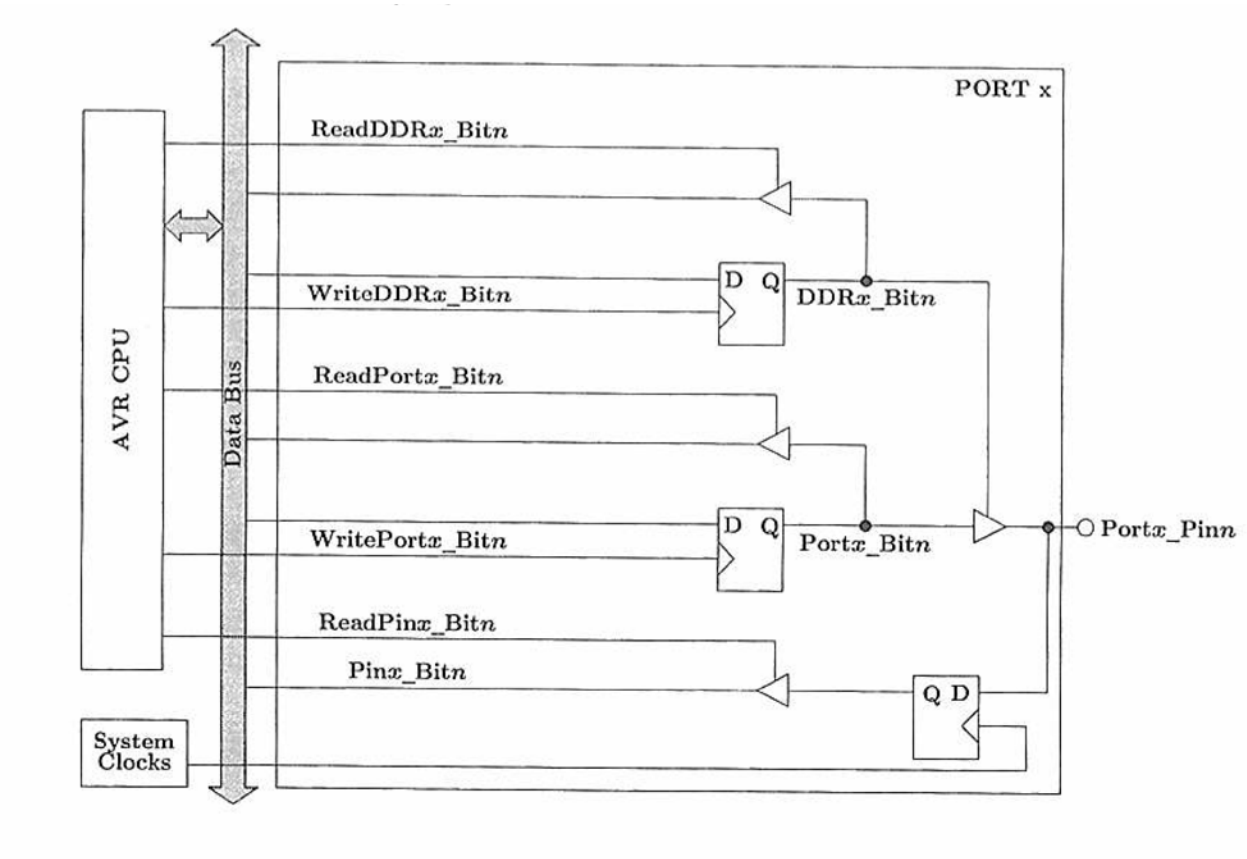
Pin-Muxing


PORT x
AVR CPU
Data Bus
ReadDDRx_Bitn
WriteDDRx_Bitn
D Q
DDRx_Bitn
DDOVx_Bitn
0
1
ReadPortx_Bitn
DDOEx_Bitn
WritePortx_Bitn
D Q
Portx_Bitn
PortOVx_Bitn
0
1
Portx_Pinn
PortOEx_Bitn
Peripheral y

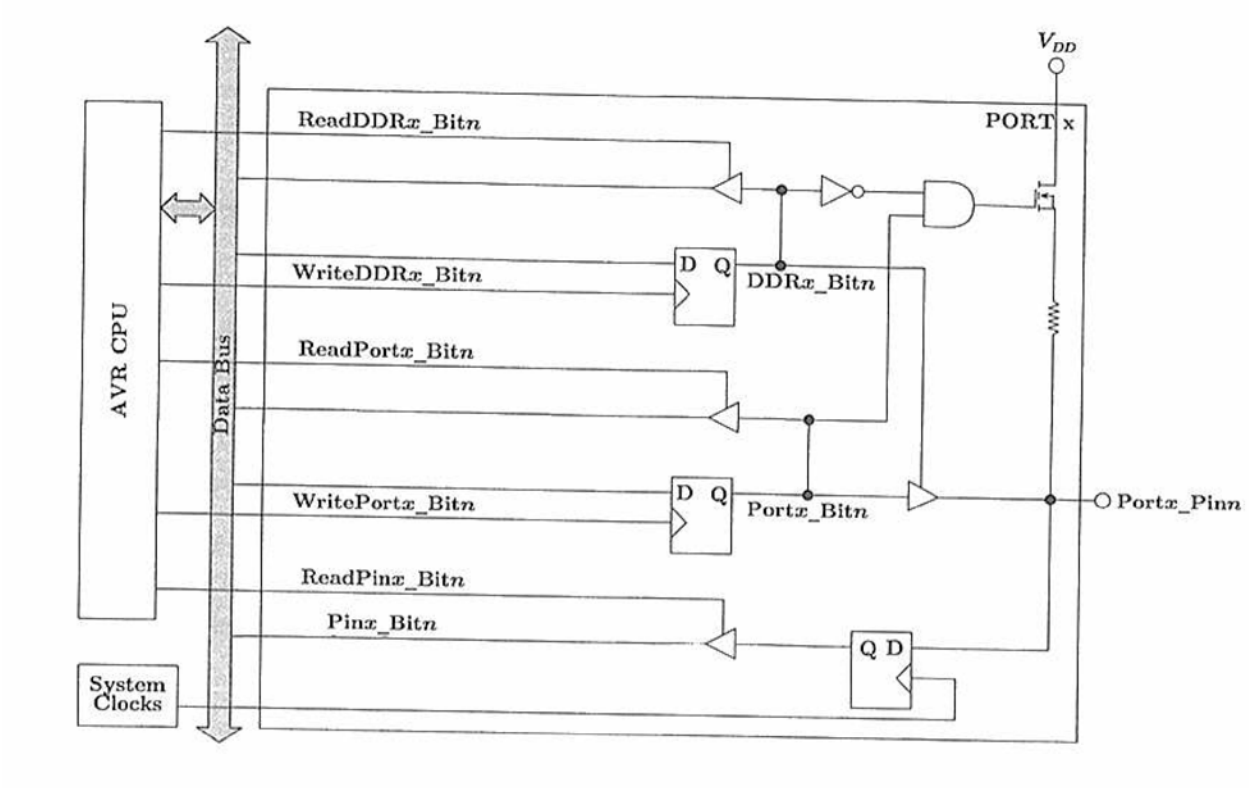
8-Bit GPIO (Output)



Single Bit GPIO Input



GPIO w/ PU


V_{DD}
PORT x
ReadDDRx_Bit$n$
WriteDDRx_Bit$n$
D Q
DDRx_Bit$n$
ReadPort$x$_Bit$n$
WritePort$x$_Bit$n$
D Q
Port$x$_Bit$n$
Port$x$_Pin$n$
ReadPin$x$_Bit$n$
Pin$x$_Bit$n$
Q D
AVR CPU
Data Bus
System Clocks

Pertinent Registers (PORT B Example)

6.4.1 PORTB - THE PORT B DATA REGISTER

Bit	7	6	5	4	3	2	1	0
0x25	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

- PORTB7-0: GPIO data value stored in bit *n*.

6.4.2 DDRB - THE PORT B DATA DIRECTION REGISTER

Bit	7	6	5	4	3	2	1	0
0x24	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

- DDRB7-0: selects the direction of pin *n*. If DDRB*n* is written '1', then PORTB*n* is configured as an output pin. If DDRB*n* is written '0', then PORTB*n* is configured as an input pin.

6.4.3 PINB - THE PORT B INPUT PINS ADDRESS

Bit	7	6	5	4	3	2	1	0
0x23	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0
Read/Write	R	R	R	R	R	R	R	R
Default	-	-	-	-	-	-	-	-

- PINB7-0: logic value present on external pin *n*.

Timer Control Registers

7.3.1 TCCR0A - TIMER/COUNTER0 CONTROL REGISTER A

Bit	7	6	5	4	3	2	1	0
0x44	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

7.3.2 TCCR0B - TIMER/COUNTER0 CONTROL REGISTER B

Bit	7	6	5	4	3	2	1	0
0x45	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00
Read/Write	W	W	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Timer Compare Registers

7.3.3 TCNT0 - TIMER/COUNTER0 REGISTER

Bit	7	6	5	4	3	2	1	0
0x46	TCNT0[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

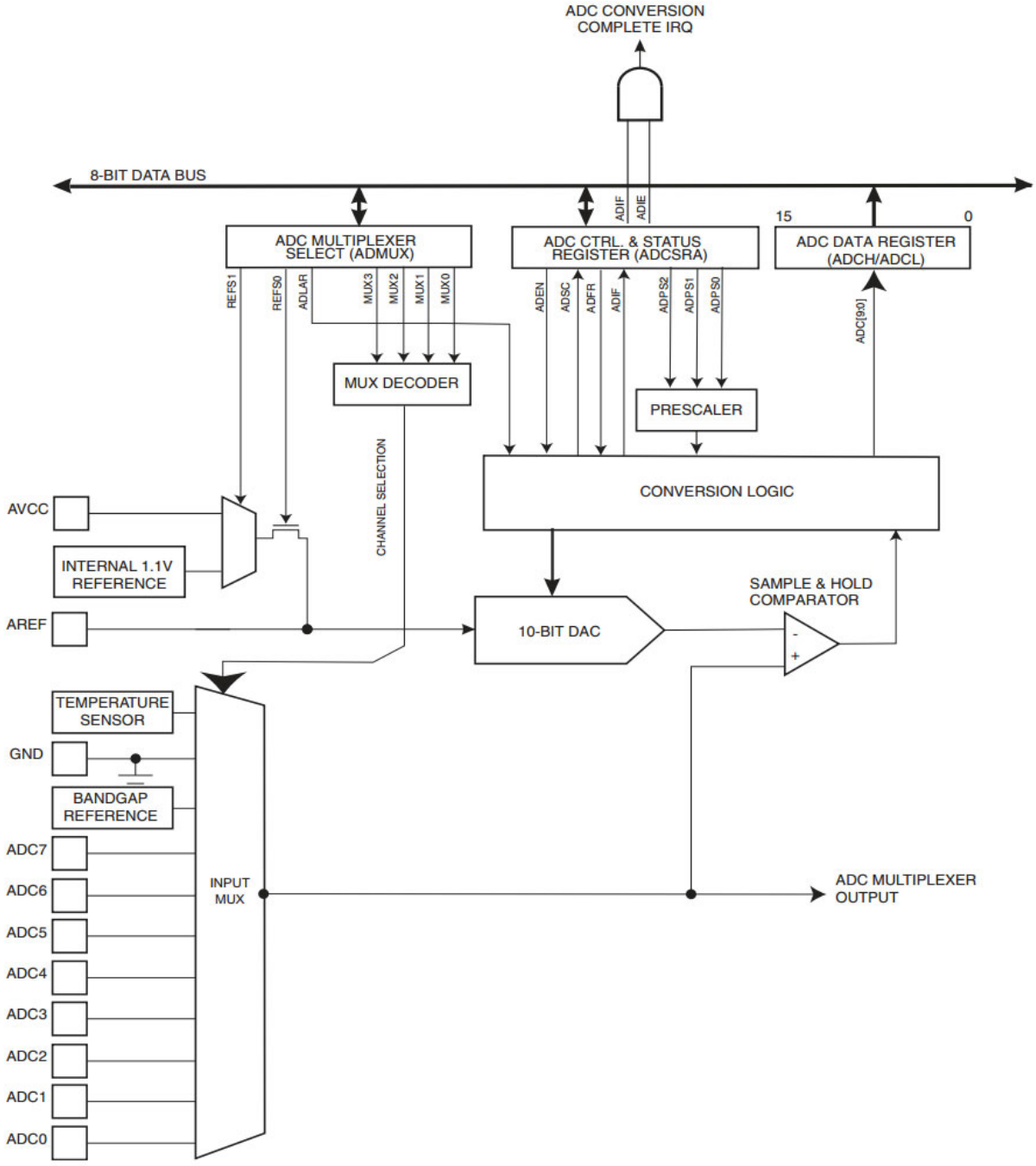
7.3.4 OCR0A - OUTPUT COMPARE0 REGISTER A

Bit	7	6	5	4	3	2	1	0
0x47	OCR0A[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

7.3.5 OCR0B - OUTPUT COMPARE0 REGISTER B

Bit	7	6	5	4	3	2	1	0
0x48	OCR0B[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

ADC Configuration



Analog Input Registers

8.3.1 ADMUX - ADC MULTIPLEXER SELECTION REGISTER

Bit	7	6	5	4	3	2	1	0
0x7C	REFS1	REFS0	ADLAR	-	MUX3	MUX2	MUX1	MUX0
Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

8.3.2 ADCSRA - ADC CONTROL AND STATUS REGISTER A

Bit	7	6	5	4	3	2	1	0
0x7A	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

8.3.3 ADCH AND ADCL - ADC DATA REGISTER

8.3.3.1 ADLAR = 0

Bit	7	6	5	4	3	2	1	0
0x79	-	-	-	-	-	-	ADC9	ADC8
0x78	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

8.3.3.2 ADLAR = 1

Bit	7	6	5	4	3	2	1	0
0x79	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2
0x78	ADC1	ADC0	-	-	-	-	-	-
Read/Write	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

8.3.4 ADCSRB - ADC CONTROL AND STATUS REGISTER B

Bit	7	6	5	4	3	2	1	0
0x7B	-	ACME	-	-	-	ADTS2	ADTS1	ADTS0
Read/Write	R	R/W	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

8.3.5 DIDR0 - DIGITAL INPUT DISABLE REGISTER 0

Bit	7	6	5	4	3	2	1	0
0x7E	-	-	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

8.3.6 ACSR - ANALOG COMPARATOR CONTROL AND STATUS REGISTER

Bit	7	6	5	4	3	2	1	0
0x50	ACD	ACBG	ACO	ACIF	ACIE	ACIC	ACIS1	ACIS0
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Default	0	0	-	0	0	0	0	0

8.3.7 DIDR1 - DIGITAL INPUT DISABLE REGISTER 1

Bit	7	6	5	4	3	2	1	0
0x7F	-	-	-	-	-	-	AIN1D	AIN0D
Read/Write	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0