RUNNING HEAD: Mobile Computing Innovations

Mobile Computing Innovations

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I pledge that this submission is solely my work, and that I have neither given,

nor received help from anyone.

**Abstract**

Mobile computing is an ever advancing field of research which has had a multitude of advancements in recent history. One of the first advancements to happen to mobile computing is ARM architecture. ARM architecture differs from x86-64 architecture in that it only includes fundamental instructions that are needed called RISC. This allows ARM processors to use less transistors for storing instructions reducing power consumption. ARM processors further increase their efficiency through integration in an SoC. This allows ARM processors to be further optimized for all the components included in an SoC. The other innovation that has greatly benefited mobile computing is the upgrade from 32-bit ARM architecture to 64-bit ARM architecture. This upgrade allows ARM processors to utilize more than 4GB of RAM per application and increases efficiency because of the increased register size.

Table of Contents

[Abstract 2](#1%19Abstract%19C)

[ARM Processors 5](#1%19ARM_Processors%19C)

**Introduction**

Mobile computing has seen many advancements throughout recent history. From the first iPhones release to now their have been a multitude of improvements to processing power, battery-life, and new features such as fingerprint sensing. These improvements are enabled by innovations in mobile computing and broader computer processing that have happened since 2000. This paper will analyze mobile computing’s most influential advancements in processing power, and power consumption.

**32-bit Architecture Limitations**

In computer processors there is a type of memory used when directly manipulating data. This is refered to as a register. There are multiple registers in a computer processors with set sizes ranging from 8-bit, 16-bit, 32-bit, 64-bit, and larger by powers of 2. Registers can store instructions, memory addresses, or data types that are being worked with. When referencing 32-bit in terms of computer processors, it is referencing the size in bits of the processors registers. 32-bit registers were the most common size before the mass upgrade to 64-bit registers in computers. Processors have multiple registers, each with an assigned purpose. The register where memory addresses were stored is one of 32-bit architectures major limitation. The memory address register is used to point to a location in random access memory (RAM) which facilitates access to that point in RAM. A 32-bit regirster means that there are 232 unique memory addresses that can be accessed in RAM, which is equivalent to 4GiB of addresses. This means that the size of RAM had a hardware limitation of 4GB on 32-bit architecture. With the onset of 64-bit architecture the limitation of 4GB had been greatly exceeded with the new theortical limit on RAM size being put at 264 bytes, exponentially larger than on 32-bit architecture There is a method to increase the total amount of RAM a computer can use on 32-bit architecture through Physical Address Extension (PAE). PAE operates through virtualizing memory that can be translated into a physical address in memory. PAE uses the virtual address to add an extra layer of translation called the Page Directory Pointer Index (PDPI), which uses 2 bits in the virtual address and and points to page directories. This extra layer of translation which allows a processor to utilize more than 4GB of RAM. The limitation of PAE is that individual applications are still limited to 4GB of RAM (2009).

**ARM Processors**

Computers have two main types of instruction sets that can be used depending on a specific use case. The two types are the x86 architecture and ARM architecture. Each of the two processors have their costs and benefits which make them stonger in some sectors than others. ARM processors are Restricted Instruction Set Computers (RISC), which are designed to work with simple instructiions where all instructions are the same size in memory. X86 processors are Complex Instruction Set Computers (CISC) where the instructions are a variety of sizes in memory and complexity. An example of a complex instruction in CISC is the MULT instruction, which can be replicated in RISC with the use of three separate instructions (*RISC vs. CISC*, n.d.). CISC processors include many instructions in its architecture which go widely unused. Since RISC instructions are much simpler than CISC instructions, only fundamentally nessasary instructions are included in the architecture. The simplicity of RISC instructions causes programs built on top of RISC to be larger in size than an equivalent CISC program. This is because multiple RISC instructions are needed to perform the same function as one CISC instruction (Aroca & Gonçalves, 2012).

**ARM Power Efficiency**

One advantage that ARM processors have over x86 is power efficiency. There are multiple design features that allow this this. The first and most important one being ARM architectures integration with its internal components. To illustrate this it is best to understand x86 bridges. A x86 processor is connected to outside chips like the GPU, I/O, and etc. through bridges. This is in contrast to ARM processors which are deeply integrated under one chip called a SoC (System on a Chip). This is one of the x86 architectures trade offs with the ARM architecture, where x86 gains in modularity it loses in integratibility. This difference among others allows ARM processors to be optimised for the components included in the chip, increasing power efficiency over its x86 counterpart (Aroca & Gonçalves, 2012). This is why ARM Processors are heavily used in mobile phones and laptops.

Another reason ARM architecture is more efficient is its use of the RISC instruction set. This is because RISC includes fewer instructions, that are more efficient because they are designed to execute in a single clock cycle. RISC processors require less transistors because of the lack of legacy instructions, which by logical extension means lesser power requirements (*RISC vs. CISC*, n.d.).

**SoC**

SoC architectures are the backbone mobile devices. Like said previously, they leverage their ARM architecture, along with complete system integration, to produce high performance, low power designs for mobile computing. A SoC will typically integrate a GPU, RAM, and CPU under one chip. This requires less space than a design with separate, GPU, RAM, and CPU chips, and is more reliable due to full system integration (*Chipset and System-on-a-Chip (SoC) Reference for Intel® NUC. . .*, n.d.).

**64-bit ARM**

One innovation that has occurred in recent years is 64-bit ARM processors (“ARM Targets Server Designs with ‘first’ 64- Bit Processor.,” 2011). In 2011 ARM released details over its new ARMv8 architecture, which included a set of 64-bit instructions, along with a set of 32-bit instructions. At the most basic level 64-bit architecture allows for processing of larger chunks of data, due to the doubling in register size from 32-bit architecture. This combined with ARM architectures high efficiency compared to x86-64 architecture and the exponential increase to the RAM size limit creates the perfect environment for advancements in mobile computing. This is why all modern mobile processors are based on ARM architecture (PratapSingh & Kumar Jain, 2014).

**Conclusion**

Mobile computing has gone through many innovations since 2000. One notable innovation being the usage of ARM architecture. ARM processors use RISC, more simple, optimized instruction set to achieve high efficency. This allows RISC processors to use less battery life than a CISC processor, making RISC architecture the perfect choice for mobile devices. Another notable innovation that occurred in the mobile phone market, and broadly computing in general, was the upgrade from 32-bit to 64-bit architecture, refering to the size of the registers. This allowed for more efficient processing of larger datatypes, such as longs. This also allowed computer programs to use more than 4GB of RAM, which was caused to a 32-bit hardware limitation. When ARM released a 64-bit instruction set, it allowed mobile processors to take advantage of the benefits of 64-bit computing.