Aiden Fox Ivey

519-574-5740 | aiden@aidenfoxivey.com | linkedin.com/in/aidenfoxivey | github.com/aidenfoxivey

Education

University of Waterloo Sep 2021 – May 2026
Bachelor of Applied Science in Computer Engineering Waterloo, ON

Experience

Tristero Jan 2024 – May 2024
Software Engineer | *Go, Python, FastAPI, SQL* (Remote) USA

- Recommended and implemented the adoption of a robust key derivation function (KDF) in the runtime, significantly enhancing cryptographic security.
- Optimized fly.io deployment pipeline, reducing Docker image build time by 90% (from 7.3 to 0.7 seconds).
- Developed a custom git history analysis tool to detect and report inadequately obfuscated private keys, enhancing repository security, finding over 5 exposed private keys.

Cosine Networks Apr 2023 - Aug 2023
Firmware Developer | *Rust, Swift* Waterloo, ON

- Engineered a cross-platform Rust library with Swift FFI, enabling seamless native GUI applications across iOS, macOS, and Windows.
- Showcased an innovative Wireguard-based security system to potential investors at Collision Conf. 2023.
- Developed a high-performance router authentication server using asynchronous Rust and gRPC protocols.
- Implemented and cross-compiled a Rust-based OpenWRT module for MIPS64 architecture, expanding firmware capabilities.

Huawei Sep 2022 - May 2023
Network Researcher | *Python, C++, Docker, PyTorch* Markham, ON

- Developed and presented MLACC, a novel network traffic analysis tool, at APNET23 conference.
- Applied PyTorch and SciPy to analyze link-level network traffic patterns, enhancing understanding of flow dynamics.
- Optimized WebRTC testbench, reducing codebase size by 17% while maintaining full functionality.

Government of Ontario Jan 2022 - Apr 2022
Developer | *Python, PyTorch, Tesseract OCR, Java* Toronto, ON

- Developed an advanced document scanning and classification system using machine learning techniques.
- Implemented an RNN-based tool with PyTorch, achieving 15% higher accuracy and 5% fewer false positives compared to the proprietary alternative.
- Engineered robust image processing algorithms to align and clean scanned documents, enhancing OCR accuracy.
- Integrated Google's Tesseract for OCR, optimizing the pipeline for efficient document digitization and classification.

Projects

Custom CRC8 ASIC | *Verilog, Python*

- Designed an application specific integrated circuit (ASIC) that combinationally generates the CRC-8 checksum of the input bits using Verilog and Python.
- Submitted ASIC design to be TinyTapeout to be printed on a wafer in November 2024.

Lox Tree Walk Interpreter | *OCaml*

- Created a tree walk interpreter for the language Lox using OCaml.
- Implemented support for garbage collection, closures, and scoped variables.

Open Source

Contributed to LLVM, CPython, Sublime Package Manager, Zig, Construct. View at github.com/aidenfoxivey.

Technical Skills

Languages: Python, Go, Rust, Java, SQL, OCaml, C, C++, ARM Assembly, VHDL, SystemVerilog
Tools: React, Node.js, Flask, ExpressJS, FastAPI, PyTorch, LLVM, Docker, Github Actions, AWS