MANAGEMENT AND ANALYSIS OF PHYSICS DATASET (MOD. A)

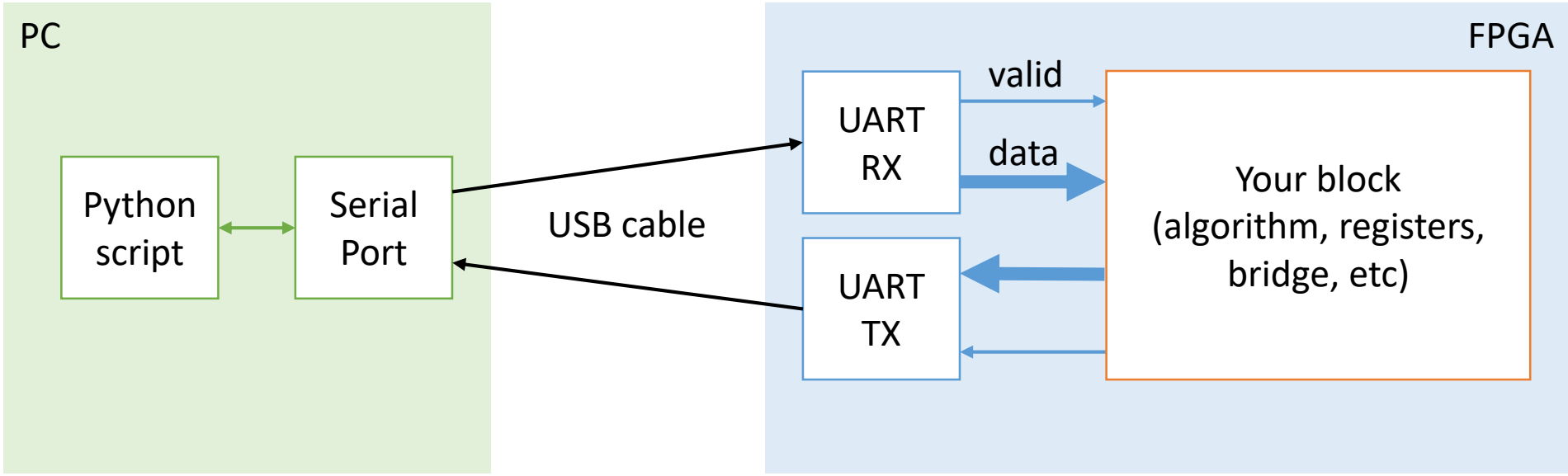
Exam

Oral Exam

- Discussion of a technical report
  - Every group should prepare a short report on a project chosen by the group itself (please try to coordinate among groups)
  - Relevant part of VHDL code can be attached
  - It should be sent to the teachers at least 3 days before the day of the exam
  - It will be discussed at the exam
  - If the code has bugs is not an issue, what matters most is that you show that you are able to use properly VHDL and you have tackled the problem in a consistent way -> VHDL is an hardware description language
- Discussion of a selected paper
  - Each student should study and present a paper
  - Every student of a group should discuss a different paper

Projects

- All the proposed projects need the UART



- They have different difficulty levels -> they will be evaluated accordingly

Algorithms

- Implement one algorithm typically used in the low level processing of physical data
- Exercise it with a test dataset (channel number, timestamp, amplitude…)
- Compare the results with a python simulation

1. Coincidences in a sliding time window
   - Simple multiplicity on different channels
   - Delayed coincidences
   - Multiple partitions
2. Sorting
   - For instance Sorting network, Bubble sort…
   - Any other algorithm?
   - Discussion on tradeoff latency/resources
3. Digital filter
   - For instance FIR
   - Any other algorithm?
   - Discussion on tradeoff latency/resources

Registers

- Implement a set of register that can be controlled by python scripts via UART
- Implement Read/Write operations
- Registers are locally stored in the FPGA and are used as memory or mapped to I/O (led, switch, etc)
- Discussion on multi-register transfer (buffer)
- Discussion on single bit modification
- Discussion on concurrent access

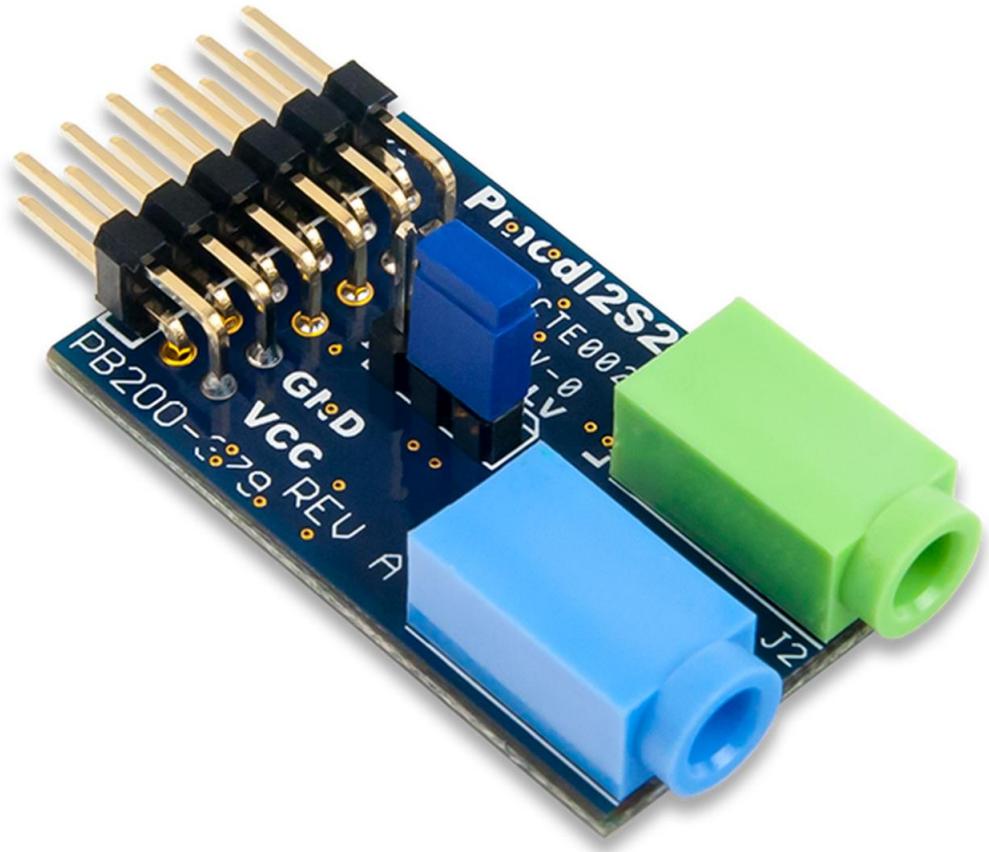
Read/Write Flash Memory

- Serial Peripheral Interface protocol
  - Serial
  - Synchronous
- Flash memory is a SPI slave and FPGA the master
- Read and Write instructions are implemented at the application layer

- Implement a UART to SPI bridge (data received by UART are sent to SPI and vice versa)
- Program the flash memory with Vivado (indirect programming) and verify its content
- Write some data on the flash memory and read them back

PMOD Audio

- Stereo input and output
- A/D Converter
- D/A Converter
- I2S protocol to FPGA
- Pass through reference design
- https://digilent.com/reference/pmod/pmodi2s2/start



- Signal processing filters (e.g. FIR)
- Audio slow down effect (decimation)
- Eco effect