Management and analysis of physics datasets, Part. 1

Seventh Laboratory

Antonio Bergnoli bergnoli@pd.infn.it
14/12/2021

Laboratory Introduction
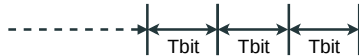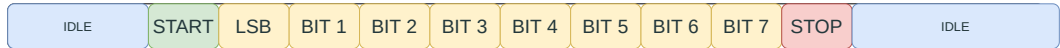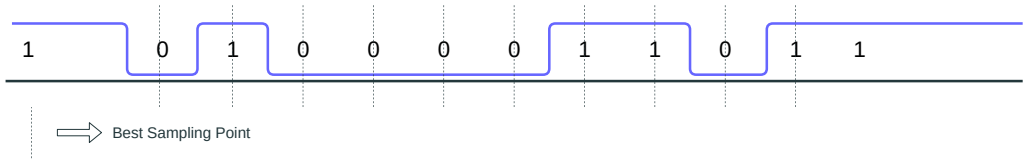
- Build the UART receiver unit

Uart Receiver

The bits are recovered by sampling at the best sampling point: the middle of the baudrate period

Transmit Character 'a' (ASCII CODE hexadecimal: 61, binary: 01100001) at 115200 Bit/second, no parity bit

| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

⟹ Best Sampling Point

| IDLE | START | LSB | BIT 1 | BIT 2 | BIT 3 | BIT 4 | BIT 5 | BIT 6 | BIT 7 | STOP | IDLE |

Tbit | Tbit | Tbit

Tbit=1/115200 s = 8,68 us

The UART receiver consists of two main modules:

- The sampler generator
- The main state machine module
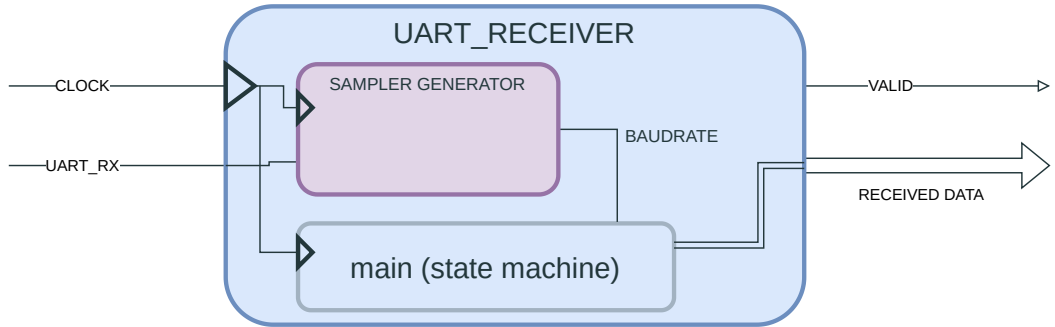
The Sampler Generator module is needed to provide the main UART receiver module with the data sampling pulses.

Like the trasmitter needed the Baudrate generator to transmit the UART bits, now the pulse generator dœs the same thing, but the pulses are now needed to sample the incoming bits.

The Sampler Generator

Just like the UART transmitter main module, the sampler generator is made up of 3 different submodules:

- The pulse generator
- The state machine
- the delay line

The behaviour of the sampler generator is the following:

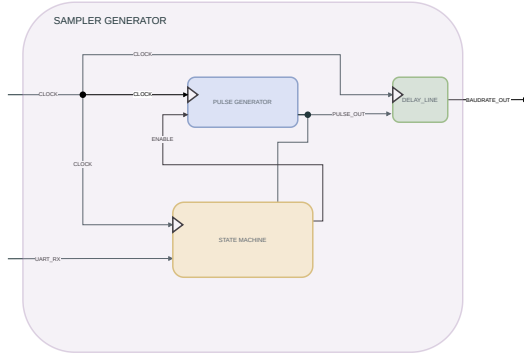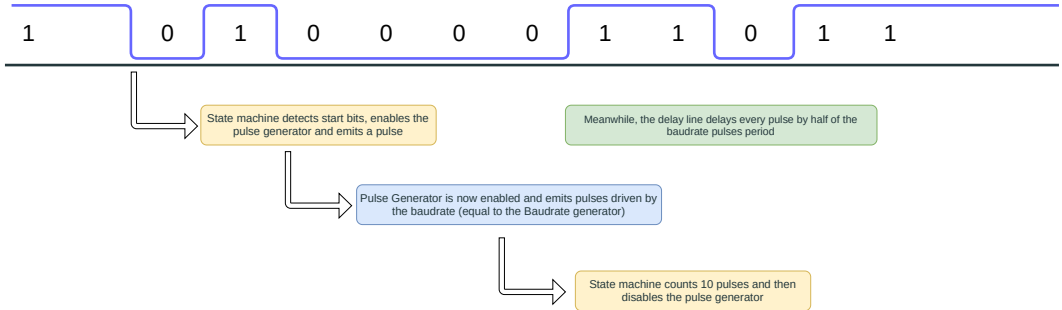Transmit Character 'a' (ASCII CODE hexadecimal: 61, binary: 01100001) at 115200 Bit/second, no parity bit

| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

State machine detects start bits, enables the pulse generator and emits a pulse

Meanwhile, the delay line delays every pulse by half of the baudrate pulses period

Pulse Generator is now enabled and emits pulses driven by the baudrate (equal to the Baudrate generator)

State machine counts 10 pulses and then disables the pulse generator

- Design the Sampler Generator module and simulate it
- Design the UART Receiver module and simulate it