Lab session

Agenda

- Introduction
- Lab1 □ LTspice familiarity
- Lab2 □ SRAM cell simulation
- Lab3 □

Introduction

- Tool : LTSPICE
- Model files : Arizona State University PTM
  - 16nm PTM-MG HP NMOS, HP PMOS
  - NFET : http://ptm.asu.edu/modelcard/PTM-MG/modelfiles/hp/16nfet.pm
  - PFET : http://ptm.asu.edu/modelcard/PTM-MG/modelfiles/hp/16pfet.pm
- Nominal supply : 850mV
  - Supply variation : +/-10%
- Channel length : 20nm (Min : 10nm ; Maximum : 30nm)
- Width :
  - For a planar FET ; width is a number
  - For a Fin FET ; width is number of fins

Width of finfets

Effective Channel Width = (2 * Height of Fin) + Thickness of the fin

W= (2*w1) + w2

hfin= 2.6e-008 ; 26nm=w1
tfin= 1.2e-008 ; 12nm=w2

For 16nm ; for a single fin device
Device width = 64nm
Total width of an ‘n` fin device : n*64nm

We have to do this because LT spice does not understand finfet width or atleast I could not find it.

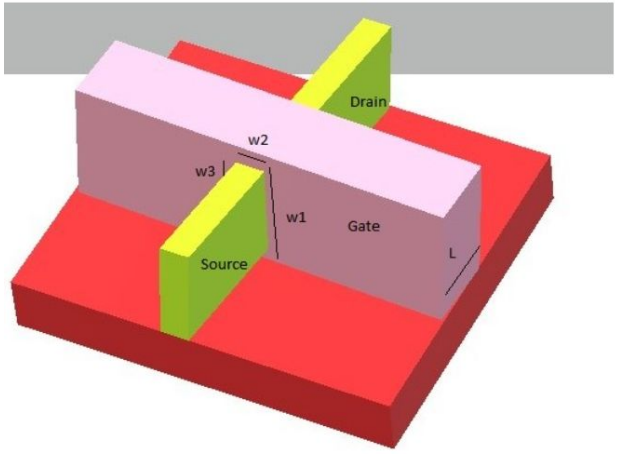
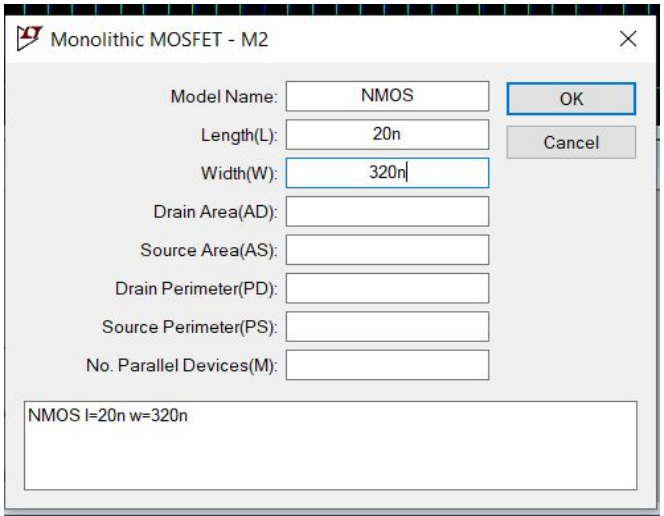


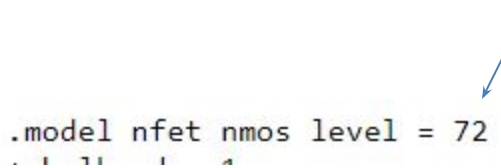
Figure 1: Structure of FinFET

http://www.signoffsemi.com/finfet/

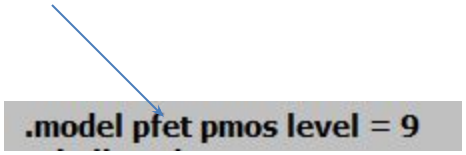


Models

- PTM models are BSIM CMG level 72 models
- LTSPICE does not understand level 72



- Change this to level 9



- Use spice directive to include model files

Questions

Lab1

LAB 1

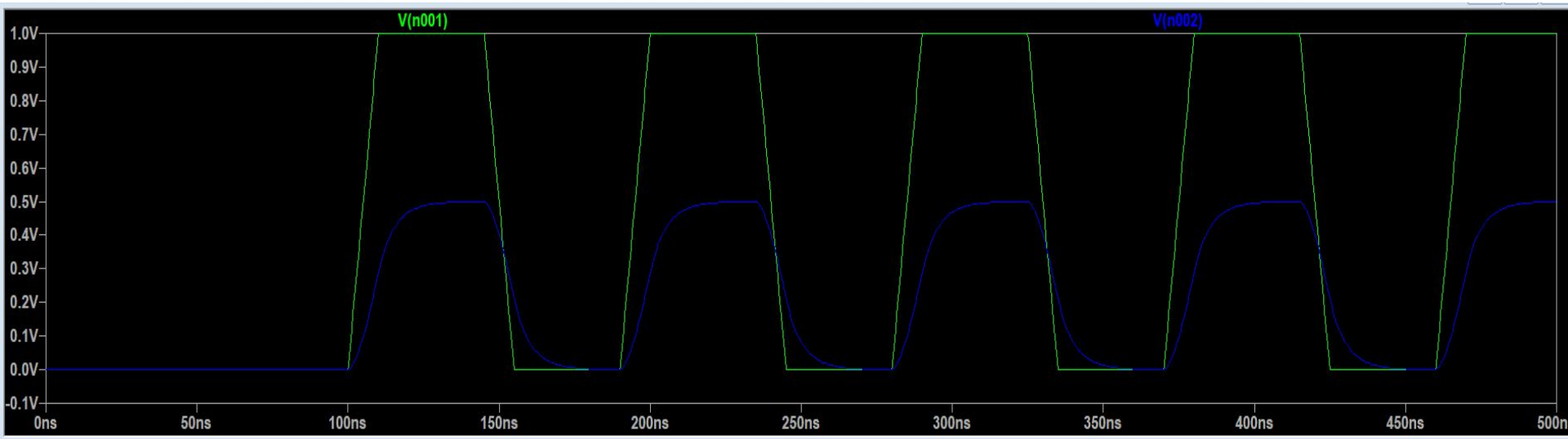
Agenda

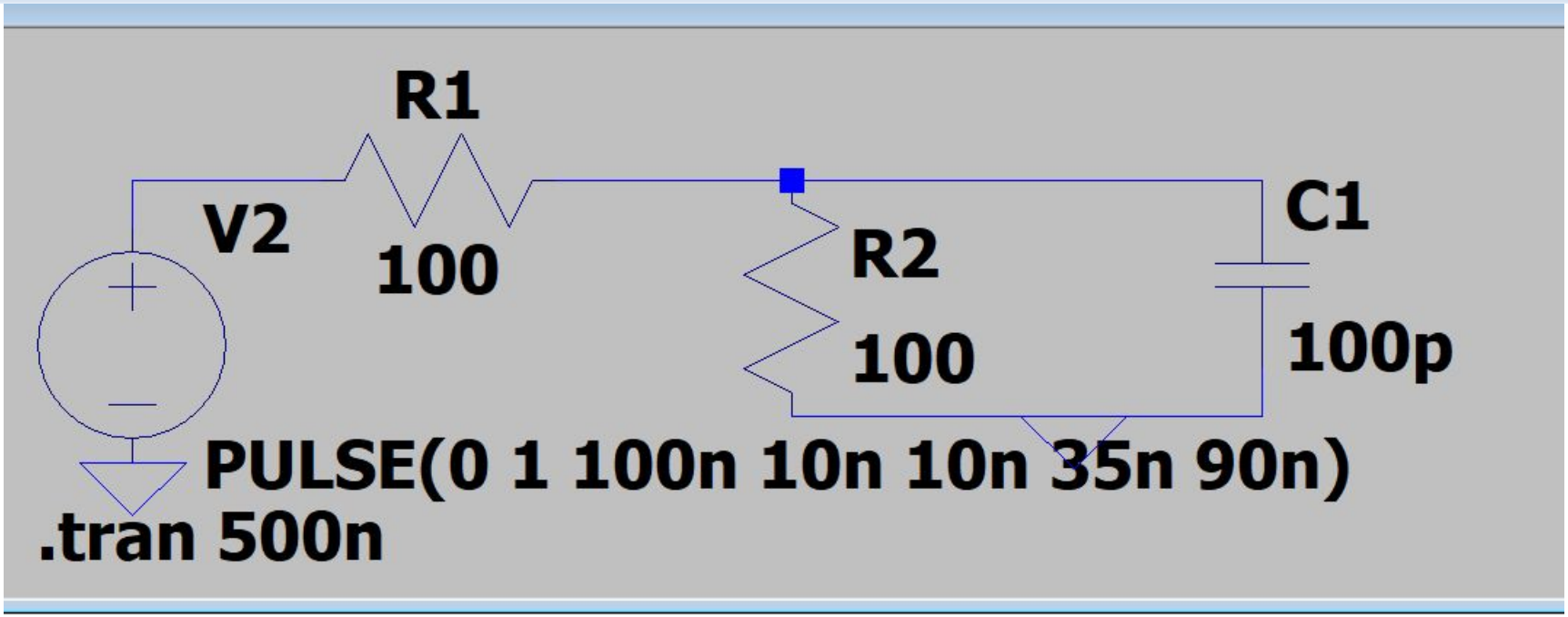
- Understand basic analysis types in LTSpice
- Run an inverter transient and DC analysis
- Assignment :
  - Calculate power of a nominal sized inverter driving a load of 1fF /5fF
  - Calculate Fan out of 1 (FO1) and Fan out of 4 (F04) delay of nominally sized inverter at nominal and +/-10% supply
  - Calculate leakage power of a 50fin inverter and compare it with a 22nm planar FET inverter of same width

Analysis type

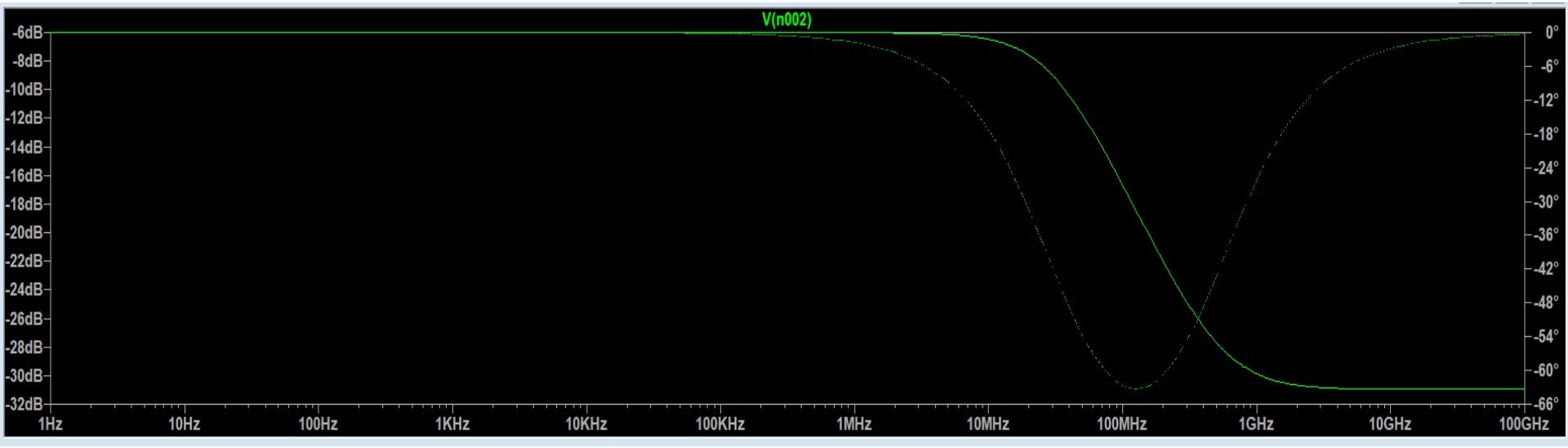
- Ltspice supports following analysis types
  - Transient
    - We will be using this in most of our work.
  - DC
    - A bit to find dc-operating points
  - AC
    - Gain analysis

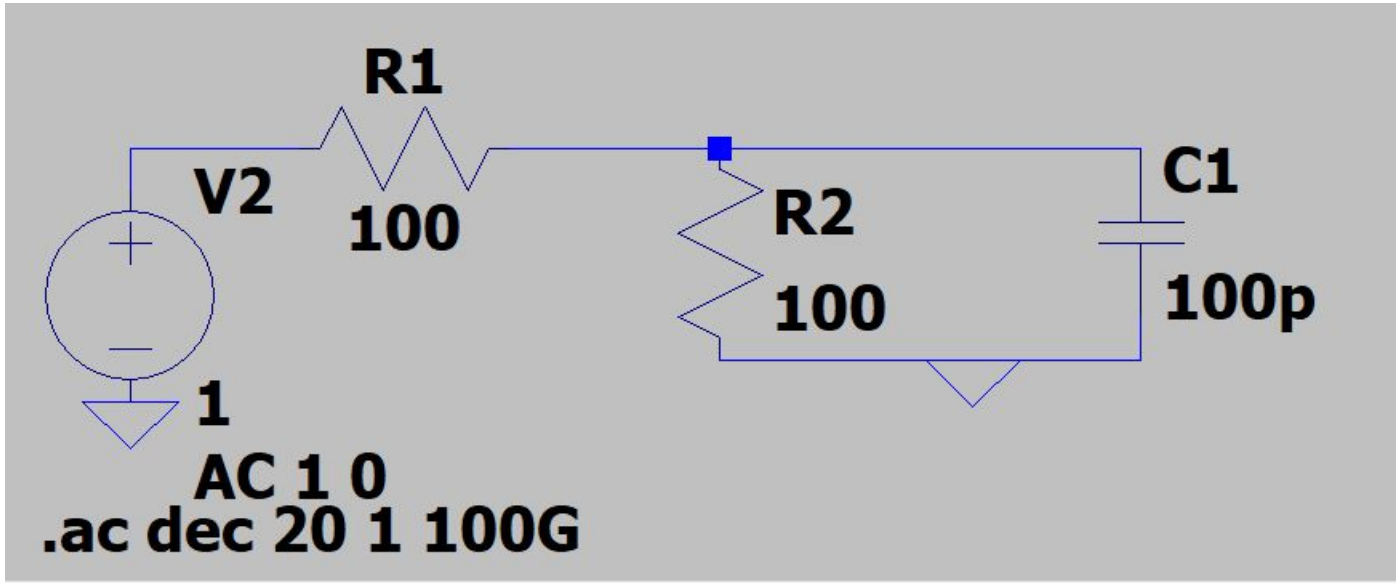
Simple RC circuit (Tran)



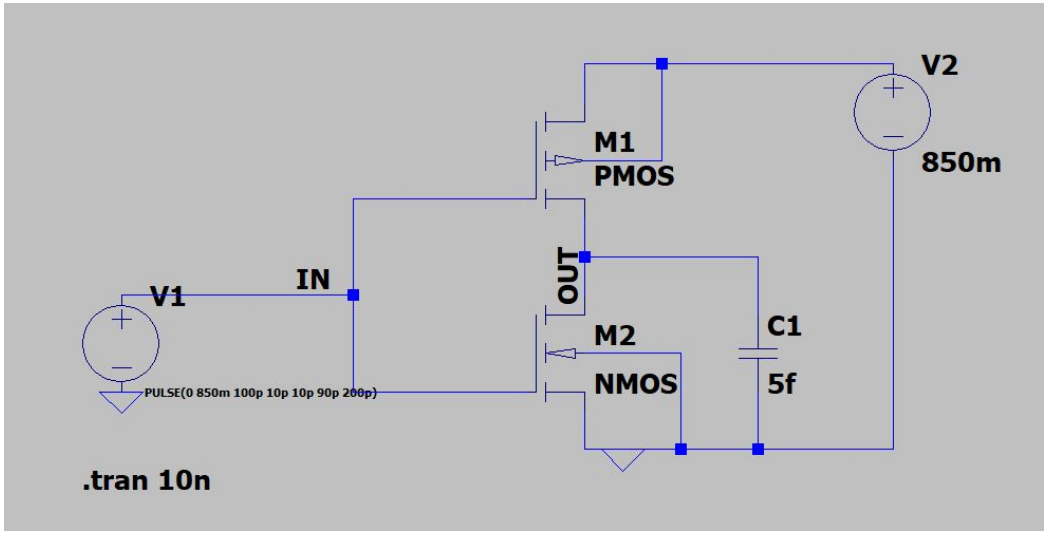


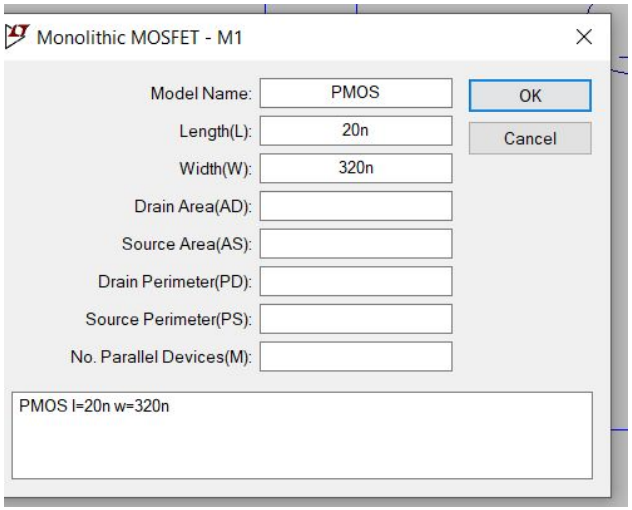
Simple RC circuit (AC analysis)

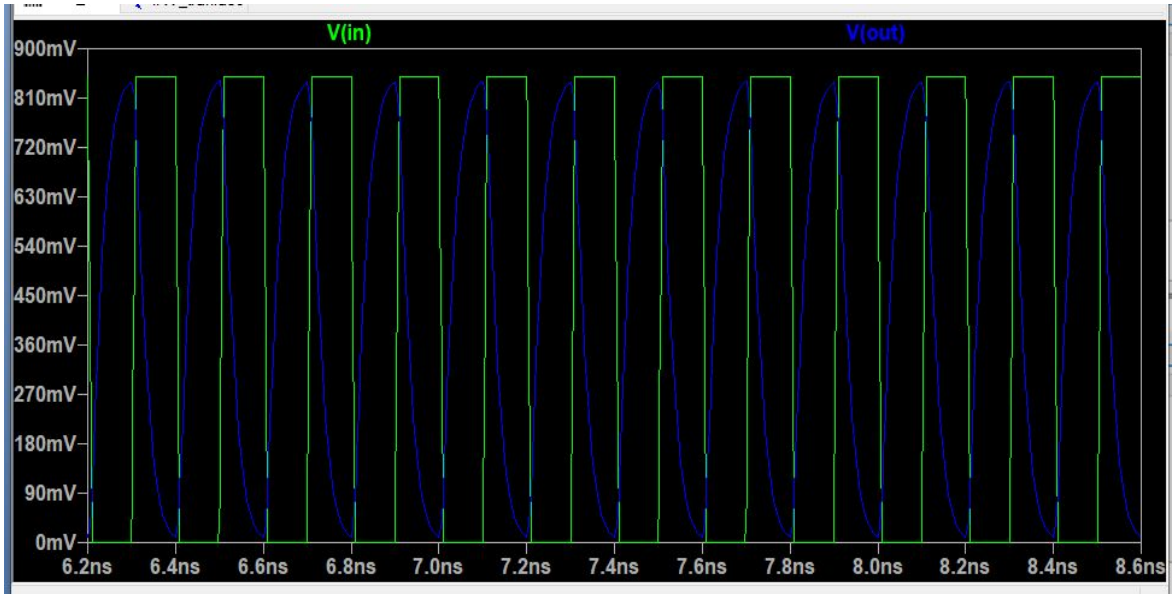


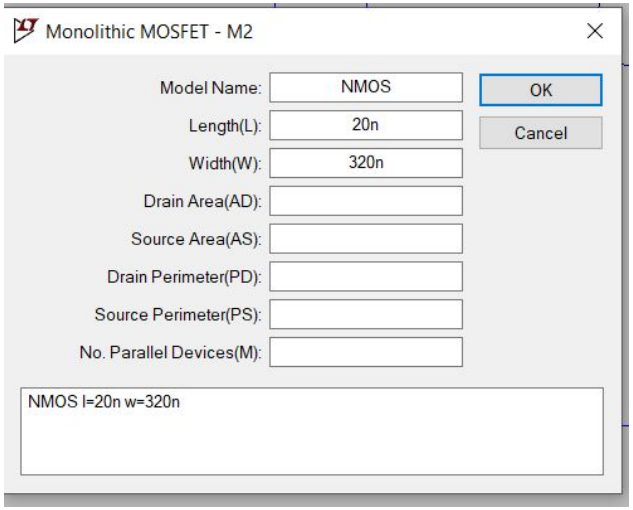


Inverter (tran)

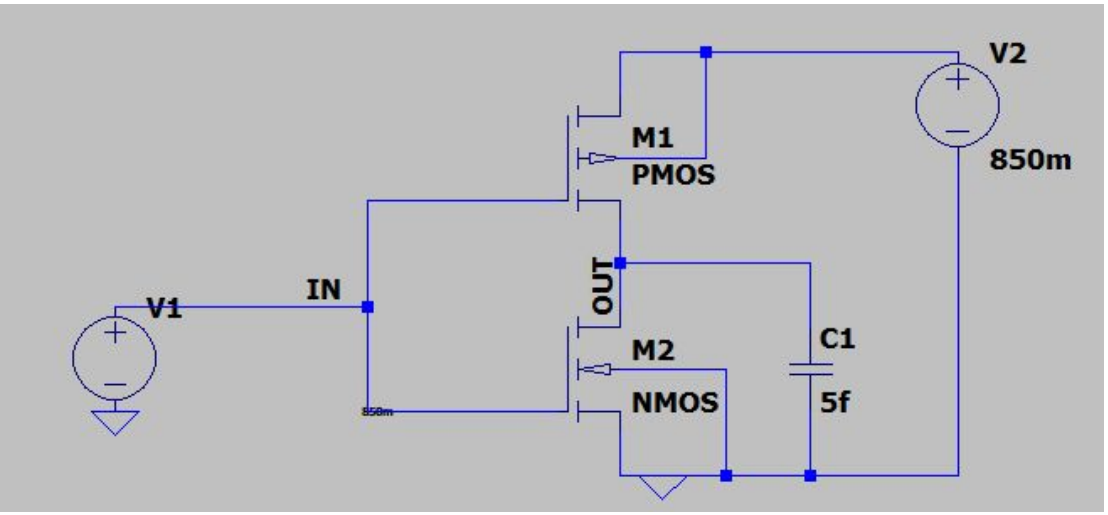


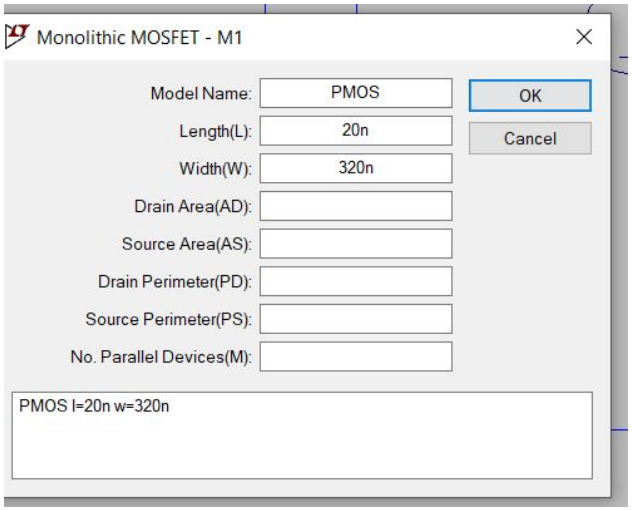


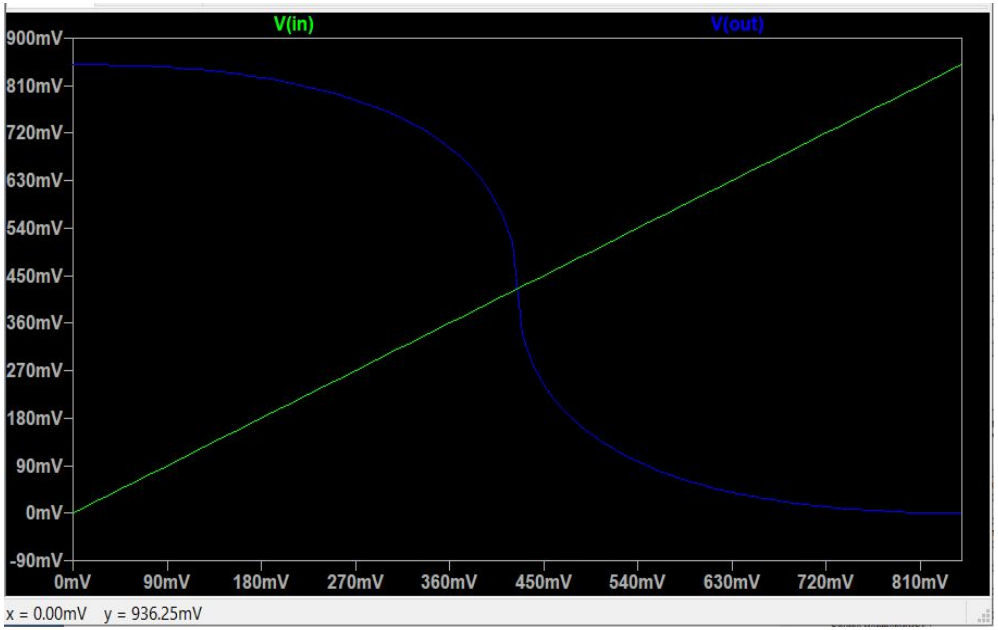


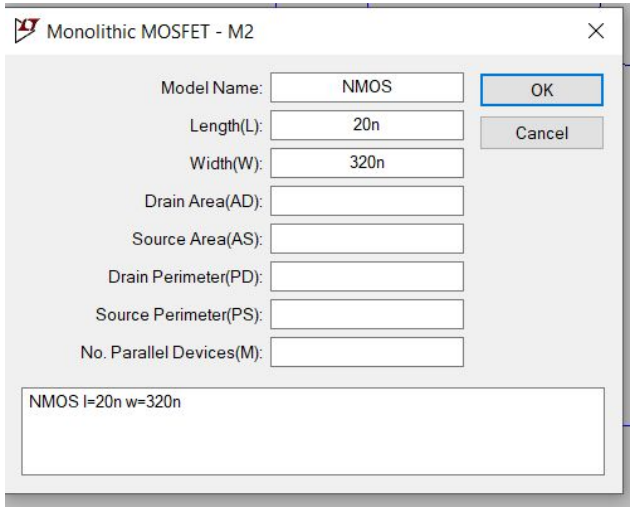


Inverter (dc)

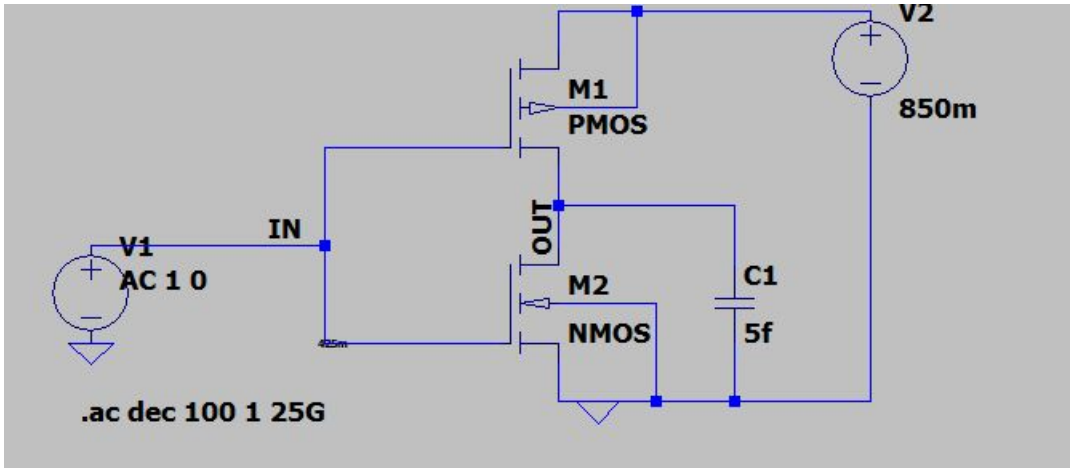

V2
850m
M1
PMOS
IN
V1
OUT
M2
NMOS
C1
5f
850m

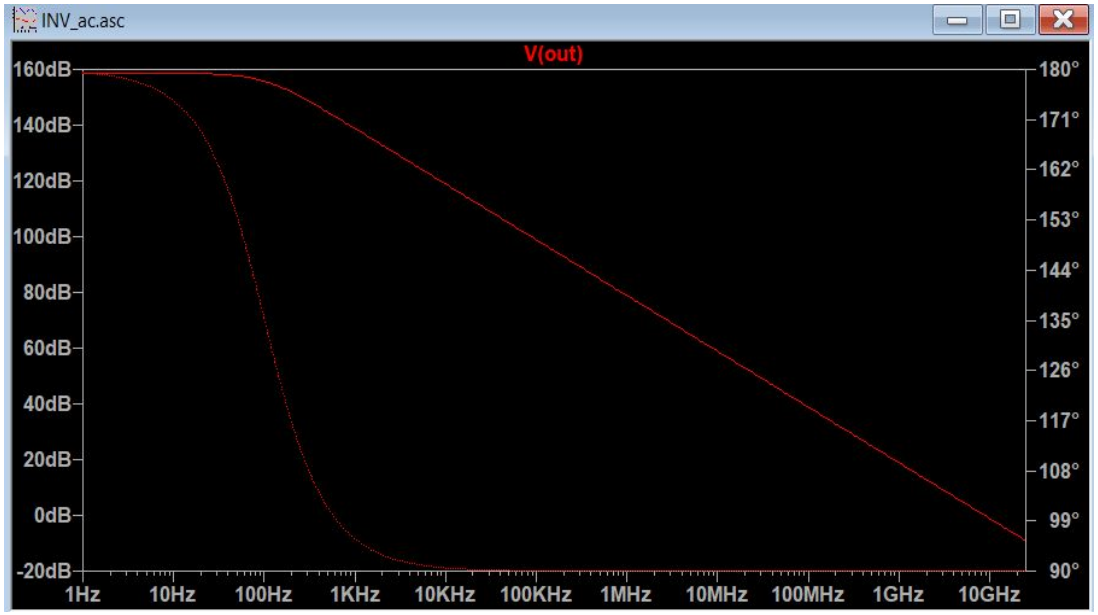

Monolithic MOSFET - M1
Model Name: PMOS
Length(L): 20n
Width(W): 320n
Drain Area(AD):
Source Area(AS):
Drain Perimeter(PD):
Source Perimeter(PS):
No. Parallel Devices(M):
OK
Cancel
PMOS l=20n w=320n

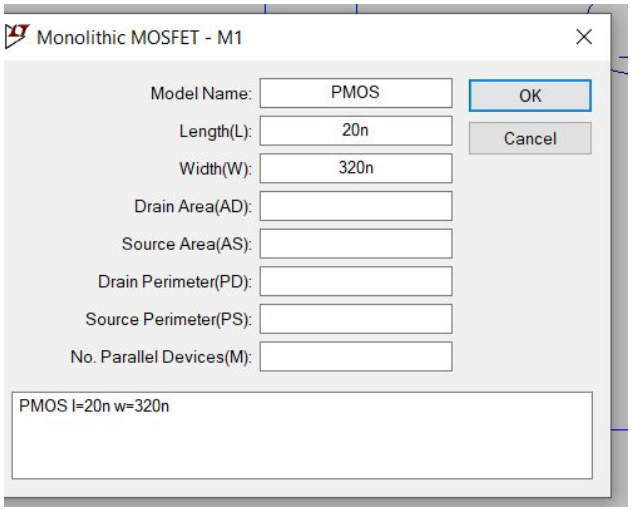

V(in)
V(out)
900mV
810mV
720mV
630mV
540mV
450mV
360mV
270mV
180mV
90mV
0mV
-90mV
0mV
90mV
180mV
270mV
360mV
450mV
540mV
630mV
720mV
810mV
x = 0.00mV y = 936.25mV

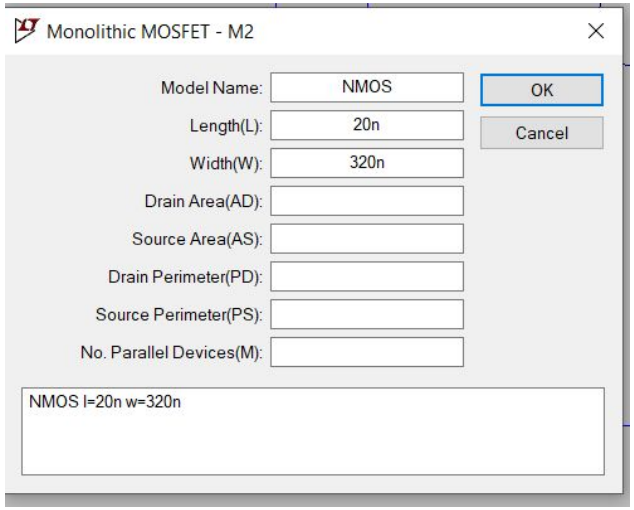

Monolithic MOSFET - M2
Model Name: NMOS
Length(L): 20n
Width(W): 320n
Drain Area(AD):
Source Area(AS):
Drain Perimeter(PD):
Source Perimeter(PS):
No. Parallel Devices(M):
OK
Cancel
NMOS l=20n w=320n

Inverter (ac)


V2
850m
M1
PMOS
IN
OUT
V1
AC 1 0
M2
NMOS
C1
5f
.ac dec 100 1 25G


INV_ac.asc
V(out)
160dB
140dB
120dB
100dB
80dB
60dB
40dB
20dB
0dB
-20dB
180°
171°
162°
153°
144°
135°
126°
117°
108°
99°
90°
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
100MHz
1GHz
10GHz


Monolithic MOSFET - M1
Model Name: PMOS
Length(L): 20n
Width(W): 320n
Drain Area(AD):
Source Area(AS):
Drain Perimeter(PD):
Source Perimeter(PS):
No. Parallel Devices(M):
OK
Cancel
PMOS l=20n w=320n


Monolithic MOSFET - M2
Model Name: NMOS
Length(L): 20n
Width(W): 320n
Drain Area(AD):
Source Area(AS):
Drain Perimeter(PD):
Source Perimeter(PS):
No. Parallel Devices(M):
OK
Cancel
NMOS l=20n w=320n

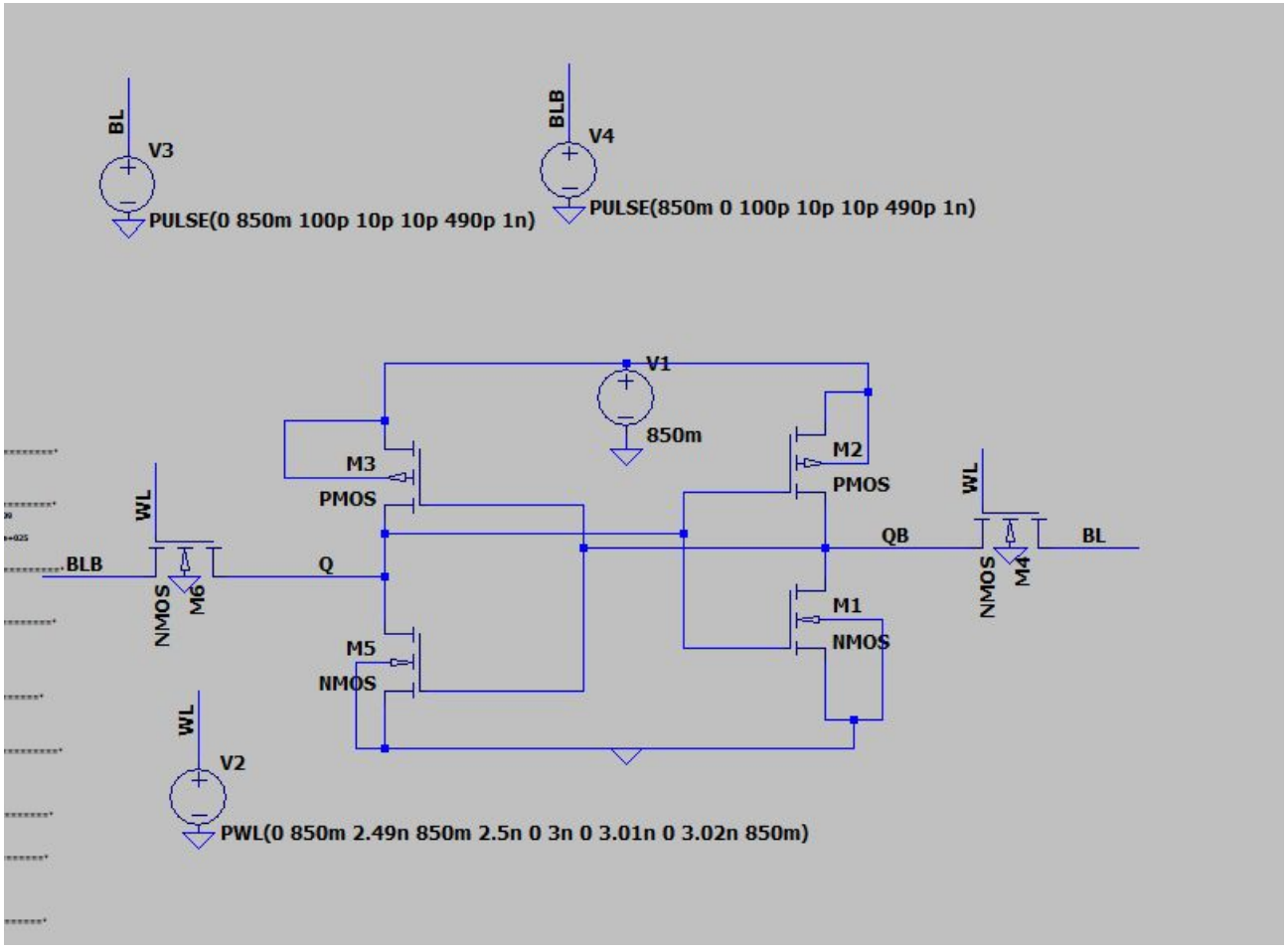
Pending items

- Create symbol
- Use symbol for analysis

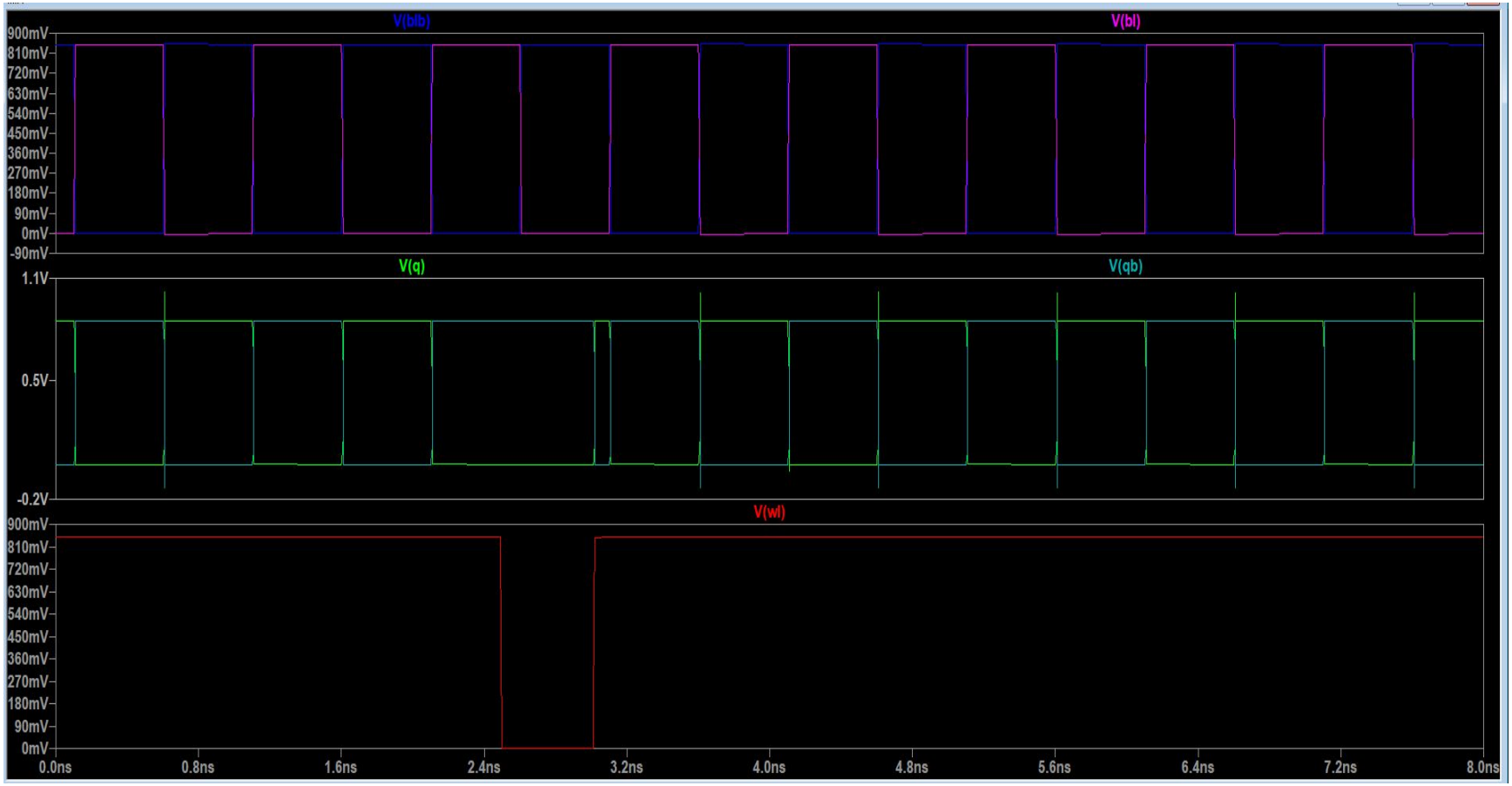
6T SRAM cell

LAB 2

6T SRAM cell


BL
V3
PULSE(0 850m 100p 10p 10p 490p 1n)
BLB
V4
PULSE(850m 0 100p 10p 10p 490p 1n)
V1
850m
M3
PMOS
M2
PMOS
WL
BLB
NMOS
M6
Q
QB
WL
NMOS
M4
BL
M1
NMOS
M5
NMOS
WL
V2
PWL(0 850m 2.49n 850m 2.5n 0 3n 0 3.01n 0 3.02n 850m)

6T SRAM cell


V(blb)
V(bl)
900mV
810mV
720mV
630mV
540mV
450mV
360mV
270mV
180mV
90mV
0mV
-90mV
V(q)
V(qb)
1.1V
0.5V
-0.2V
V(wl)
900mV
810mV
720mV
630mV
540mV
450mV
360mV
270mV
180mV
90mV
0mV
0.0ns
0.8ns
1.6ns
2.4ns
3.2ns
4.0ns
4.8ns
5.6ns
6.4ns
7.2ns
8.0ns

6T SRAM CELL SNM

- E. Seevinck, F. J. List and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," in *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, Oct. 1987, doi: 10.1109/JSSC.1987.1052809.

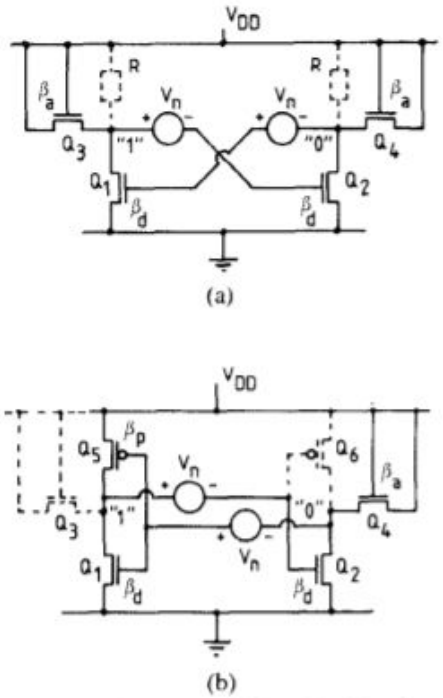
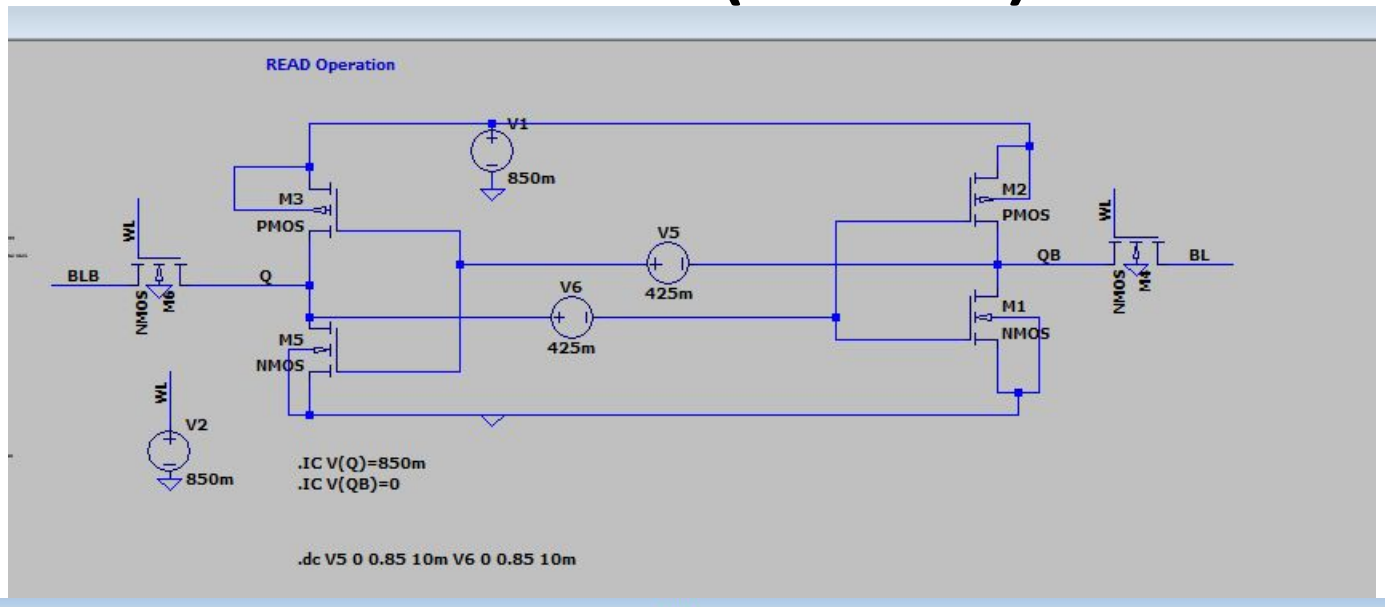
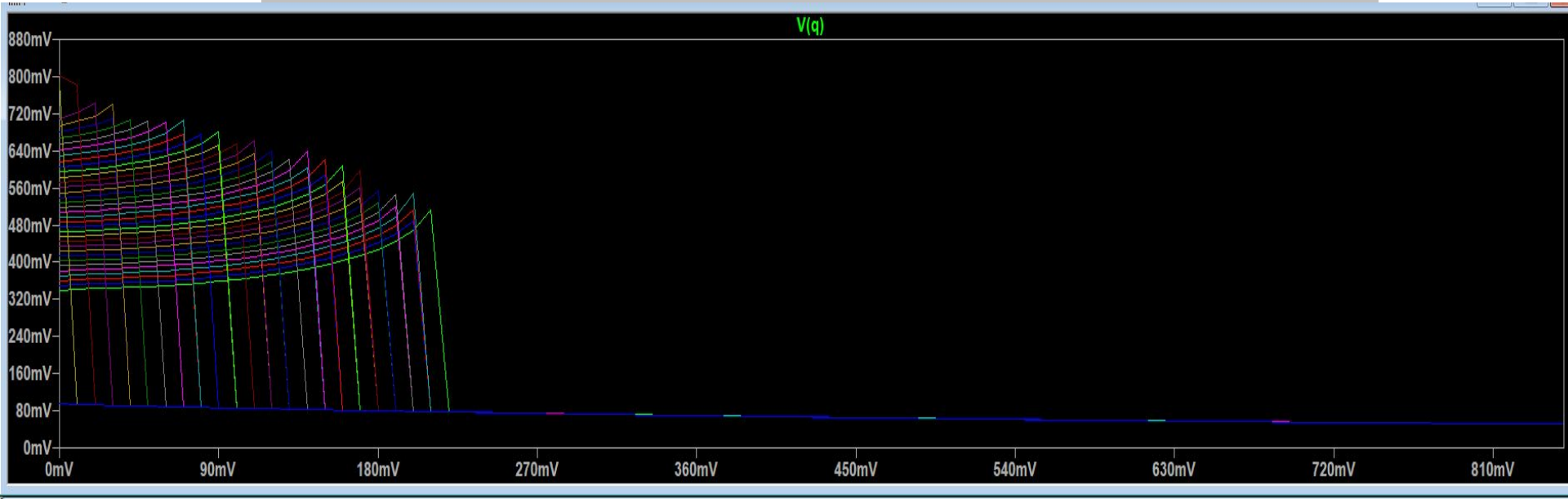


Fig. 4. (a), (b) Circuit diagrams of SRAM cells when accessed, with static-noise sources V_n inserted.

6T SRAM (SNM)


READ Operation
V1
850m
M3
PMOS
WL
BLB
NMOS
M6
Q
V5
425m
V6
425m
M2
PMOS
QB
BL
M1
NMOS
M5
NMOS
V2
850m
.IC V(Q)=850m
.IC V(QB)=0
.dc V5 0 0.85 10m V6 0 0.85 10m


V(q)
880mV
800mV
720mV
640mV
560mV
480mV
400mV
320mV
240mV
160mV
80mV
0mV
0mV
90mV
180mV
270mV
360mV
450mV
540mV
630mV
720mV
810mV

Reference

- https://engineering.purdue.edu/~vlsi/ECE559_Fall09/HW/HW6_Solution.pdf

Assignment

- Redo the exercise for 8T and 10T Sram cell