

Lab session

# Agenda

- Introduction
- Lab1 ☐ LTspice familiarity
- Lab2 ☐ SRAM cell simulation
- Lab3 ☐

# Introduction

- Tool : LTSPICE
- Model files : Arizona State University PTM
  - 16nm PTM-MG [HP NMOS](#), [HP PMOS](#)
  - NFET :  
[http://ptm.asu.edu/modelcard/PTM-MG/modelfiles/hp/16nfet.p  
m](http://ptm.asu.edu/modelcard/PTM-MG/modelfiles/hp/16nfet.p<br/>m)
  - PFET :  
[http://ptm.asu.edu/modelcard/PTM-MG/modelfiles/hp/16pfet.p  
m](http://ptm.asu.edu/modelcard/PTM-MG/modelfiles/hp/16pfet.p<br/>m)
- Nominal supply : 850mV
  - Supply variation : +/-10%
- Channel length : 20nm ( Min : 10nm ; Maximum : 30nm)
- Width :
  - For a planar FET ; width is a number
  - For a Fin FET ; width is number of fins

# Width of finfets

Effective Channel Width = (2 \* Height of Fin) +  
Thickness of the fin

$$W = (2 * w1) + w2$$

$h_{fin} = 2.6e-008$  ;  $26nm = w1$

$t_{fin} = 1.2e-008$  ;  $12nm = w2$

For 16nm ; for a single fin device

Device width = 64nm

Total width of an 'n' fin device :  $n * 64nm$

We have to do this because LT spice does not understand finfet width or atleast I could not find it.

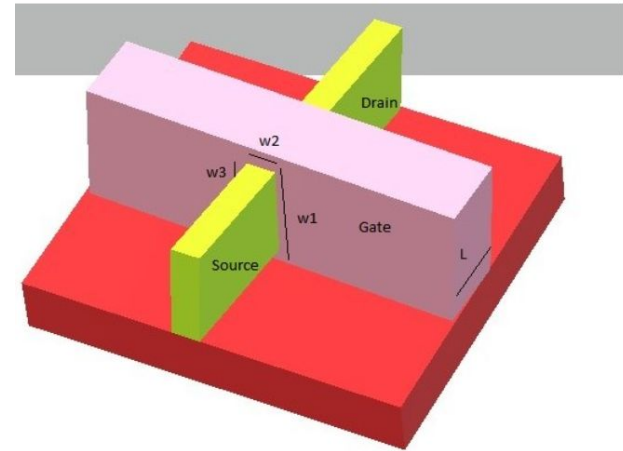


Figure 1: Structure of FinFET

<http://www.signoffsemi.com/finfet/>

A screenshot of a software window titled "Monolithic MOSFET - M2". It contains several input fields for MOSFET parameters. The "Model Name" field is set to "NMOS". The "Length(L)" field is set to "20n". The "Width(W)" field is set to "320n". There are also empty fields for "Drain Area(AD)", "Source Area(AS)", "Drain Perimeter(PD)", "Source Perimeter(PS)", and "No. Parallel Devices(M)". At the bottom, a text box displays "NMOS l=20n w=320n". There are "OK" and "Cancel" buttons on the right side of the window.


# Models

- PTM models are BSIM CMG level 72 models
- LTSPICE does not understand level 72



```
.model nfet nmos level = 72
```

- Change this to level 9



```
.model pfet pmos level = 9
```

- Use spice directive to include model files

# Questions

Lab1

# LAB 1

# Agenda

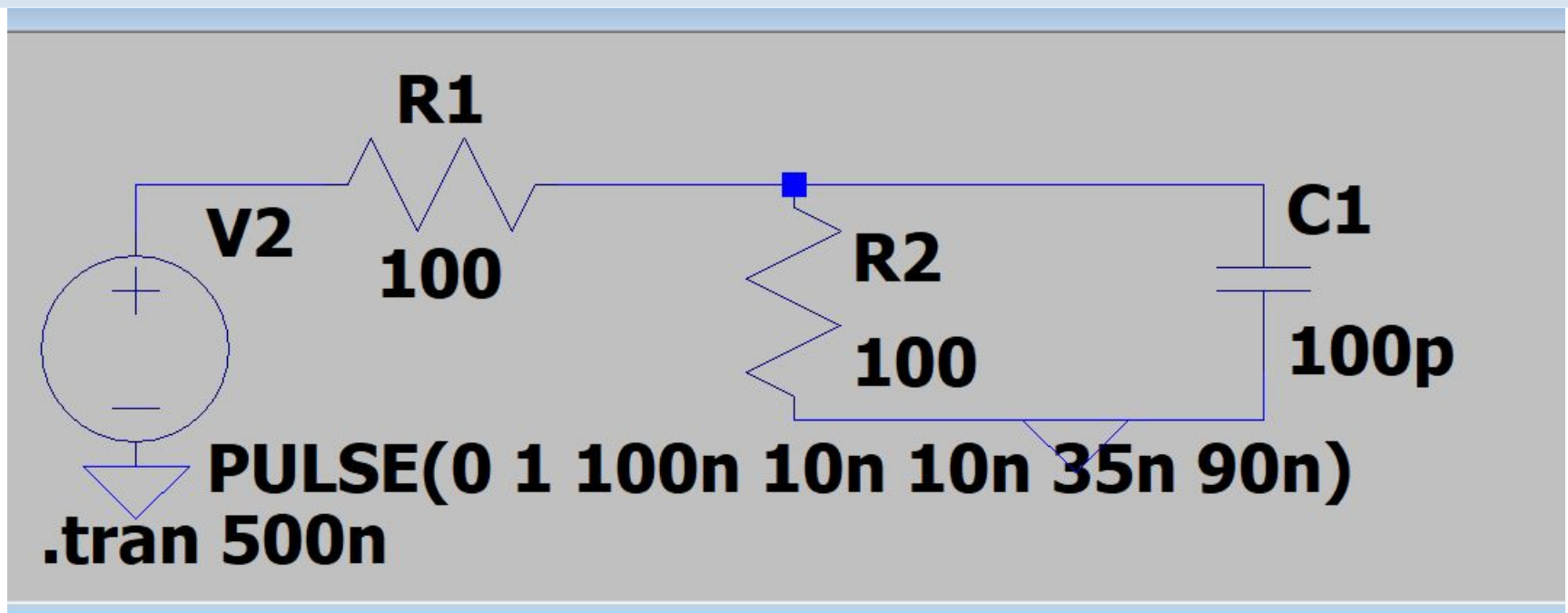
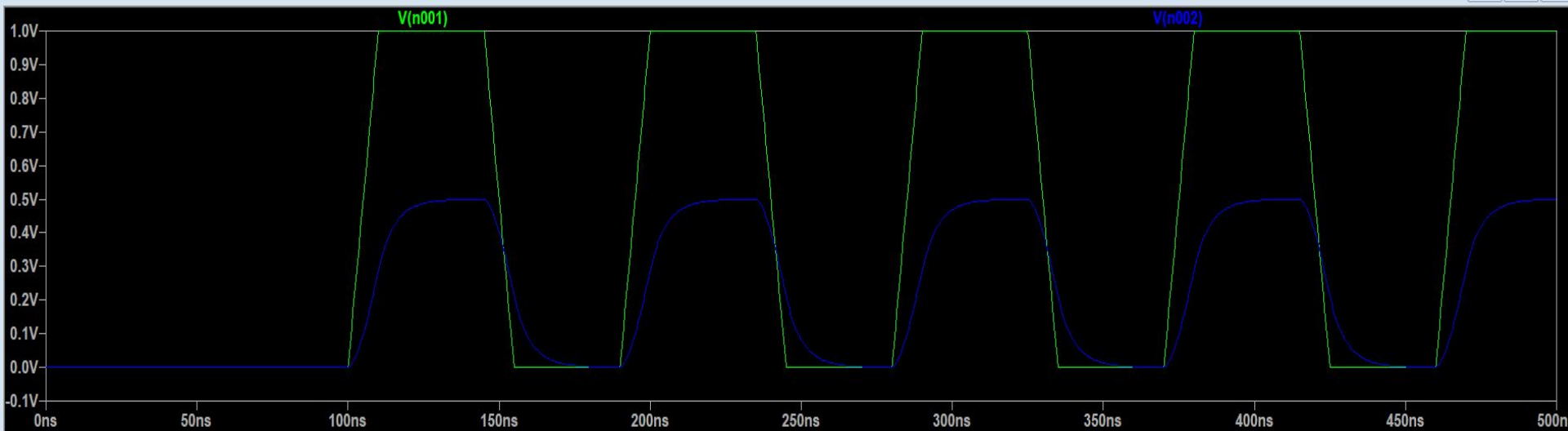
- Understand basic analysis types in LTSpice
- Run an inverter transient and DC analysis
- Assignment :
  - Calculate power of a nominal sized inverter driving a load of 1fF /5fF
  - Calculate Fan out of 1 (FO1) and Fan out of 4 (FO4) delay of nominally sized inverter at nominal and +/-10% supply
  - Calculate leakage power of a 50fin inverter and compare it with a 22nm planar FET inverter of same width



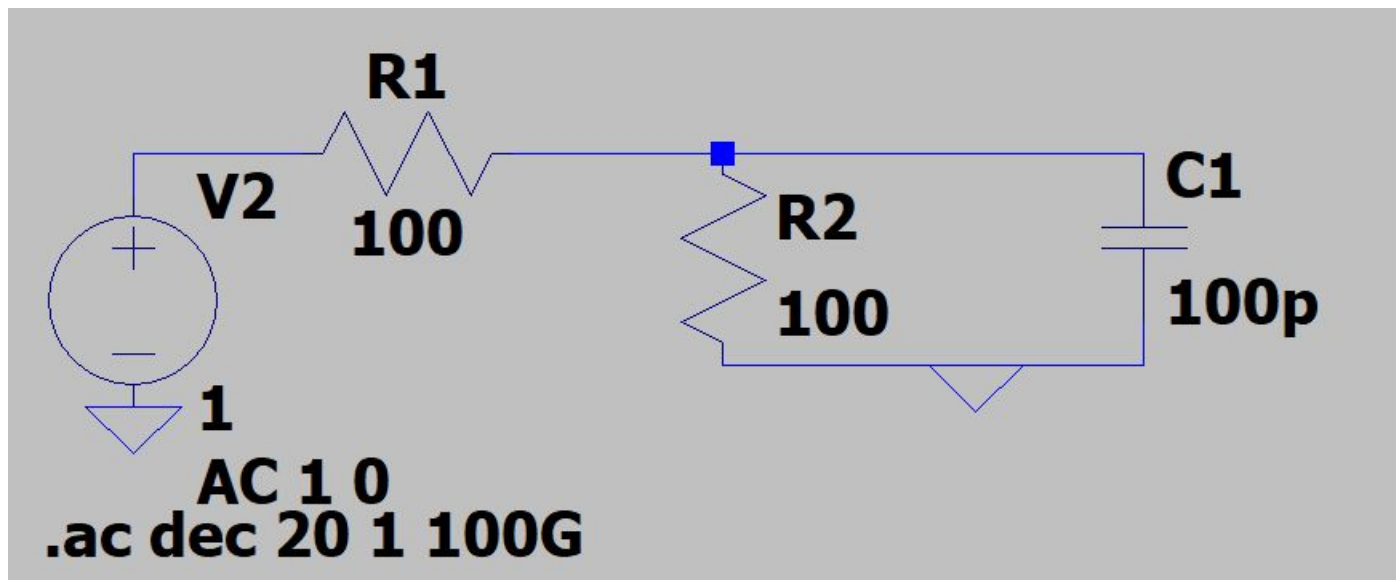
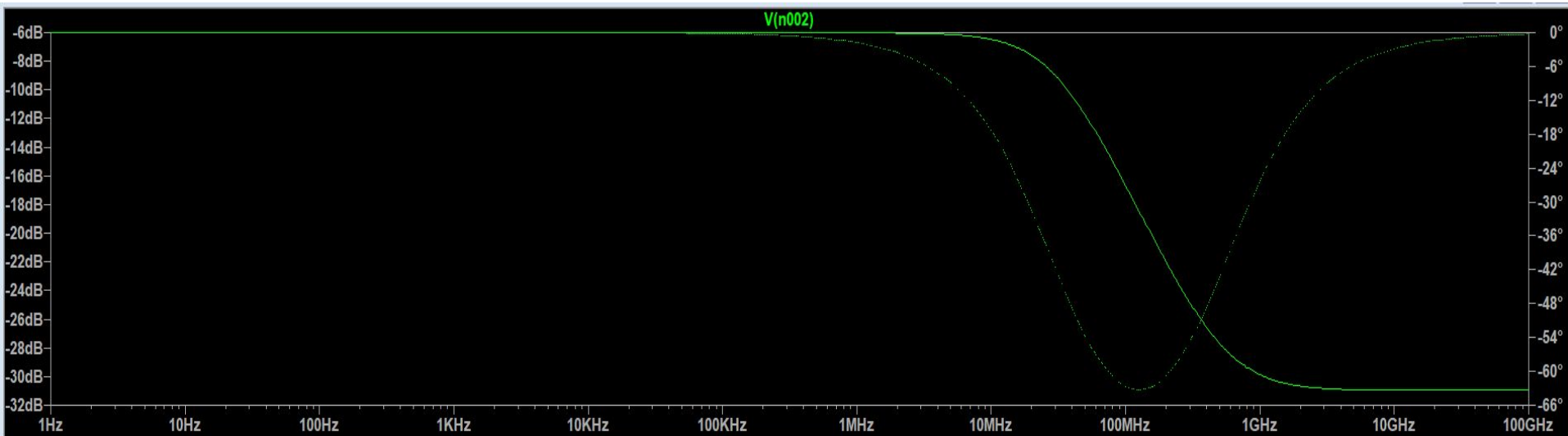
# Analysis type

- Ltspice supports following analysis types
  - Transient
    - We will be using this in most of our work.
  - DC
    - A bit to find dc-operating points
  - AC
    - Gain analysis

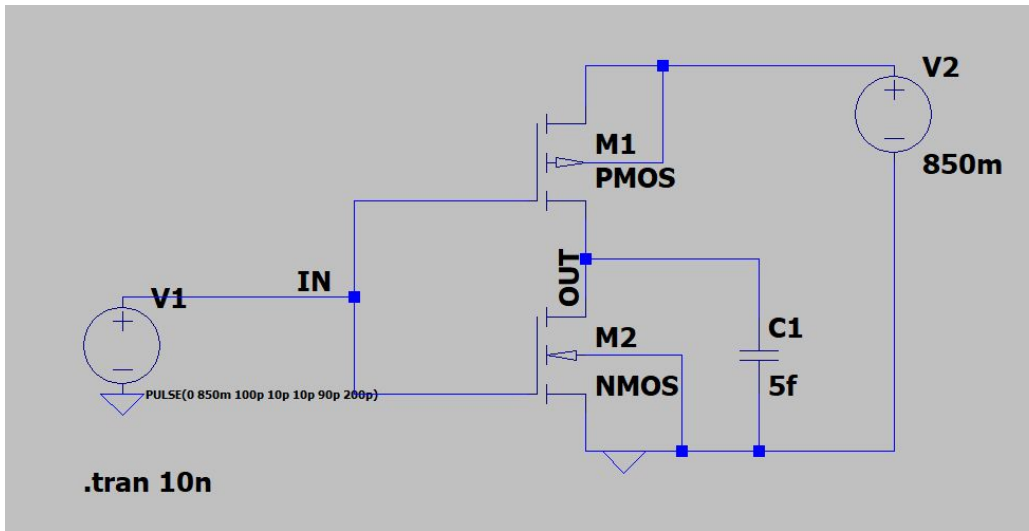
# Simple RC circuit (Tran)



# Simple RC circuit (AC analysis )



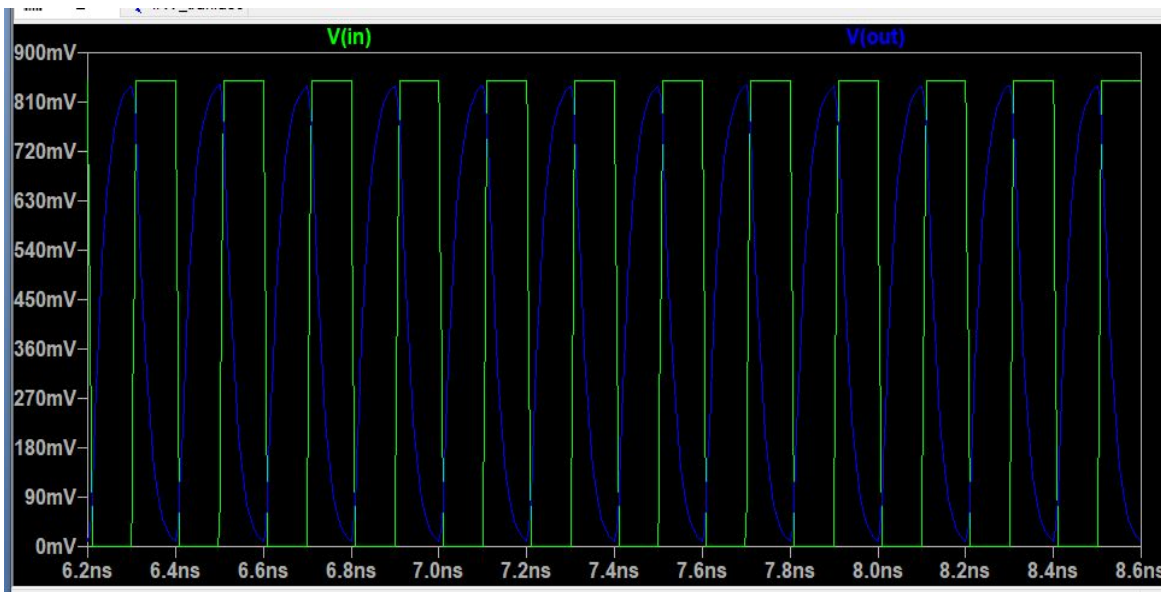
# Inverter (tran)



Monolithic MOSFET - M1

Model Name:	PMOS	OK
Length(L):	20n	Cancel
Width(W):	320n	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		

PMOS l=20n w=320n

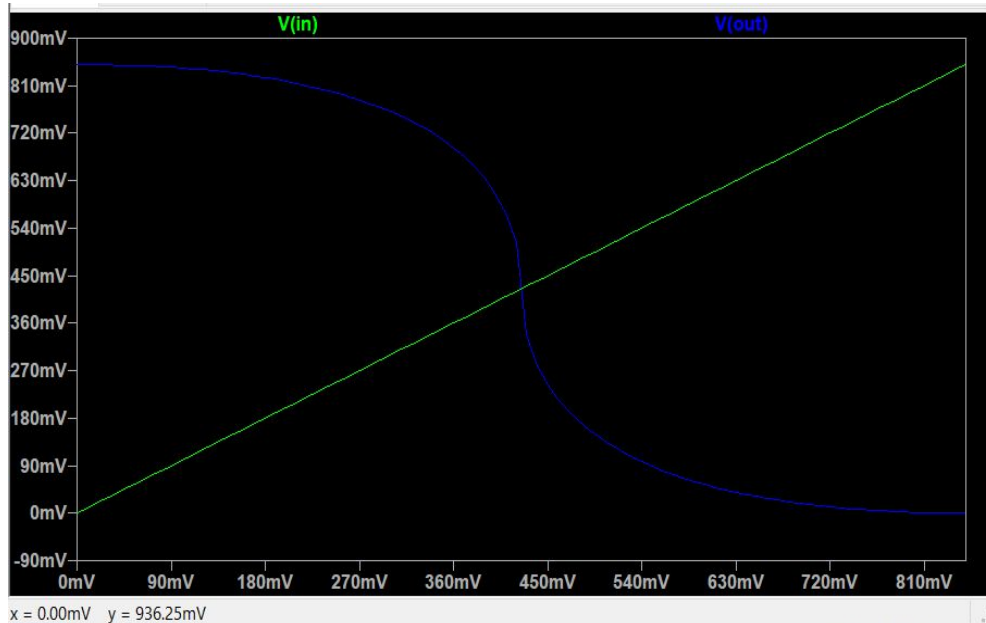
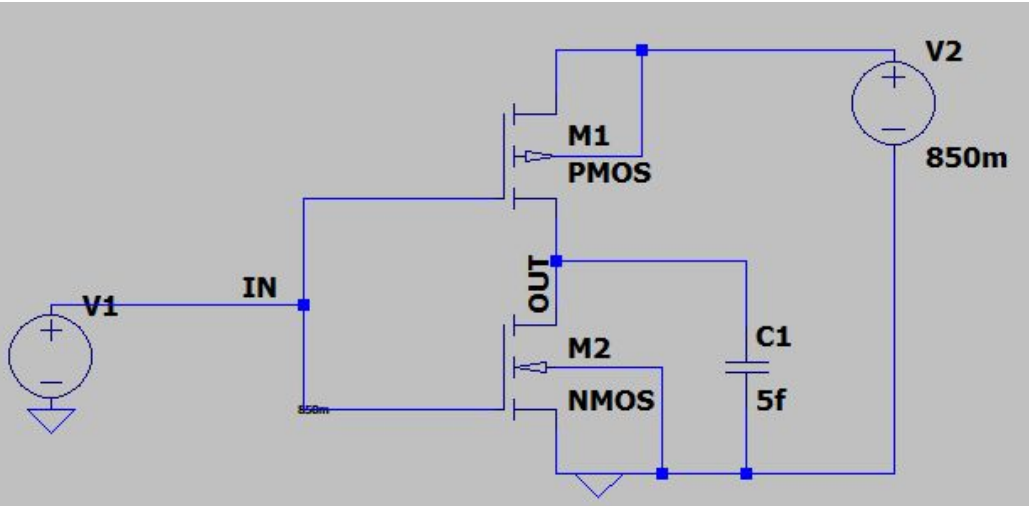


Monolithic MOSFET - M2

Model Name:	NMOS	OK
Length(L):	20n	Cancel
Width(W):	320n	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		

NMOS l=20n w=320n

# Inverter (dc)



Monolithic MOSFET - M1

Model Name:	PMOS	OK
Length(L):	20n	Cancel
Width(W):	320n	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		

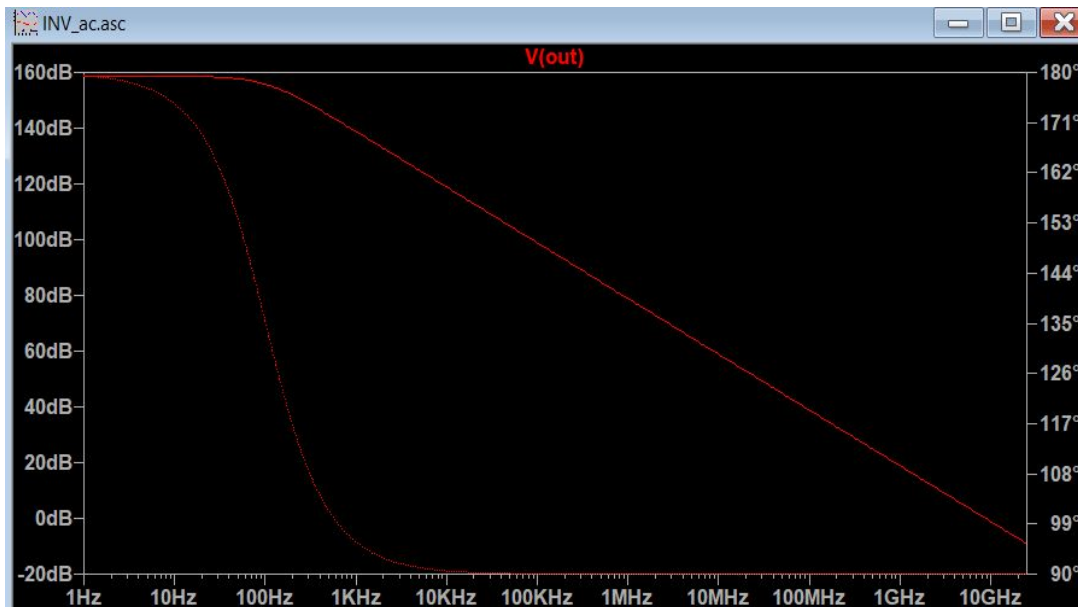
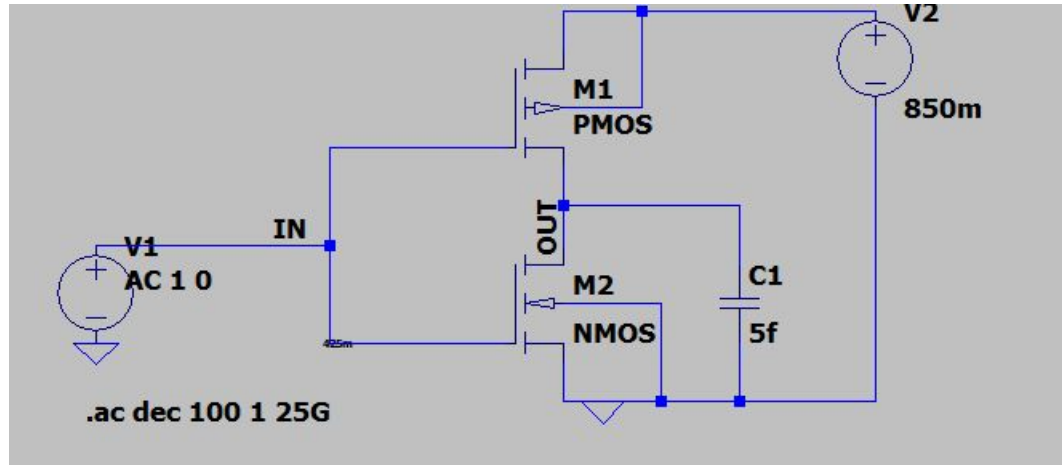
PMOS l=20n w=320n

Monolithic MOSFET - M2

Model Name:	NMOS	OK
Length(L):	20n	Cancel
Width(W):	320n	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		

NMOS l=20n w=320n

# Inverter (ac)



Monolithic MOSFET - M1

Model Name:	PMOS	OK
Length(L):	20n	Cancel
Width(W):	320n	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		

PMOS l=20n w=320n

Monolithic MOSFET - M2

Model Name:	NMOS	OK
Length(L):	20n	Cancel
Width(W):	320n	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		

NMOS l=20n w=320n

# Pending items

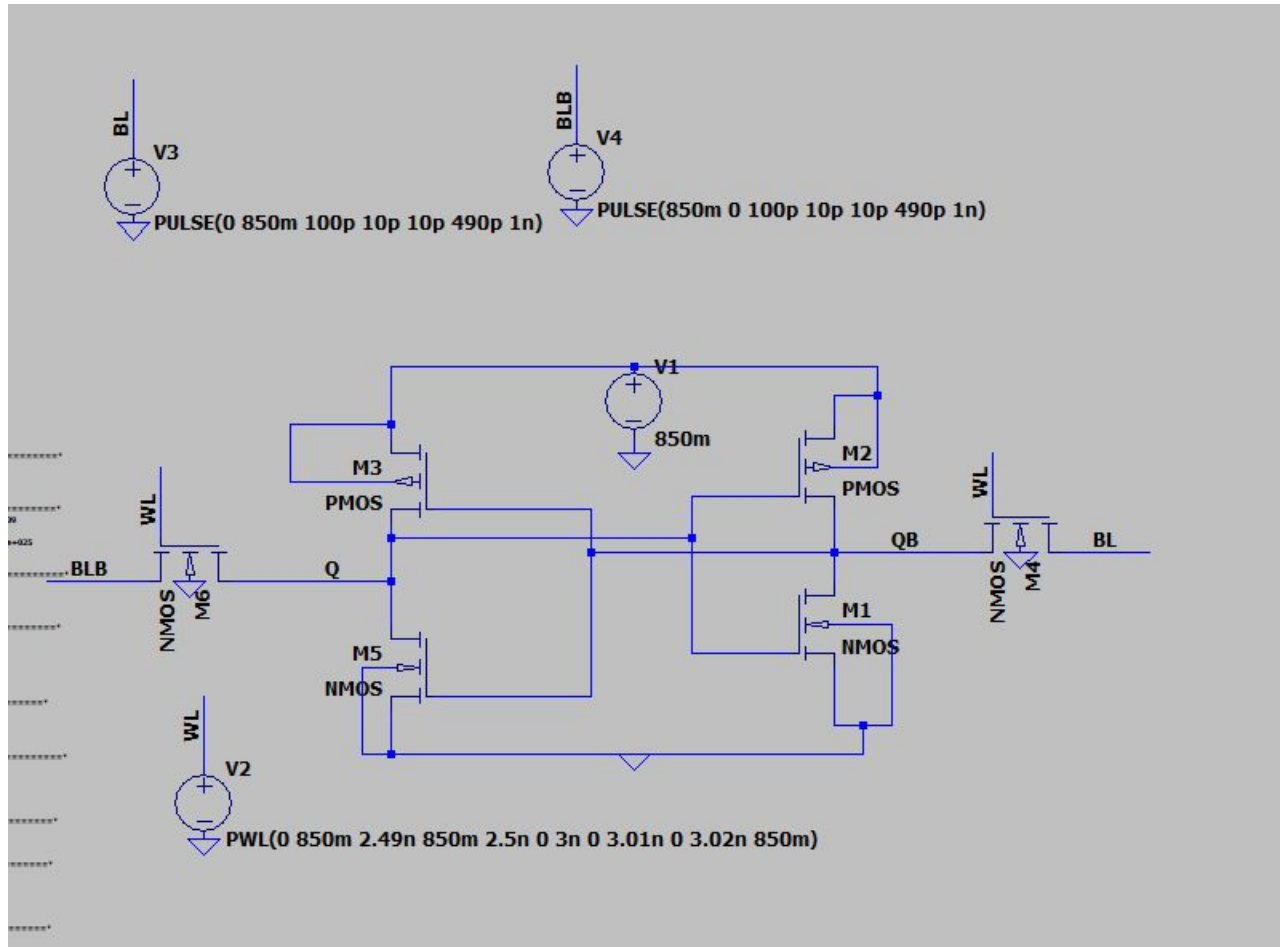
- Create symbol
- Use symbol for analysis

6T SRAM cell

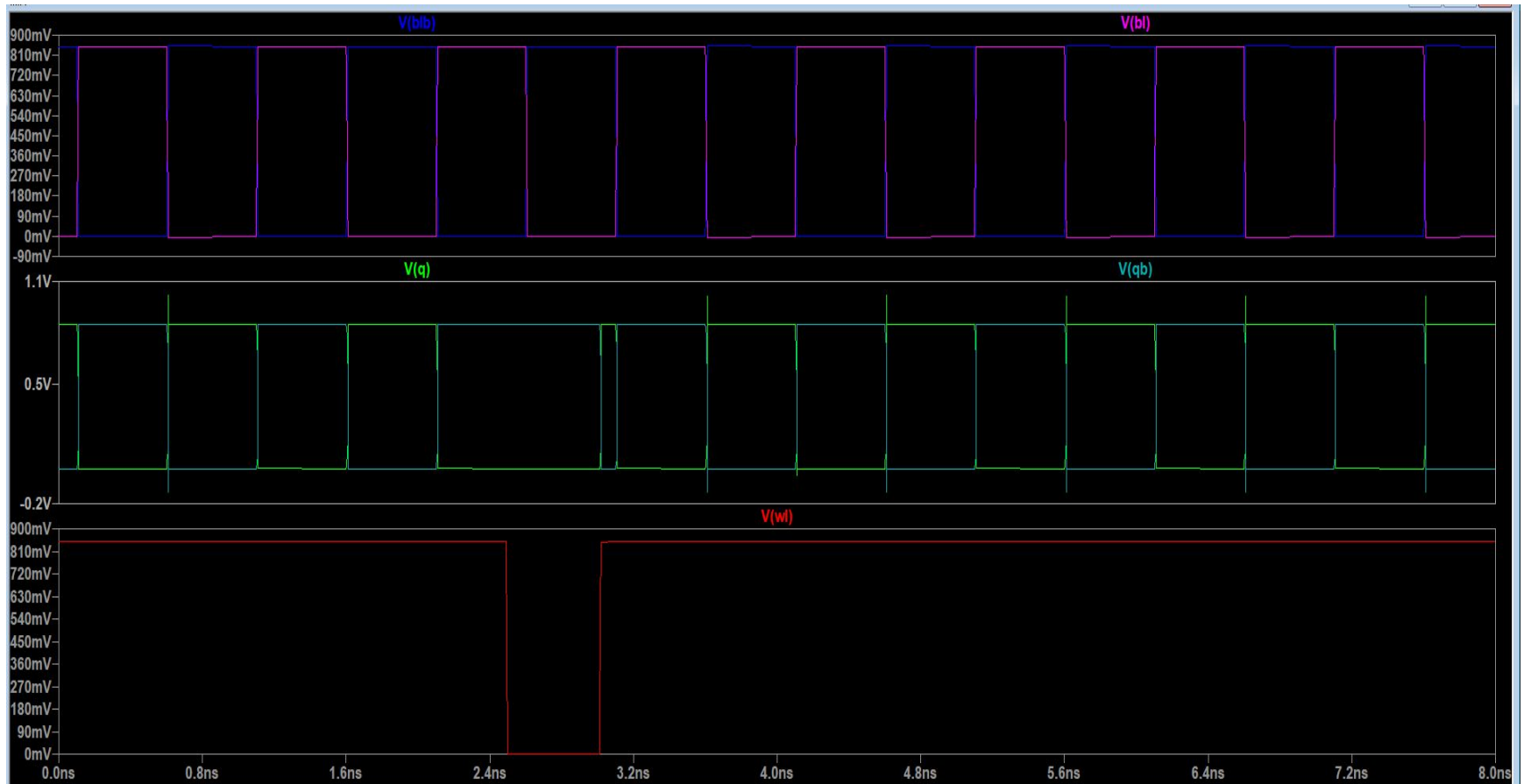
# LAB 2



# 6T SRAM cell



# 6T SRAM cell



# 6T SRAM CELL SNM

- E. Seevinck, F. J. List and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," in *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, Oct. 1987, doi: 10.1109/JSSC.1987.1052809.

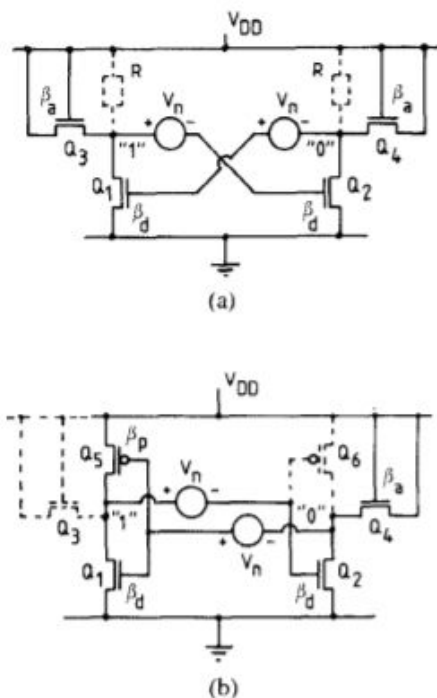
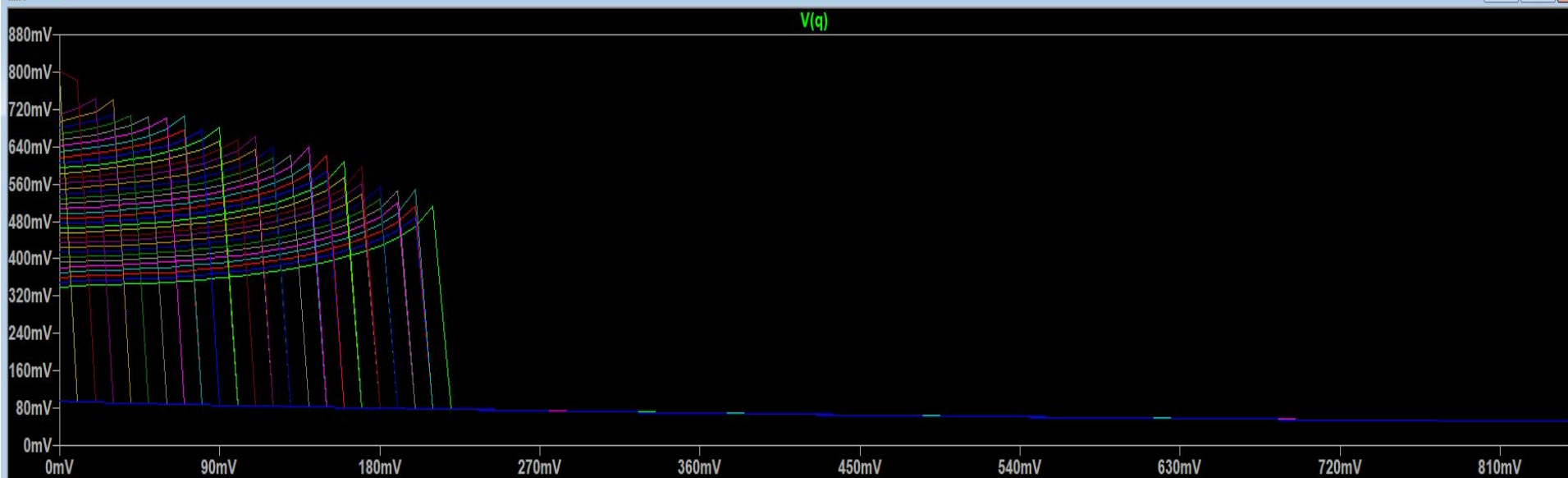
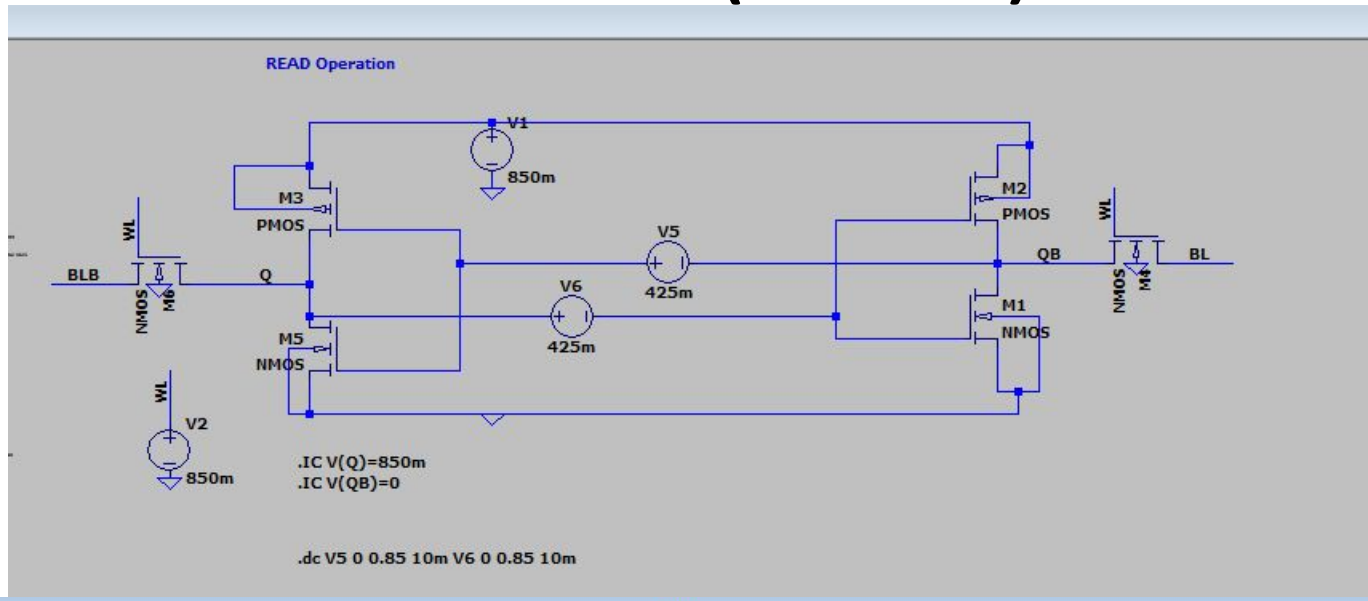


Fig. 4. (a), (b) Circuit diagrams of SRAM cells when accessed, with static-noise sources  $V_n$  inserted.

# 6T SRAM (SNM)



# Reference

- [https://engineering.purdue.edu/~vlsi/ECE559\\_Fall09/HW/HW6\\_Solution.pdf](https://engineering.purdue.edu/~vlsi/ECE559_Fall09/HW/HW6_Solution.pdf)

# Assignment

- Redo the exercise for 8T and 10T Sram cell