IEEE CAS Bangalore Chapter

MEMORY DESIGN WORKSHOP, AUG 2021

Hands-on Lab Session Report, 14 August 2021 - 29 Aug 2021

Group: 2
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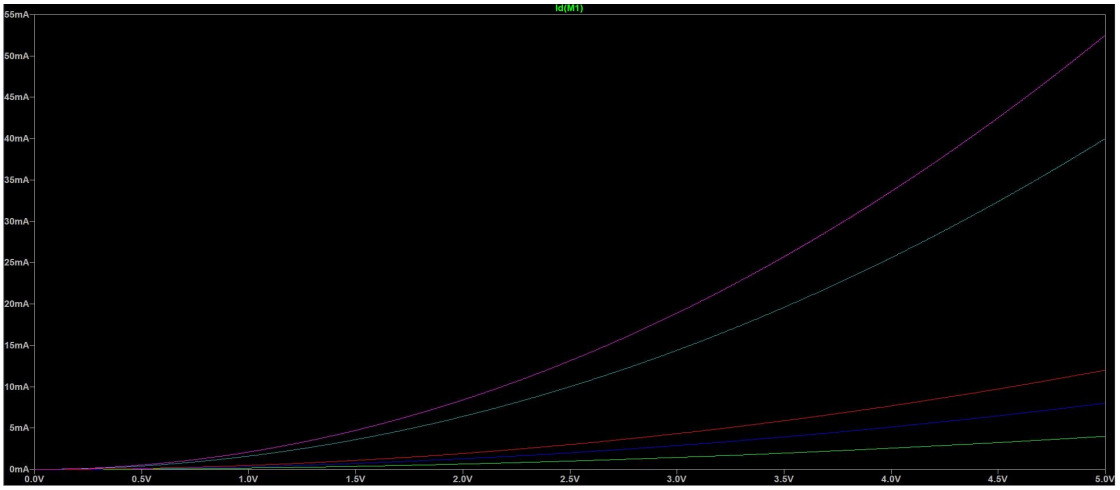
- LAB 1 - To plot I-V Characteristics for an NMOS
- LAB 2 - To perform dc & transient analysis of an inverter
- LAB 3 - To perform 6T SRAM cell simulation and plot its SNM
- LAB 4 - To Perform 8T and 10T SRAM cell simulation and plot their SNM

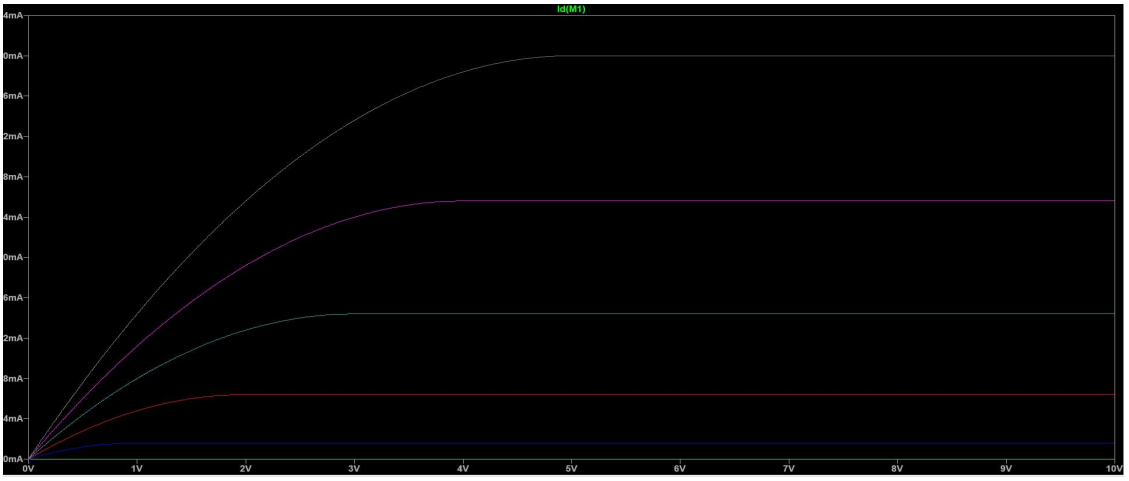
LAB 1 - To Plot I-V Characteristics for an NMOS

- Output Waveform for Id-Vgs characteristics :



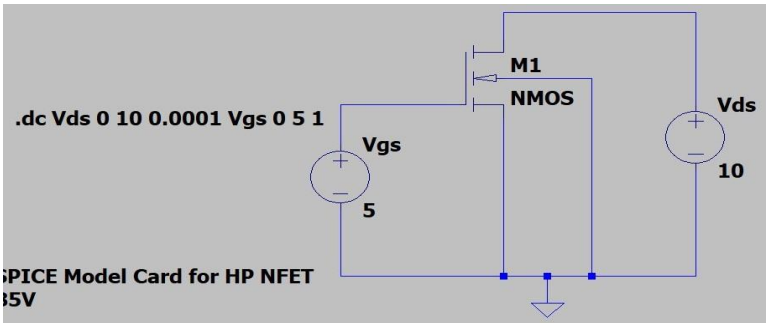
Different colors showing different values of Id when w = 320, 640, 960, 3200, 4200n

- Output Waveform for Id-Vds characteristics :



Different colors showing different values of Id when Vgs = 0, 1, 2, 3, 4, 5 V

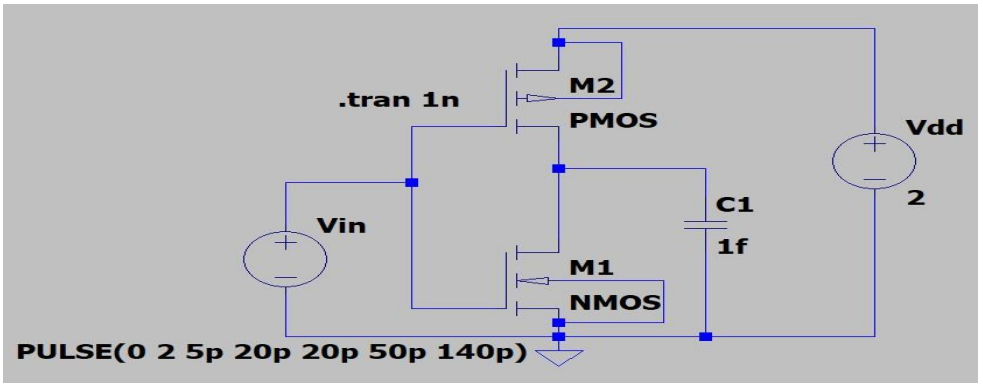
- Circuit Diagram of NMOS :



Change the operation commands and component values according to the requirements.

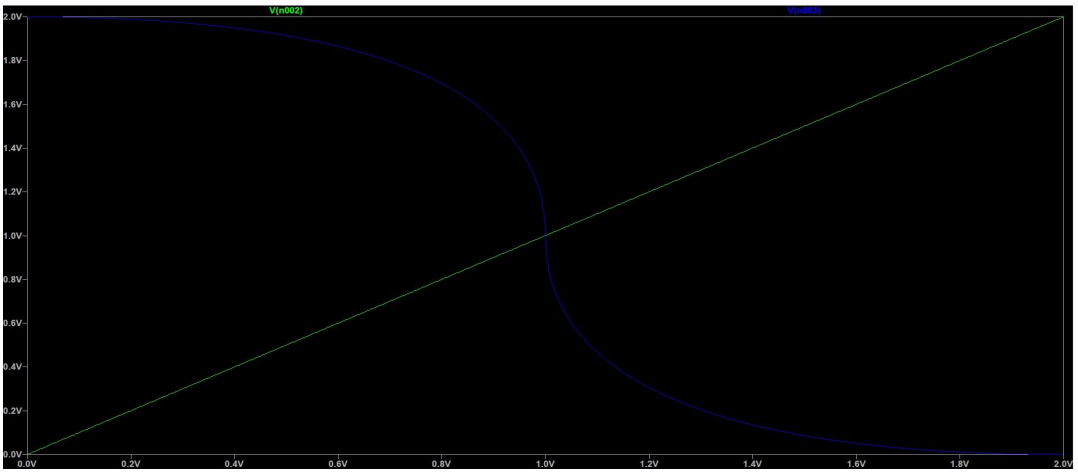
Lab 2: AC, DC, Transient and Power analysis of CMOS Inverter

- Circuit Diagram of CMOS Inverter :

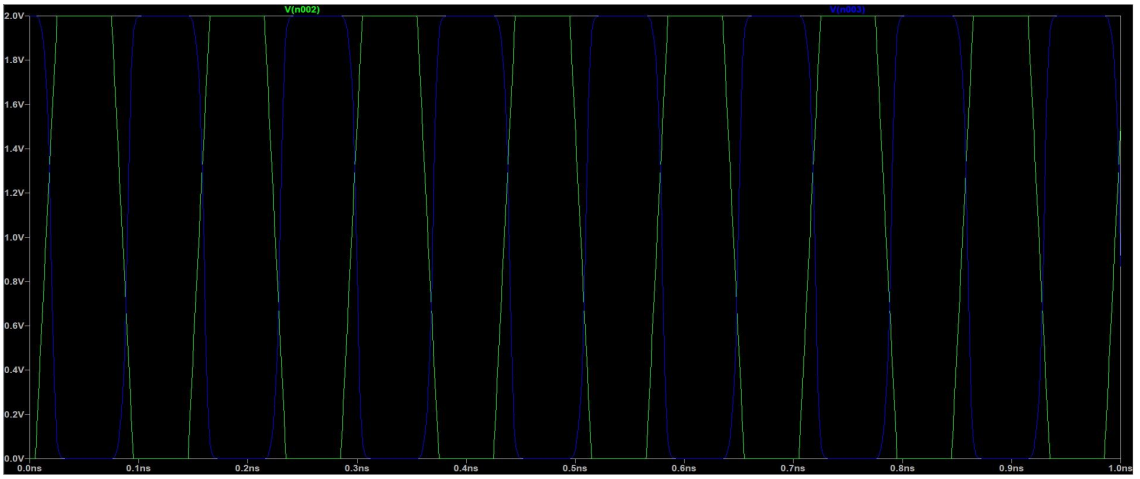


Change the operation commands and component values according to the requirements.

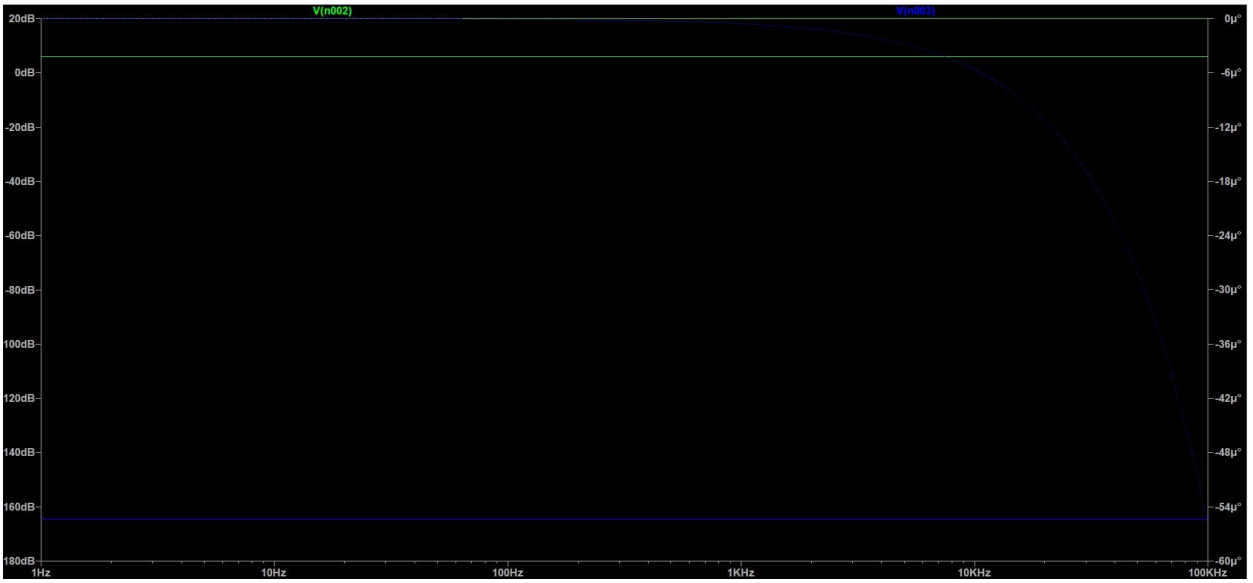
- DC Analysis :



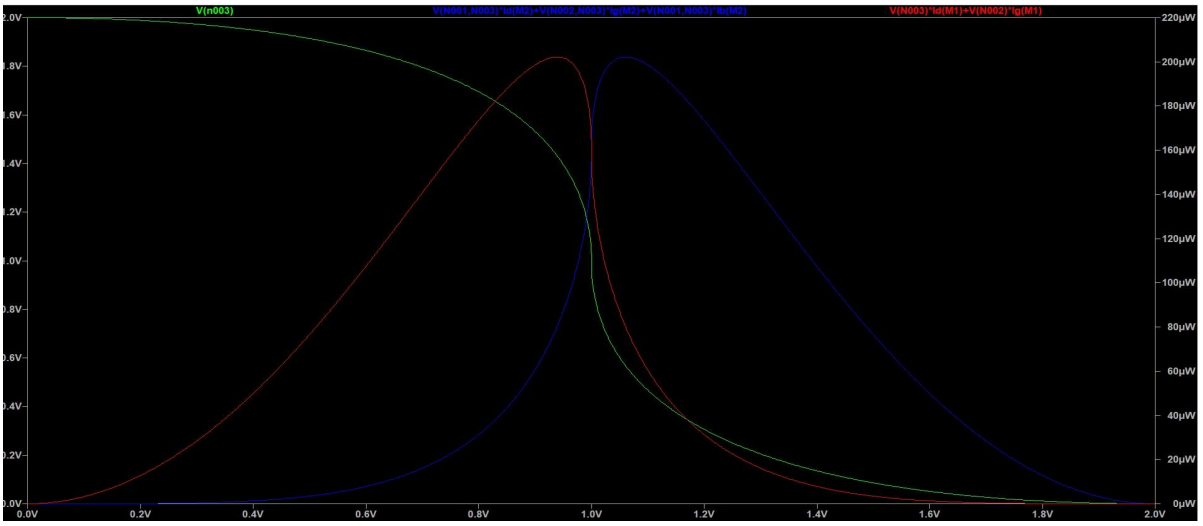
- Transient Analysis :



- AC Analysis :

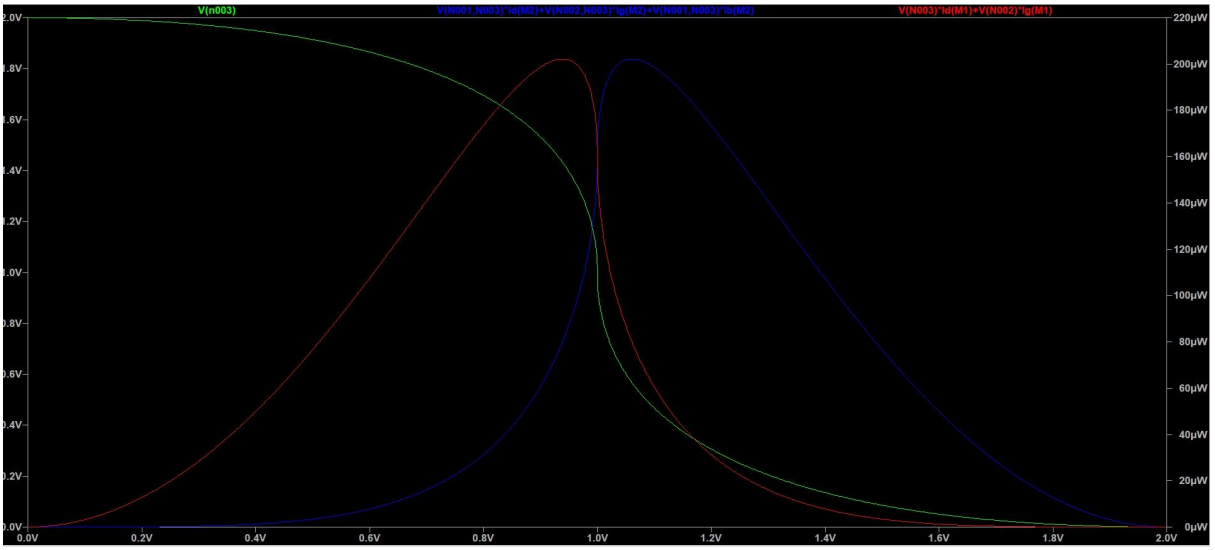


- Power Analysis:
  - ❖ LOAD = 1 fF



Total Power consumed by CMOS Inverter = 201.78 µW (PMOS) + 202.57 µW (NMOS)

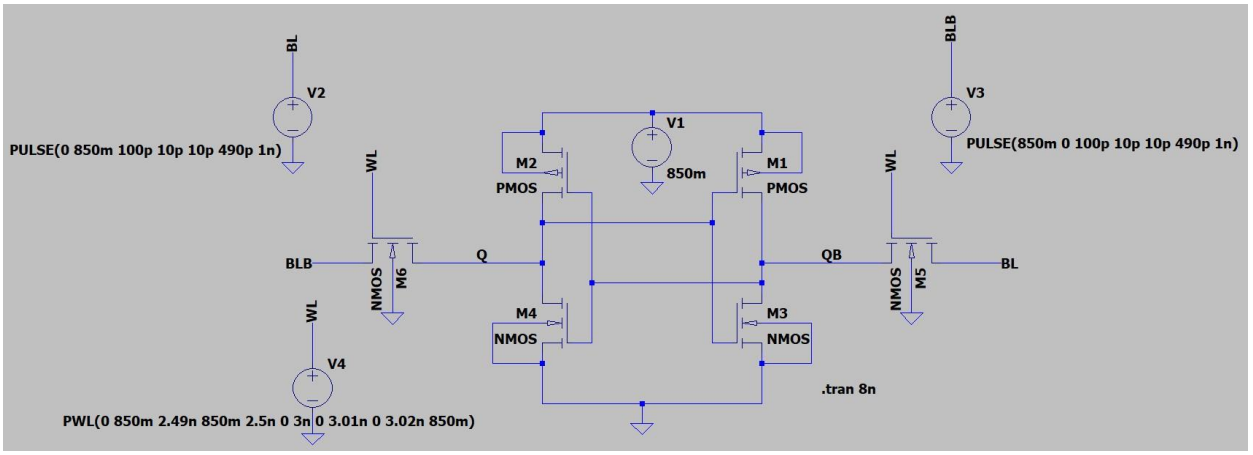
  - ❖ LOAD = 5 fF



Total Power consumed by CMOS Inverter = 202.57 µW (PMOS) + 202.83 µW (NMOS)

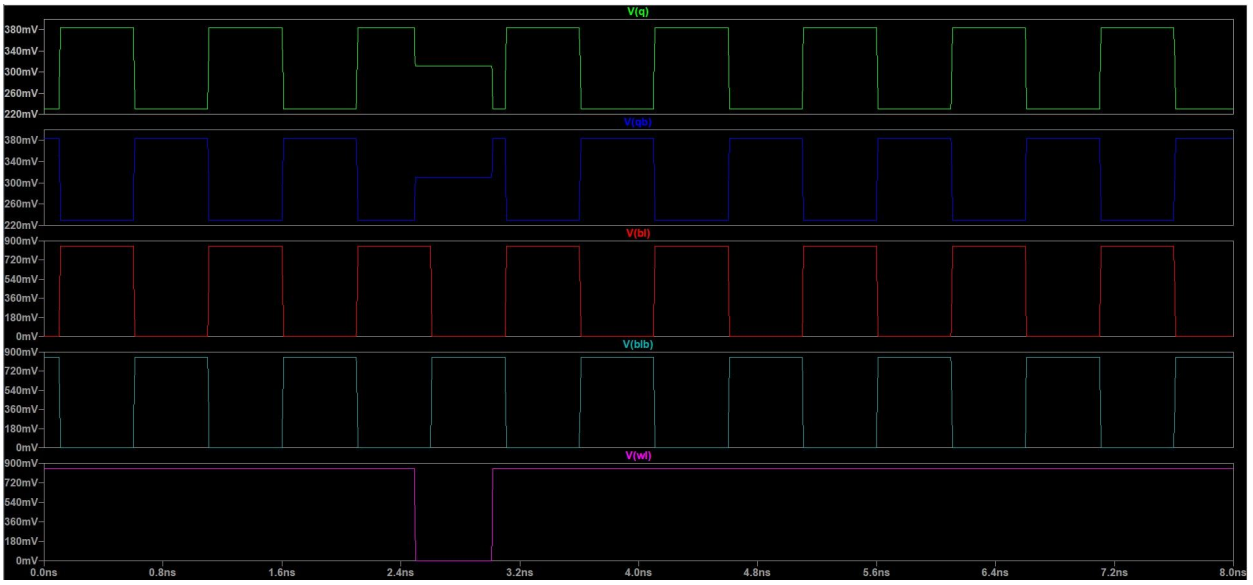
Lab 3: Desing and Analysis of 6T SRAM Cell

- Circuit Diagram of 6T SRAM Cell :

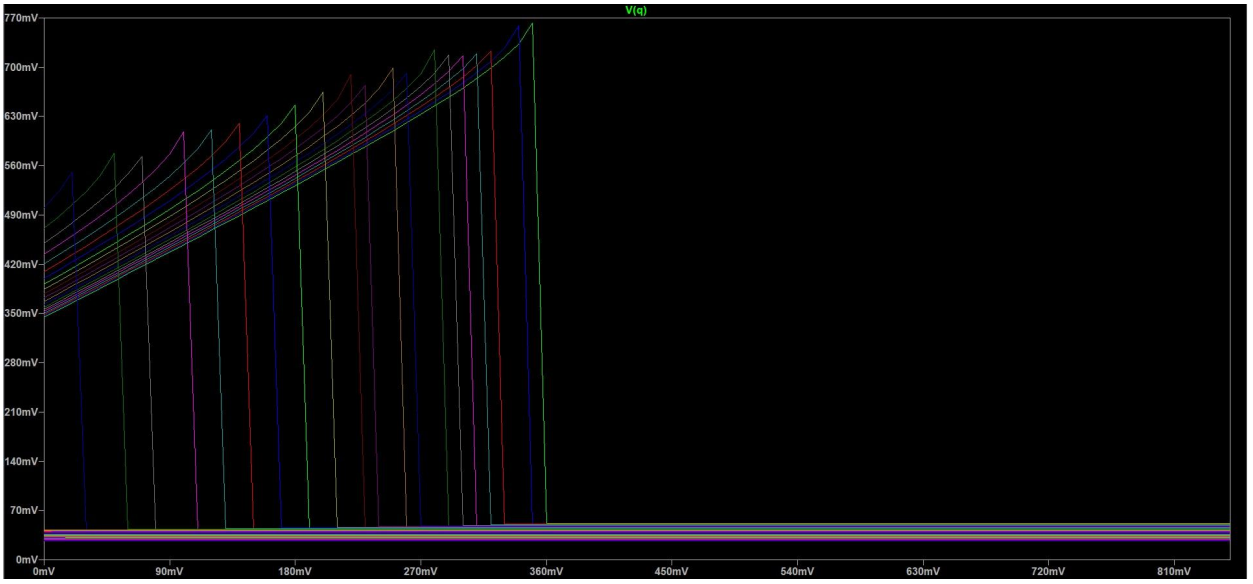


Change the operation commands and component values according to the requirements.

- Transient Analysis of 6T SRAM Cell :

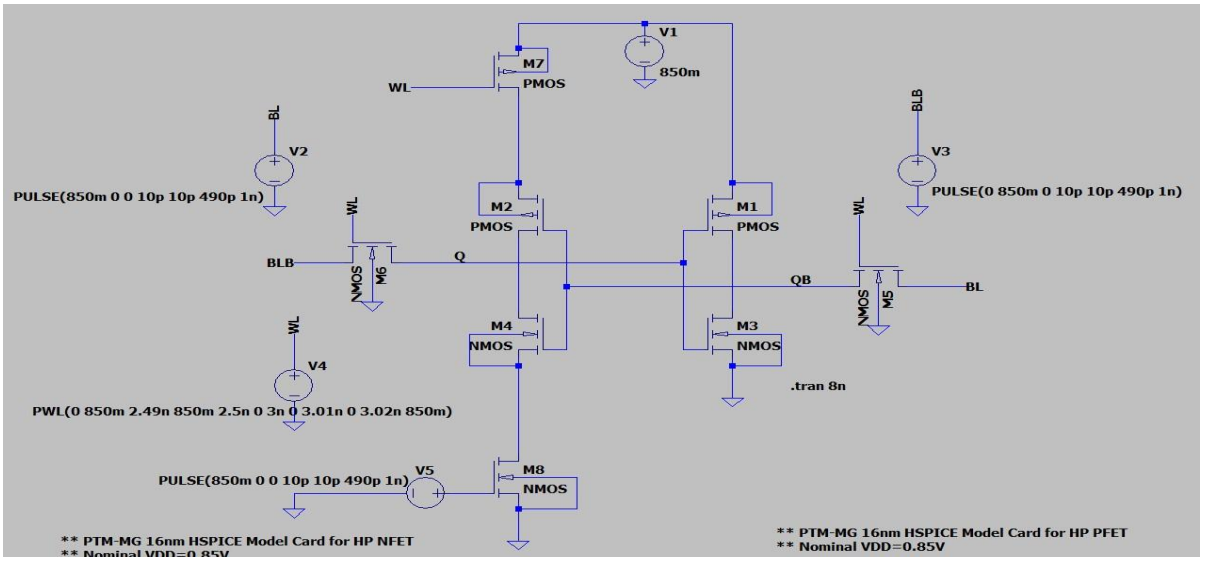


- Static-Noise Margin Analysis of 6T SRAM Cell :



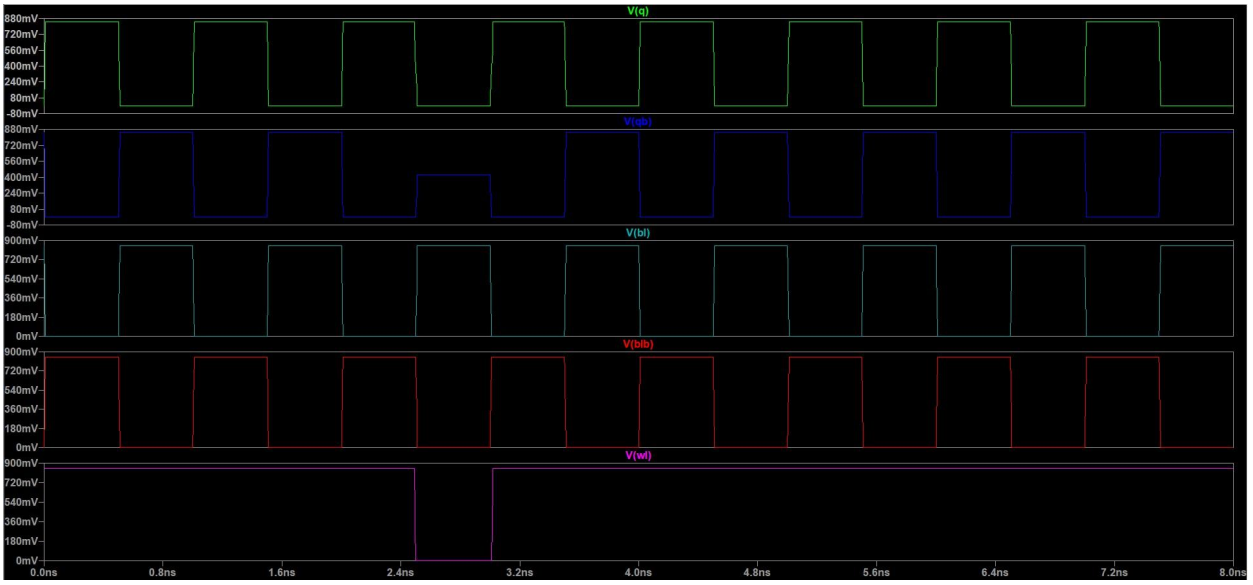
Lab 4 a: Desing and Analysis of 8T SRAM Cell

- Circuit Diagram of 8T SRAM Cell :

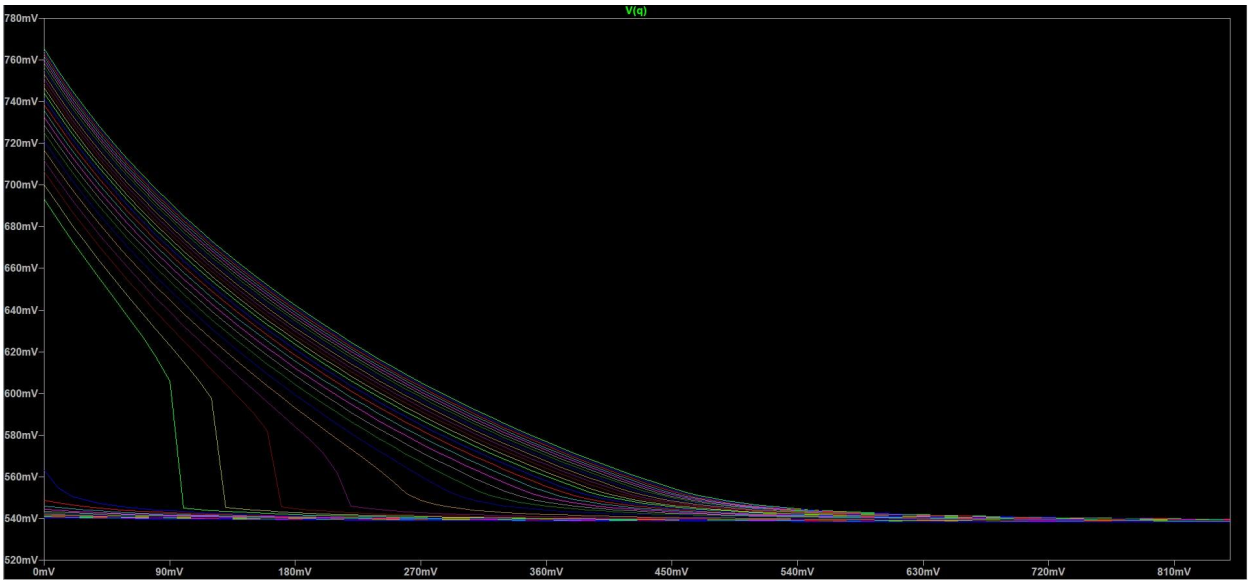


Change the operation commands and component values according to the requirements.

- Transient Analysis of 8T SRAM Cell :

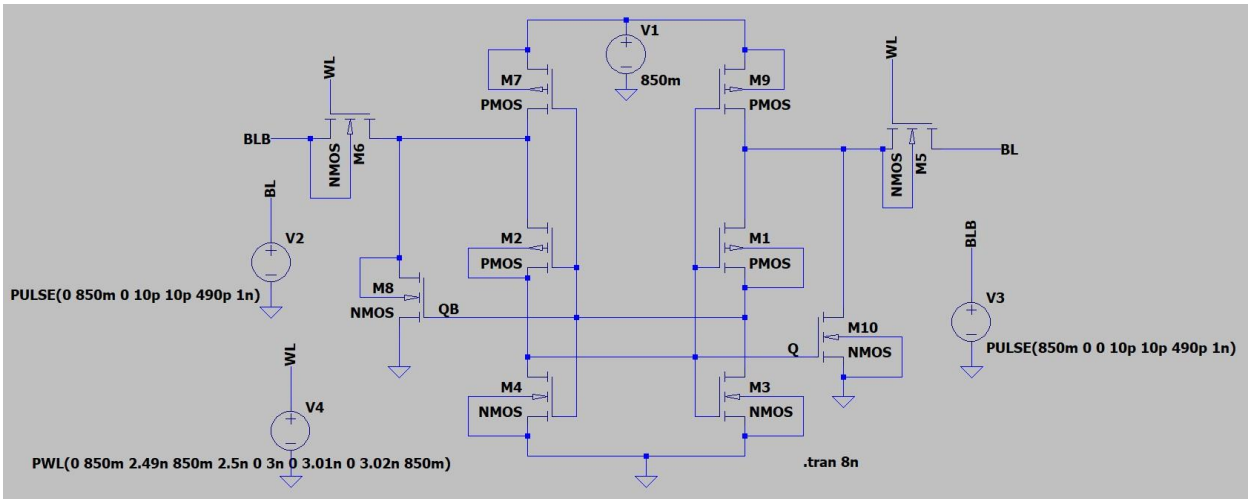


- Static-Noise Margin Analysis of 8T SRAM Cell :



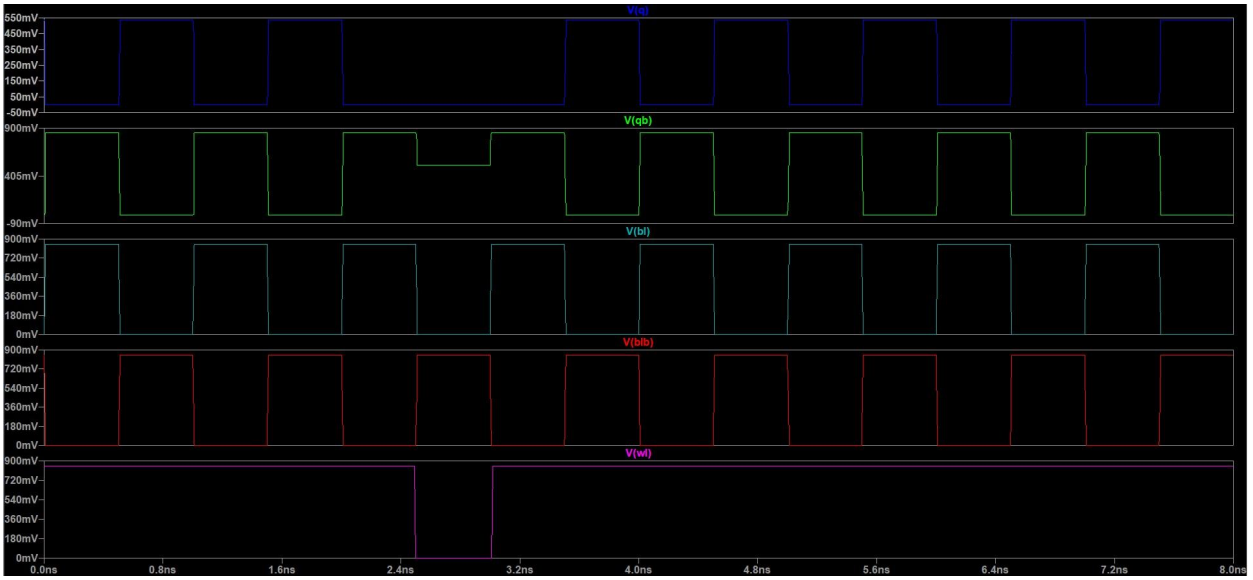
Lab 4 b: Desing and Analysis of 10T SRAM Cell

- Circuit Diagram of 10T SRAM Cell :



Change the operation commands and component values according to the requirements.

- Transient Analysis of 10T SRAM Cell :



- Static-Noise Margin Analysis of 10T SRAM Cell :