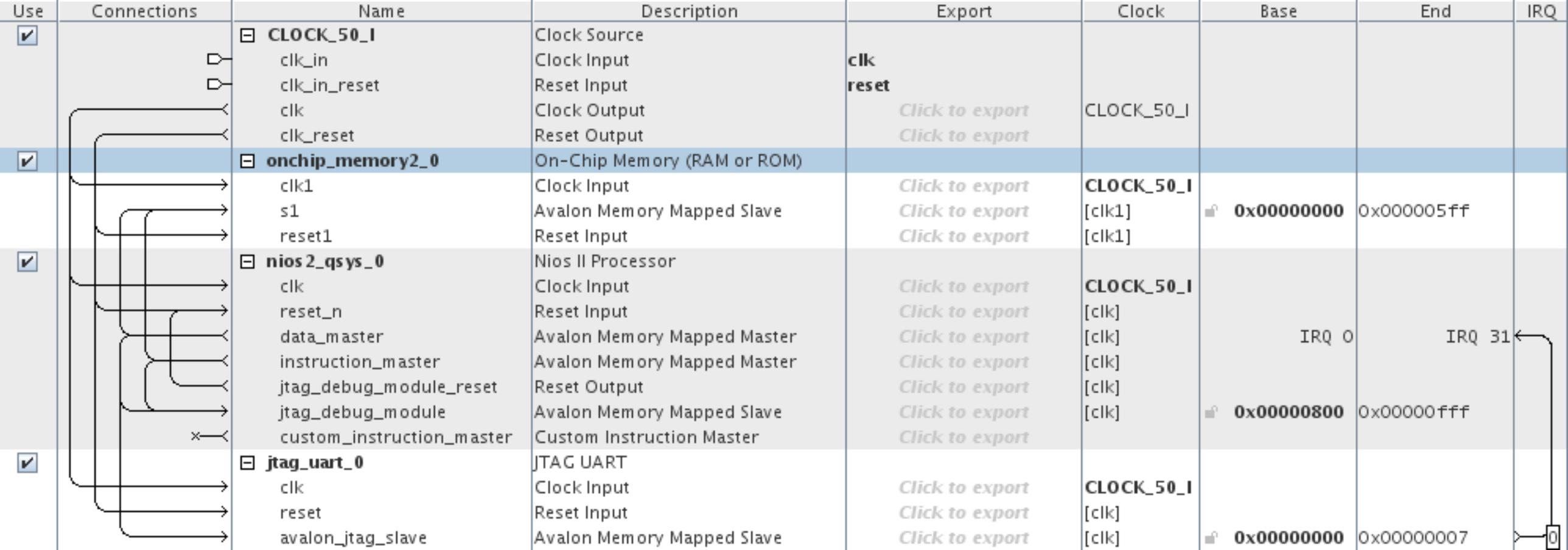
Use
Connections
Name
Description
Export
Clock
Base
End
IRQ
CLOCK_50_I
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
Click to export
CLOCK_50_I
clk_reset
Reset Output
Click to export
onchip_memory2_0
On-Chip Memory (RAM or ROM)
clk1
Clock Input
Click to export
CLOCK_50_I
s1
Avalon Memory Mapped Slave
Click to export
[clk1]
0x00000000
0x000005ff
reset1
Reset Input
Click to export
[clk1]
nios2_qsys_0
Nios II Processor
clk
Clock Input
Click to export
CLOCK_50_I
reset_n
Reset Input
Click to export
[clk]
data_master
Avalon Memory Mapped Master
Click to export
[clk]
IRQ 0
IRQ 31
instruction_master
Avalon Memory Mapped Master
Click to export
[clk]
jtag_debug_module_reset
Reset Output
Click to export
[clk]
jtag_debug_module
Avalon Memory Mapped Slave
Click to export
[clk]
0x00000800
0x00000fff
custom_instruction_master
Custom Instruction Master
Click to export
jtag_uart_0
JTAG UART
clk
Clock Input
Click to export
CLOCK_50_I
reset
Reset Input
Click to export
[clk]
avalon_jtag_slave
Avalon Memory Mapped Slave
Click to export
[clk]
0x00000000
0x00000007
0