Dr. Alistair Finch

Cambridge, UK

📞 +44 (0)7122 454443 | ✉️ alistair.finch@email.com | 🔗 LinkedIn: linkedin.com/in/alistairfinch

Professional Summary

Highly innovative and results-oriented CPU Architect with over 17 years of progressive experience in architecting high-performance and low-power microprocessors. Proven ability to lead and empower architecture teams from initial concept through successful tape-out, specializing in RISC architecture and system-level optimization. Expertise in advanced modeling and rigorous verification methodologies, consistently pushing the boundaries of modern CPU core development.

Core Competencies

- **RISC Architecture & Microarchitecture Design:** Deep understanding of instruction set architectures and microarchitectural implementation.
- **High-Performance & Low-Power CPU Design:** Expertise in balancing performance demands with energy efficiency constraints.
- **Pipeline & Cache Design:** Architecting and optimizing complex pipeline structures and multi-level cache hierarchies.
- **Performance Modeling & Simulation:** Utilizing advanced tools and methodologies to predict and analyze CPU performance.
- **RTL Design (Verilog):** Proficient in hardware description language for implementing and verifying digital circuits.
- **Technical Leadership & Cross-Functional Team Management:** Proven ability to build, mentor, and lead high-performing engineering teams.

Professional Experience

Director of RISC Core Development | OrionArc, Cambridge, UK | 2018 – Present

- **Led the architecture and development** of OrionArc's next-generation RISC CPU cores, strategically targeting both data center and embedded markets.
- **Built and scaled a high-performing team** of architects and RTL engineers, successfully delivering multiple core revisions on schedule and within specifications.
- **Oversaw the implementation of advanced power management techniques**, achieving a **30% improvement in power efficiency** compared to previous

generations.
- **Collaborated closely with silicon partners and EDA vendors** to optimize design methodology and streamline verification flows, resulting in reduced development timelines.

Principal CPU Architect | ARM Holdings, Cambridge, UK | 2008 – 2018

- **Spearheaded architectural design efforts** for multiple generations of ARM Cortex cores, contributing to the widespread adoption of SoCs in mobile and embedded markets.
- **Pioneered innovative techniques** in pipeline restructuring and dynamic frequency scaling, yielding significant gains in both power and thermal performance.
- **Authored comprehensive internal design specifications** and delivered compelling performance projections to executive leadership, influencing strategic product decisions.
- **Mentored and guided junior architects**, fostering their technical growth and establishing best practices in architectural modeling and documentation across the team.

Education

PhD in Computer Architecture | University of Cambridge, UK | Graduated: 2008

- Dissertation: “Adaptive Microarchitectural Techniques for Energy-Efficient Processor Design”
- Supervised by Professor [Fictional Name], Cambridge Computer Lab

Technical Skills

- **Hardware Languages:** Verilog, SystemVerilog
- **Tools:** Synopsys Design Compiler, ModelSim, Gem5, Simics
- **Concepts:** Superscalar Design, Branch Prediction, Out-of-Order Execution
- **Operating Systems:** Linux, Embedded RTOS environments

Languages

- English (Native)