Priya Sharma

Austin, Texas, USA

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Professional Summary

Accomplished AI Hardware Architect with over 13 years of experience in SoC design, ASIC development, and machine learning acceleration. Proven track record of leading complex chip design projects from concept to production. Expertise in power-efficient architectures and edge computing solutions, with deep expertise in SystemVerilog, hardware-software co-design, and AI inference optimization. Currently leading next-generation AI chip design at OrionArc.

Professional Experience

OrionArc – Austin, TX

Lead AI Chip Architect | 2022 – Present

- Architected a next-generation AI accelerator chip optimized for edge deployments, improving performance-per-watt by 30% over industry benchmarks.
- Led a 12-member cross-functional team through RTL design, verification, and tape-out phases, ensuring on-time and within-budget delivery.
- Collaborated with software teams to optimize compiler and runtime for custom tensor cores, maximizing hardware utilization and performance.
- Spearheaded integration of advanced power management features using custom dynamic voltage scaling, reducing power consumption by 25%.

Qualcomm – Austin, TX

Senior Staff Engineer – AI Hardware Acceleration | 2016 – 2022

- Designed AI compute subsystems for Snapdragon processors, focusing on neural network acceleration and heterogeneous compute optimization.
- Developed custom AI instruction sets and supervised their integration with software compilers, streamlining the development process.
- Reduced inference latency for on-device ML workloads by over 40% through hardware-software co-optimization.
- Co-authored 5 patents related to efficient matrix computation and dataflow architectures.

NXP Semiconductors – Austin, TX

SoC Design Engineer | 2011 – 2016

- Contributed to design and verification of automotive-grade SoCs with emphasis on power integrity and signal timing closure.
- Implemented RTL modules for memory controllers and bus interconnects in SystemVerilog.
- Worked closely with physical design teams to optimize floorplanning for low-power operation.
- Participated in silicon bring-up and validation across multiple product lines.

Education

Master of Science in Electrical & Computer Engineering

University of Texas at Austin — 2011

Skills

- SoC Design & Verification
- AI/ML Hardware Acceleration
- SystemVerilog, Verilog, UVM
- ASIC Design Flow & Tape-out
- Power Management & DVFS
- Edge AI & Embedded Systems

Languages

- English (Fluent)
- Hindi (Native)

Salary Expectation

USD 220,000 per annum