HIGH-VOLTAGE MIXED-SIGNAL IC

UC1601

65x132 STN Controller-Driver

MP Specifications
Revision 1.2

April 8, 2008

ULTRACHIP

The Coolest LCD Driver, Ever!!

Table of Content

UC1601

Single-Chip, Ultra-Low Power
65COM by 132SEG
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1601 is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power column and row drivers, the IC contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA, and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver support 65x132 graphics STN LCD panels.
- Support both row ordered and column ordered display buffer RAM access.
- Support industry standard 3-wire and 4-wire serial bus (S9 and S8), and 8-bit parallel bus (8080 or 6800 mode).
- Ultra-low power consumption under all display patterns.
- Support four multiplexing rates at 65, 49, 33, and 25.
- Software programmable frame rates at 76 and 95 Hz.
- 6-x internal charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.
- On-chip bypass capacitor for V_{LCD} makes V_{LCD} bypass capacitor optional.
- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.
- Very low pin count (10-pin) allows exceptional image quality in COG format on conventional ITO glass.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- V_{DD} (analog) range (Typ.) : 2.5V ~ 3.3V
  V_{DD} (digital) range (Typ.) : 2.5V ~ 3.3V
  LCD V_{OP} range: 5.0V ~ 11.5V
- Software programmable 4 temperature compensation coefficients.
- Available in gold bump dies
  Bump pitch: 50μM min.
  Bump gap: 18μM min.

ORDERING INFORMATION

Part Number	Description
UC1601xGAD	Gold Bumped Die

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

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LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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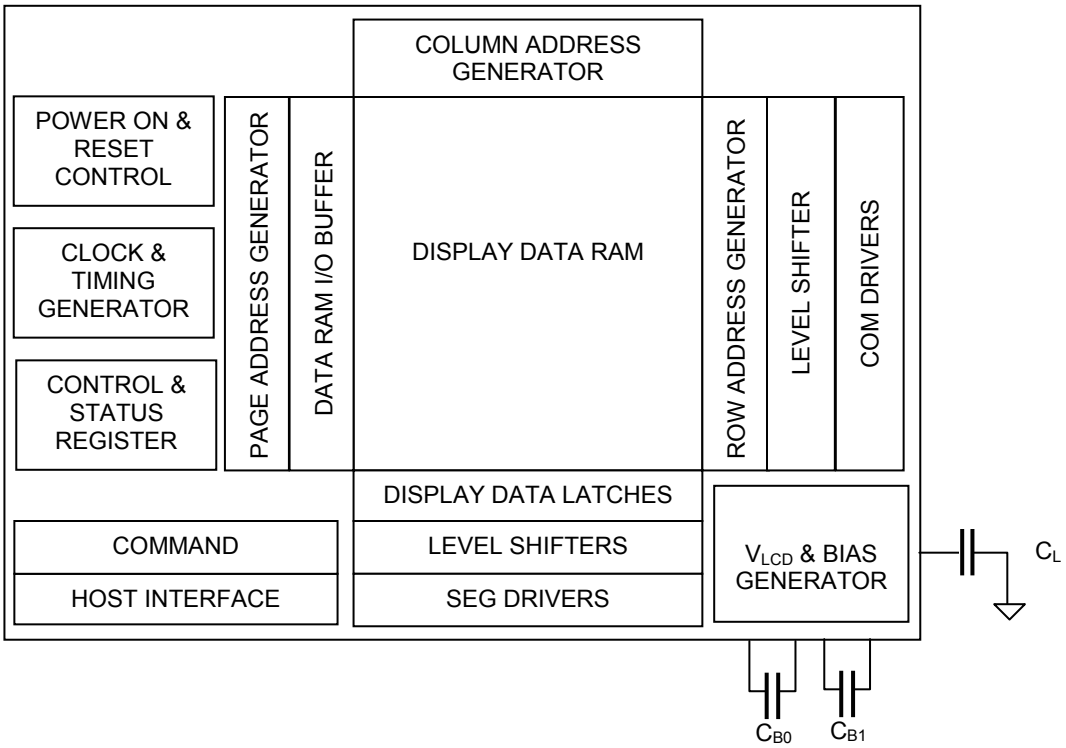
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	3 3 2	V_{DD} supplies for display data RAM and digital logic, V_{DD2} supplies for V_{LCD} and V_D generator, V_{DD3} supplies for V_{BIAS} and other analog circuits. V_{DD2}/V_{DD3} should be connected to the same power source. But V_{DD} can be connected to a source voltage no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: V_{DD}+1.0V ⩾ $V_{DD2/3}$ ⩾ V_{DD} ITO trace resistance needs to be minimized for V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	4 4	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. In COG applications, minimize the ITO resistance for both V_{SS} and V_{SS2}.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+} V_{B1-} V_{B0+} V_{B0-}	PWR	2 2 2 2	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. In COG application, the resistance of these ITO traces directly affects the SEG driving strength of the resulting LCD module. Minimize these trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR	1 1	Main LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} source is used, connect external V_{LCD} source to V_{LCDIN} pins and leave V_{LCDOUT} open. By-pass capacitor C_L is optional. It can be connected between V_{LCD} and V_{SS}. When C_L is used, keep the ITO trace resistance under 300 Ω.

NOTE

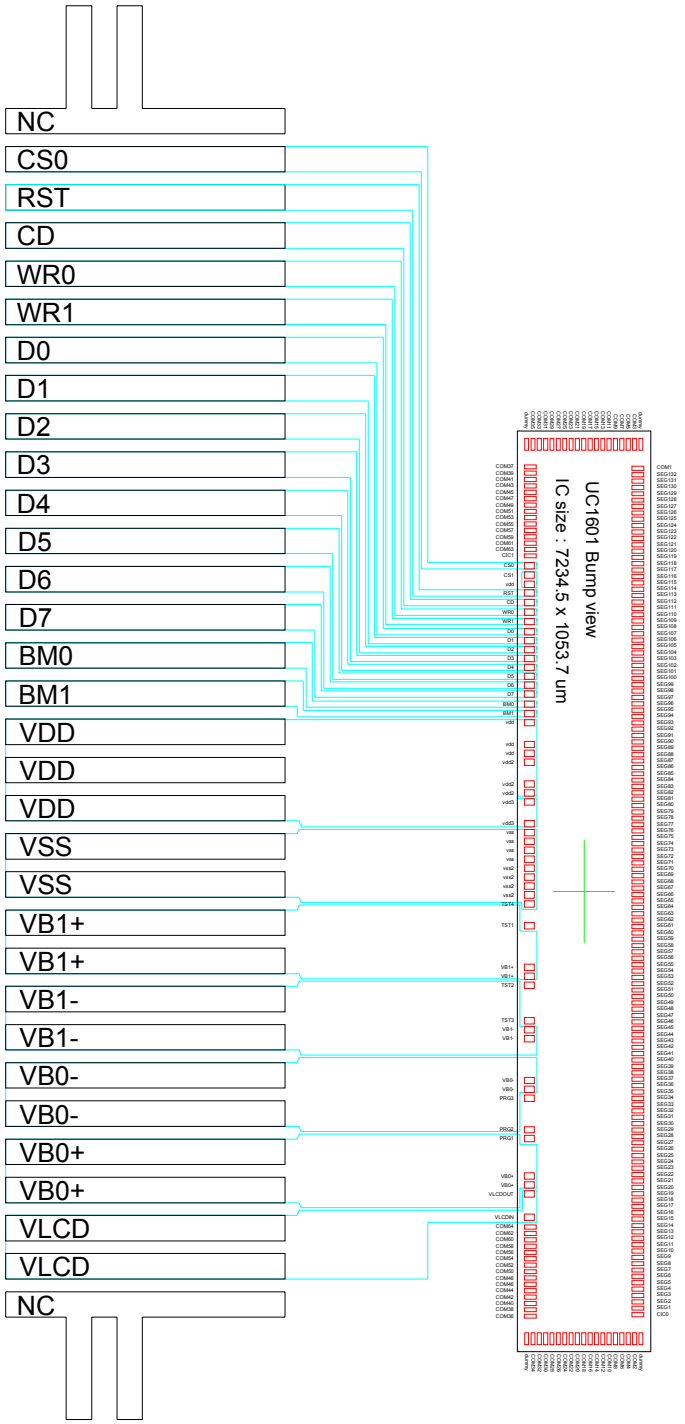
- Recommended capacitor values:
  C_B: 100x ~ 200x LCD load capacitance or 1.0μF (2V), whichever is higher.
  C_L: 10nF ~ 30nF (25V) is appropriate for most applications.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode: “HL”: 8080 “HH”: 6800
BM[1:0] “LH”: S9 “LL”: S8</td></tr>
<tr><td>CS1
CS0</td><td>I</td><td>1
1</td><td>Chip Select or Chip Address. In parallel mode and S8 mode, chip is selected when CS0=”L” and CS1=”H”. When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1601 has built-in Power-On Reset and Software Reset command, RST pin is not required for proper chip operation.
A noise filter is built in chip to prevent the accidental chip reset, for example in an ESD test. When RST is not used, connect the pin to V_{DD}.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select the incoming command if it is a control instruction or for display data. CD pin is not used in S9 mode, connect it to V_{DD} or V_{SS}.
”L”: control instruction ”H”: display data</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR [1:0] controls the read/write operation of the host interface. See Host Interface section for details.
The meaning of WR [1:0] depends on whether the interface is in the 6800 mode, or the 8080 mode. In serial modes, these two pins are not used and can be connected to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D [0] to SCK, D [3] to SDA.
<table>
<tr><th></th><th>BM=1x
(Parallel)</th><th>BM=0x
(Serial)</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td></td></tr>
<tr><td>D2</td><td>D2</td><td></td></tr>
<tr><td>D3</td><td>D3</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td></td></tr>
<tr><td>D5</td><td>D5</td><td></td></tr>
<tr><td>D6</td><td>D6</td><td>-</td></tr>
<tr><td>D7</td><td>D7</td><td>-</td></tr>
</table>
In COG applications, be careful to control ITO trace resistance, as it will affect effective output level of SDA.
Connect any unused pins to V_{SS}.</td></tr>
</table>

Name	Type	Pins	Description
HIGH VOLTAGE LCD DRIVER OUTPUT			
SEG1 ~ SEG132	HV	132	SEG (column) driver outputs. Support up to 132 pixels. Leave unused driver outputs open.
COM1 ~ COM64	HV	64	COM (row) driver outputs. Support up to 64 rows. Leave unused COM driver outputs open.
CIC	HV	2	Icon driver outputs. Leave it open if not used.
MISC. PINS			
V_{DDX}		1	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus on chip, and they are provided to facilitate chip packaging in COG and COF applications. There is no need to connect V_{DDX} to V_{DD} externally. These pins should not be used to provide V_{DD} power to the chip.
TST4	I	1	Test control. Connect to GND.
TST3 TST2 TST1	I/O	1 1 1	Test I/O pins. Leave these pins open during normal use.
TP3 TP2 TP1	I	1 1 1	Test control. Leave these pins open during normal use.

Note: Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COM*X* or SEG*X* will correspond to index *X*-1, and the value range for those index register will be 0~63 for COM and 0~131 for SEG.

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The typical operation condition of UC1601, V_{DD}=2.3V, should be met under all operating conditions. Unless V_{DD} and $V_{DD2/3}$ ITO trances can each be controlled to be 5 Ω or lower; otherwise V_{DD}-$V_{DD2/3}$ separation can cause the actual on-chip V_{DD} to drop below V_{DD}=2.3V during high speed data write condition. Therefore, for COG, V_{DD}-$V_{DD2/3}$ separation requires very careful ITO layout and very stringent testing before MP.

CONTROL REGISTERS

UC1601 contains registers that control the operation of the chip. These registers can be modified by software commands. The commands supported by UC1601 are described in the next section. The following table is a summary of all the registers defined by UC1601 and their default values.

Name: Symbolic reference of the register.
Bits: Number of bits in this register.
Default: Register value after the chip power up or system reset. The bold numbers show these defaults.
Description: Register meaning and functions.

Name	Bits	Default	Description
SL	6	0H	Scroll Line. Scroll the displayed image up by *SL* rows. The valid SL value is between 0 (for no scrolling) and 63. Setting SL outside of this range causes undefined effects on the displayed image. This register does not affect icon output CIC.
CR	8	0H	Return Column Address. Useful for cursor implementation.
CA	8	0H	Display Data RAM Column Address. Value range is 0~131. (Used Display Data RAM access from Host Interface)
PA	4	0H	Display Data RAM Page Address. Value range 0~8. (Used Display Data RAM access from Host Interface)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_D. 00: 6 01: 7 10: 8 **11: 9**
TC	2	0H	Temperature Compensation (per ^oC). **00: -0.05%** 01: -0.10% 10: -0.15% 11: -0.20%
PM	8	C0H	Electronic Potentiometer to fine tune the value of V_{LCD}
OM	2	–	Operating Modes (read only) 00: Reset 01: (Not used) 10: Sleep 11: Normal
RS	1		Reset in progress. Host Interface not ready
PC	3	6H	Power Control. PC [0]: **0: LCD: ≤ 15nF** 1: LCD: > 15nF PC [2:1]: 00: External V_{LCD} 01: Internal V_{LCD} (Low V_{LCD}, used when V_{LCD} < 7V) **11: Internal V_{LCD} (standard)**
APC0	8	4DH	Advanced Program Control. Default value should work fine.

Name	Bits	Default	Description
MR	2	2H	Multiplexing rate control: 00b: 25 01b: 33 10b: 49 **11b: 65**
DC	3	00H	Display Control: DC[0]: PXV: Pixels Inverse (bit-wise data inversion. Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**)
AC	4	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (**Default 1: ON**) AC[1]: Auto-Increment order **0: Column (CA) first** 1: Page (PA) first AC[2]: PID: PA(page address) auto increment direction (**L:+1** H:-1) AC[3]: CUM: Cursor update mode, (Default **0: OFF**) when CUM=1, CA increment on write only, wrap around suspended
LC	4	0H	LCD Control: LC[0]: Reserved. LC[1]: MX, Mirror X (Column sequence inversion) (Default: **OFF**) LC[2]: MY, Mirror Y (Row sequence inversion) (Default: **OFF**) LC[3]: Frame Rate **0b: 76 fps** 1b: 95 fps

COMMAND TABLE

The following is a list of host commands supported by UC1601

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle

\# Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	-	MX	MY	RS	WA	DE	–		N/A	
4.	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA [3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA [7:4]	0
5.	Set Multiplexing Rate	0	0	0	0	1	0	0	0	#	#	Set MR [1:0]	11b: 65
6.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b: -0.05%/°C
7.	Set Panel Loading	0	0	0	0	1	0	1	0	0	#	Set PC[0]	0b: < 15nF
8.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[2:1]	11b
9.	Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0],	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#	R = 0, or 1	
10.	Set Scroll Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
11.	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
12.	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	C0H
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
13.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14.	Set Frame Rate	0	0	1	0	1	0	0	0	0	#	Set LC[3]	0b
15.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17.	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0
18.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	0	Set LC[2:1]	0
19.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
20.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
21.	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#	Do not use.	
22.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 9
23.	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	N/A
24.	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	N/A

* Any bit patterns other than what is listed above may result in NOP (No Operation).

COMMAND DESCRIPTION

1. Write Data Byte to Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

2. Read Data Byte from Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Write/Read Data Byte (Command 1,2) access display data RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increment or decrement automatically after each bus cycle, depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of the page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches the end of the page, CA will be reset to 0 and PA will increase or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM, PA will be wrapped around to the other end of RAM and continue. (See command 30, Window Programming, for more details)

3. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	-	MX	MY	RS	WA	DE	-	-

Status flag definitions:

MX: Status of register LC[1], mirror X.
MY: Status of register LC[2], mirror Y.
RS: Reset in progress. If RS=1.host interface will be inaccessible.
WA: Status of register AC[0]. Automatic column/row wrap around.
DE: Display enable flag. DE=1 when display is enabled.

4. Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address - LSB, CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address - MSB, CA[7:4]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA value range: **0**~131

5. Set Multiplexing Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Multiplexing Rate, MR[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**0**	MR1	MR0

Set the multiplexing rate of the chip:

00b= 25 01b= 33 10b= 49 **11b= 65**

6. Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp., TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.05%/C 01b= -0.10%/C 10b= -0.15%/C 11b= -0.20%/C

7. Set Panel Loading

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading, PC[0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**0**	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: **0b≤ 15nF** 1b > 15nF

8. Set Pump Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control, PC[2:1]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC2	PC1

Set PC[2:1] to program the build-in charge pump stages.

00b= External V_{LCD} 01b= Internal V_{LCD} (V_{LCD} < 7V) **11b= Internal V_{LCD} (standard)**

9. Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control, APC[R][7:0](Double-byte command)	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
	0	0	APC register parameter							

For UltraChip only. Please Do *NOT* use.

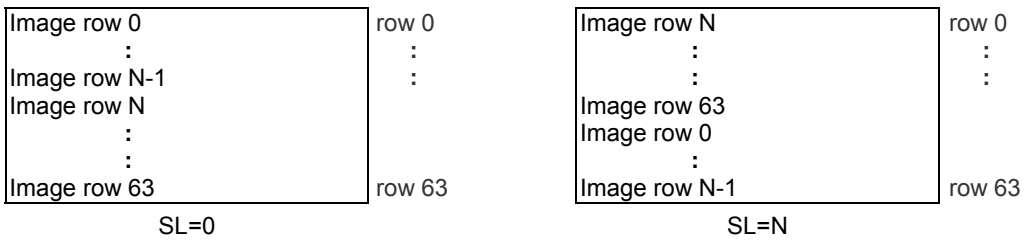
10. Set Scroll Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line, SL[5:0]	0	0	**0**	**1**	SL5	SL4	SL3	SL2	SL1	SL0

Set the scroll line number. Possible value = **0-63**

Scroll line setting will scroll the displayed image up by *SL* rows.

Icon output CIC will not be affected by `Set Scroll Line` command.



11. Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address, PA[3:0]	0	0	**1**	**0**	**1**	**1**	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface. Each page of SRAM corresponds to 8 COM lines on LCD panel, except for the last page. The last page corresponds to the icon output CIC.

Possible value = **0~8.**

12. Set V_{BIAS} Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer, PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM[7:0]							

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 255**

13. Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Address Control, AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control. It controls the auto-increment behavior of CA and PA.

AC[0] - WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or PA will increment by one step.

AC[1] – Auto-Increment order
0 : column (CA) increment (+1) first until CA reach CA boundary, then PA will increment by (+/-1).
1 : page (PA) increment (+/-1) first until PA reach PA boundary, then CA will increment by (+1).

AC[2] – PID, page address (PA) auto increment direction (0/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether page address will be adjusted by +1 or –1.

14. Set Frame Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate, LC [3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	LC3

Program LC [3] for frame rate setting

0b: 76 fps 1b: 95 fps
(fps: frame-per-second)

15. Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON, DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

16. Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display, DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

17. Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable, DC[2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	DC2

This command is for programming register DC[2]. When DC[2] is set to 1, UC1601 will first exit from sleep mode, restore the power and then turn on COM drivers and SEG drivers.

18. Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Control, LC[2:1]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	0

Set LC[2:1] for COM (row) mirror (MY), SEG (column) mirror (MX).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 50-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

19. System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset.

Control register values will be reset to their default values. Data store in RAM will not be affected.

20. NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

21. Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do *NOT* use.

22. Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio, BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b= 6 01b= 7 10b= 8 **11b= 9**

23. Reset Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=0 CA=CR	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This command is used to reset cursor update mode function.

24. Set Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**

This command is used for set cursor update mode function. When cursor update mode sets, UC1601 will update register CR with the value of register CA. The column address CA will increment with write RAM data operation but the address wraps around will be suspended no matter what WA setting is. However, the column address will not increment in read RAM data operation. The set cursor update mode can be used to implement “write after read RAM” function. The column address (CA) will be restored to the value, which is before the set cursor update mode command, when reset cursor update mode.

The purpose of this pair commands and their feature is to support “write after read” function for cursor implementation.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate (*MR*) is completely software programmable in UC1601 via the register MR.

The allowable MR value is defined in the following table:

MR	0	1	2	3
Multiplex Rate	25	33	49	65

Table 1: Bias Ratios

BIAS SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e. $BR = V_{LCD}/V_{BIAS}$, where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$, etc.

UC1601 supports four bias ratios (BR) as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6	7	8	9

Table 2: Bias Ratios

The tunable range of V_{BIAS} is from 0.8 V to 1.32 V at 25 °C.

V_{BIAS} TEMPERATURE COMPENSATION

V_{BIAS} is a temperature compensated reference voltage. V_{BIAS} increases automatically as ambient temperature cools down.

For all four TC, V_{BIAS} are normalized to a same voltage at 25 °C. The compensation coefficients are given below:

TC	0	1	2	3
% per °C	-0.05	–0.10	–0.15	–0.20

Table 3: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[2:1]. For good product reliability, it is recommended to keep V_{LCD} under 11.5 V for all temperature conditions.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by four control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two design constants. The values are provided in the Figure on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment is the recommended method for V_{LCD} fine-tuning.

For applications where mechanical manual fine-tuning of V_{LCD} becomes necessary, then V_{BIAS} pin may be used with an external trim pot to fine tune the V_{LCD}. Please refer to Application Notes for more detailed discussion on this subject.

LOAD DRIVING STRENGTH

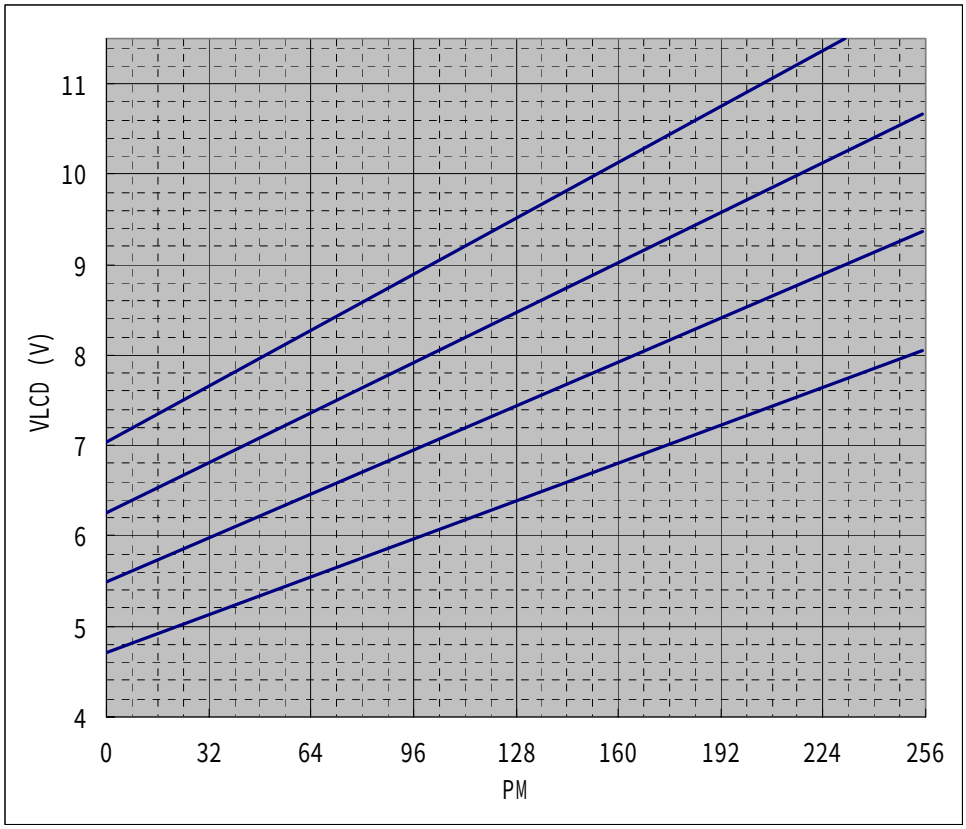
UC1601's power supply circuits are designed to handle LCD panels with load capacitance up to ~30nF when V_{DD2} = 2.5V, and up to ~35nF when $V_{DD2} \geq$ 3V.

POWER UP/DOWN SEQUENCE

Due to the use of fully embedded power supply, built-in power ready detector, and draining circuit, there is no explicit power up, power down sequences for UC1601 controllers when using internal V_{LCD} generator.

On the other hand, caution must be exercised when external V_{LCD} source is used. The general rule of thumb is to make sure Display Enable is OFF before connecting or disconnecting external V_{LCD} sources.

V_{LCD} QUICK REFERENCE



V_{LCD} Programming Curve.

BR	C_{V0} (V)	C_{PM} (mV)	PM	V_{LCD} Range (V)
6	4.712	13.093	0	4.712
			255	8.051
7	5.494	15.220	0	5.494
			255	9.375
8	6.266	17.236	0	6.266
			255	10.661
9	7.038	19.348	0	7.038
			231	11.507

Note:

1. The maximum reliable V_{LCD} operating value is at 11.5V.
2. For best reliability, keep V_{LCD} under **11.5V** over all temperature.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

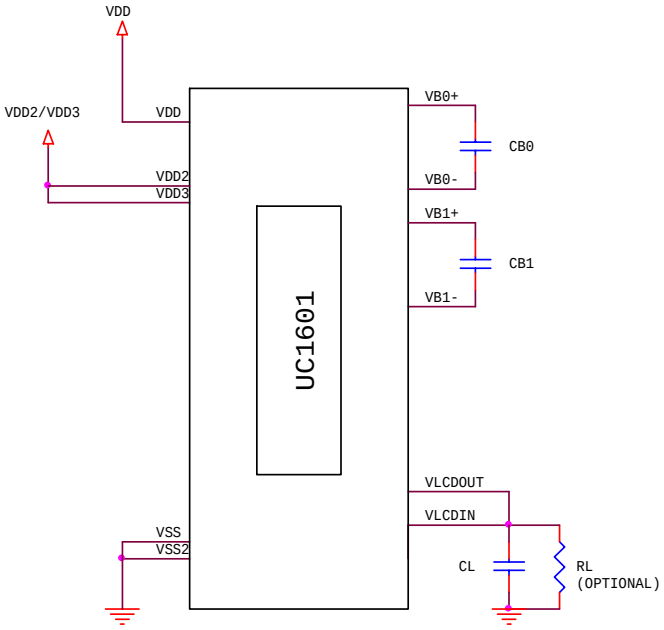


FIGURE 1: Reference circuit using internal Hi-V generator circuit

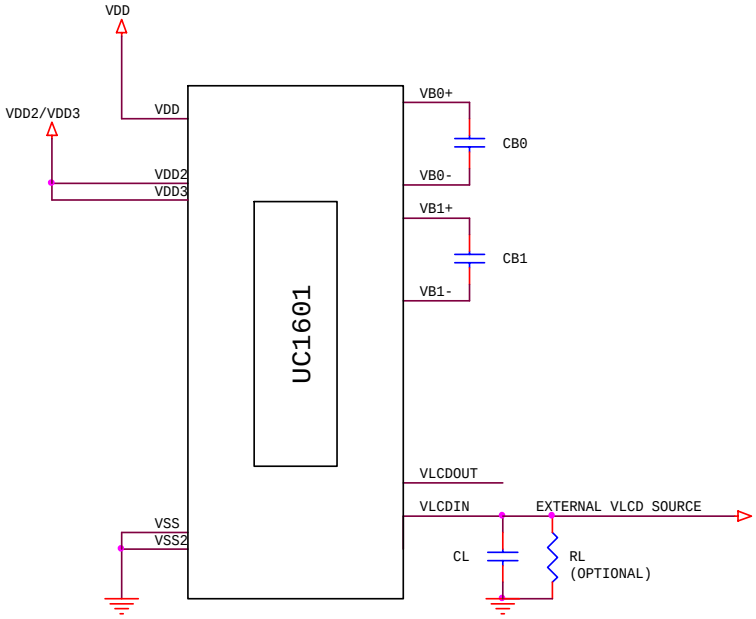


FIGURE 2: Reference circuit using external Hi-V source

Note

- Recommended component values:
  C_B: 100x~200x LCD load capacitance or 1.0uF (2V), whichever is higher.
  C_L: 10nF ~ 30nF (25V) is appropriate for most applications.
  R_L: 10MΩ. Acts as a draining circuit when the power is abnormally shut down.
- The illustrated resistor values are for reference only. Please optimize for specific requirements of each application.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1601 contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Two different frame rates are provided for system design flexibility: 76 fps and 95 fps.

Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG and COM drivers are in idle mode, their outputs are connected to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM*x* (where x = 1~64) refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display ON* command. When DC[2] is set to OFF (logic “0”), both column and row drivers will become idle and UC1601 will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”,and UC1601 will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on row drivers and proper column drivers.

ALL PIXELS ON (APO)

When set, this flag will force all active column drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, active column drivers will output the inverse of the value it received from the display buffer RAM. This flag has no impact on data stored in RAM.

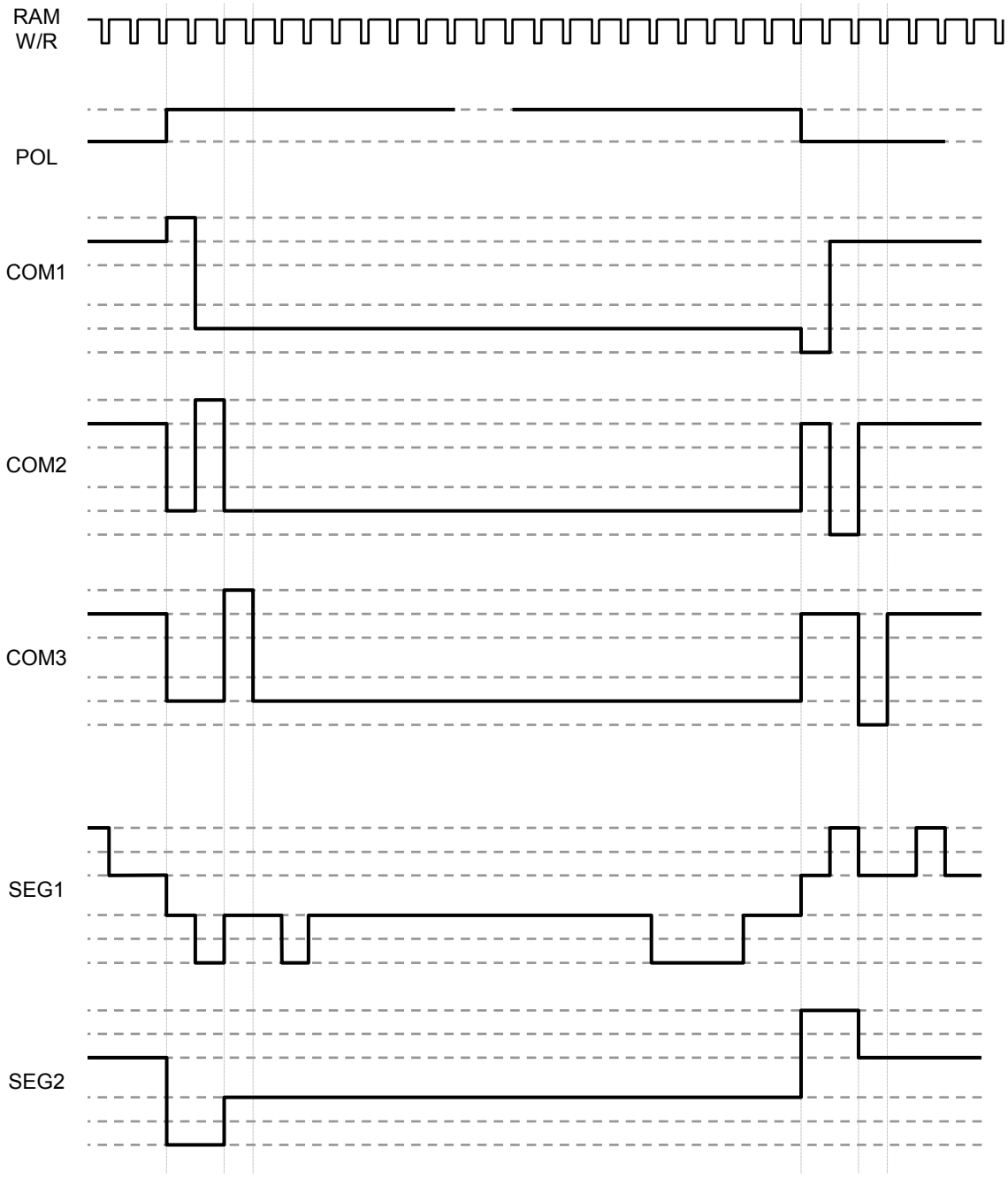


FIGURE 3: COM and SEG Electrode Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1601 supports two 8-bit parallel bus protocols and two serial bus protocols. Designers can choose either the 8-bit parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules and minimize connector pins.

Bus Type		8080	6800	SPI (S8)	SPI (S9)
Control & Data Pins	BM[1:0]	10b	11b	00b	01b
	CS[1:0]	Chip Select			
	CD	Control/Data			–
	WR0	$\overline{WR}$	R/$\overline{W}$	–	
	WR1	$\overline{RD}$	EN	–	
	Access	Read/Write		Write Only	
	D[7:0]	8-bit bus (Tri-state)		D0=SCK, D3=SDA	

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

Table 4: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1601 internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that, every time memory address is modified, either in parallel mode or serial mode, by either *Set CA* or *Set PA* command, a dummy read cycle need to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

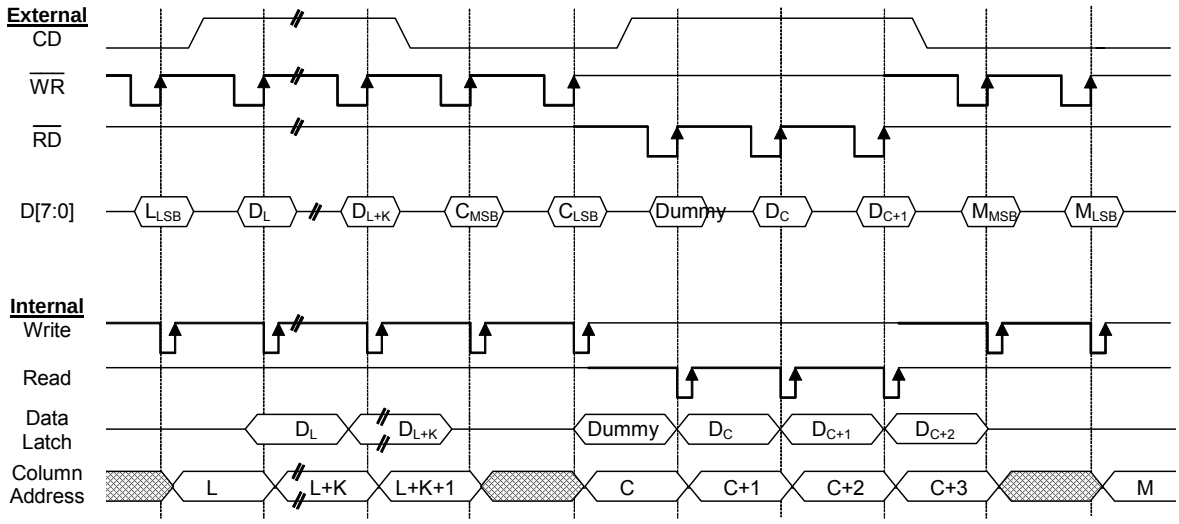


Figure 4: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1601 supports two serial modes, 4-wire mode (BM=00), and 3-wire mode (BM=01). The mode of interface is determined during power-up process by the value of BM[1:0].

4-WIRE SERIAL INTERFACE (S8)

Only write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

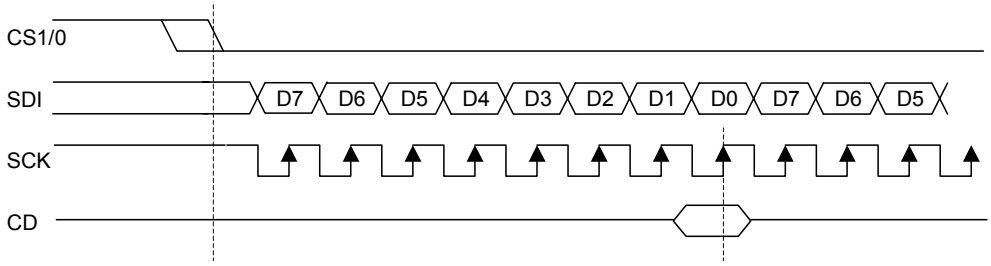


Figure 5.a: 4-wire Serial Interface (S8)

3-WIER SERIAL INTERFACE (S9)

Only write operations are supported in 3-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}.

The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

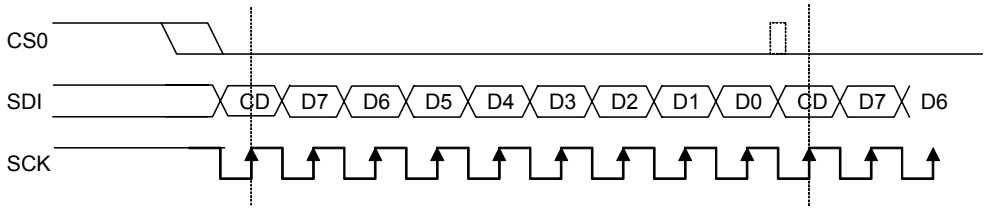


Figure 5.b: 3-wire Serial Interface (S9)

HOST INTERFACE REFERENCE CIRCUIT

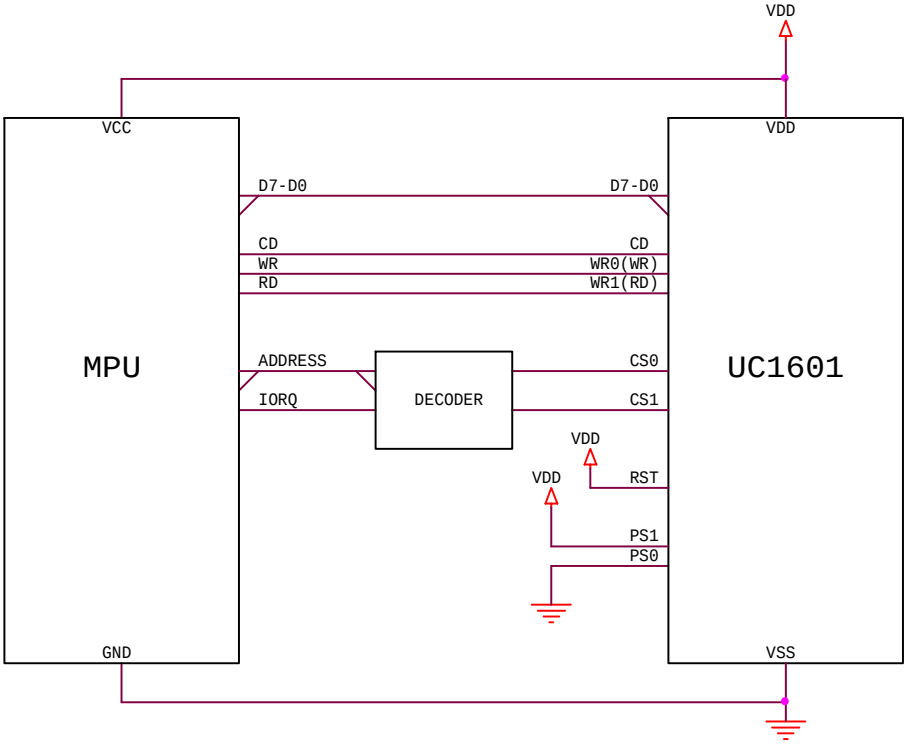


FIGURE 6: 8080/8bit parallel mode reference circuit

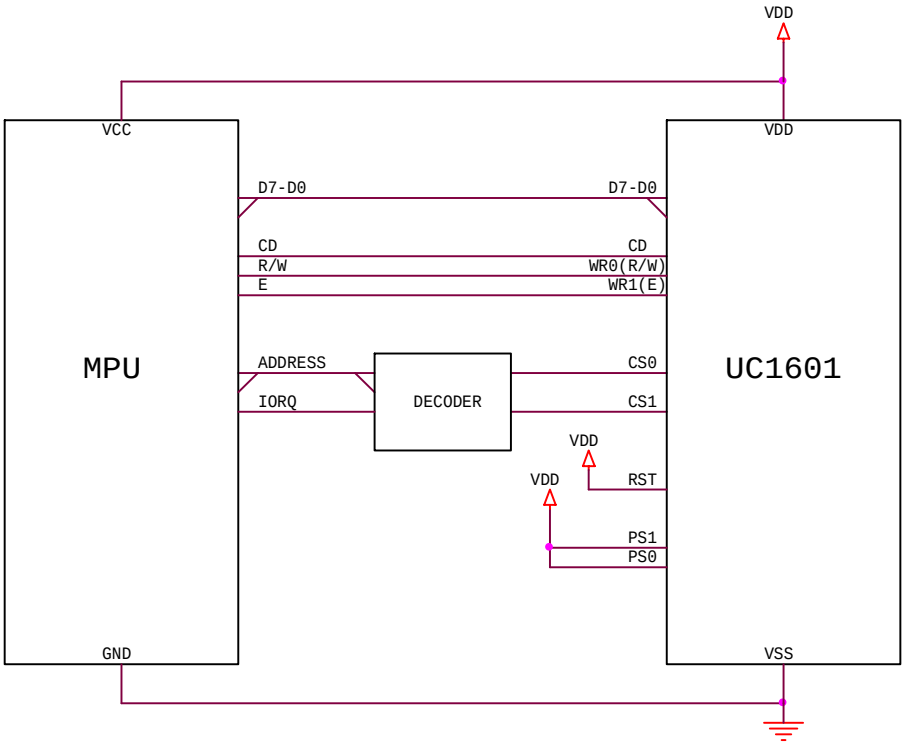


FIGURE 7: 6800/8bit parallel mode reference circuit

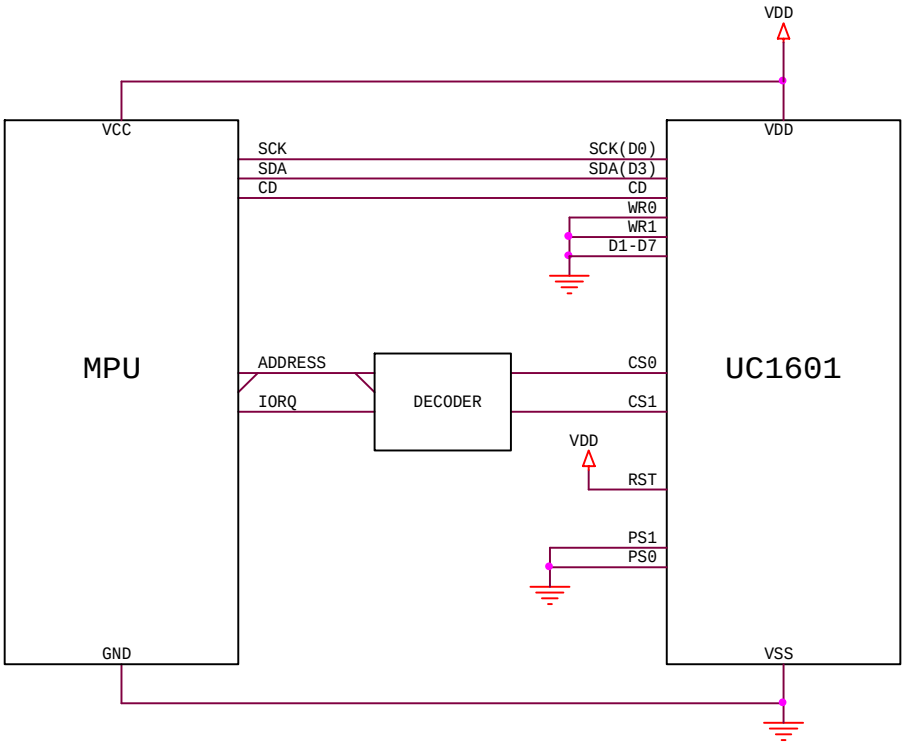


FIGURE 8: Serial-8 serial mode reference circuit

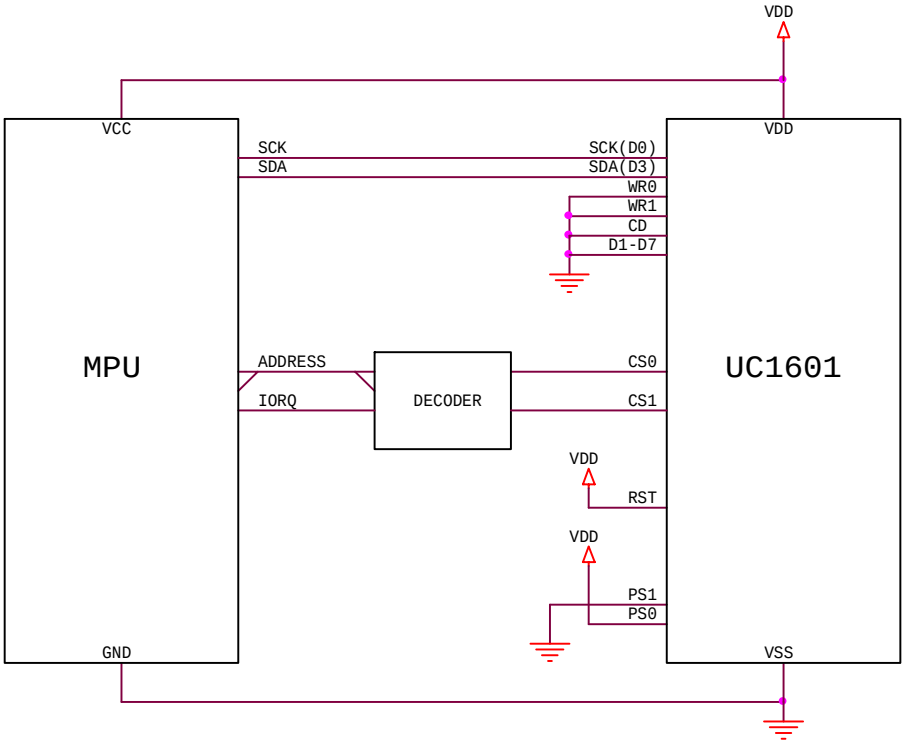


FIGURE 9: Serial-9 serial mode reference circuit

Note: RST pin is optional. When RST pin is not used, connect the pin to V_{DD}.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 65x132.

After setting CA and RA, the next two data write cycle will store the data for the specified pixel to the proper memory location.

columns. When Mirror X (MX, LC[2]) is OFF, the 1st column of memory data will correspond to the 1st and 2nd column of LCD pixels, etc.

DISPLAY DATA RAM ACCESS

The memory used in UC1601 Display Data RAM (RAM??) is a special purpose dual port RAM that allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row (131), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 7), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (131–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW SCANNING

For each field, the scanning starts at R1 through R*m*, where *m* depends on the setting of MR.

Row electrode scanning orders are not affected by Start Line (SL), or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, 64)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

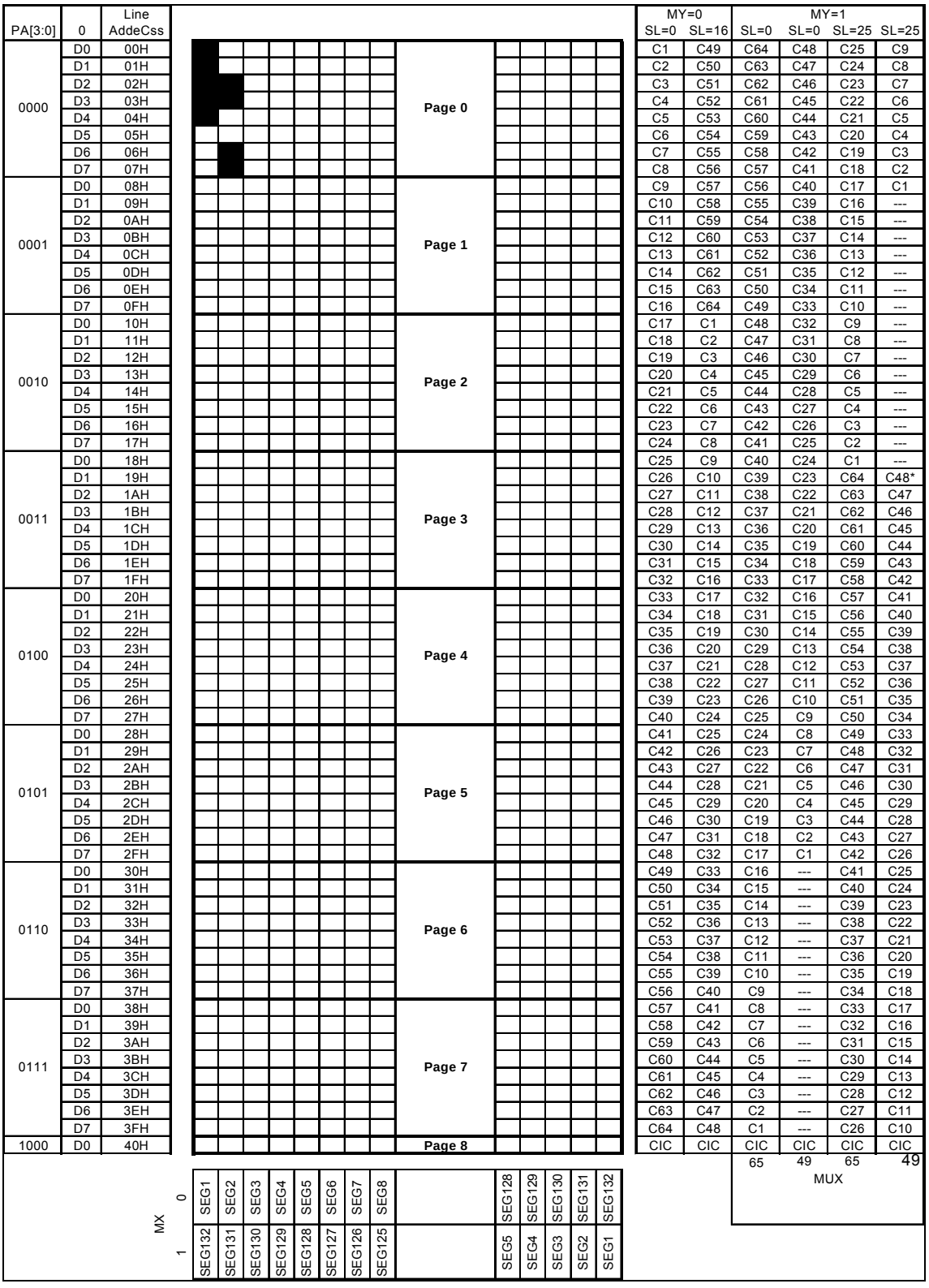
The above *Line* generation formula produce the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MR -1*, *64*)
Otherwise
Line = Mod(*Line-1* , *64*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.



PA[3:0]	0	Line AddeCss	Page	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=0	MY=1 SL=25	MY=1 SL=25
0000	D0	00H	Page 0	C1	C49	C64	C48	C25	C9
	D1	01H		C2	C50	C63	C47	C24	C8
	D2	02H		C3	C51	C62	C46	C23	C7
	D3	03H		C4	C52	C61	C45	C22	C6
	D4	04H		C5	C53	C60	C44	C21	C5
	D5	05H		C6	C54	C59	C43	C20	C4
	D6	06H		C7	C55	C58	C42	C19	C3
	D7	07H		C8	C56	C57	C41	C18	C2
0001	D0	08H	Page 1	C9	C57	C56	C40	C17	C1
	D1	09H		C10	C58	C55	C39	C16	---
	D2	0AH		C11	C59	C54	C38	C15	---
	D3	0BH		C12	C60	C53	C37	C14	---
	D4	0CH		C13	C61	C52	C36	C13	---
	D5	0DH		C14	C62	C51	C35	C12	---
	D6	0EH		C15	C63	C50	C34	C11	---
	D7	0FH		C16	C64	C49	C33	C10	---
0010	D0	10H	Page 2	C17	C1	C48	C32	C9	---
	D1	11H		C18	C2	C47	C31	C8	---
	D2	12H		C19	C3	C46	C30	C7	---
	D3	13H		C20	C4	C45	C29	C6	---
	D4	14H		C21	C5	C44	C28	C5	---
	D5	15H		C22	C6	C43	C27	C4	---
	D6	16H		C23	C7	C42	C26	C3	---
	D7	17H		C24	C8	C41	C25	C2	---
0011	D0	18H	Page 3	C25	C9	C40	C24	C1	---
	D1	19H		C26	C10	C39	C23	C64	C48*
	D2	1AH		C27	C11	C38	C22	C63	C47
	D3	1BH		C28	C12	C37	C21	C62	C46
	D4	1CH		C29	C13	C36	C20	C61	C45
	D5	1DH		C30	C14	C35	C19	C60	C44
	D6	1EH		C31	C15	C34	C18	C59	C43
	D7	1FH		C32	C16	C33	C17	C58	C42
0100	D0	20H	Page 4	C33	C17	C32	C16	C57	C41
	D1	21H		C34	C18	C31	C15	C56	C40
	D2	22H		C35	C19	C30	C14	C55	C39
	D3	23H		C36	C20	C29	C13	C54	C38
	D4	24H		C37	C21	C28	C12	C53	C37
	D5	25H		C38	C22	C27	C11	C52	C36
	D6	26H		C39	C23	C26	C10	C51	C35
	D7	27H		C40	C24	C25	C9	C50	C34
0101	D0	28H	Page 5	C41	C25	C24	C8	C49	C33
	D1	29H		C42	C26	C23	C7	C48	C32
	D2	2AH		C43	C27	C22	C6	C47	C31
	D3	2BH		C44	C28	C21	C5	C46	C30
	D4	2CH		C45	C29	C20	C4	C45	C29
	D5	2DH		C46	C30	C19	C3	C44	C28
	D6	2EH		C47	C31	C18	C2	C43	C27
	D7	2FH		C48	C32	C17	C1	C42	C26
0110	D0	30H	Page 6	C49	C33	C16	---	C41	C25
	D1	31H		C50	C34	C15	---	C40	C24
	D2	32H		C51	C35	C14	---	C39	C23
	D3	33H		C52	C36	C13	---	C38	C22
	D4	34H		C53	C37	C12	---	C37	C21
	D5	35H		C54	C38	C11	---	C36	C20
	D6	36H		C55	C39	C10	---	C35	C19
	D7	37H		C56	C40	C9	---	C34	C18
0111	D0	38H	Page 7	C57	C41	C8	---	C33	C17
	D1	39H		C58	C42	C7	---	C32	C16
	D2	3AH		C59	C43	C6	---	C31	C15
	D3	3BH		C60	C44	C5	---	C30	C14
	D4	3CH		C61	C45	C4	---	C29	C13
	D5	3DH		C62	C46	C3	---	C28	C12
	D6	3EH		C63	C47	C2	---	C27	C11
	D7	3FH		C64	C48	C1	---	C26	C10
1000	D0	40H	Page 8	CIC	CIC	CIC	CIC	CIC	CIC
						65	49	65	49
							MUX		

MX																
0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG128	SEG129	SEG130	SEG131	SEG132
1	SEG132	SEG131	SEG130	SEG129	SEG128	SEG127	SEG126	SEG125		SEG5	SEG4	SEG3	SEG2	SEG1

Example for memory mapping: let MX = 0, MY = 0, SL = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1: 00011111b
⇒ Page 0 SEG 2: 11001100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1601 has two different types of Reset:
Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1601 enters RESET sequence:

- Operation mode will be "Reset"
- System Status bit RS will stay as "1" until the Reset process is completed. When RS=1, the IC will only respond to *Get Status* command. All other commands are ignored.
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1601 has three operating modes (OM):
Reset, Sleep, Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 5: Operating Modes

CHANGING OPERATION MODE

Two commands will initiate OM transitions:
Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter power saving mode.

OM changes are synchronized with the edges of UC1601 internal clock. To ensure consistent system states, wait at least 10μS after *Set Display Enable or System Reset* command.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 6: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1601 consumes very little energy in Sleep mode (typically under 2μA).

EXITING SLEEP MODE

UC1601 contains internal logic to check whether V_{LCD} and V_D are ready before releasing row and column drivers from their OFF states. When exiting Sleep Mode and Reset Mode, column and row drivers will not be activated until UC1601 internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1601 power-up sequence is simplified by built-in "Power Ready" flags and by the automatic invocation of *System-Reset* command after *Power-ON-Reset*. System programmer is required to wait for only 5 ~ 10 ms before starting to issue commands to UC1601. No additional commands or waits are required between enabling of the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on V_{DD}, Vdd2/3 should be started not later than V_{DD}.

Delay allowance between V_{DD} and Vdd2/3 is illustrated as Figure 12.

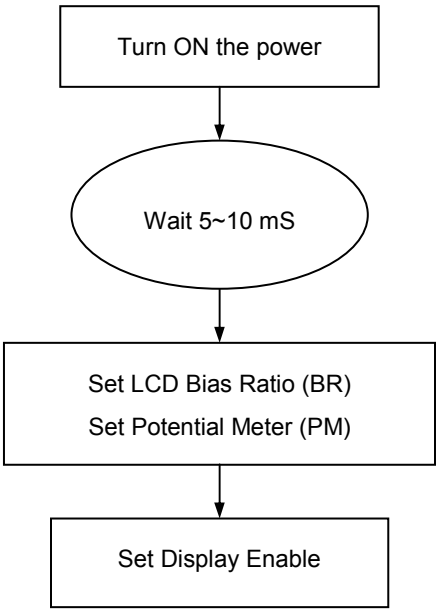


FIGURE 10: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L causing abnoraml residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

UC1601 will *not* drain V_{LCD} when internal V_{LCD} is not used. System designer should take care to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

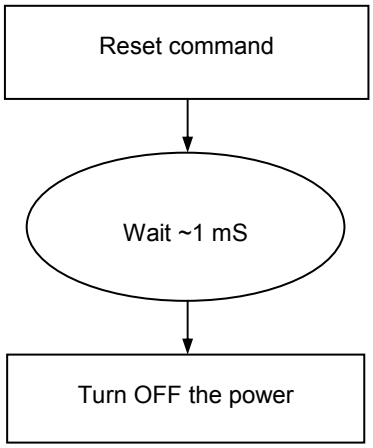


FIGURE 11: Reference Power-Down Sequence

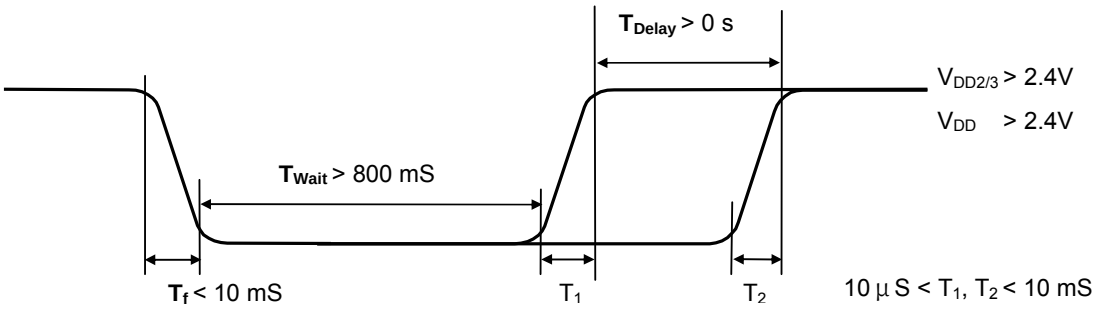


Figure 12: Delay allowance and Power Off-On Sequence

Sample Command Sequences for Power Management
The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)
W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).
Type Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~5mS after V_{DD} is ON
C	0	0	0	0	1	0	0	1	#	#	(6) Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	(18) Set LCD Mapping Control	
A	0	0	1	0	1	0	0	0	0	#	(14) Set Frame Rate	Fine tune for power, flicker, contrast.
C	0	0	1	1	1	0	1	0	#	#	(22) Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(12) Set V_{BIAS} Potentiometer	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	(17) Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	(19) System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	(17) Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	(17) Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is, therefore, highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1601 require special "ESD Sensitivity" consideration in particular:

Test Mode / Pin Name	MM* V_{DD}	MM* V_{SS}	HBM* V_{DD}	HBM* $+V_{SS}$
VB1+	Pass 75V	Pass 75V	Pass 1500V	Pass 1500V
VB1-	Pass 75V	Pass 75V	Pass 1500V	Pass 1500V
VB0+	Pass 75V	Pass 75V	Pass 1500V	Pass 1500V
VB0-	Pass 75V	Pass 75V	Pass 1500V	Pass 1500V
$V_{LCDIN}/_{OUT}$	Pass 150V	Pass 150V	Pass 1500V	Pass 1500V
COM/SEG Driver pins	Pass 100V	Pass 100V	Pass 1500V	Pass 1500V

* MM: Machine Mode; HBM: Human Body Mode

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 - notes 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.2	V
V_{LCD}	LCD Generated voltage	-0.3	+12.0	V
V_{IN} / V_{OUT}	Any input/output	-0.4	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Notes

1. V_{DD} is based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.4	2.5~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.4	2.5~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant$ 2.4V, 25^{O}C			11.5	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant$ 2.4V, 25^{O}C	0.80		1.32	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 11V		2	3	kΩ
$R_{0(COM)}$	COM output impedance	V_{LCD} = 11V		2	3	kΩ
F_{FR}	Average Frame Rate	LC[3] = 0b	66	76	--	Hz

POWER CONSUMPTION

V_{DD} =2.7V,
V_{LCD} = 10.8V
Mux Rate = 65,
C_B = 1μF

Bias Ratio = 11b,
Frame Rate = 0b,
Bus mode = 6800,
Temperature = 25^{o}C,

PM = 192,
Panel Loading (PC[0]) $\leqslant$ 0b,
C_L = 30nF,
All outputs are open circuit.

Display Pattern	Conditions	Typ.	Max.
All-OFF	Bus = idle	143	215
2-pixel checker	Bus = idle	158	237
-	Bus = idle (standby current)	-	5

AC CHARACTERISTICS

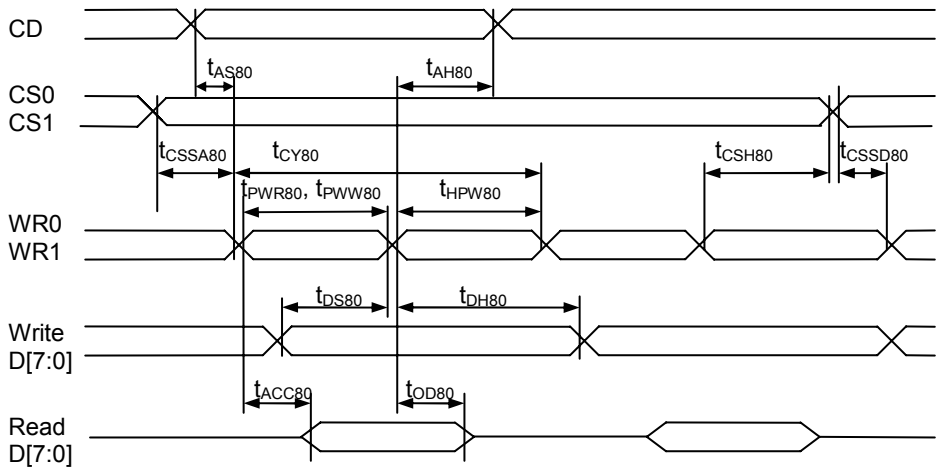


FIGURE 13: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.6V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 40	–	nS
t_{CY80}		System cycle time		135	–	nS
t_{PWR80}	WR1	Pulse width (read)		65	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80}	WR0, WR1	High pulse width		65	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 20	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	50 50	nS
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		nS

(2.4V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 60	–	nS
t_{CY80}		System cycle time		280	–	nS
t_{PWR80}	WR1	Pulse width (read)		95	–	nS
t_{PWW80}	WR0	Pulse width (write)		95	–	nS
t_{HPW80}	WR0, WR1	High pulse width		95	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 30	–	nS
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	50 50	nS
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		nS

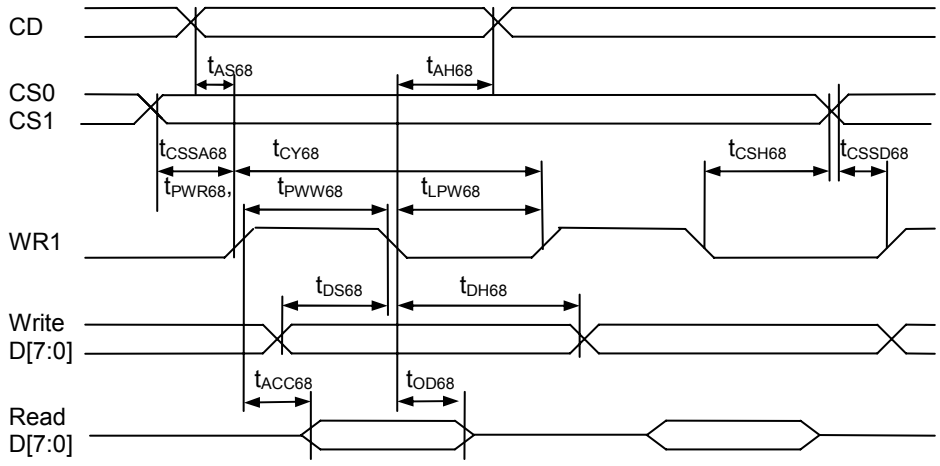


FIGURE 14: Parallel Bus Timing Characteristics (for 6800 MCU)

($2.5V \leqslant V_{DD} < 3.6V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 40	–	nS
t_{CY68}		System cycle time		135	–	nS
t_{PWR68}	WR1	Pulse width (read)		65	–	nS
t_{PWW68}		Pulse width (write)		65	–	nS
t_{LPW68}		Low pulse width		65	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 15	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	50 50	nS
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		nS

($2.4V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 60	–	nS
t_{CY68}		System cycle time		200	–	nS
t_{PWR68}	WR1	Pulse width (read)		95	–	nS
t_{PWW68}		Pulse width (write)		95	–	nS
t_{LPW68}		Low pulse width		95	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 30	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	50 50	nS
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		nS

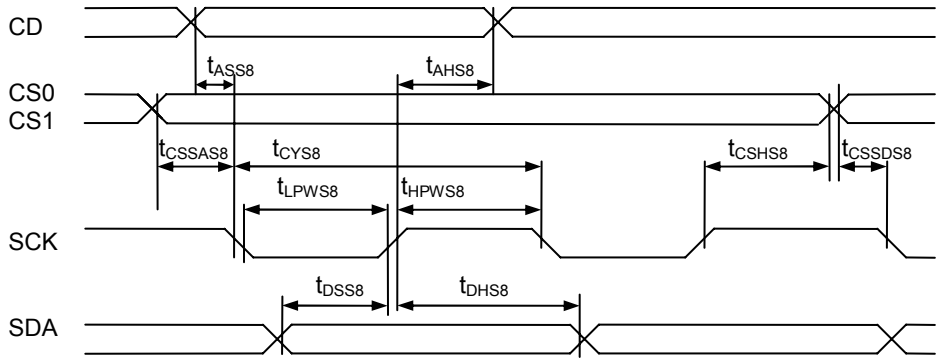


FIGURE 15: Serial Bus Timing Characteristics (for S8)

($2.5V \leqslant V_{DD} < 3.6V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		40	–	nS
t_{CYS8}	SCK	System cycle time		135	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 15	–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10 20		nS

($2.4V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		60	–	nS
t_{CYS8}	SCK	System cycle time		200	–	nS
t_{LPWS8}		Low pulse width		95	–	nS
t_{HPWS8}		High pulse width		95	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 25	–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10 20		nS

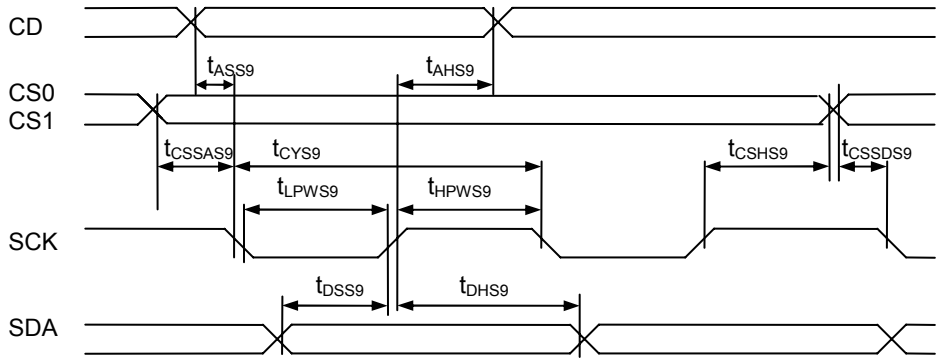


FIGURE 16: Serial Bus Timing Characteristics (for S9)

(2.5V ⩽ V_{DD} < 3.6V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS9}	CD	Address setup time		0	–	nS
t_{AHS9}		Address hold time		40	–	nS
t_{CYS9}	SCK	System cycle time		135	–	nS
t_{LPWS9}		Low pulse width		65	–	nS
t_{HPWS9}		High pulse width		65	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 15	–	nS
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10 20		nS

(2.4V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS9}	CD	Address setup time		0	–	nS
t_{AHS9}		Address hold time		60	–	nS
t_{CYS9}	SCK	System cycle time		200	–	nS
t_{LPWS9}		Low pulse width		95	–	nS
t_{HPWS9}		High pulse width		95	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10 20		nS

FIGURE 17: Reset Characteristics

(2.4V ≤ V_{DD} < 3.6V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1	–	µS

PHYSICAL DIMENSIONS

DIE SIZE:
7284.5 x 1103.7 μM^2

DIE THICKNESS:
0.5 mm

BUMP HEIGHT:
17 µM (within die)
(H_{MAX} – H_{MIN}) within die < 2 µM

COM/SEG SIZE:
32 x 94 µM (Typical)

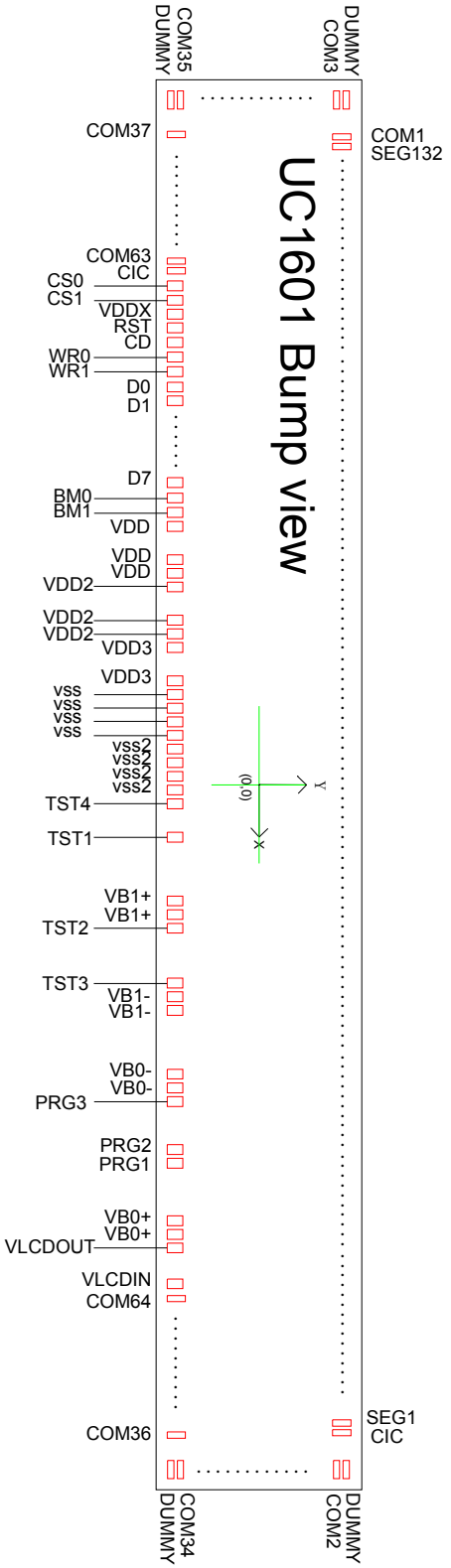
MINIMUM BUMP PITCH:
50 µM

MINIMUM BUMP GAP:
18 µM

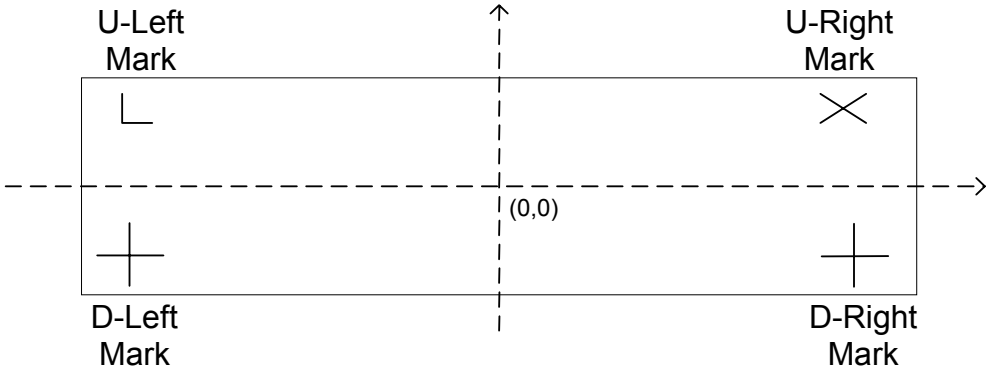
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

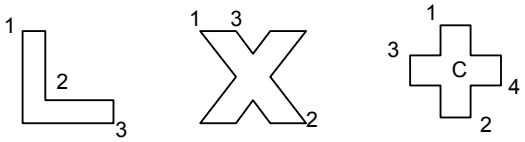
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

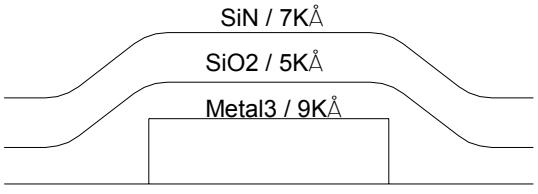
COORDINATES:

	U-Left Mark		U-Right Mark	
	X	Y	X	Y
1	-3420.6	470.6	3389.9	470.6
2	-3412.8	454.6	3423.6	446.9
3	-3397.1	446.9	3400.7	470.7

	D-Left Mark Center		D-Right Mark Center	
	X	Y	X	Y
1	-3409.6	-449.3	3407.0	-449.3
2	-3404.1	-476.8	3412.5	-476.8
3	-3420.6	-460.3	3396.0	-460.3
4	-3393.1	-465.8	3423.6	-465.8
C	-3406.8	-463.1	3409.8	-463.1

(The values of the x-coordinate and the y-coordinate in the table are after rounded.)

TOP METAL AND PASSIVATION:



FOR NON-OTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad name	X	Y	W	H
1	DUMMY	-3514.3	447.4	94	32
2	COM3	-3514.3	397.4	94	32
3	COM5	-3514.3	347.4	94	32
4	COM7	-3514.3	297.4	94	32
5	COM9	-3514.3	247.4	94	32
6	COM11	-3514.3	197.4	94	32
7	COM13	-3514.3	147.4	94	32
8	COM15	-3514.3	97.4	94	32
9	COM17	-3514.3	47.4	94	32
10	COM19	-3514.3	-2.7	94	32
11	COM21	-3514.3	-52.7	94	32
12	COM23	-3514.3	-102.7	94	32
13	COM25	-3514.3	-152.7	94	32
14	COM27	-3514.3	-202.7	94	32
15	COM29	-3514.3	-252.7	94	32
16	COM31	-3514.3	-302.7	94	32
17	COM33	-3514.3	-352.7	94	32
18	COM35	-3514.3	-402.7	94	32
19	DUMMY	-3514.3	-452.7	94	32
20	COM37	-3337.2	-423.9	32	94
21	COM39	-3287.2	-423.9	32	94
22	COM41	-3237.2	-423.9	32	94
23	COM43	-3187.2	-423.9	32	94
24	COM45	-3137.2	-423.9	32	94
25	COM47	-3087.2	-423.9	32	94
26	COM49	-3037.2	-423.9	32	94
27	COM51	-2987.2	-423.9	32	94
28	COM53	-2937.2	-423.9	32	94
29	COM55	-2887.2	-423.9	32	94
30	COM57	-2837.2	-423.9	32	94
31	COM59	-2787.2	-423.9	32	94
32	COM61	-2737.2	-423.9	32	94
33	COM63	-2687.2	-423.9	32	94
34	CIC	-2637.2	-423.9	32	94
35	CS0	-2560.6	-430.9	50	80
36	CS1	-2485.8	-430.9	50	80
37	VDDX	-2415.2	-430.9	50	80
38	RST	-2344.8	-430.9	50	80
39	CD	-2270.0	-430.9	50	80
40	WR0	-2195.2	-430.9	50	80
41	WR1	-2120.4	-430.9	50	80
42	D0	-2041.0	-430.9	50	80
43	D1	-1971.0	-430.9	50	80
44	D2	-1901.0	-430.9	50	80
45	D3	-1831.0	-430.9	50	80
46	D4	-1761.0	-430.9	50	80
47	D5	-1691.0	-430.9	50	80
48	D6	-1621.0	-430.9	50	80
49	D7	-1551.0	-430.9	50	80

#	Pad name	X	Y	W	H
50	BM0	-1471.6	-430.9	50	80
51	BM1	-1396.8	-430.9	50	80
52	VDD	-1326.2	-430.9	50	80
53	VDD	-1155.2	-430.9	50	80
54	VDD	-1085.2	-430.9	50	80
55	VDD2	-1015.2	-430.9	50	80
56	VDD2	-844.2	-430.9	50	80
57	VDD2	-774.2	-430.9	50	80
58	VDD3	-704.2	-430.9	50	80
59	VDD3	-533.2	-430.9	50	80
60	VSS	-463.2	-430.9	50	80
61	VSS	-393.2	-430.9	50	80
62	VSS	-323.2	-430.9	50	80
63	VSS	-253.2	-430.9	50	80
64	VSS2	-183.2	-430.9	50	80
65	VSS2	-113.2	-430.9	50	80
66	VSS2	-43.2	-430.9	50	80
67	VSS2	26.8	-430.9	50	80
68	TST4	97.5	-430.9	50	80
69	TST1	268.5	-430.9	50	80
70	VB1+	595.9	-430.9	50	80
71	VB1+	666.2	-430.9	50	80
72	TST2	736.2	-430.9	50	80
73	TST3	1017.3	-430.9	50	80
74	VB1-	1087.6	-430.9	50	80
75	VB1-	1157.6	-430.9	50	80
76	VB0-	1485.0	-430.9	50	80
77	VB0-	1555.2	-430.9	50	80
78	TP3	1625.2	-430.9	50	80
79	TP2	1872.4	-430.9	50	80
80	TP1	1942.6	-430.9	50	80
81	VB0+	2236.9	-430.9	50	80
82	VB0+	2307.1	-430.9	50	80
83	VLCDOUT	2377.1	-430.9	50	80
84	VLCDIN	2561.0	-430.9	50	80
85	COM64	2637.2	-423.9	32	94
86	COM62	2687.2	-423.9	32	94
87	COM60	2737.2	-423.9	32	94
88	COM58	2787.2	-423.9	32	94
89	COM56	2837.2	-423.9	32	94
90	COM54	2887.2	-423.9	32	94
91	COM52	2937.2	-423.9	32	94
92	COM50	2987.2	-423.9	32	94
93	COM48	3037.2	-423.9	32	94
94	COM46	3087.2	-423.9	32	94
95	COM44	3137.2	-423.9	32	94
96	COM42	3187.2	-423.9	32	94
97	COM40	3237.2	-423.9	32	94
98	COM38	3287.2	-423.9	32	94

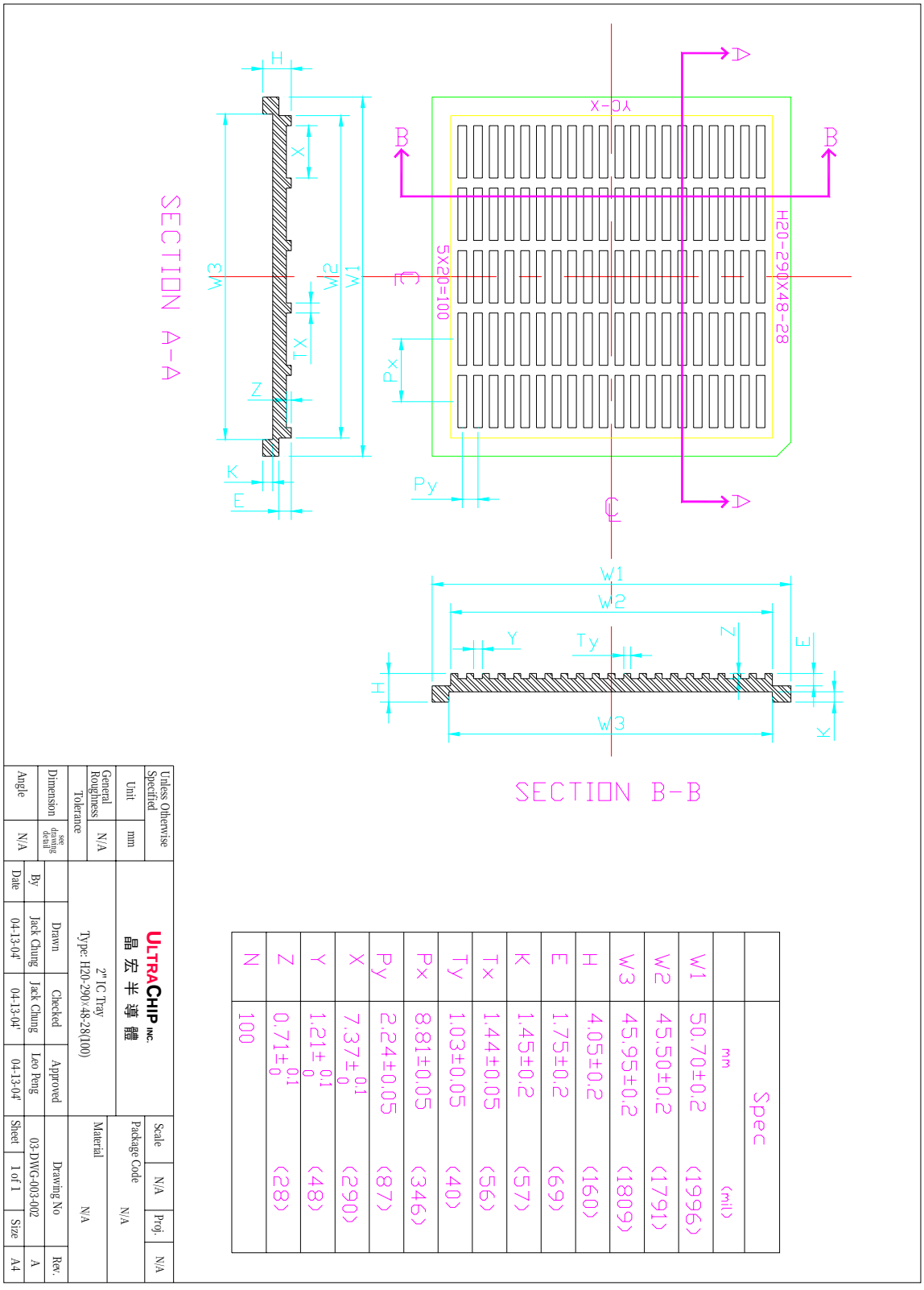
#	Pad name	X	Y	W	H
99	COM36	3337.2	-423.9	32	94
100	DUMMY	3514.3	-452.7	94	32
101	COM34	3514.3	-402.7	94	32
102	COM32	3514.3	-352.7	94	32
103	COM30	3514.3	-302.7	94	32
104	COM28	3514.3	-252.7	94	32
105	COM26	3514.3	-202.7	94	32
106	COM24	3514.3	-152.7	94	32
107	COM22	3514.3	-102.7	94	32
108	COM20	3514.3	-52.7	94	32
109	COM18	3514.3	-2.7	94	32
110	COM16	3514.3	47.4	94	32
111	COM14	3514.3	97.4	94	32
112	COM12	3514.3	147.4	94	32
113	COM10	3514.3	197.4	94	32
114	COM8	3514.3	247.4	94	32
115	COM6	3514.3	297.4	94	32
116	COM4	3514.3	347.4	94	32
117	COM2	3514.3	397.4	94	32
118	DUMMY	3514.3	447.4	94	32
119	CIC	3325.0	423.9	32	94
120	SEG1	3275.0	423.9	32	94
121	SEG2	3225.0	423.9	32	94
122	SEG3	3175.0	423.9	32	94
123	SEG4	3125.0	423.9	32	94
124	SEG5	3075.0	423.9	32	94
125	SEG6	3025.0	423.9	32	94
126	SEG7	2975.0	423.9	32	94
127	SEG8	2925.0	423.9	32	94
128	SEG9	2875.0	423.9	32	94
129	SEG10	2825.0	423.9	32	94
130	SEG11	2775.0	423.9	32	94
131	SEG12	2725.0	423.9	32	94
132	SEG13	2675.0	423.9	32	94
133	SEG14	2625.0	423.9	32	94
134	SEG15	2575.0	423.9	32	94
135	SEG16	2525.0	423.9	32	94
136	SEG17	2475.0	423.9	32	94
137	SEG18	2425.0	423.9	32	94
138	SEG19	2375.0	423.9	32	94
139	SEG20	2325.0	423.9	32	94
140	SEG21	2275.0	423.9	32	94
141	SEG22	2225.0	423.9	32	94
142	SEG23	2175.0	423.9	32	94
143	SEG24	2125.0	423.9	32	94
144	SEG25	2075.0	423.9	32	94
145	SEG26	2025.0	423.9	32	94
146	SEG27	1975.0	423.9	32	94
147	SEG28	1925.0	423.9	32	94
148	SEG29	1875.0	423.9	32	94
149	SEG30	1825.0	423.9	32	94

#	Pad name	X	Y	W	H
150	SEG31	1775.0	423.9	32	94
151	SEG32	1725.0	423.9	32	94
152	SEG33	1675.0	423.9	32	94
153	SEG34	1625.0	423.9	32	94
154	SEG35	1575.0	423.9	32	94
155	SEG36	1525.0	423.9	32	94
156	SEG37	1475.0	423.9	32	94
157	SEG38	1425.0	423.9	32	94
158	SEG39	1375.0	423.9	32	94
159	SEG40	1325.0	423.9	32	94
160	SEG41	1275.0	423.9	32	94
161	SEG42	1225.0	423.9	32	94
162	SEG43	1175.0	423.9	32	94
163	SEG44	1125.0	423.9	32	94
164	SEG45	1075.0	423.9	32	94
165	SEG46	1025.0	423.9	32	94
166	SEG47	975.0	423.9	32	94
167	SEG48	925.0	423.9	32	94
168	SEG49	875.0	423.9	32	94
169	SEG50	825.0	423.9	32	94
170	SEG51	775.0	423.9	32	94
171	SEG52	725.0	423.9	32	94
172	SEG53	675.0	423.9	32	94
173	SEG54	625.0	423.9	32	94
174	SEG55	575.0	423.9	32	94
175	SEG56	525.0	423.9	32	94
176	SEG57	475.0	423.9	32	94
177	SEG58	425.0	423.9	32	94
178	SEG59	375.0	423.9	32	94
179	SEG60	325.0	423.9	32	94
180	SEG61	275.0	423.9	32	94
181	SEG62	225.0	423.9	32	94
182	SEG63	175.0	423.9	32	94
183	SEG64	125.0	423.9	32	94
184	SEG65	75.0	423.9	32	94
185	SEG66	25.0	423.9	32	94
186	SEG67	-25.0	423.9	32	94
187	SEG68	-75.0	423.9	32	94
188	SEG69	-125.0	423.9	32	94
189	SEG70	-175.0	423.9	32	94
190	SEG71	-225.0	423.9	32	94
191	SEG72	-275.0	423.9	32	94
192	SEG73	-325.0	423.9	32	94
193	SEG74	-375.0	423.9	32	94
194	SEG75	-425.0	423.9	32	94
195	SEG76	-475.0	423.9	32	94
196	SEG77	-525.0	423.9	32	94
197	SEG78	-575.0	423.9	32	94
198	SEG79	-625.0	423.9	32	94
199	SEG80	-675.0	423.9	32	94
200	SEG81	-725.0	423.9	32	94

#	Pad name	X	Y	W	H
201	SEG82	-775.0	423.9	32	94
202	SEG83	-825.0	423.9	32	94
203	SEG84	-875.0	423.9	32	94
204	SEG85	-925.0	423.9	32	94
205	SEG86	-975.0	423.9	32	94
206	SEG87	-1025.0	423.9	32	94
207	SEG88	-1075.0	423.9	32	94
208	SEG89	-1125.0	423.9	32	94
209	SEG90	-1175.0	423.9	32	94
210	SEG91	-1225.0	423.9	32	94
211	SEG92	-1275.0	423.9	32	94
212	SEG93	-1325.0	423.9	32	94
213	SEG94	-1375.0	423.9	32	94
214	SEG95	-1425.0	423.9	32	94
215	SEG96	-1475.0	423.9	32	94
216	SEG97	-1525.0	423.9	32	94
217	SEG98	-1575.0	423.9	32	94
218	SEG99	-1625.0	423.9	32	94
219	SEG100	-1675.0	423.9	32	94
220	SEG101	-1725.0	423.9	32	94
221	SEG102	-1775.0	423.9	32	94
222	SEG103	-1825.0	423.9	32	94
223	SEG104	-1875.0	423.9	32	94
224	SEG105	-1925.0	423.9	32	94
225	SEG106	-1975.0	423.9	32	94
226	SEG107	-2025.0	423.9	32	94
227	SEG108	-2075.0	423.9	32	94
228	SEG109	-2125.0	423.9	32	94
229	SEG110	-2175.0	423.9	32	94
230	SEG111	-2225.0	423.9	32	94
231	SEG112	-2275.0	423.9	32	94
232	SEG113	-2325.0	423.9	32	94
233	SEG114	-2375.0	423.9	32	94
234	SEG115	-2425.0	423.9	32	94
235	SEG116	-2475.0	423.9	32	94
236	SEG117	-2525.0	423.9	32	94
237	SEG118	-2575.0	423.9	32	94
238	SEG119	-2625.0	423.9	32	94
239	SEG120	-2675.0	423.9	32	94
240	SEG121	-2725.0	423.9	32	94
241	SEG122	-2775.0	423.9	32	94
242	SEG123	-2825.0	423.9	32	94
243	SEG124	-2875.0	423.9	32	94
244	SEG125	-2925.0	423.9	32	94
245	SEG126	-2975.0	423.9	32	94
246	SEG127	-3025.0	423.9	32	94
247	SEG128	-3075.0	423.9	32	94
248	SEG129	-3125.0	423.9	32	94
249	SEG130	-3175.0	423.9	32	94
250	SEG131	-3225.0	423.9	32	94
251	SEG132	-3275.0	423.9	32	94
252	COM1	-3325.0	423.9	32	94

(The values of the x-coordinate and the y-coordinate in the table are after rounded.)

TRAY INFORMATION



	Spec
	mm (mil)
W1	50.70±0.2 (1996)
W2	45.50±0.2 (1791)
W3	45.95±0.2 (1809)
H	4.05±0.2 (160)
E	1.75±0.2 (69)
K	1.45±0.2 (57)
Tx	1.44±0.05 (56)
Ty	1.03±0.05 (40)
Px	8.81±0.05 (346)
Py	2.24±0.05 (87)
X	$7.37^{+0.1}_{0}$ (290)
Y	$1.21^{+0.1}_{0}$ (48)
Z	$0.71^{+0.1}_{0}$ (28)
N	100

Unless Otherwise Specified		ULTRACHIP INC. 晶宏半導體				Scale	N/A	Proj.	N/A
Unit	mm					Package Code	N/A		
General Roughness	N/A	2" IC Tray Type: H20-290×48-28(100)				Material	N/A		
Tolerance						Drawing No	03-DWG-003-002	Rev.	A
Dimension	see drawing detail		By	Date		Sheet	1 of 1	Size	A4
Angle	N/A								
			Drawn	Jack Chung	04-13-04'				
			Checked	Jack Chung	04-13-04'				
			Approved	Leo Peng	04-13-04'				

REVISION HISTORY

Revision	Contents	Date of Rev.
Origin	UC1601(C) v0.2	Aug. 10, 2004
0.6	First Release	Aug. 12, 2004
0.61	(1) V_{DD} (Digital) range is adjusted: 1.8V ~ 3.3V → 2.4V~3.3V (Section "Feature Highlights", page 1; Section "Specifications" – DC Characteristics, page 32: Section "AC Characteristics", Pp 33~38)	Aug. 13, 2004
	(2) The table is updated. (Section "ESD Consideration", page 30)	
0.8	(1) Part Number is corrected: UC1601xGBD → UC1601xGAD (Section "Ordering Information", page 2)	Sep. 1, 2004
	(2) The V_{LCD} formula is updated. (Section "V_{LCD} Quick Reference", page 16)	
	(3) The Reference Circuit drawings are recovered. (Section "Host Interface Reference Circuit, Pp 22 ~23)	
	(4) The Condition for average frame rate, f_{FR}, is corrected: LC[3] = 1b → 0b (Section "Specifications" – DC Characteristics, page 32)	
	(5) Some AC timings are adjusted. (Section "AC Characteristics", Pp 33~38)	
0.9	(1) A COG section is added. (Section "Recommended COG Layout", page 7)	Sep. 23, 2004
	(2) Figure 12, Delay allowance and Power Off-On Sequence, is updated to indicate the change of V_{DD} minimum (1.8V → 2.4V). (Section "Reset and Power Management", page 28)	
1.0	(1) For LC[3] setting, 2-bit presentation is corrected as 1-bit: "00" → "0" "01" → "1". (Section "Command Description" – (14) Set Frame Rate, page 13; "Specification" – Power Consumption, page 32)	Nov. 4, 2004
	(2) The recommended value for C_L is corrected: 12V → 25V (Section "Hi-V Generator and Bias Reference Circuit", page 18)	
	(3) In the "Operating Mode" table, the status of "Draining Circuit" in Sleep mode is corrected: "OFF" → "ON" (4) Most contents of subsection "Changing Operation Mode" are re-written. (Section "Reset & Power Management", page 27)	
	(5) Subsection "Extended Display OFF" is removed. (6) Subsection "Brief Display OFF" is renamed as "Display OFF". (Section "Reset & Power Management", page 29)	
	(7) Average Frame Rate, F_{FR}, is adjusted: Min. : 70 → 66 Max. : 85 → "–" (dash) (Section "Specifications" – DC Characteristics, page 32)	
	(8) The Tray drawing is updated. (Section "Tray Information", page 44)	
1.1	(1) PC[0]: 00 and 01 are corrected: 00 and 01 → 0 and 1 (Section "Control Register" – the PC entry, page 8; "Command Description" – (7) Set Panel Loading, page 12)	Nov. 4, 2005

Revision	Contents	Date of Rev.
1.1	(2) "BZ" related contents are removed: "System Status bits RS and BZ…" → "System Status bit RS…" (Section "Reset and Power Management" – Reset Status, page 27)	Nov. 4, 2005
	(3) The note paragraph under the Display OFF table is removed. (Section "Reset and Power Management" – Sample Command Sequence for Power Management, page 29)	
	(4) Point 2 is removed. (Section "ESD Consideration", page 30)	
	(5) More experiment conditions are listed. (Section "Specifications" – Power Consumption, page 32)	
	(6) In Figure 13, WR0 is added. In Figure 14, WR0 is corrected as WR1. (Section "AC Characteristics", pages 33, 35)	
	(7) The data are updated. (Section "Physical Dimension", page 39)	
1.2	(1) V_{DD} range (Typical) : 2.4V~3.3V --> 2.5V~3.3V $V_{DD2/3}$ range (Typical) : 2.4V~3.3V --> 2.5V~3.3V V_{DD} (Max.) : 3.3V --> 3.6V $V_{DD2/3}$ (Max.) : 3.3V --> 3.6V (Section "Feature Highlight", page 1; "DC Characteristics", page 34; "AC Characteristics", Pp 35~40)	Apr. 8, 2008
	(2) The description of sub-section Power-Down Sequence is updated. (Section "Reset & Power Management", page 30)	