No RailCom

dccPreambleStartBit

dccPreamble

dccStartBitPacket

dccData

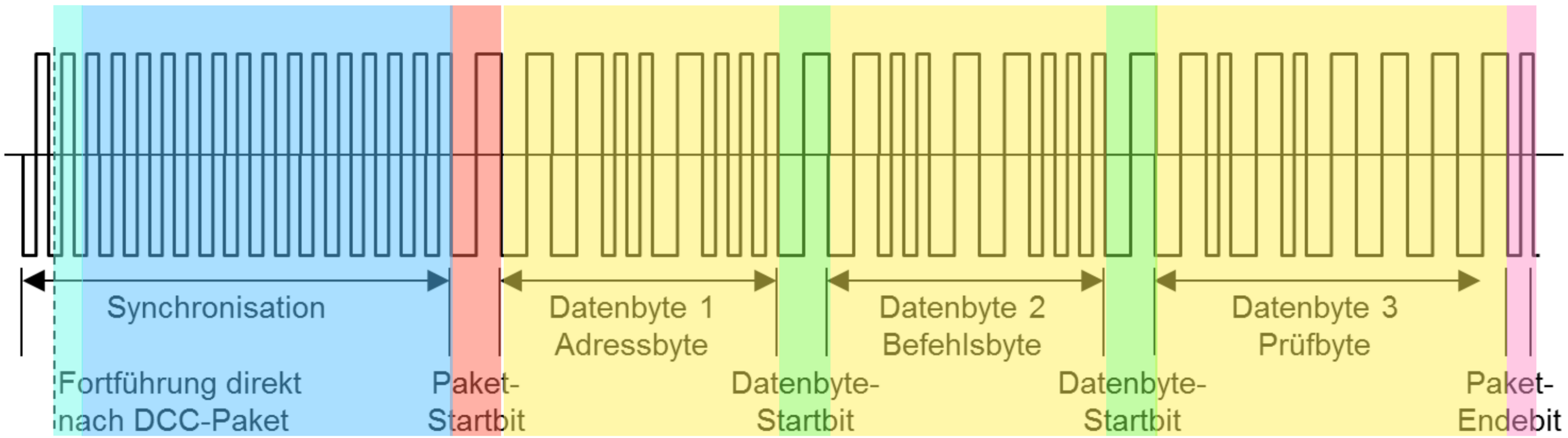
dccStartBitData

dccData

dccStartBitData

dccData

dccEndBit



RailCom

dccEndBit

dccRailComStartBit

dccRailComGap

dccPreambleStartBit

dccPreamble

dccStartBitPacket

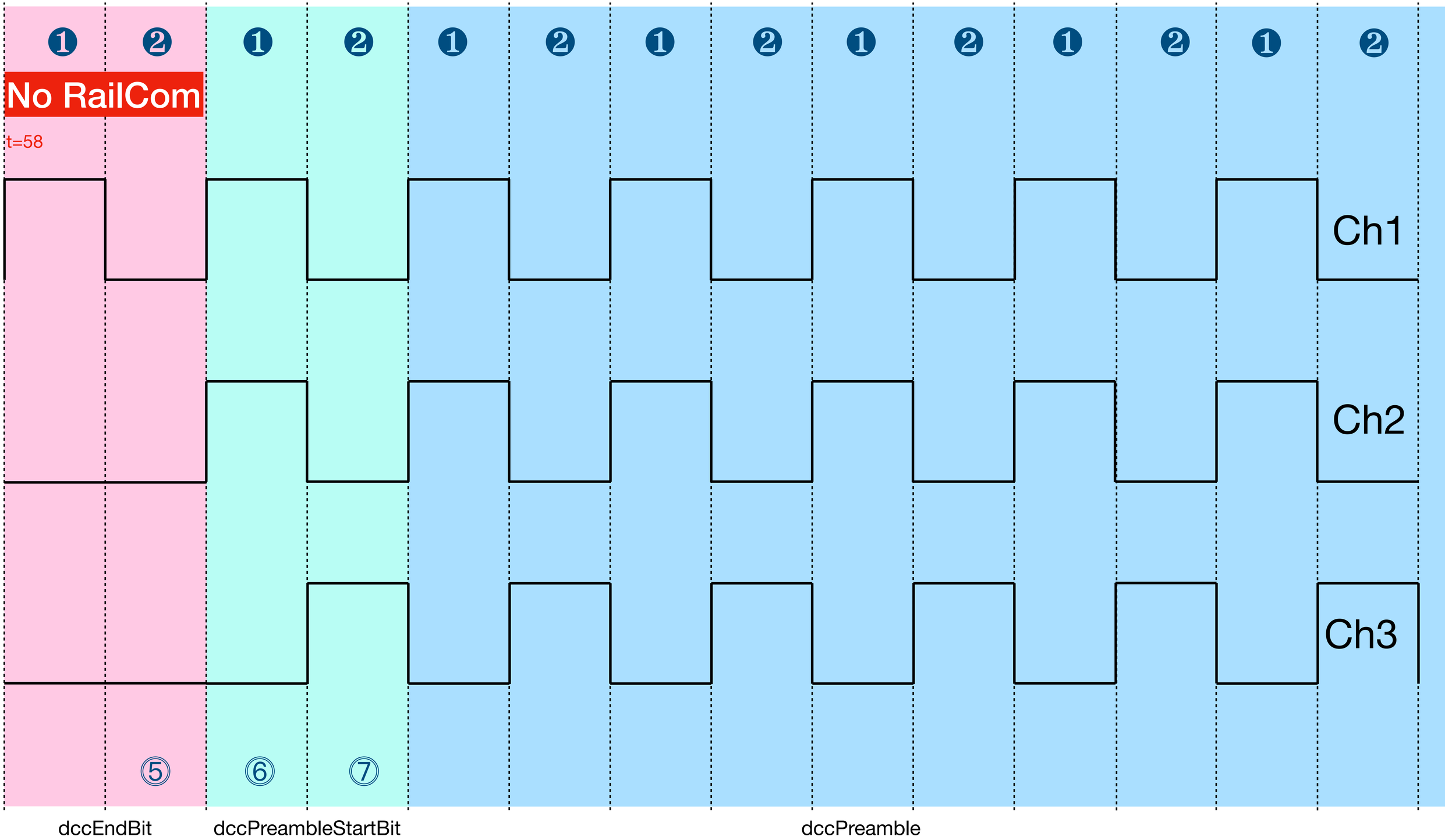
1 0

❶ ❷ ❶ ❷ ❶ ❷ ❶ ❷ ❶ ❷ ❶ ❷ ❶ ❷ ❶ ❷ ❶ ❷ ❶ ❷

Ch1

Ch2

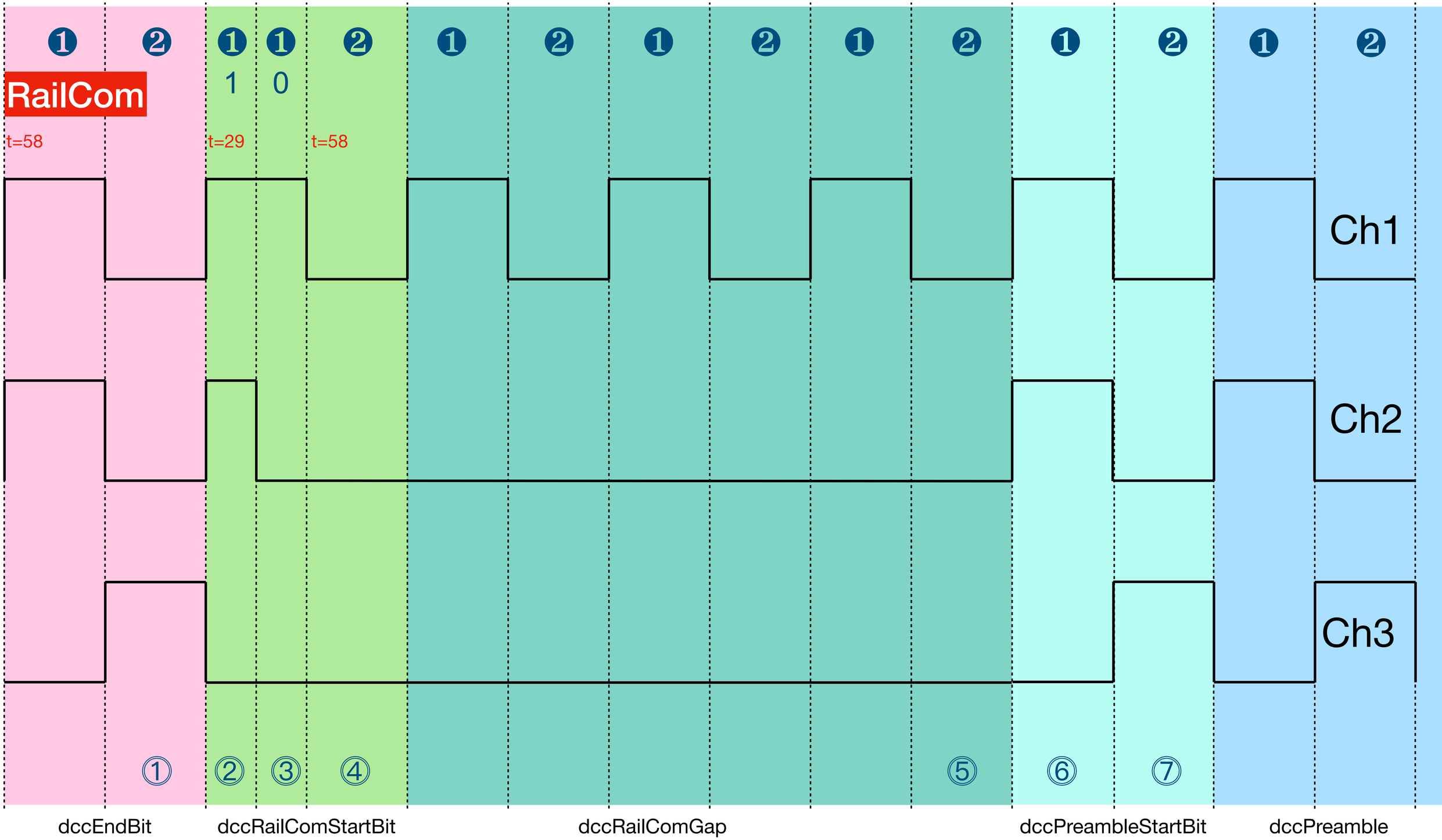
Ch3



⑤ => dccPreambleStartBit / Enable toggle CH2

⑥ Enable toggle CH3

⑦ => dccPreamble



① => dccRailComStartBit

② t = 29 / Disable toggle CH1 & CH3

③ Enable toggle CH1 / Disable toggle CH2

④ => dccRailComGap / t = 58

⑤ => dccPreambleStartBit / Enable toggle CH2

⑥ Enable toggle CH3

⑦ => dccPreamble

MEGA 2560

```
  *d1reg ^= d1bit; // Toggle
  if (CH1_toggle) {*d1reg ^= d1bit;} // Toggle, if allowed

  Current Z21PG Pins: 6 (DCC), 11 (DCC S88/LocoNet), 39 (NDCC)


  TIMER4 Pins: 6 (OC4A, PH3),  7 (OC4B, PH4),  8 (OC4C, PH5)

  TIMER3 Pins: 5 (OC3A, PE3),  2 (OC3B, PE4),  3 (OC3C, PE5)
  TIMER5 Pins: 44 (OC5A, PL3),  45 (OC5B, PL4),  46 (OC5C, PL5)
```

TCCRnA |= (1<<COMnx0); // enable toggle
TCCRnA &= ~(1<<COMnx0); // disable toggle

TCCR4A |= (1<<COM4A0); // enable toggle CHA
TCCR4A &= ~(1<<COM4A0); // disable toggle CHA
TCCR4A |= (1<<COM4B0); // enable toggle CHB
TCCR4A &= ~(1<<COM4B0); // disable toggle CHB
TCCR4A |= (1<<COM4C0); // enable toggle CHC
TCCR4A &= ~(1<<COM4C0); // disable toggle CHC

DxCore: Single Compare Match (Split Mode / Single Slope CTC)” → CNT reset automatisch bij compare match