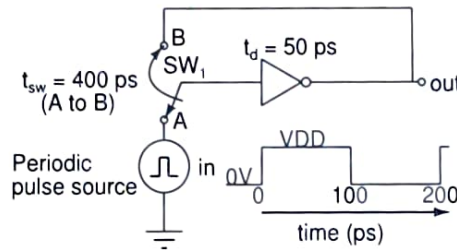


**VLSI Design (EC2.201) : Mid-Semester Exam**  
 Monsoon 2024, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava)  
 Date : 23<sup>rd</sup> Sep, 2024, Duration : 1 hr 30 min, Max. Marks : 20

**Instructions:**

- Clearly write your assumptions (if any)
- Delay unit ( $\tau$ ) has the conventional meaning as discussed in lectures
- Students are allowed to use 2 A-4 sheets of own handwritten notes
- Use of calculator is allowed

1. (a) As shown in Fig. 1, switch  $SW_1$  is moved from A to B at time  $t_{sw} = 400$  ps. Input to output delay of the inverter ( $t_d$ ) is 50 ps. Plot  $in$  and  $out$  for  $t = 0$  to  $t = 600$  ps. Plot the  $out$  signal. [2]



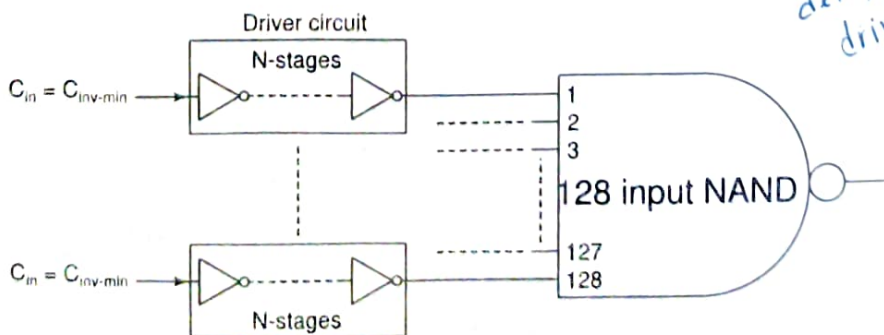
**Figure 1**

- (b) Using static CMOS logic style, design a logic gate to implement the following function

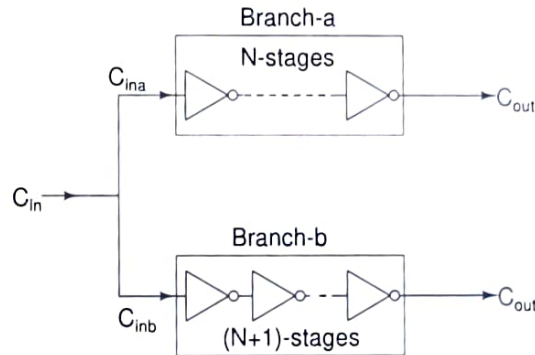
$$Y = \overline{AB + CD}$$

Considering  $\frac{\mu_n}{\mu_p} = m$ , size the gate to equalize its delay to that of a minimum size inverter (NMOS width is  $W$ ) in the same technology node. [2]

2. Suppose you are asked to design an inverter chain with total path effort  $H = 1000$ . Find the values of the delay obtained by using inverters with stage effort 3, 4 and 5 respectively, in terms of delay unit ( $\tau$ ). Consider the parasitic delay of inverter is 1 delay unit. [4]
3. As shown in the Fig. 2, consider a 128 input NAND gate, which has been implemented using static CMOS logic, where all pull-up devices are connected in parallel and all pull-down devices are connected in series to draw equivalent current as a minimum size inverter ( $W_n = W, W_p = 2W, L_n = L_p = L$ ). Each input of the NAND gate requires a driver circuit realized by a chain of inverters, which must have an input capacitance equivalent to the minimum sized inverter. Considering a stage effort ( $f_i = \frac{C_{out_i}}{C_{in_i}}$ ) of 3.59 for each inverter ( $I_i$ ) in the chain, design the driver circuit such that its delay is minimum. Compute the delay of your circuit in terms of delay units ( $\tau$ ). It is given that the parasitic delay of inverter is 1 delay unit. [6]



4. Consider the fork circuit shown in Fig. 3, where branch-a has  $N$  inverters and branch-b has  $(N+1)$  inverters. Fork circuit is designed so as to minimize and equalize the delay on each branch (a and b). In the figure,  $H_a = \frac{C_{out}}{C_{ina}}$ ,  $H_b = \frac{C_{out}}{C_{inb}}$  and  $C_{in} = C_{ina} + C_{inb}$ .



**Figure 3**

- (a) Consider  $H = \frac{C_{out}}{C_{in}} = \frac{20}{3}$  and  $\rho_{inv} = 0$  delay unit. Find the capacitance ratio ( $\frac{C_{ina}}{C_{inb}}$ ) and delay in  $\tau$  units for  $N=1$  such that delay of the two branches are equalized. [4]
- (b) Consider  $H_a = \frac{500}{33}$  and  $H_b = \frac{500}{42}$  and  $\rho_{inv} = 1$  delay unit. Compare the delays of branch-a and branch-b for the fork structures with  $N=1, 2$  &  $3$ . Which fork structure (1-2, 2-3 or 3-4) gives minimum delay. [2]

*Good luck !!*