

Analog Electronic Circuits (EC2.103) : Endsem exam
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 Date : 1st May, 2024, Duration : 3 Hours, Max. Marks : 30

Instructions:

- Clearly write your assumptions (if any)
- You can use own handwritten short notes (maximum 2 A-4 sheets both sides) in the exam hall
- Use of mobile phone and computers are not allowed during this exam

1. Consider M_1 is biased in saturation for the amplifier circuit shown in Figure 1 and channel length modulation effect is also present. Assume coupling capacitance (C_{C1}, C_{C2}) have negligible impedances at the frequency of interest.

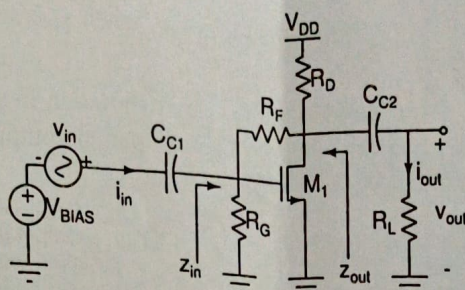


Figure 1

- Draw small signal model of the amplifier and derive voltage gain $\frac{v_{out}}{v_{in}}$. [2 Mark]
- Derive the expression for Z_{in} . [2 Mark]
- Derive the expression for the current gain $A_i = \frac{i_{out}}{i_{in}}$. [2 Mark]

2. For the circuit shown in fig. 2,

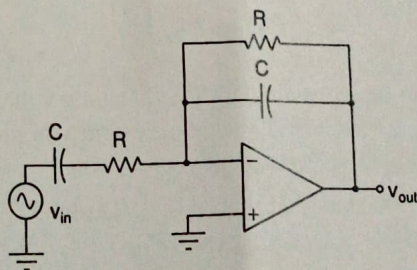


Figure 2

- Derive the voltage gain transfer function $A_v(s) = \frac{v_{out}(s)}{v_{in}(s)}$. Find the poles and zeros. [2 Mark]
- Sketch the Bode magnitude plot for $A_v(s)$. Clearly mention slopes, pole and zero values on the plot. [2 Mark]
- What is the frequency range for which the circuit acts like a differentiator. Explain briefly. What will be the effect of the high frequency noise on the circuit, discuss briefly. [2 Mark]

3. Answer the following:

- Consider the circuits shown in figure 3. It is given that the cut-in voltage of the diode is 0.7 V, thermal voltage $V_T = 25$ mV, $V_{IN} = 10$ V, $v_{in} = \sin(\omega_0 t)$ V and $R = 10$ k Ω . As shown in the figure, find v_{OUT} . [2 Mark]

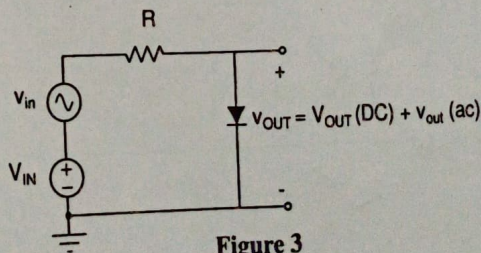


Figure 3

- (b) As shown in Fig. 4(a), derive the overall transconductance (G_m) of the combination of N devices. It is given that the transconductance of a Q_i transistor is g_{mi} , where $i = 1$ to N . [2 Mark]

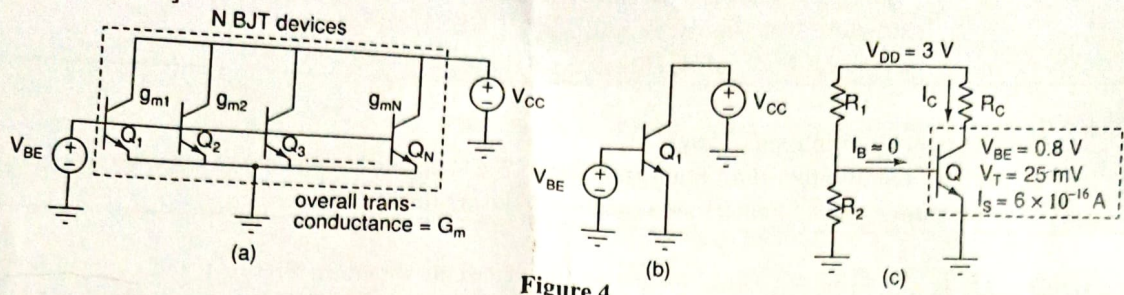


Figure 4

- (c) For the circuit shown in Fig. 4(c), find the % change in I_C if V_{BE} decreases by 1%. [2 Mark]
4. (a) For the circuit shown in Fig. 5(a), plot v_{out} vs v_{in} , when v_{in} ranges from negative to positive values. [3 Mark]
- (b) Draw voltage transfer characteristics of the circuit shown in Fig. 5(b) by sweeping v_{in} from $-V_{DD}$ to $+V_{DD}$. Clearly mark the voltage levels (input and output) and directions on the plot. It is given that $R_1 = 2R_2$ and $V_B = \frac{3V_{DD}}{4}$. [3 Mark]

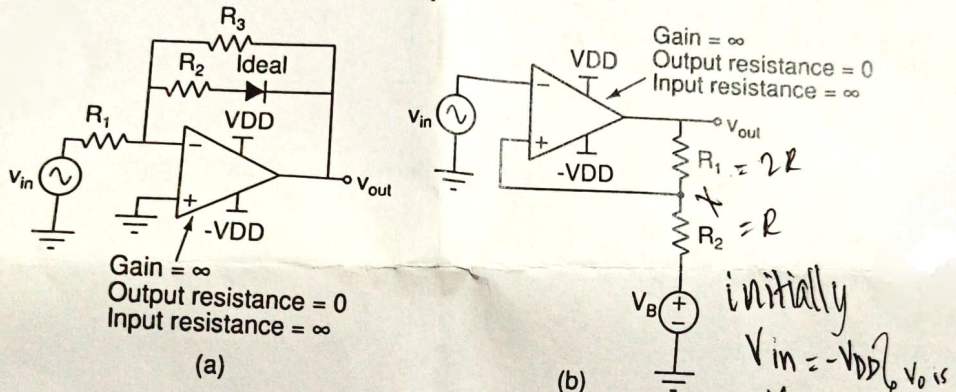


Figure 5

5. (a) Briefly discuss the method for extracting NMOS threshold voltage (V_T) parameter from SPICE simulations. Which mode of MOSFET operation would you prefer and why? Give necessary circuit setup, equations and graphs to support your answer. [2 Mark]
- (b) For Fig. 6, derive $A_v = \frac{v_{out}}{v_{in}}$ (you can ignore C_C). Design (I_D , W/L and resistor values) for $A_v = 5$, $R_S = 0\Omega$, $R_3 = 500\Omega$, total DC power (P_{DC}) ≤ 2 mW, $V_{DD} = 1.8$ V, $V_{GS} = 0.8$ V, $V_{R3} = 0.55$ V, $\mu_n C_{ox} = 100 \mu A/V^2$, $V_{TH} = 0.5$ V and $\lambda = 0$. [4 Mark]

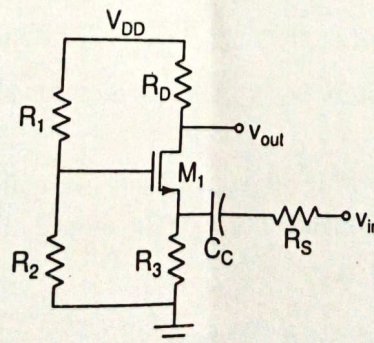


Figure 6

Good luck !!

at $-V_{DD}$
 $\left(\frac{V_{DD}}{2} - V_{in} \right) A \rightarrow v_{out}$