VLSI Design (EC2.201) : End-semester exam

Monsoon 2024, CVEST, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava)

Date : 23rd November, 2024, Duration : 3 Hours, Max. Marks : 30

Instructions:

- Read paper carefully and clearly write your assumptions (if any)
- Use commonly represented transistor parameter notations wherever required
- You are allowed to use 2 A-4 sheets of own hand written notes (no photocopy or printed material)
- Calculators are allowed

1. (a) Draw the VTC for the bi-stable latch comprising back-to-back connected two inverters. Clearly label metastable and stable points on the graph. With the help of VTC, explain what should be ensured to correctly read the stored information and write any desired information at the latch nodes. [2]

   (b) Consider the circuit shown in Fig. 1. It is given that at $t = 0$, $v_1 = v+x$, $v_2 = v-x$ and all transistors are in saturation. Derive the expression for the rate of change of the difference voltage (x) with respect to time. From the obtained expression, comment on the functionality of the circuit. [4]

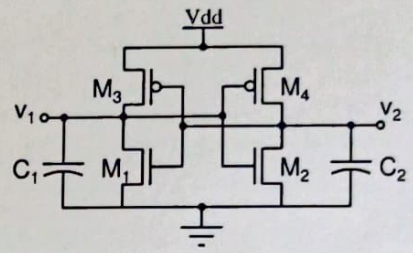


Figure 1

2. (a) Consider the circuit shown in Fig. 2. Given that $V_{DDH} = 3.3V$, $V_{DDL} = 1.8V$, voltage level at *Input* ranges from 0 V to 1.8 V. Identify the static voltage levels at points P, A and B for $Input = 0\ V$ and $Input = 1.8V$. What do you think is the function of this circuit? [3]

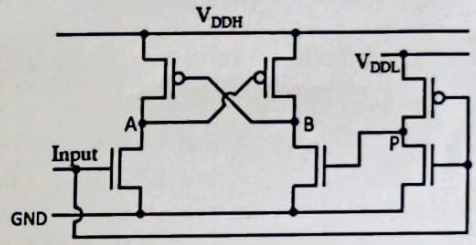
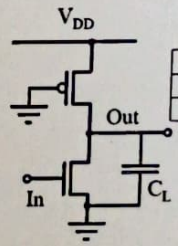


Figure 2

   (b) Consider the circuit shown in Fig. 3. Given that $V_{DD} = 3.3V$ and $C_L = 100$ fF. Find the ratio of (W/L) values for the NMOS and PMOS such that the static output voltage is equal to 0.3V when the input voltage is 3V. [3]



Parameter	N Channel	P Channel
μC_{ox}	$45\mu A/V^2$	$22\mu A/V^2$
V_T	0.6 V	-0.6 V

Figure 3

3. For 1-bit full adder, the carry and sum bits can be defined as $C_{out} = A.B + Cin.(A + B)$ and $s = \overline{C_{out}}.(A + B + C_{in}) + A.B.C_{in}$, respectively. Prove that $Y = \overline{C_{out}} = \overline{A}.\overline{B} + \overline{C_{in}}.(\overline{A} + \overline{B})$. Give a static CMOS implementation of $Y = f\{A, B, C_{in}\}$. Also give static CMOS implementation of $C_{out} = f\{\overline{A}, \overline{B}, \overline{C_{in}}\}$, considering complement of the variables are also available. What is your observation from above two circuits? Discuss briefly. [3]

4. The output carry in a Carry-Look-Ahead (CLA) adder can be quickly generated by pre-computing propagate (p_i) and generate (g_i) signals for each bit position (i), which are defined as $p_i = a_i \oplus b_i$ and $g_i = a_i.b_i$, respectively, where a_i and b_i are the input bits. The carry out ($c_{(i+1)}$) of the i^{th} bit position can be written as $c_{(i+1)} = (p_i.c_i) + g_i$ and thus, $c_{(i+1)}$ can be expressed entirely in terms of the p_i, g_i and c_0, and sum can be represented as $sum_i = p_i \oplus c_{i-1}$.

(a) Since $c_{(i+1)} = (p_i.c_i) + g_i$, show that $p_i = a_i + b_i$ can be used instead of $p_i = a_i \oplus b_i$ (it will help to simplify the hardware implementation). Also give static implementation of $\overline{c_{(i+1)}} = f(a_i, b_i, c_i)$. [2]

(b) Since, $c_{(i+1)} = g_i + (p_i.c_i) = g_i + (p_i.g_{i-1} + p_i.p_{i-1}c_{i-1}) = ...$, the static implementation for the computation of carry term as a logic expression depending on all a_i, b_i and c_0 will incur significant delay and therefore it is rarely used. A faster way could be to use dynamic implementation. Consider the circuit shown in Fig.4. Find $\overline{c_{(i+1)}}$ for pre-charge phase ($clk = 0$) and evaluate phase ($clk = 1$). Can the circuit be used to implement the required logic ($c_{(i+1)} = (p_i.c_i) + g_i$) to pre-compute carry in CLA. Discuss briefly. [3]

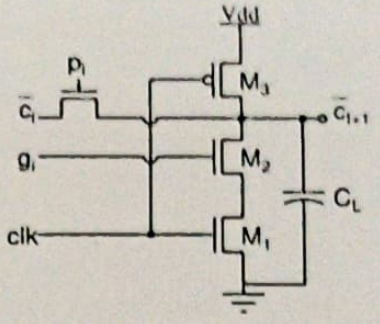


Figure 4

5. (a) Briefly explain setup and hold time for the clocked CMOS latch shown in Fig. 5. How can setup and hold time violations be fixed post fabrication? [2]

(b) Consider the scenario shown in Fig. 6. Find the maximum delay (t_{pdmax}) and minimum delay (t_{pdmin}) of the combinational logic such that setup and hold time violations are avoided for the circuit. It is given that clock to propagation delay (t_{pcq}), setup time (t_{su}) and hold time (t_h) for D flip-flops are 5 ns, 4 ns and 2 ns, respectively. Clock period (T_{clk}) is 10 ns and the buffer delay (t_{skew}) is 5 ns. Clearly draw timing diagram and show your calculations. [4]

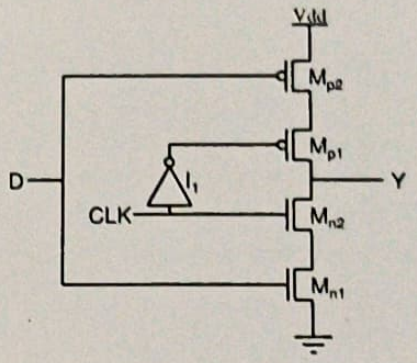


Figure 5

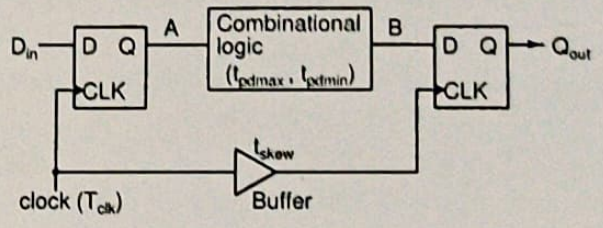


Figure 6

6. (a) Find the delay of a fanout-of-4 (FO4) inverter, where the inverter drives four identical inverters. You can consider the parasitic delay of inverter (ρ_{inv}) = 1 delay unit. [1]

(b) Find the logical effort of a four input NOR gate implemented in static CMOS logic style. Show the method to calculate it. What will be the parasitic delay (ρ_{NOR-4}) of this 4 input NOR gate in terms of ρ_{inv} (Hint: parasitic delay $\propto$ effective width seen at output). If this four-input NOR gate drives single inputs of 8 identical NOR gates simultaneously. Find the delay in the driving NOR gate in terms of delay units. [3]

Good luck !!