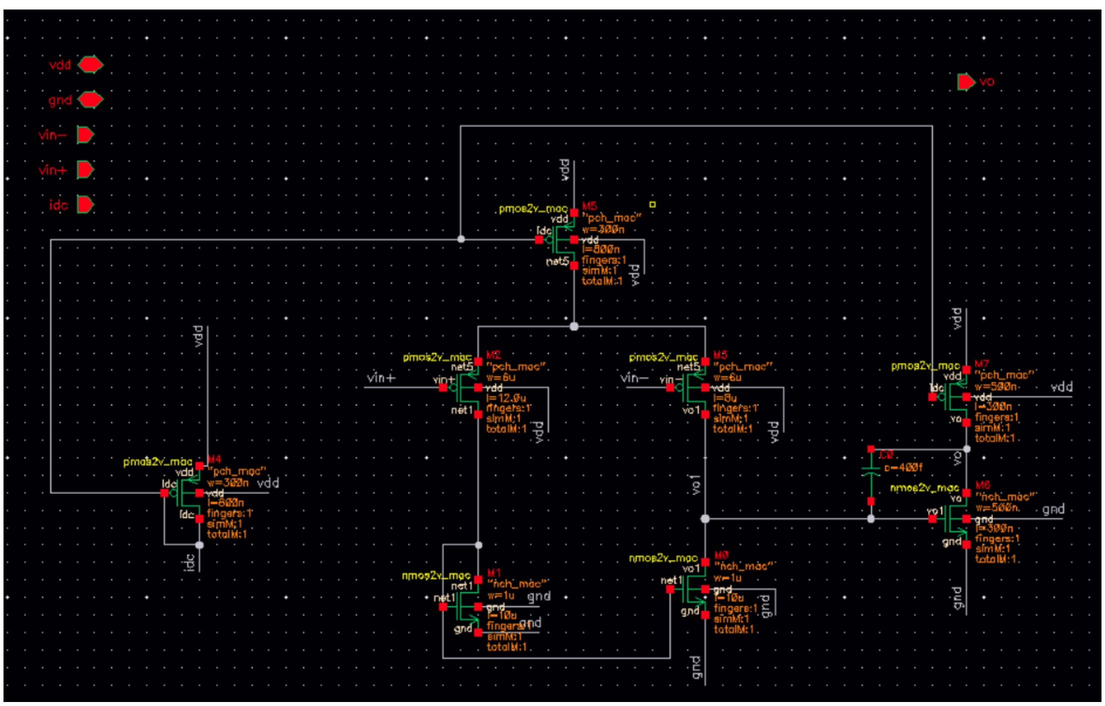
# 2-Stage Miller Compensated opamp

## Specifications :

- Input common-mode voltage : 250mV
- Minimum supply voltage : 1.6V
- Temperature Range : -40oC to 125oC
- Open loop-gain : > 75dB
- Load capacitance : 1pF
- Unity gain frequency : > 1MHz
- Power consumption : < 10uW
- Phase margin : atleast 60 deg (considering worst cases)

## Schematic:




## Components:

### I. Current Mirror:

A current mirror is used to maintain stability across PVT variations. It ensures the set reference current flows through the transistors. It eliminates the need for multiple current sources.

### II. Differential Amplifier:

1. PMOS differential input pair:

Since input common mode voltage is small(around 250mV), PMOS is preferred since it doesn't need that high a voltage to turn ON.

2. NMOS active load pair:

NMOS allows the same current with a smaller overdrive voltage leaving more room for output swing.

### III. CS Amplifier:

Vout from differential amplifier is reasonably high so we feed it into the gate of an NMOS transistor for further amplification. NMOS transistors also have a higher gm in general so we can get achieve a higher gain.

### IV. Miller compensation

Adding a miller capacitor introduces a dominant pole in the frequency response ensuring sufficient phase margin(reducing phase shift at unity gain frequency).

## Design Procedure :

### Power: < 10uW

max vdd=1.98(considering 10% variation)

⇒ total current < 5.05uA

total current = current through differential amp + current through cs amp + I_ref

I_ref = 700n

current through differential amp = 700n(divided both ways)

current through cs amp = 2.8u (trying to let max possible current for high gm2)

### Unity gain bandwidth: > 1MHz

$$w_u = \frac{gm_1}{Cc} >> 10^6$$

$$gm_1 >> 400 \cdot 10^{-15} \cdot 10^6$$

$$gm_1 = 400 \cdot 10^{-15} \cdot 10^6 \cdot 10 = 4u$$

**Phase margin: atleast 60 degrees**

$$180 - \tan^{-1}\left(gm_1 r_1 r_2 gm_2\right) - \tan^{-1}\left(\frac{gm_1}{gm_2} \cdot \frac{1pF}{Cc}\right) - \tan^{-1}\left(\frac{gm_1}{gm_2}\right)$$

$$90 - \tan^{-1}\left(\frac{gm_1}{gm_2} \cdot \frac{1pF}{Cc}\right) - \tan^{-1}\left(\frac{gm_1}{gm_2}\right)$$

$$\tan^{-1}\left(\frac{gm_1}{gm_2} \cdot \frac{1pF}{Cc}\right) + \tan^{-1}\left(\frac{gm_1}{gm_2}\right) < 30$$

$$\tan^{-1}\left(\frac{gm_1}{gm_2} \cdot \frac{1pF}{Cc}\right) << 30$$

$$\frac{4 \cdot 10^{-6}}{\tan(30)} \cdot \frac{10^{-12}}{800 \cdot 10^{-15}} << gm_2$$

$$gm_2 >> 8.6u$$

**Gain : >75dB (open loop)**

A=gm1*gm2*r1*r2

r1=ro3 || ro0

r2= ro7 || ro6

| | |
|---|---|
| gm1 | 4.179u |
| ron1 | 180.3M |
| rop1 | 124.2M |
| gm2 | 34.59u |
| ro1 | 657.6K |
| ro2 | 3.799M |
| r1 | 73.54M |
| r2 | 560.6K |
| gain | 5.959K |
| gain_db | 75.5 |

by fixing the ratio (w/L), the value of ro can be increased by increasing magnitude of w and L thereby effectively increasing gain

### Sizing :

1. M4, M5 have the same size(current mirror)

$$\left(\frac{w}{L}\right) = \frac{I_D}{UnCox \cdot \left(V_{GS} - V_{TH}\right)^2} = \frac{700n}{\left(177 \cdot 10^{-6}\right) \cdot (0.1)^2}$$

(w/L)=0.39

Vov is set to 100mV to account for PVT variations and square law is used to approximate values

2. M7 needs to provide a current that is 4 times higher(CS Amp) so (w/L is 0.39*4=1.56)

had to use a slightly higher value(1.66) to meet the current requirements

3. PMOS differential pair(set gm so that ugb>1MHz)

$$gm_1 = 400 \cdot 10^{-15} \cdot 10^6 \cdot 10 = 4u$$

$$gm = 2 \cdot \frac{I_D}{(Vov)}$$

$$Vov = \left(\frac{\left(4 \cdot 10^{-6}\right)}{2 \cdot 350 \cdot 10^{-9}}\right)^{-1} = 175m$$

$$\left(\frac{w}{L}\right) = \frac{gm}{UnCox(Vov)} = \frac{\left(4 \cdot 10^{(-6)}\right)}{\left(177 \cdot 10^{-6}\right) \cdot (0.175)} = 0.13$$

since square law is only an approximation I used the following eqn to adjust vov and get the required gm

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{UnCox\left(\frac{w}{L}\right)}}$$

4. NMOS Active Load

only requirement is to bias it such that its in saturation

current will be 350n

$$\left(\frac{w}{L}\right) = \frac{I_D}{UnCox \cdot \left(V_{GS} - V_{TH}\right)^2} = \frac{350n}{\left(495.3 \cdot 10^{-6}\right) \cdot (0.2)^2} = 0.07$$

had to use w/L = 0.1

5. NMOS (cs amp)

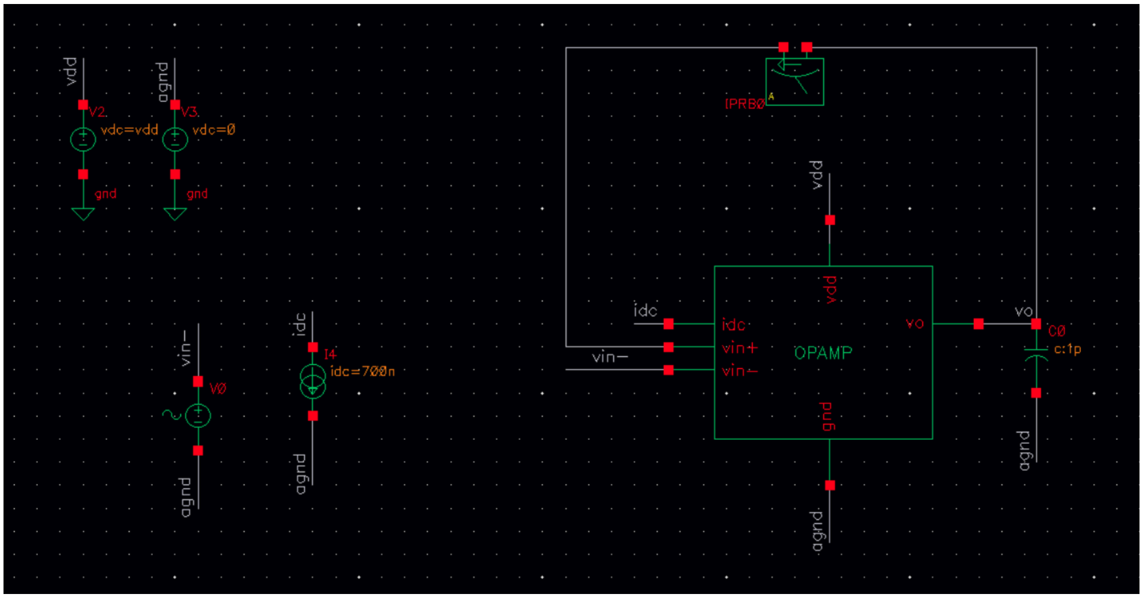
gm2=40u(10 times gm1 for good phase margin)

$$gm = 2 \cdot \frac{I_D}{(Vov)}$$

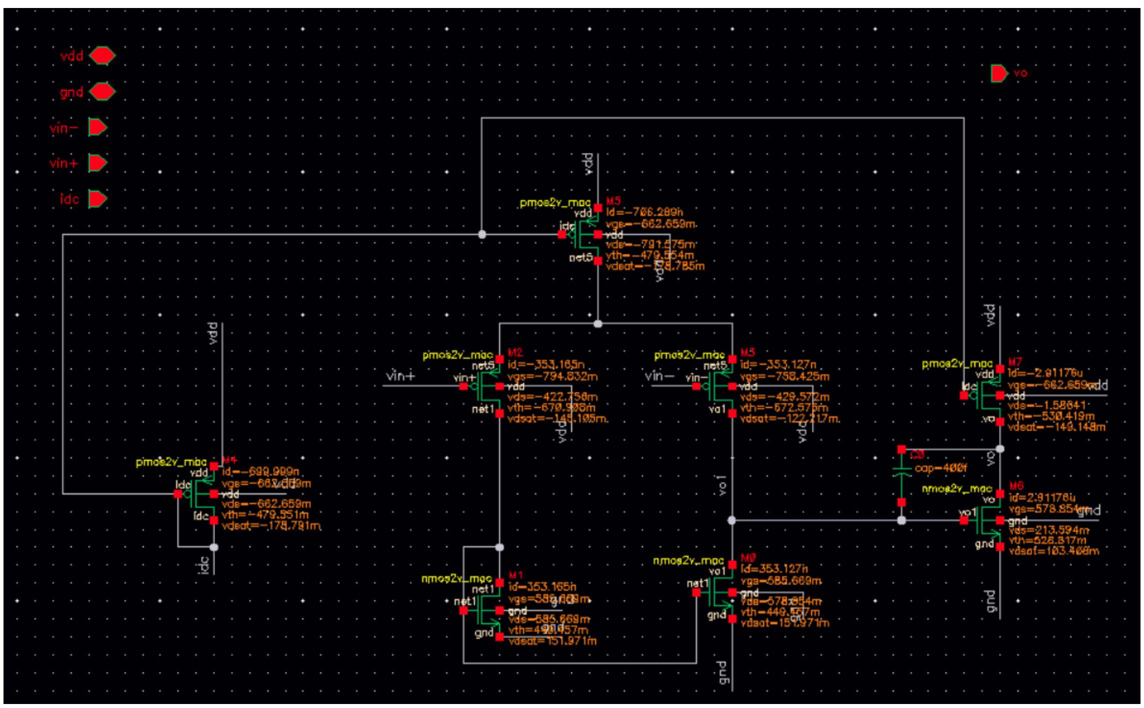
$$Vov = \left(\frac{40 \cdot 10^{-6}}{2 \cdot 2.8 \cdot 10^{-6}}\right)^{-1} = 140m$$

$$\left(\frac{w}{L}\right) = \frac{gm}{UnCox(Vov)} = \frac{\left(40 \cdot 10^{(-6)}\right)}{\left(177.3 \cdot 10^{-6}\right) \cdot (0.14)} = 1.6$$

## Test setup :



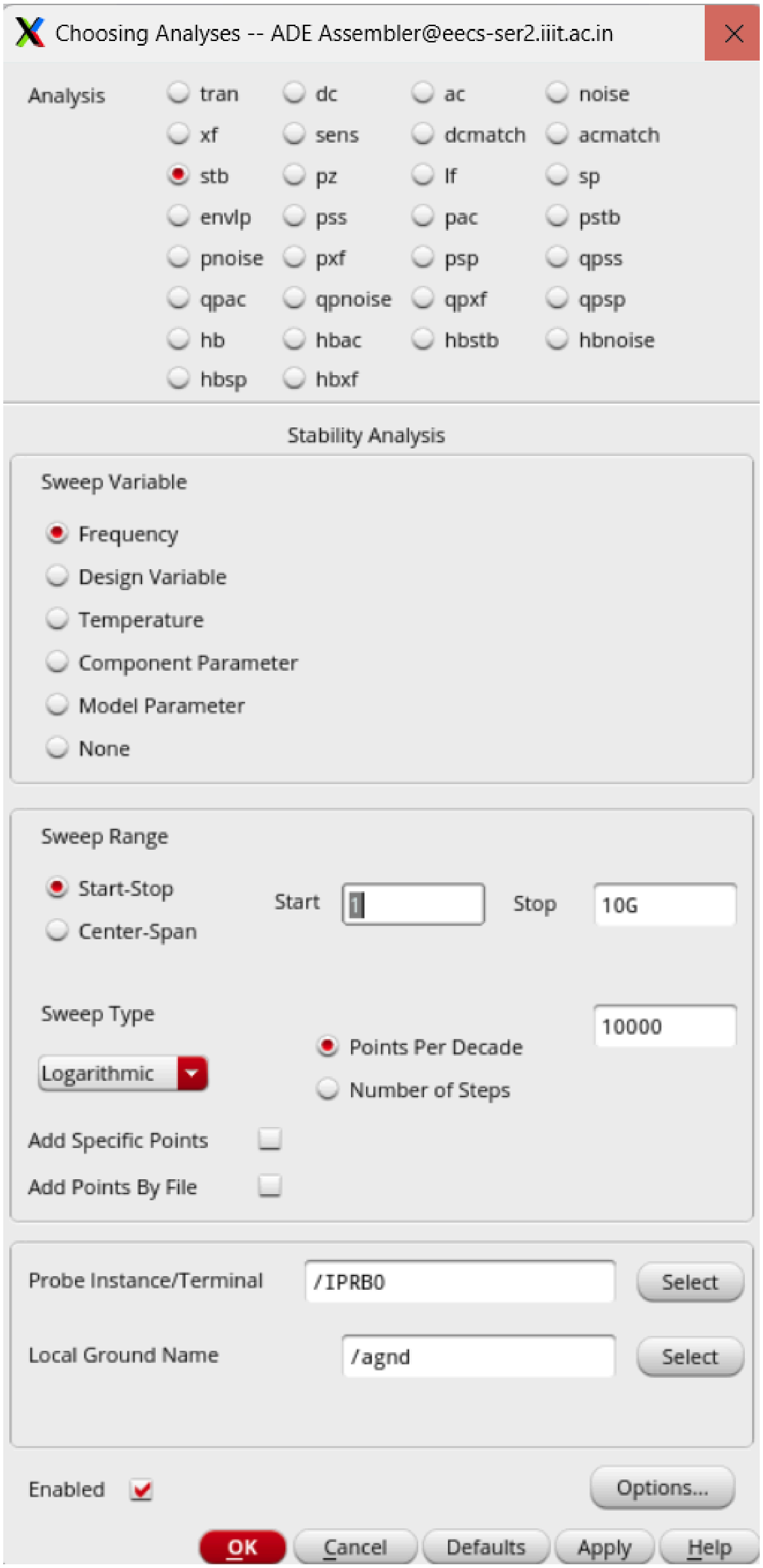
## DC Operating Point :



## ADE Setup :

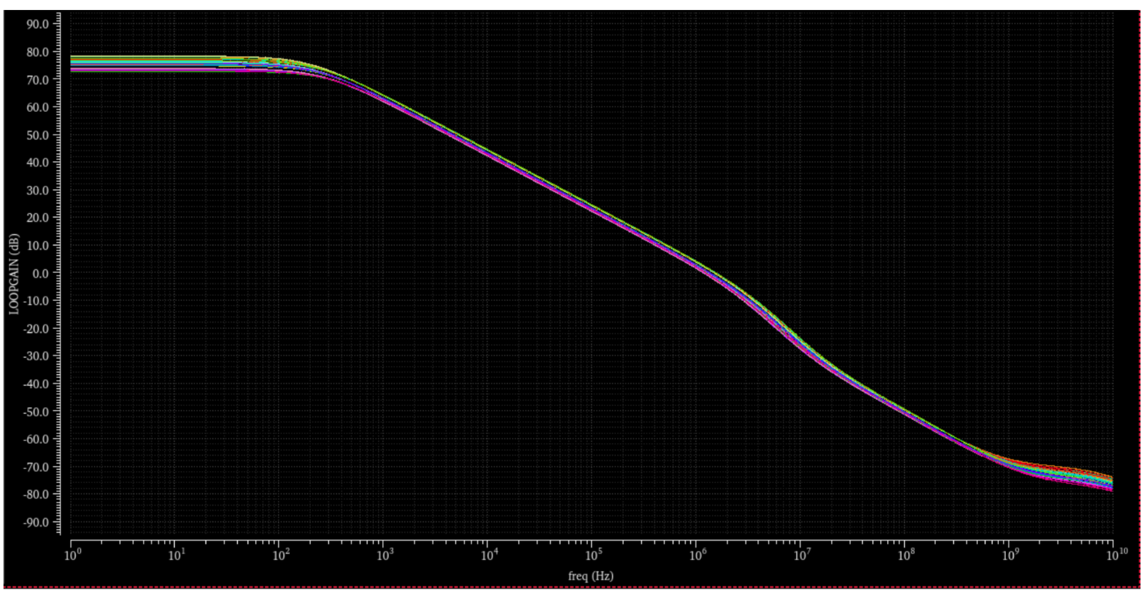
vdd→ 1.62 1.8 1.98

| | | |
|---|---|---|
| id1 | expr | (- OP("/I0/M3" "ids")) |
| id2 | expr | (- OP("/I0/M7" "ids")) |
| power | expr | ((id1 + id2 + 7e-07) * VAR("vdd")) |


Choosing Analyses -- ADE Assembler@eecs-ser2.iiit.ac.in
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
acmatch
stb
pz
lf
sp
envlp
pss
pac
pstb
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
hb
hbac
hbstb
hbnoise
hbsp
hbxf
Stability Analysis
Sweep Variable
Frequency
Design Variable
Temperature
Component Parameter
Model Parameter
None
Sweep Range
Start-Stop
Center-Span
Start
1
Stop
10G
Sweep Type
10000
Points Per Decade
Logarithmic
Number of Steps
Add Specific Points
Add Points By File
Probe Instance/Terminal
/IPRB0
Select
Local Ground Name
/agnd
Select
Enabled
Options...
OK
Cancel
Defaults
Apply
Help

| Corners | ☑ Nominal | ☐ tt | ☐ ss | ☐ ff |
|---|---|---|---|---|
| | | | | |
| Temperature | | -40 27 125 | -40 27 125 | -40 27 125 |
| Design Variables | | | | |
| Click to add | | | | |
| Parameters | | | | |
| Click to add | | | | |
| Model Files | | | | |
| cor_std_mos.scs | | ☑ tt | ☑ ss | ☑ ff |
| cr018gpii_v1d0.scs | | ☑ stat_noise | ☑ stat_noise | ☑ stat_noise |
| Click to add | | | | |
| Model Group(s) | | <modelgroup> | <modelgroup> | <modelgroup> |
| Click to add | | | | |
| Tests | | | | |
| ☑ ..._opamp_tb_1 | ☑ | ☑ | ☑ | ☑ |
| ☐ ..._opamp_tb_2 | ☑ | ☑ | ☑ | ☑ |
| ☐ ..._opamp_tb_3 | ☑ | ☑ | ☑ | ☑ |
| ...mber of Corners | 1 | 3 | 3 | 3 |

## Results :



42 rows

| Point | Output | Nominal | Pass/Fail | tt_0 | tt_1 | tt_2 | ss_0 | ss_1 | ss_2 | ff_0 | ff_1 | ff_2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Filter | Filter | Filter | Filter | Filter | Filter | Filter | Filter | Filter | Filter | Filter | Filter | Filter |
| Parameters: vdd=1.62 | | | | | | | | | | | | |
| 1 | /vo | | | | | | | | | | | |
| 1 | ro2 | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | OP("/I0/M6" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | OP("/I0/M5" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | OP("/I0/M4" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | OP("/I0/M3" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | OP("/I0/M2" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | OP("/I0/M1" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | OP("/I0/M0" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 1 | Phase Margin | 60.23 | | 59.27 | 60.23 | 59.98 | 57.52 | 58.77 | 58.86 | 60.42 | 61.26 | 60.8 |
| 1 | Phase Margin Fr... | 1.325M | | 1.506M | 1.325M | 1.209M | 1.478M | 1.295M | 1.178M | 1.533M | 1.355M | 1.241M |
| 1 | Loop Gain Phase | | | | | | | | | | | |
| 1 | Loop Gain dB20 | | | | | | | | | | | |
| 1 | power | 6.345u | | 5.844u | 6.345u | 6.809u | 5.482u | 5.994u | 6.51u | 6.078u | 6.558u | 6.967u |
| Parameters: vdd=1.8 | | | | | | | | | | | | |
| 2 | /vo | | | | | | | | | | | |
| 2 | ro2 | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 2 | OP("/I0/M6" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 2 | OP("/I0/M5" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 2 | OP("/I0/M4" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 2 | OP("/I0/M3" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 2 | OP("/I0/M2" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 2 | OP("/I0/M1" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 2 | OP("/I0/M0" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 2 | Phase Margin | 60.62 | | 59.6 | 60.62 | 60.43 | 57.84 | 59.15 | 59.32 | 60.77 | 61.65 | 61.25 |
| 2 | Phase Margin Fr... | 1.326M | | 1.513M | 1.326M | 1.208M | 1.485M | 1.297M | 1.176M | 1.54M | 1.356M | 1.24M |
| 2 | Loop Gain Phase | | | | | | | | | | | |
| 2 | Loop Gain dB20 | | | | | | | | | | | |
| 2 | power | 7.137u | | 6.576u | 7.137u | 7.655u | 6.158u | 6.732u | 7.309u | 6.853u | 7.388u | 7.843u |
| Parameters: vdd=1.98 | | | | | | | | | | | | |
| 3 | /vo | | | | | | | | | | | |
| 3 | ro2 | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | OP("/I0/M6" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | OP("/I0/M5" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | OP("/I0/M4" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | OP("/I0/M3" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | OP("/I0/M2" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | OP("/I0/M1" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | OP("/I0/M0" "re... | 2 | pass | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 3 | Phase Margin | 60.95 | | 59.92 | 60.95 | 60.82 | 58.15 | 59.49 | 59.72 | 61.09 | 62.01 | 61.65 |
| 3 | Phase Margin Fr... | 1.327M | | 1.519M | 1.327M | 1.206M | 1.49M | 1.298M | 1.175M | 1.546M | 1.357M | 1.238M |
| 3 | Loop Gain Phase | | | | | | | | | | | |
| 3 | Loop Gain dB20 | | | | | | | | | | | |
| 3 | power | 7.941u | | 7.321u | 7.941u | 8.514u | 6.844u | 7.479u | 8.118u | 7.643u | 8.233u | 8.733u |