PHASE 1: 6T SRAM CELL

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6-transistor (6T) SRAM cell is the fundamental storage element in static RAM.

It stores a single bit of data (“0” or “1”) using two cross-coupled CMOS inverters, which maintain a stable bistable state as long as power is supplied.

Each cell can be **read** or **written** through two **access transistors**, controlled by the **word line (WL)** and connected to the **bit lines (BL, BLB)**.

COMPONENTS

WORDLINE (WL)

Its used to set the operation the SRAM performs. It is used to enable/disable the access transistors.
It controls all the cells in a single row of the memory array.

- When **WL = 1 (activated):**
  - Access transistors turn ON.
  - The cell can **read** or **write** through the bit lines.
- When **WL = 0 (deactivated):**
  - Access transistors turn OFF.
  - Cell is **isolated** from bit lines. It retains its data.

BITLINE (BL and ~BL)

They’re used to read from or write to the cell. These two lines carry **opposite logic levels** during both **read** and **write** operations.

They serve as **bidirectional** data paths:

- **During a read:** They act as **sensing lines**.
- **During a write:** They act as **data input lines**.

There are 2 Bit Lines as it helps with performing Read and Write operations faster.

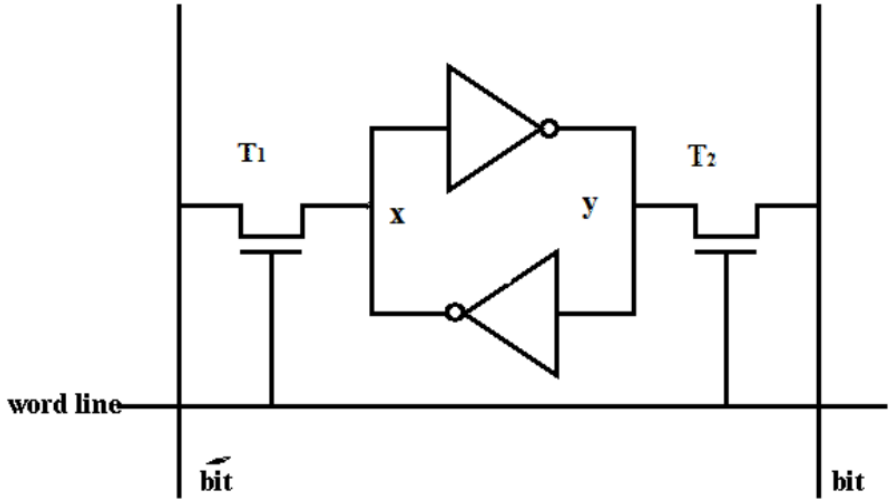
ACCESS TRANSISTORS (M5, M6)

They’re used to connect or disconnect the cell from the Bitlines during read/write.

When the **word line (WL)** is:

- **LOW (0):**
  - M5 and M6 are OFF → cell is isolated.
  - Data is **retained** internally (Hold mode).
- **HIGH (1):**
  - M5 and M6 are ON → cell is connected to Bitlines.
  - Allows **read or write** operation, depending on Bitline voltages.

CROSS COUPLED INVERTERS



Each inverter consists of a **pull-up pMOS** and a **pull-down nMOS** transistor:

M2, M4 are PULL UP PMOS and M1, M3 are PULL DOWN NMOS.

INV1 is made of M1 and M2. INV2 is made of M3 and M4.

These two inverters are **cross-coupled**:

- The **output of INV1 (Q)** connects to the **input of INV2**,
- The **output of INV2 ($\overline{Q}$)** connects to the **input of INV1**.

This cross-coupling creates a **positive feedback loop** that makes the circuit **bistable**, meaning:

- It can **permanently stay** in either of two stable states as long as power is provided:
  - Q = 1, $\overline{Q}$ = 0 → stores logic 1
  - Q = 0, $\overline{Q}$ = 1 → stores logic 0

MODES

IDLE

Stored data is retained as long as power is supplied to the inverters.

This mode is entered when -

- WL = 0 → access transistors (M5, M6) are OFF.

- The two cross-coupled inverters reinforce each other:

  if Q = 1 → Q̄ = 0, and vice versa.

• Because there is **no current path** to BL or ~BL the stored data is retained indefinitely.

READ

In this mode we can read what value is stored in the SRAM cell.

To perform this operation -

- Word Line: **WL = 1** (Access transistors ON)
- Bit Lines: **BL and ~BL precharged to VDD**
- Sense Amplifier: Enabled after a short delay

STEPS

- **Precharge :**

  Both BL and ~BL are charged to VDD before WL is activated.

- **Word Line Activated:**

  WL = 1 → Access transistors connect internal nodes Q and Q̄ to BL and ~BL respectively.

- **Small Differential Development:**
  - If cell stores **Q = 1**, **Q̄ = 0**:
    - The node Q (1) connects to BL → BL remains close to VDD.
    - The node Q̄ (0) connects to ~BL → ~BL starts to **discharge slightly** through M5 and M6.
  - If cell stores **Q = 0**, **Q̄ = 1**, the opposite occurs:
    - BL discharges slightly; ~BL remains high.
- **Sensing:**
  - The **sense amplifier** detects which line is slightly lower.
  - Since the difference is small , differential sensing allows **high-speed and low-power** read.
- **Restoring:**

- Once data is read, WL is turned off again.
- Precharge circuits restore both BL and ~BL to VDD for the next cycle.

WRITE

In this mode we can write onto the SRAM a bit value.

To perform this operation -

- WL = 1 → Access transistors ON
- Bit lines are actively driven by the **write driver circuit**:
  - To write '1': BL = 1 (VDD), ~BL = 0 (GND)
  - To write '0': BL = 0 (GND), ~BL = 1 (VDD)

STEPS

- **Setup Bit Lines:**
  - Write drivers force complementary voltages on BL and BL̄.
    - Example: To write 0 → BL = 0, ~BL = 1
- **Activate Word Line:**
  - WL = 1 → Access transistors connect bit lines to storage nodes.
- **Overpower and Flip the Cell:**
  - The node connected to BL = 0 starts to discharge.
  - The cross-coupled feedback ensures that once one side starts dropping, the opposite side rises quickly.
  - The inverters **regenerate** the new stable state (new data stored).
- **Finish Write:**
  - WL is turned off → Access transistors OFF.
  - The bit lines are returned to precharge state.

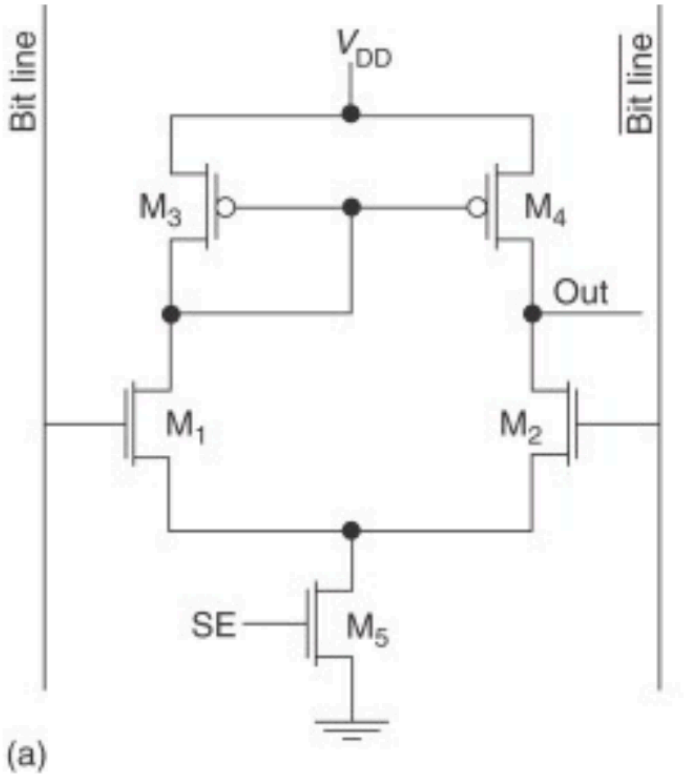
PRECHARGING

Before every **read or write**, both **bit lines (BL and ~BL)** are brought to a **known voltage level**.

Precharge sets both Bitlines to a known voltage (usually Vdd) so the sense amplifier can reliably detect the tiny voltage difference during a Read. It also ensures Bitlines can swing fully during Writes and prevents floating voltages when idle.

SENSE AMPLIFIER

The Sense Amplifier is a **small, high-speed differential amplifier** used during the **read operation** in SRAM.



Its used to recognize which bit is stored in the READ operation.

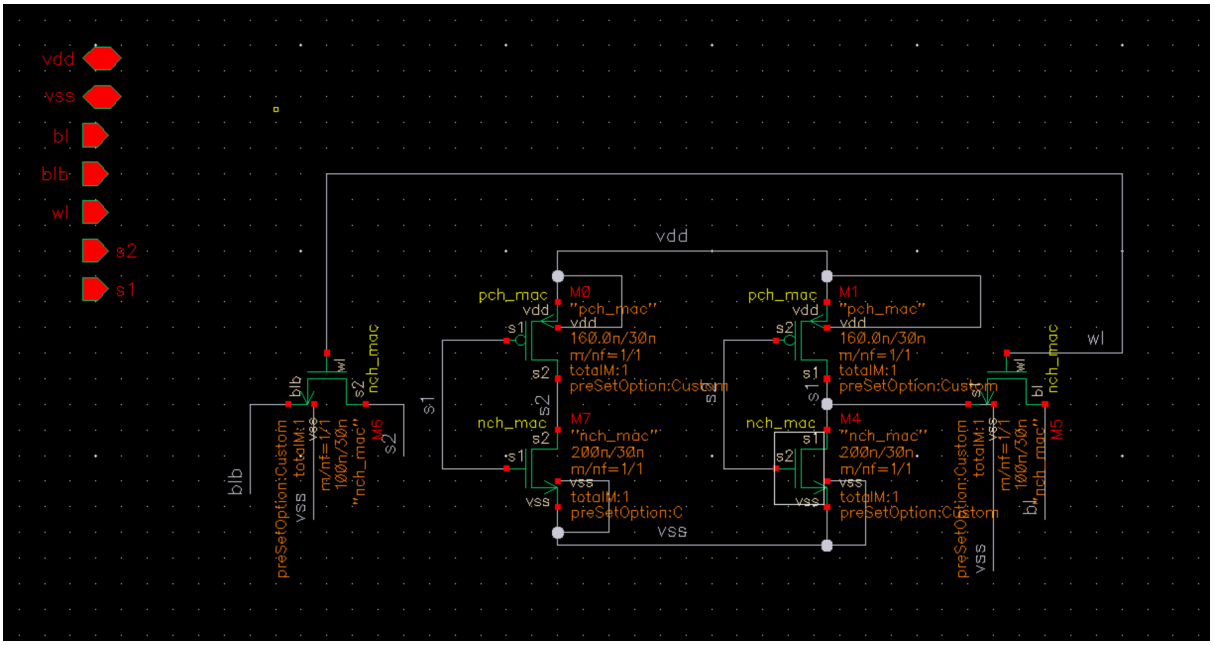
When a voltage difference develops across its terminals, it amplifies it and based on whether it is positive or negative it can quickly identify if 0 or 1 was stored.

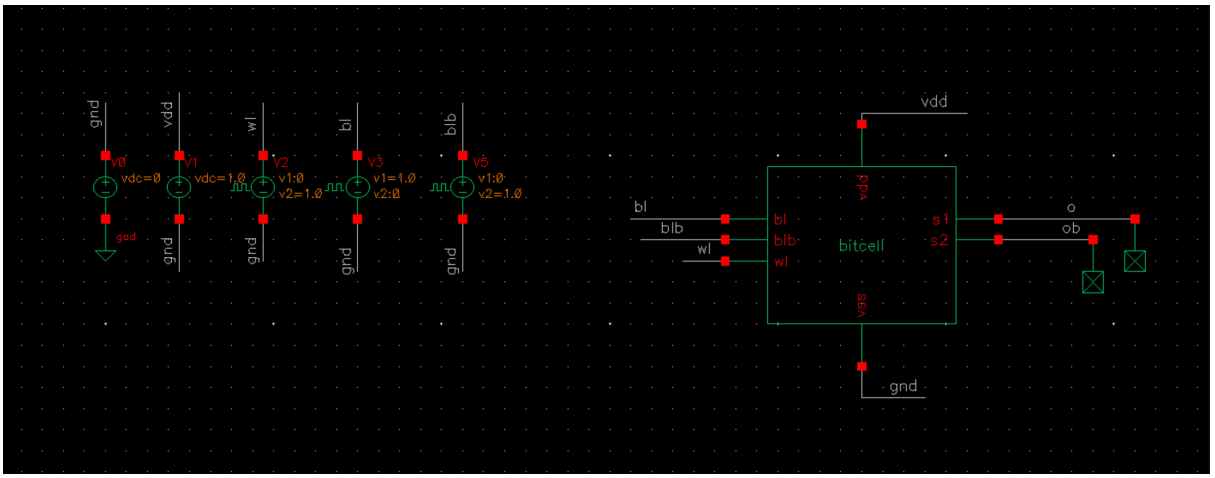
- **0 stored:** BL → discharges slightly → SA detects BL < ~BL → outputs 0
- **1 stored:** ~BL → discharges slightly → SA detects BL > ~BL → outputs 1

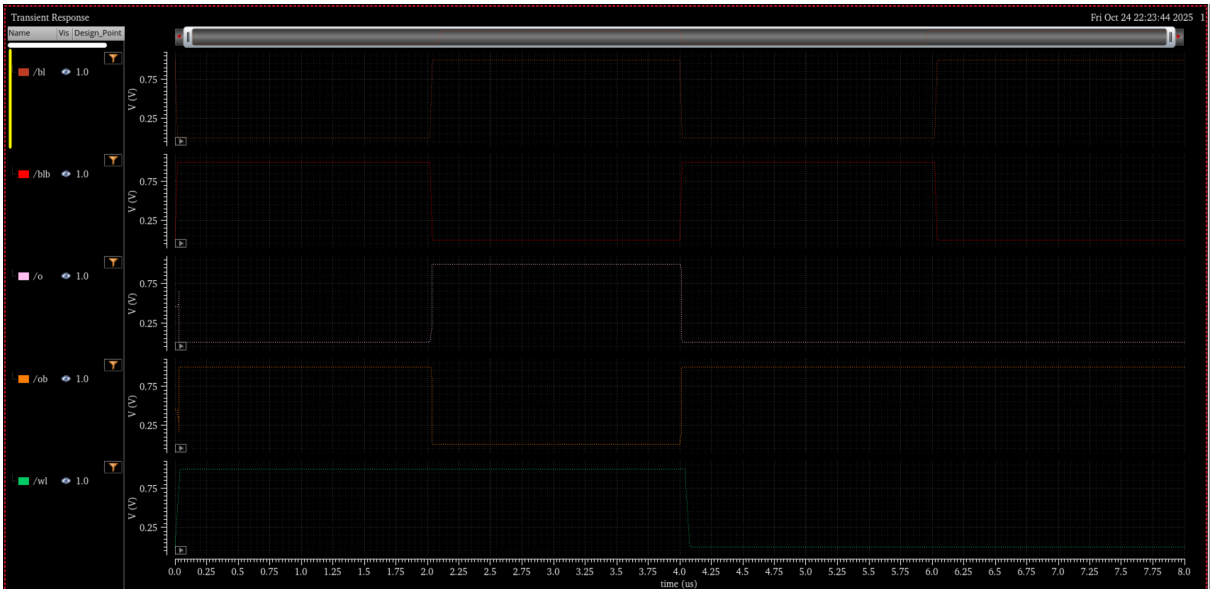
It mainly used because -

- Without differential sensing, detecting small voltage swings would be too slow.
- Positive feedback in the SA ensures **full rail-to-rail swing**.

W/L RATIOS (28 TSMC)



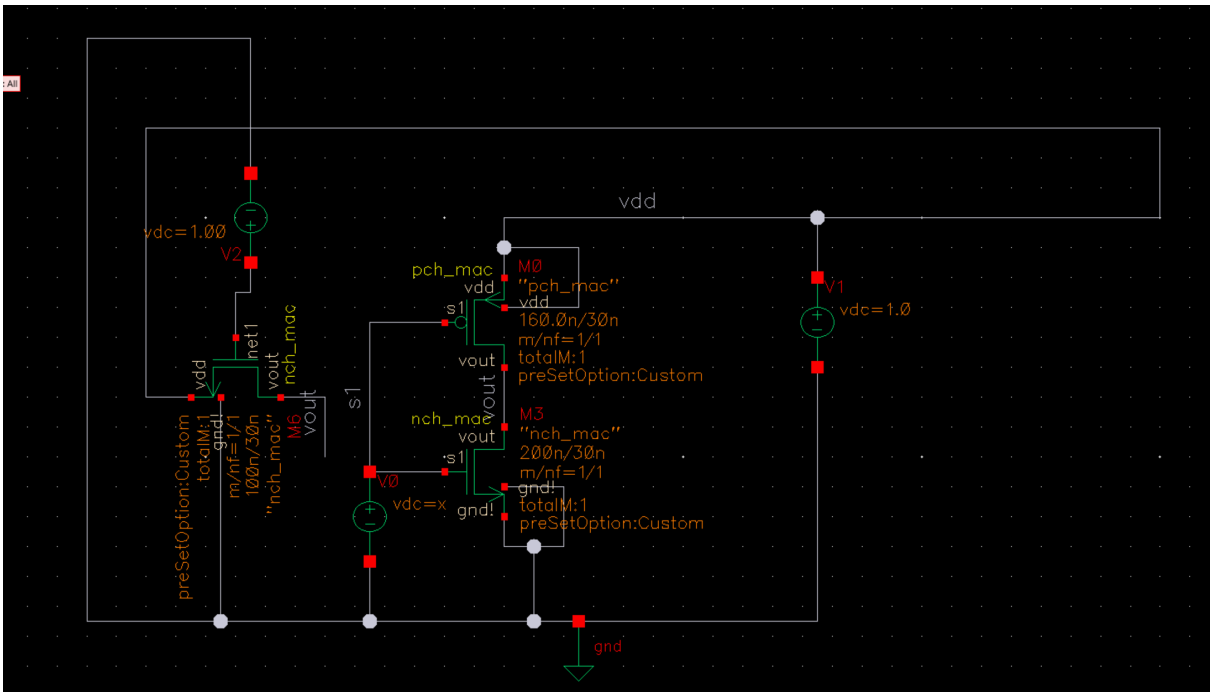


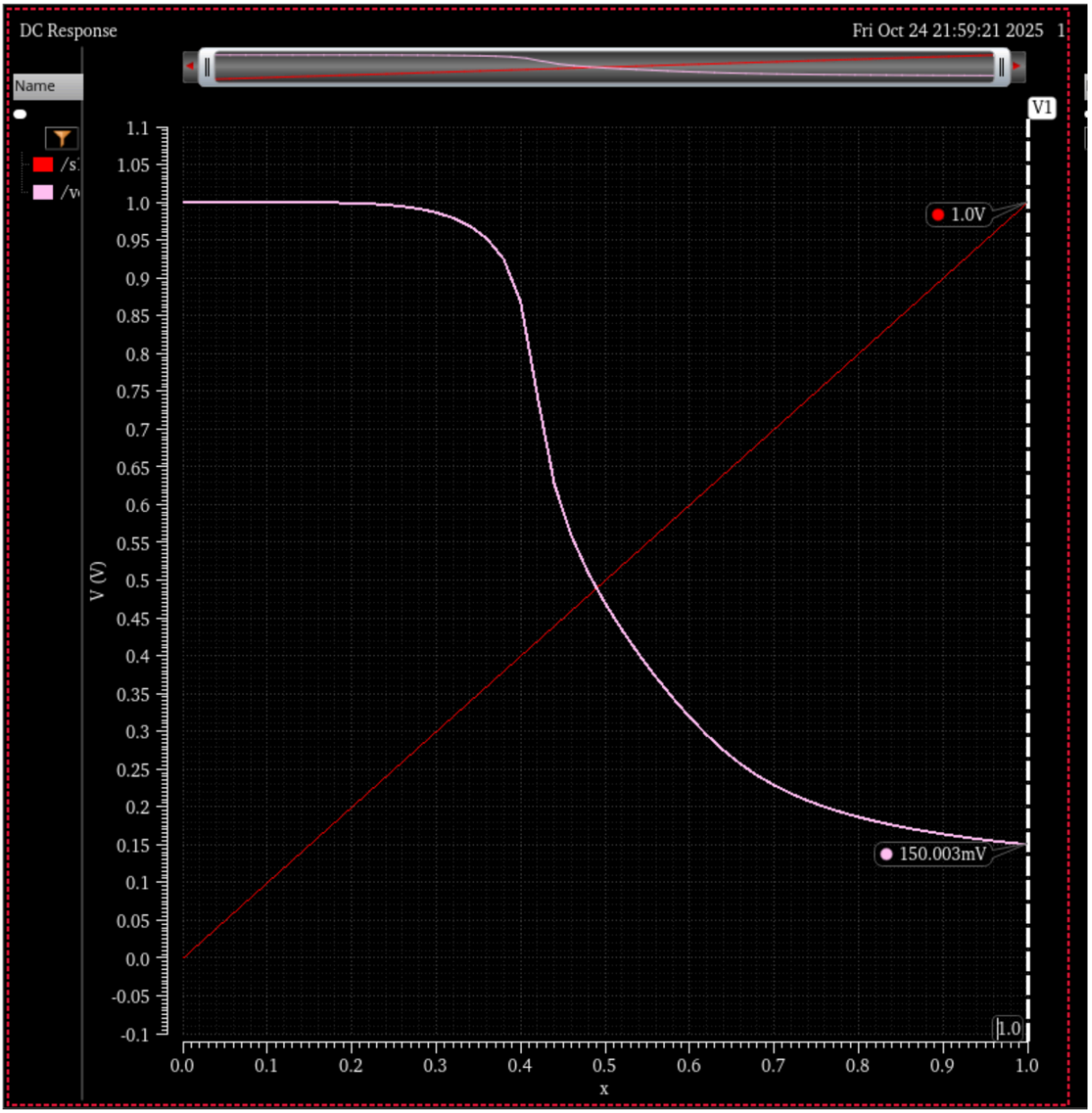


The plots show the **transient voltage responses** of the word line (WL), bit lines (BL and BL), and the output node (Q) during **read and write operations** for the chosen W/L sizing in the 28 nm TSMC process.

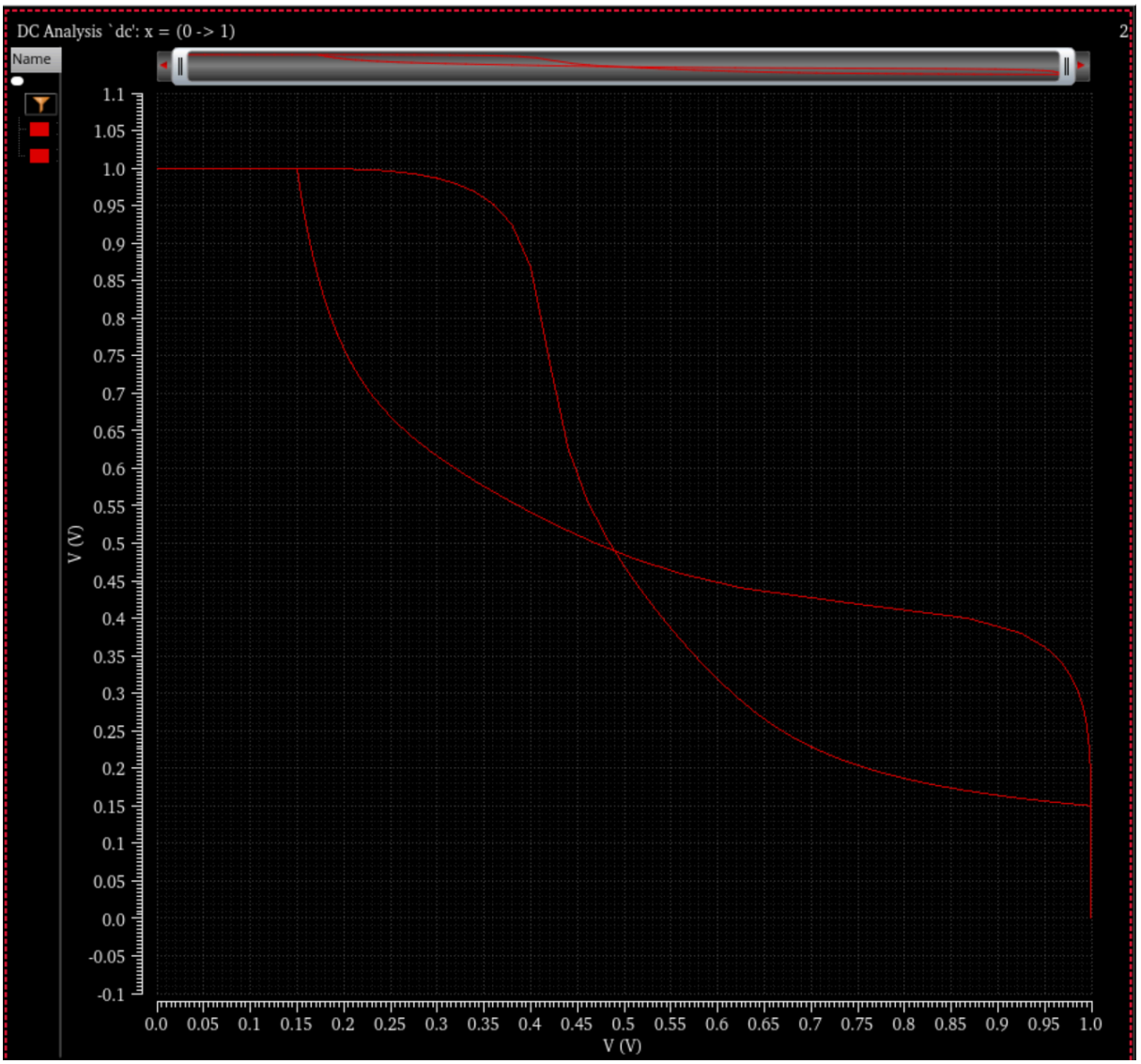
NOISE MARGINS

Read Static Noise Margin (SNM)



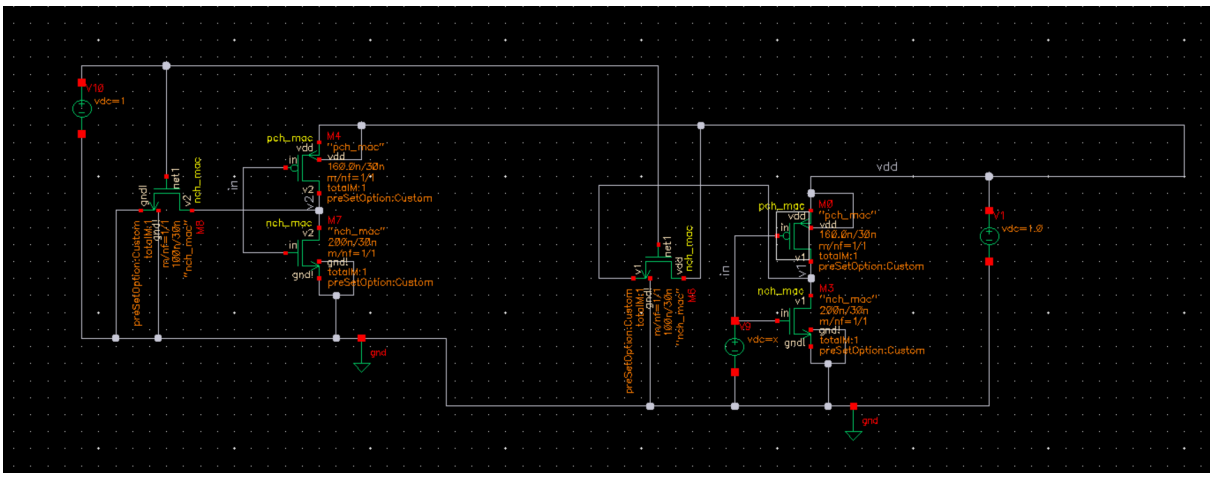


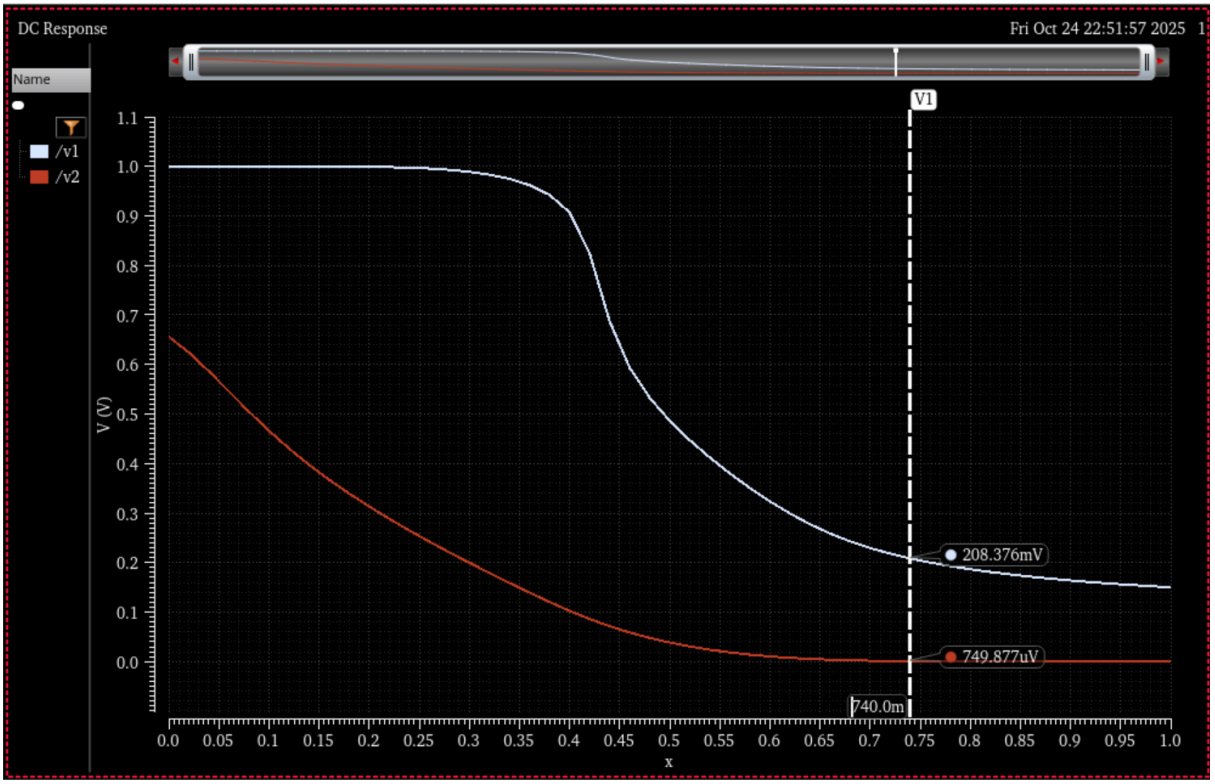
This plot shows the **voltage transfer characteristics (VTC)** of the two cross-coupled inverters that form the 6T SRAM cell. One inverter's VTC is mirrored and overlapped with the other to form a **butterfly-shaped curve**.



- The **Static Noise Margin (SNM)** is defined as the **length of the side of the largest possible square** that can fit between the two inverter curves.
- It represents the **maximum DC noise voltage** the cell can tolerate without flipping its stored bit during idle/read.
- The point where both inverter curves **intersect** being close to **VDD/2 (≈ 0.9 V for VDD = 1.8 V)** indicates that both inverters have **equal strength** and **balanced noise immunity**.
- The butterfly curve is symmetric, meaning the cell can tolerate equal noise margins for both ‘0’ and ‘1’ states — ideal for reliable operation.
- The worst-case voltage rise in the SRAM cell during a read is 150.003mV.

Write Noise Margin (WNM)





- During a write operation, one of the bitlines is pulled low while WL = 1.
- The WNM is the m**inimum Bit Line voltage difference** required to successfully **flip the stored value** during a write operation.
- It depends on the strength of the **access transistors** and the **pull-up PMOS**.
  - Stronger access → higher write-ability.
  - Stronger pull-up → harder to write (lower WNM).

- The **threshold voltage** at which the latch flips defines the write margin.
- A higher WNM ensures easy data writing but can compromise read stability if access transistors become too dominant.
- The worst-case cell voltage during a write (which is found from measuring V1 when V2 is at 0V) is 208.376mV.

Proof for sizing

WA=100 nm, W_PD=160 nm, W_PU=200 nm, L=30 nm (28 nm)

1) MOSFET saturation equation

$$I_{D,\text{sat}} = \tfrac{1}{2}\,\mu\,C_{ox}\,\frac{W}{L}\,(V_{GS}-V_T)^2\,(1+\lambda V_{DS})$$

For first-order ratios, we take $\lambda \approx 0$ and define $\beta = \mu C_{ox}\,\frac{W}{L}$ so that

$$I_{D,\text{sat}} = \tfrac{1}{2}\,\beta\,V_{ov}^2, \quad V_{ov} = V_{GS}-V_T$$

2) Read stability (cell ratio CR)

Condition: $I_{PD} \geq I_A$ at equal V_{ov}.

$$\frac{I_{PD}}{I_A} = \frac{\beta_{PD}}{\beta_A} = \frac{(W/L)_{PD}}{(W/L)_A} = \frac{5.33}{3.33} \approx 1.60$$

3) Write-ability (access vs pull-up)

Condition: βA·WA>βPU·WPU

General ratio:

$$\frac{I_A}{I_{PU}} = \frac{\beta_A}{\beta_{PU}}\left(\frac{V_{ov,n}}{V_{ov,p}}\right)^2$$

$$\frac{I_A}{I_{PU}} \approx \frac{\mu_n}{\mu_p}\,\frac{(W/L)_A}{(W/L)_{PU}} \approx 2.5 \times \frac{3.33}{6.67} \approx 1.25$$