Homework 02 (Solutions)

1.(电路图略)

a. X = NOT (NOT(A) OR (A AND B AND C))
X=$\overline{\bar{A}+ABC}=\overline{\bar{A}+BC}$=A$\overline{BC}$

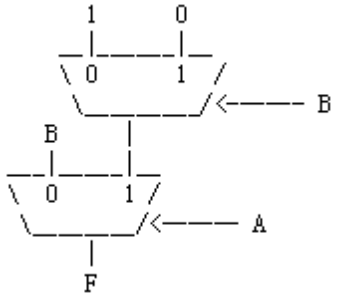
b. Y = NOT ((A OR B) AND (A AND B AND C))
Y=$\overline{(A+B)ABC}=\overline{ABC}$

A	B	C	X	Y
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

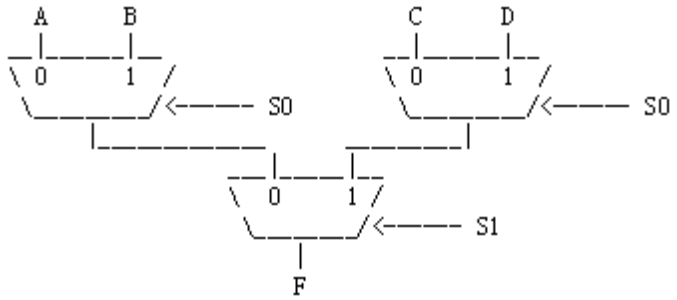
2. a. Z = A XOR B = A$\bar{B}$+$\bar{A}$B = ($\bar{A}$+$\bar{B}$)(A+B) = $\overline{\overline{(\bar{A}+B)(A+\bar{B})}}$

使用 **2-1 mux：**

Z = A XOR B = A$\bar{B}$+$\bar{A}$B = $\bar{A}$B +A($\bar{B}$ · 1+B· 0)

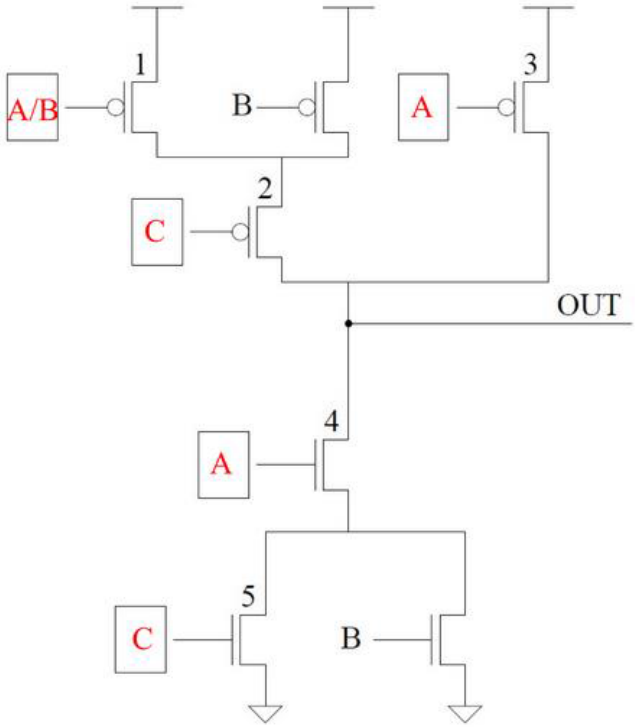


b.



S1	S0	OUT
0	0	A
0	1	B
1	0	C
1	1	D

3.



A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Figure 1

4. Figure 3.36 is a 2-input mux, which combinational logic i.e., D is the output of the circuit. Figure 3.37 is a storage element, which stores the data value previously stored in latch.

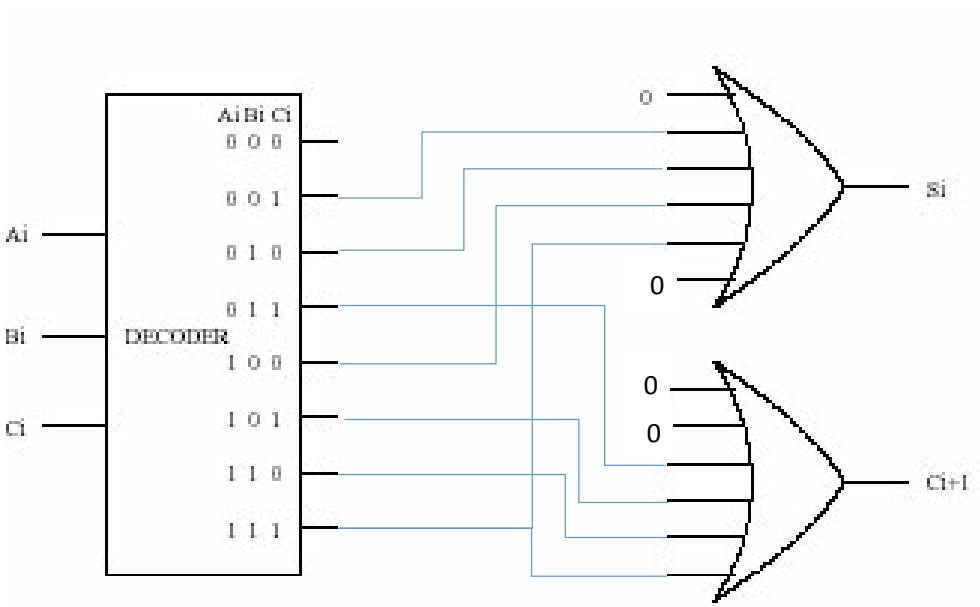
5. a. 3

b. 12

c. You can construct a tree-like structure:

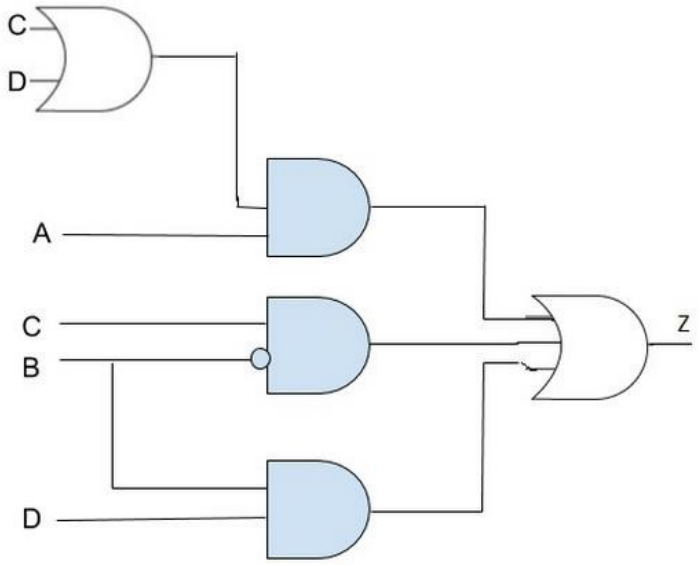
Z=(A AND B)AND(C AND D) AND E

6.



7. Z = A(C+D)+BD+$\bar{B}$C

(warning:C and D can't be true at same time.)



A	B	C	D	ALARM
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	x
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	x
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	x
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	x

8. a.

A	B	G	E	L
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

b. G = A$\bar{B}$ E = A$\bar{B}$+$\bar{A}$B L =$\bar{A}$B

c. Y = G[3] + E[3]G[2] + E[3]E[2]G[1] + E[3]E[2]E[1]G[0]

9. Every 6 clock cycles a pattern repeats.

Because 50 = 6*8+2 ,after 50 cycles the state will be the same as after 2 cycles.

It will be in state **111000** after 50 cycles

10.

a. (100*100)*4*100*4*101*2*901 = 2912032000000.

2^41 < 2912032000000 < 2^42 so we need **42 bits**

b. Total 43 bits

1. 7 x 2 bits
2. 2 bits
3. 7 bits
4. 2 bits
5. 7 bits
6. 1 bit
7. 4 bits for minutes 6 bits for seconds

c. The assignments in part b are easier to decode.

11.

a. Since there are four floors, you will need 2 bits to represent a floor. Let the logic variable C[1:0] represent the current floor, R[1:0] represent the requested floor, and D[1:0] represent the floor the elevator should go to given a current floor and a requested floor. Shown below is the truth table for this combinational logic circuit.

C1	C0	R1	R0	D1	D0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	1	0

b.00 for 1st floor,01 for 2nd floor,10 for 3rd floor,11 for 4th floor.